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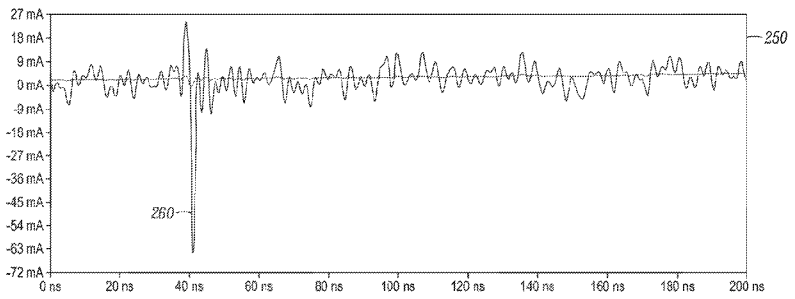


FIG. 3

(57) Abstract: Methods and systems for modulating an amplifier power supply to efficiently attain amplified RF output power with much lower power dissipation than existing amplifiers.

FIBER-OPTIC NODE WITH FORWARD DATA CONTENT DRIVEN POWER CONSUMPTION

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. Provisional App. No. 61/867,550 entitled "Fiber-Optic Node with Forward Data Content Driven Power Consumption", filed August 19, 2013, the contents of which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] A cable television (CATV) system is capable of providing a variety of media content, such as video, data, voice, or high-speed Internet services to subscribers. The CATV provider typically delivers the media content from a head end to its subscriber's client devices over a transmission network such as a coaxial network, a fiber optic network, or a hybrid fiber/coax (HFC) network. Requirements for data throughput (or bandwidth) in these CATV networks are growing exponentially as customers demand more content, data services, etc. Though improvements in encoding efficiencies and transport protocols have thus far allowed cable operators to keep pace with subscriber and competitive demands, it is important to continue the analysis of the various network elements that can enhance or inhibit the overall performance of next-generation cable networks.

[0003] Most of the radio frequency (RF) amplifiers within the cable television

network operate in what is referred to as a “class A” mode of operation, which provides a very high fidelity signal, often quantified in terms of signal-to-noise and signal-to-2nd, 3rd, 4th, 5th... harmonic distortion products. However, the power consumption for the class A mode of operation is on the order of 100 times higher than the composite power of an RF output signal. This higher power consumption results from the need to accommodate significant and frequent 'peak to average' deviations from the effective signal power, which may include setting the output RF rms amplitude of the amplifier at no more than roughly 25% of the output rail-to-rail range of either voltage or current, depending on the implementation. The higher demand for power consumption drives up the cost of cable network products that require RF gain blocs (e.g., head end optical transmitters and receivers, fiber-optic nodes, RF distribution amplifiers). Thus, it is desirable to reduce the power dissipation in a CATV network without compromising output signal power in relation to noise. It would be even more desirable to reduce the power dissipation in a CATV network while improving output signal power in relation to noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] For the purpose of illustrating embodiments described below, there are shown in the drawings example constructions of the embodiments; however, the embodiments are not limited to the specific methods and instrumentalities disclosed. In the drawings:

[0005] FIG. 1 illustrates an example CATV system.

[0006] FIG. 2 illustrates a schematic diagram of a representative basic push-pull transistor amplifier.

[0007] FIG. 3 illustrates the output current that results from an exemplary input current to the amplifier shown in FIG. 2

[0008] FIG. 4 illustrates the transistor current provided by the amplifier for FIG. 2 in a biased state when providing the amplified signal of FIG. 3.

[0009] FIG. 5 illustrates an embodiment of the disclosed digital forward receiver.

[0010] FIG. 6 illustrates an embodiment for modifying an amplifier biasing.

[0011] FIG. 7 illustrates the shape of a signal to amplify.

[0012] FIG. 8 illustrates an embodiment of a peak detect algorithm.

[0013] FIG. 9 illustrates the input and output waveforms that result from the embodiment shown in FIG. 8.

[0014] FIG. 10 illustrates an output signal peak when a bias current is high.

[0015] FIG. 11 illustrates exemplary transistor currents.

[0016] FIG. 12 illustrates an input signal and output signal scaled to approximately the same magnitude and compared.

[0017] FIG. 13 illustrates an exemplary linearization function.

[0018] FIG. 14 illustrates an embodiment with two voltage sources driving a transistor amplifier.

[0019] FIG. 15 illustrates a power supply having energy stored in an inductor that supports power delivery during normal operation and during voltage transients.

[0020] FIG. 16 illustrates an exemplary power supply that delivers a fixed current.

[0021] FIG. 17 illustrates an exemplary embodiment that replaces a power supply with a capacitor.

[0022] It should be understood that, while the accompanying figures illustrate embodiments that include the portions of the disclosure claimed, and explain various principles and advantages of those embodiments, the details displayed are not

necessary to understand the illustrated embodiments, as the details depicted in the figures would be readily apparent to those of ordinary skill in the art having the benefit of the present disclosure.

DETAILED DESCRIPTION

[0023] The present disclosure describes systems and methods that reduce power consumption in a CATV network, including (1) systems that improve the power efficiency of a node in a CATV network by drawing power based on a signal; and (2) methods that use signal envelope information to reduce power consumption in a CATV transmission system. As described in more detail later in this specification, disclosed systems and methods utilize and expand on many digital forward path concepts, including but not limited to: 1) analog to digital (A2D) RF signal conversion at one end of a communication link (e.g., at the head end transmitter side for digital forward path transmission); 2) oversampling, i.e. sampling at a rate larger than the Nyquist frequency of twice the sampled bandwidth so as to enable implementation of sharp digital filtering, which reduces the number of binary data bits required for RF signal reassembly; 3) compression coding, e.g., Huffman-type encoding, to further reduce the number of binary bits required for RF signal reassembly; 4) optical on/off transmission over required distances, but less than 100 miles which is limit specified by the Data Over Cable Service Interface Specification (DOCSIS®) standard; and 5) data decompression at a receiver followed by digital to analog (D2A) signal conversion in order to reassemble an originally encoded RF signal from a transmitter.

[0024] Also, the present disclosure describes systems and methods that introduce a delay to be implemented after received data from a signal is decompressed

but prior to the decompressed signal data being amplified by a gain block. During the delay, the decompressed data is used to predict the magnitude of the signal envelope that is going to be amplified by the gain block at an incrementally later time. The magnitude of the signal envelope is then used to generate an auxiliary signal that drives the power supply to the RF gain block in a manner that minimizes the required voltage/current for the gain block, and thus minimizes the power consumed by the block. Moreover, a delayed auxiliary signal based on the predicted magnitude of the signal envelope in combination with the, optionally delayed, signal itself can be used as a feed-forward pre-distortion signal that corrects for distortion introduced by the RF gain block when amplifying the signal envelope.

[0025] The systems and methods disclosed in the present application can be particularly useful for reducing the power consumption of a fiber optical node that has a large number of RF outputs, and acts as the last amplifier before servicing customer premises - in architectures alternatively referred to as "fiber to the last active" (FTTLA), Node plus zero (N+0), or fiber deep architectures - because in such nodes the RF signals at the output of the node typically consume a relatively large amount of power. It should be understood, however, that other architectures or components of other architectures may benefit from the disclosed techniques, such as upstream or return path A2D/D2A systems, or digital return receivers. Further, the disclosed techniques could be applied to regulating RF gain stages of other digital forward receivers, even if the receiver is not the last RF gain stage in the downstream architecture. Additional details for various embodiments are described in more detail below.

[0026] FIG. 1 shows an exemplary cable television (CATV) system 100 operable to deliver high-definition digital entertainment and telecommunications such

as video, voice, and high-speed Internet services. Generally speaking, the CATV system 100 refers to the operational (e.g., geographical) footprint of an entertainment and/or information services franchise that provides entertainment and/or information services to a subscriber base spanning one or more towns, a region, or a portion thereof. Particular entertainment and/or information services offered by the franchise (e.g., entertainment channel lineup, data packages, etc.) may differ from system to system. Some large cable companies operate several cable communication systems (e.g., in some cases up to hundreds of systems), and are known generally as Multiple System Operators (MSOs).

[0027] The cable network can take the form of an all-coax, all-fiber, or hybrid fiber/coax (HFC) network, e.g., fiber to the last amplifier (FTTA). For purposes of illustration only, FIG. 1 depicts a hybrid fiber-coaxial (HFC) network. An HFC network is a broadband network that combines optical fiber and coaxial cable, strategically placing fiber nodes to provide services to a plurality of homes. It should be understood that the systems and methods disclosed in the present application may be employed in various networks and the HFC network is merely shown as a non-limiting example.

[0028] The network shown in FIG. 1 is an HFC broadband network that combines the use of optical fiber and coaxial connections. The network includes a head end 102 that receives analog video signals and digital bit streams representing different services (e.g., video, voice, and Internet) from various digital information sources. For example, the head end 102 may receive content from one or more video on demand (VOD) servers, IPTV broadcast video servers, Internet video sources, or other suitable sources for providing IP content.

[0029] An IP network 108 may include a web server 110 and a data source

112. The web server 110 is a streaming server that uses the IP protocol to deliver video-on-demand, audio-on-demand, and pay-per view streams to the IP network 108. The IP data source 112 may be connected to a regional area or backbone network (not shown) that transmits IP content. For example, the regional area network can be or include the Internet or an IP-based network, a computer network, a web-based network or other suitable wired or wireless network or network system.

[0030] At the head end 102, the various services are encoded, modulated and up-converted onto RF carriers, combined onto a single electrical signal and inserted into a broadband optical transmitter. A fiber optic network extends from the cable operator's master/regional head end 102 to a plurality of fiber optic nodes 104. The head end 102 may contain an optical transmitter or transceiver to provide optical communications through optical fibers 103. Regional head ends and/or neighborhood hub sites may also exist between the head end and one or more nodes. The fiber optic portion of the example HFC network 100 extends from the head end 102 to the regional head end/hub and/or to a plurality of nodes 104. The optical transmitter converts the electrical signal to a downstream optically modulated signal that is sent to the nodes. In turn, the optical nodes convert inbound signals to RF energy and return RF signals to optical signals along a return path. In the specification, the drawings, and the claims, the terms "forward path" and "downstream" may be interchangeably used to refer to a path from a head end to a node, a node to a subscriber, or a head end to a subscriber. Conversely, the terms "return path", "reverse path" and "upstream" may be interchangeably used to refer to a path from a subscriber to a node, a node to a head end, or a subscriber to a head end. Also, in the specification, in the drawings, and the claims a node may be any digital hub between a head end and a customer home that transports local requests over the CATV

network. Forward path optical communications over the optical fiber may be converted at the nodes to Radio Frequency (RF) communications for transmission over the coaxial cable to the subscribers. Conversely, return path RF communications from the subscribers are provided over coaxial cables and are typically converted at a node to optical signals for transmission over the optical fiber to the head end. Each node 104 may contain a return path transmitter that is able to relay communications upstream from a subscriber device 106 to the head end 102.

[0031] Each node 104 serves a service group comprising one or more customer locations. By way of example, a single node 104 may be connected to thousands of cable modems or other subscriber devices 106. In an example, a fiber node may serve between one and two thousand or more customer locations. In an HFC network, the fiber optic node 104 may be connected to a plurality of subscriber devices 106 via coaxial cable cascade 111, though those of ordinary skill in the art will appreciate that the coaxial cascade may comprise a combination of RF amplifiers, taps & splitters and coaxial cable. In some implementations, each node 104 may include a broadband optical receiver to convert the downstream optically modulated signal received from the head end or a hub to an electrical signal provided to the subscribers' devices 106 through the coaxial cascade 111. Signals may pass from the node 104 to the subscriber devices 106 via the RF cascade 111, which may be comprised of multiple amplifiers and active or passive devices including cabling, taps, splitters, and in-line equalizers. It should be understood that the amplifiers in the RF cascade 111 may be bidirectional, and may be cascaded such that an amplifier may not only feed an amplifier further along in the cascade but may also feed a large number of subscribers. The tap is the customer's drop interface to the coaxial system. Taps are designed in various values to allow amplitude consistency along the

distribution system.

[0032] The subscriber devices 106 may reside at a customer location, such as a home of a cable subscriber, and are connected to the cable modem termination system (CMTS) 120 or comparable component located in a head end. A client device 106 may be a modem, e.g., cable modem, MTA (media terminal adaptor), set top box, terminal device, television equipped with set top box, Data Over Cable Service Interface Specification (DOCSIS) terminal device, customer premises equipment (CPE), router, or similar electronic client, end, or terminal devices of subscribers. For example, cable modems and IP set top boxes may support data connection to the Internet and other computer networks via the cable network, and the cable network provides bi-directional communication systems in which data can be sent downstream from the head end to a subscriber and upstream from a subscriber to the head end.

[0033] The techniques disclosed herein may be applied to systems compliant with DOCSIS. The cable industry developed the international Data Over Cable System Interface Specification (DOCSIS®) standard or protocol to enable the delivery of IP data packets over cable systems. In general, DOCSIS defines the communications and operations support interface requirements for a data over cable system. For example, DOCIS defines the interface requirements for cable modems involved in high-speed data distribution over cable television system networks. However, it should be understood that the techniques disclosed herein may apply to any system for digital services transmission, such as digital video or Ethernet PON over Coax (EPoc). Examples herein referring to DOCSIS are illustrative and representative of the application of the techniques to a broad range of services carried over coax.

[0034] References are made in the present disclosure to a Cable Modem

Termination System (CMTS) in the head end 102. In general, the CMTS is a component located at the head end or hub site of the network that exchanges signals between the head end and client devices within the cable network infrastructure. In an example DOCSIS arrangement, for example, the CMTS and the cable modem may be the endpoints of the DOCSIS protocol, with the hybrid fiber coax (HFC) cable plant transmitting information between these endpoints. It will be appreciated that architecture 100 includes one CMTS for illustrative purposes only, as it is in fact customary that multiple CMTSs and their Cable Modems are managed through the management network.

[0035] The CMTS 120 hosts downstream and upstream ports and contains numerous receivers, each receiver handling communications between hundreds of end user network elements connected to the broadband network. For example, each CMTS 120 may be connected to several modems of many subscribers, e.g., a single CMTS may be connected to hundreds of modems that vary widely in communication characteristics. In many instances several nodes, such as fiber optic nodes 104, may serve a particular area of a town or city. DOCSIS enables IP packets to pass between devices on either side of the link between the CMTS and the cable modem.

[0036] It should be understood that the CMTS is a non-limiting example of a component in the cable network that may be used to exchange signals between the head end and subscriber devices 106 within the cable network infrastructure. For example, other non-limiting examples include a Modular CMTS (M-CMTS™) architecture or a Converged Cable Access Platform (CCAP).

[0037] An EdgeQAM (EQAM) 122 or EQAM modulator may be in the head end or hub device for receiving packets of digital content, such as video or data, re-packetizing the digital content into an MPEG transport stream, and digitally

modulating the digital transport stream onto a downstream RF carrier using Quadrature Amplitude Modulation (QAM). EdgeQAMs may be used for both digital broadcast, and DOCSIS downstream transmission. In CMTS or M-CMTS implementations, data and video QAMs may be implemented on separately managed and controlled platforms. In CCAP implementations, the CMTS and edge QAM functionality may be combined in one hardware solution, thereby combining data and video delivery.

[0038] Orthogonal frequency-division multiplexing (OFDM) may utilize smaller sub-bands (compared to QAM carriers). For example, while a conventional DOCSIS QAM carrier is 6 MHz wide, the CATV system may employ orthogonal frequency division multiplexing (OFDM) technology with OFDM carriers that are approximately 25 kHz to 50 kHz wide. Thus, where previously 100 QAM carriers were used, thousands of OFDM subcarriers may be used. OFDM technology may be suitable for noisy signal conditions and may enable use of more of the available spectrum without reducing the quality of server. In example implementations, a cable network may use the QAM modulation for downstream speeds and boost upstream speeds using OFDM.

[0039] FIG. 2 shows a representative schematic of a basic push-pull transistor amplifier 200 that amplifies an input signal 210 driven by a differential voltage from supply V2 to produce an output signal 220 through resistor R14. The amplifier 100 draws current supplied to two transistors Q1 and Q2 to provide the desired amplified signal voltage across the resistor R12. Resistors R11 and R12 set an input impedance to the amplifier of around 200 Ohms. Power supply V4 provides a common voltage to the inputs that is used to set a current bias point of the amplifier. Each transistor has a feedback resistor R2 and R4, respectively to the collectors of the transistors, which

are connected to the low impedance differential load R10 that is provided the output voltage signal 220 across it. Transformer 230 connected to voltage source V1 is also used to bias the amplifier by providing a high impedance to differential signals and a low impedance to common mode current.

[0040] FIG. 3 shows the input current 250 through resistor R11 and the output current 260 through the resistor R14 of the amplifier circuit 200, for a multi-channel modulated RF signal typical for CATV nodes. The current gain is large (> 20x). The output amplitude is usually close to an average rms value but occasionally high amplified signal peaks occur. The peak values are typically on the order of 6 times the rms value with a relatively low probability (in time) on the order of 10^-6. However, since amplifier clipping leads to bit errors in RF communication links, the amplifiers must amplify these peaks with high fidelity even though the occurrence rate is relatively low.

[0041] In order to provide the required current gain to amplify a signal with the large signal peaks shown in FIG. 3, the amplifier must usually be biased at a high current. Thus can be most easily seen in FIG. 4, which shows the amplifier current used by the transistor Q2 in the amplifier 200 of FIG. 2 where the amplifier is biased at approximately 80 mA. When amplifying the signal 250 shown in FIG. 3, during the peak in output voltage the current in the transistor Q2 falls to just under 10 mA. At 0 mA the amplifier would have been unable to further amplify the signal and clipping distortion would have occurred. Stated differently, were the amplifier circuit 200 not biased to 80 mA but biased at a lower point, or alternatively, if the input to the amplifier had a higher signal peak to be amplified, clipping would have occurred along with the attendant signal degradation (bit error) that accompanies distortion from amplifier clipping.

[0042] RF amplifiers in an HFC network typically operate in a "Class A" mode of operation, meaning that they provide a high fidelity amplified signal where the bit error rate should be no more than approximately 10^{-8}. As just noted, given that the signal peaks occur at a rate of 10^{-6}, i.e. 100 times the frequency of the required bit error rate, the RF amplifiers in an HFC network must provide a sufficiently high bias point that only approximately one in a hundred or less of the amplified signal peaks are clipped. Because the signal peaks occur so infrequently, however, and because the signal peaks are approximately six times higher than the rms value of the signal, biasing the amplifier to account for the signal peaks makes the amplifier circuit highly inefficient. In a typical case, for example, to provide 100mW of total RF output of the amplified signal, about 10W of power is required, i.e. only about 1% of the power supply to the amplifier is used to provide the RF energy output while the remainder of the power is consumed to bias the amplifier at a current that is almost always much higher than necessary to amplify the signal, except for the infrequent signal peaks.

[0043] There are more than four million amplifiers dispersed throughout HFC networks in the United States alone. This translates into a total energy consumption in the millions of dollars per year, which as just noted is mostly energy that is only needed to amplify highly sporadic signal peaks.

[0044] FIG. 5 shows an exemplary receiver 300 capable of being used in a node 104 to modulate an amplifier power supply so as to efficiently attain amplified RF output power with much lower power dissipation than existing amplifiers. The receiver 300 may preferably include a decompression module 310 that receives radio frequency data and decompresses it, but could also include other means to generate a digital waveform. Prior to amplifying the decompressed data, the receiver 300 introduces a delay 320 before processing the signal by an optional pre-distortion

module 330 and inputting the signal to a D2A converter 340 that drives the input signal to an amplifier 350 having a gain block 360 and power supply 370.

[0045] During the delay 320, the receiver 300 preferably includes an analysis module 380 that analyzes the decompressed radio frequency data, i.e. the same data that comprises the input signal to the amplifier 350, and uses the data to create a modulation signal to the power supply 370 through D2A converter 390. The modulation signal can comprise any one of a number of alternate forms. For example, in a simple embodiment, the power supply 370 may be modulated in a binary manner between a normal (low) bias point used during the periods when the signal is not experiencing signal peaks and a peak (high) bias point when the signal is experiencing signal peaks. Because of the delay 320, the bias point of the amplifier 350 may be modulated in a synchronous manner with the signal that it amplifies so that the bias point is raised as the signal experiences a peak and is lowered as the signal falls from the peak. In other embodiments, more complicated modulation schemes may be employed, such as switching the bias between more than two bias points to account for variances in the amplitudes among signal peaks, or even modulating the bias voltage or current of the amplifier in a manner that is linear with respect to the signal amplitude at any point in time. It should be understood that the delay 320 may be introduced at any time before amplifying the data so that the amplified data coincides with the modulation signal, and that the illustration of the delay occurring after decompression is illustrative only, particularly given that some systems may not include compressed data, or otherwise need to decompress data for amplification.

[0046] The receiver 300 may also optionally include many of the components that make up a digital return transmitter, with the addition of an A2D converter. The digital forward receiver can thereby perform the function of a digital return

transmitter with bandwidths of 85, 2x85, 200 or 2x200 MHz using a bidirectional optical pluggable in the 4.25 Gbs or 11.3 Gbs port. Thus, the digital forward receiver can be converted to essentially most of the components of a node with forward and reverse traffic for a small added cost.

[0047] As can be appreciated by those of ordinary skill in the art, the receiver 300 can use signal processing to predict power envelopes and automatically compensate amplifier artifacts due to supply modulation by generating a compensation signal in the output D2A converter. The bias point of the amplifier (current and/or voltage) may be modulated to reduce amplifier dissipation. In some embodiments, the receiver 300 can dissipate on the order of 4 times less supply power for a given output power level. Less power used by the receiver 300 enables the use of smaller transistors, a smaller heat-sink, lower cost packaging, and a reduction of the node size and power consumption.

[0048] It should be noted that while embodiments disclosed herein describe a node amplifier solution for power reduction, the concepts apply for other amplifiers in the cable network. For example, embodiments may incorporate modulation of analog amplifiers cascaded in the field that may not be driven directly by D/A converters. In an amplifier in the cascade of amplifiers, lower cost amplifiers are desirable. As disclosed, embodiments for the cascaded amplifier may provide a lower cost amplifier via the reduction of the power dissipation with a higher output power capability as an option. Where the cable network has been upgraded, lower cost amplifiers that reduce power dissipation but allow higher output are desirable.

[0049] Embodiments disclosed for creating a more efficient amplifier are beneficial for existing networks and advanced or next generation networks. For example, even if an advanced architecture, e.g., the Node+0 architecture is not

adopted, amplifiers that are more power efficient are still desirable. Given that amplifiers compensate for the losses in the leg preceding them, a universal setting from the node works on a collection of amplifiers. As most amplifiers have a similar tilt and gain setting and are operated with a similar power load, by and large the same setting will apply to a chain of amplifiers. Architectures will have shorter and shorter amplifier chains to settle on advanced architectures, e.g., N+1 or N+2.

[0050] The disclosed digital forward architecture permits very low cost and power efficient nodes. For example, embodiments for the disclosed digital forward techniques allow small cost and power efficient node designs that enable node replacement and also fiber deep architectures that are currently inhibited by node cost and by maximum wavelength counts on fiber. Furthermore, in embodiments where all processing is in the digital domain, there is flexibility in the band-split of such a design. Almost any RF gain stage can benefit from the disclosed techniques where a digitized input signal is made, delayed, and used as a decision input for a power supply and predistortion input. Existing standard HFC gain stages do not have a benefit of the digitized signal, thus the disclosed digital forward (and digital return) systems disclosed may benefit from the disclosed techniques for the receiving side of the system and the corresponding output RF gain stage (with a cost effective, minimal functional blocks/cost addition).

[0051] It should be noted that various implementations for the disclosed techniques are possible wherein the supply voltage and/or the transistor bias are modulated. The push and pull transistors may be independently driven by D2A converters to permit true class B operation or class B operation combined with supply modulation. Such manipulations can cause distortions in analog the output signal; however the distortions are predictable. The digital pre-distorter 330 in the receiver

300 may optionally be used to mitigate the distortions.

[0052] FIG. 6 depicts an exemplary push-pull amplifier 400 having a power supply 410 capable of being modulated using the receiver 300 such that the bias current is high only when a high peak needs to be amplified and low otherwise by adding a voltage source V3. The voltage source V3 is driven by a signal that is generated such that the bias is high when output peaks need to be amplified. FIG. 7 shows a waveform 420 representing the voltage provided from the voltage source V3 and a waveform 430 representing the shape of the signal to amplify. The bias signal is seen to increase when an output peak needs to be amplified. In the embodiment depicted in FIGS. 6 and 7, the bias signal was digitally generated by passing samples of the signal to amplify through a peak detection circuit and a subsequent filter, while the main signal (shown in red in FIG. 7) was delayed by a number of samples such that the response of the bias signal would coincide with the signal peak.

[0053] FIG. 8 illustrates an embodiment in which an analysis module 450 may detect both positive and negative peaks, and may calculate the absolute value of the RF signal to amplify before performing a peak detection or power detection operation. The amount of delay 460 is set such that the bias signal, after filtering by filter 470, can reach a peak value concurrently with a peak in the RF input signal to amplify. The RF signal can be output to a D2A converter to create an analog signal. The control bias signal can also be output to a D2A converter to create an analog bias signal.

[0054] Resulting input waveform 480 and output waveform 490 from the embodiment of FIG. 8 are each shown in FIG. 9, which can be easily seen as a reproduction of the input and output waveforms of Fig, 3. FIG. 9 shows that the receiver's amplification of the input signal is unchanged. However, as can be seen in FIG. 10, the current from the power source V1 is no longer a constant current. The

modulation of the bias point of the transistors results in a modulation of the power supply current from the transformer 415 of FIG. 6. FIG. 10 illustrates that when the output signal peak occurs the bias is actually high, peaking as high as 200 mA in this example. On average the bias current is much lower than in the previous example; 82 mA in this case. The power consumption of the amplifier has been reduced by a factor of approximately two (as seen in comparison to waveform 430 of FIG. 7). The transistor currents are shown in FIG. 11; as with the comparison for FIG. 11 and FIG. 7, the comparison of FIG. 11 to FIG. also shows an approximate reduction in power by a factor of two, where the lowest value is again just under 10 mA, but this is accomplished by a bias current of only approximately 40mA per transistor instead of the original 80 mA.

[0055] Because the power supply via transformer 415 of FIG. 6 is insensitive to common mode current fluctuations (these are passed with little resistance) and because the differential output signal in R14 is also not sensitive to common mode fluctuations, the push-pull amplifier shown in FIG. 6 is particularly suitable for modulation of the bias current without affecting the signal to amplify because the bias control signal is self-cancelled in the output resistor R14. FIG. 12 illustrates an input signal 500 and output signal 510 that are scaled to approximately the same magnitude and compared; the input signal is amplified and reproduced with high fidelity.

[0056] In CATV systems, however, extreme requirements can be applied to the fidelity of signal amplification. It is known that there is some dependence of the distortion behavior of amplifiers on the bias point. Accordingly, FIG. 13 shows an analysis module 550 that includes a linearizer 560 that applies a linearization function in the delayed signal path to drive the amplifier, where the parameters of the linearizer can optionally be controlled by the bias point of the amplifier. The implementation of

the linearizer can be similar to linearizers used in laser optic transmitters (e.g., linearizer implementations that include digital signal implementations in FPGAs and discrete component implementations in RF components) such as U.S. Patent Nos. 8,064,777, 8,547,174 and 8,145,066 as well as U.S. Patent Application Pub. No. 20030001670. The embodiment shown in FIG. 13 is suitable for systems where the signal is digitally processed such that all operations are in the digital domain. However, it should be understood that an implementation in the analog domain with RF components is also possible, including peak detection, delay, bias signal generation and/or linearization functionalities.

[0057] It should also be understood that in some embodiments, the bias control signal and the RF signal to amplify need not be generated separately on D2A converters. For example, FIG. 14 depicts a push-pull amplifier 600 having two voltage sources 610 and 620 driving the differential transistor amplifier, each voltage source providing both bias control and RF signal information to the transistors. The overall signal amplified by the transistors can be the same as in the example depicted in FIGs. 9-11.Moreover, while the amplifier bias current can be controlled and modulated to reduce power dissipation, the amplifier bias voltage can also be controlled and modulated to reduce power dissipation or a combination thereof.

[0058] In some embodiments where the power supply is modulated, the combination of bias current and voltage supply modulation can yield further power savings, for instance by a factor of four instead of a factor of two as was shown with bias modulation only. However, the construction of a modulated voltage supply is more complex than modulating the bias current of the transistors. FIGS. 15-17 show embodiments for a power supply with energy stored in an inductor that supports power delivery during normal operation and during voltage transients FIG. 15, for

example, shows a power supply 700 with the main power supply 710 set to 11V, for example. The power supply 700 may provide current through inductor 715 with a parasitic internal resistance R1 (e.g., a 10 mOhm to 1Ohm resistor, 900 mOhm in this example). A variable voltage source 720 comprising a series connection of first fixed voltage source 725 and a second variable voltage source 730 is shown connected in parallel with the load 735. The variable voltage of the voltage supply 730 is made to be proportional to a bias control signal.

[0059] As shown in FIG. 16, in a bias voltage control transient, the voltage across load R2 peaks from around 10V to around 22 V, as seen in curve 740. The current from power supply 710, seen as curve 745, is fixed at about -1A. The current from power supply 720, seen in curve 750 peaks to about -1.2A during the transient, but otherwise it is small (-0.1 A or less). Except for the transient, nearly all the power is delivered by power source 710. Power source 720 has enough headroom to provide twice the supply voltage but only delivers power during the transient and while it is delivering power the power source 710 continues to deliver power due to the inductance of the inductor 715 that holds the current constant during the transient. As a result the average power delivered by power source 710 (1A) is much larger than the average current from source 720 (0.12 A). Since power source 725 needs to be able to reach 22V it is generally implemented with a 22 V source and a transistor stage following that to create the transient waveform. Thus we can estimate power dissipation in the voltage source 710 can be estimated at 11W (11V x 1A) and the power dissipation in voltage source 720 estimated at 2.64W (22V x 0.12A). The total, 13.64W is much lower than the 25.64W (22V x 1.12A) that would be the case if a fixed 22V power supply was used for the full current.

[0060] As shown in FIG. 17, some embodiments may replace the voltage

supply 725 by a capacitor 760. In this example, the capacitor 760 may self-charge to around 10V so that an external 22V supply is no longer needed. The capacitor 760 is large enough to retain the 10V difference during the surge and the voltage supply 720 can be driven from a 12 V supply; no other higher voltage supply is needed.

[0061] In some embodiments, the presence of inductor 715 is essential to keep the current through the transient voltage generator 730 low as the inductor 715 supports the average current during normal operation where the output voltage is close to the main power supply, the main power supply provides all the power, and the inductor 715 sustains that current during transients where the voltage could be much higher (for instance doubled) so that the transient voltage generator only needs to generate the additional current needed excluding the average current that was already provided by L1. Enhanced amplifier operation.

[0062] In one or more examples, the functions disclosed herein may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted as one or more instructions or code on a computer-readable medium and executed by a hardware-based processing unit. Computer-readable media may include computer-readable storage media, which corresponds to a tangible medium such as data storage media, or communication media including any medium that facilitates transfer of a computer program from one place to another, e.g., according to a communication protocol. In this manner, computer-readable media generally may correspond to (1) tangible computer-readable storage media which is non-transitory or (2) a communication medium such as a signal or carrier wave. Data storage media may be any available media that can be accessed by one or more computers or one or more processors to retrieve instructions, code and/or data structures for implementation of

the techniques described in this disclosure. A computer program product may include a computer-readable medium.

[0063] By way of example, and not limitation, such computer-readable storage media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage, or other magnetic storage devices, flash memory, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if instructions are transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. It should be understood, however, that computer-readable storage media and data storage media do not include connections, carrier waves, signals, or other transitory media, but are instead directed to non-transitory, tangible storage media. "Disk" and "disc" as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0064] Instructions may be executed by one or more processors, such as one or more digital signal processors (DSPs), general purpose microprocessors, application specific integrated circuits (ASICs), field programmable logic arrays (FPGAs), or other equivalent integrated or discrete logic circuitry. Accordingly, the term "processor," as used herein may refer to any of the foregoing structure or any

other structure suitable for implementation of the techniques described herein. In addition, in some aspects, the functionality described herein may be provided within dedicated hardware and/or software modules configured for encoding and decoding, or incorporated in a combined codec. Also, the techniques could be fully implemented in one or more circuits or logic elements.

[0065] The techniques of this disclosure may be implemented in a wide variety of devices or apparatuses. Various components, modules, or units are described in this disclosure to emphasize functional aspects of components configured to perform the disclosed techniques, but do not necessarily require realization by different hardware units. Rather, as described above, various units may be combined in a codec hardware unit or provided by a collection of interoperative hardware units, including one or more processors as described above, in conjunction with suitable software and/or firmware.

Claims:

1. A device having a processor for generating a signal output from a digital to analog converter (DAC), the digital signal having a first component to be amplified by an amplifier, and a second component for modulating a bias point of the amplifier, where the second component is based on the first component.

2. The device of claim 1 including a third component of the digital signal capable of use to pre-distort the first component prior to digital to analog conversion and amplification.

3. The device of claim 2 where the third component is based on the first component and a signal envelope of the first component.

4. The device of claim 1 where the first component and the second component have an associated delay between them.

5. The device of claim 1 where pre-distortion information is transmitted to the amplifier with said digital signal, the pre-distortion information based on said signal and an envelope of said signal.

6. A method for modulating a bias point of the amplifier, the method comprising:

receiving a first signal and a second signal

amplifying said first signal by an amplifier such that the amplified signal modulates the bias of the amplifier to reduce the power usage of the amplifier.

7. The method of claim 6 where the first signal includes a first component to be amplified by the amplifier and a second component for modulating a bias point of the amplifier, where the second component is based on the first component.

8. The method of claim 7 where the first signal includes a third component of the signal for pre-distorting the first component prior to amplification.

9. The method of claim 8 where the third signal is based on a signal envelope of the first signal.

10. The method of claim 6 where the first component and the second component have an associated delay between them.

11. The method of claim 6, further comprising transmitting pre-distortion information to the amplifier with said signal, the pre-distortion information based on said signal and an envelope of said signal.

12. A system within a CATV network for reducing a power usage of an amplifier, said system comprising:

(a) a processor that receives data to be converted to a first signal;

(b) the amplifier that amplifies said first signal; and

(c) a signal analyzer for analyzing the signal to determine a second signal for modulating a bias point of the amplifier.

13. The system of claim 12 where the amplifier includes a power supply

modulated by said second signal.

14. The system of claim 12 where said processor adds pre-distortion information to said first signal for said amplifier along with said first signal.

15. The system of claim 14 where the pre-distortion information is based on said signal and an envelope of said signal.

16. The system of claim 12 including a transmitter that transmits an amplified said first signal to a second amplifier along with said second signal

17. The system of claim 16 where the second signal is added to the output of said amplifier.

18. The system of claim 12 where said amplifier includes a plurality of transistors, each driven by a respective D/A converter that respectively converts a pre-distorted component of said first signal.

19. The system of claim 12 where said first signal is provided to said amplifier at a delay relative to said second signal.

20. The system of claim 12 further comprising:

a power supply providing bias to the amplifier with an inductor connected to a fixed voltage,

a capacitor connected to the amplifier power supply to generate a variable voltage, wherein the variable voltage is controlled by a signal derived from the envelope of a signal output from the amplifier.

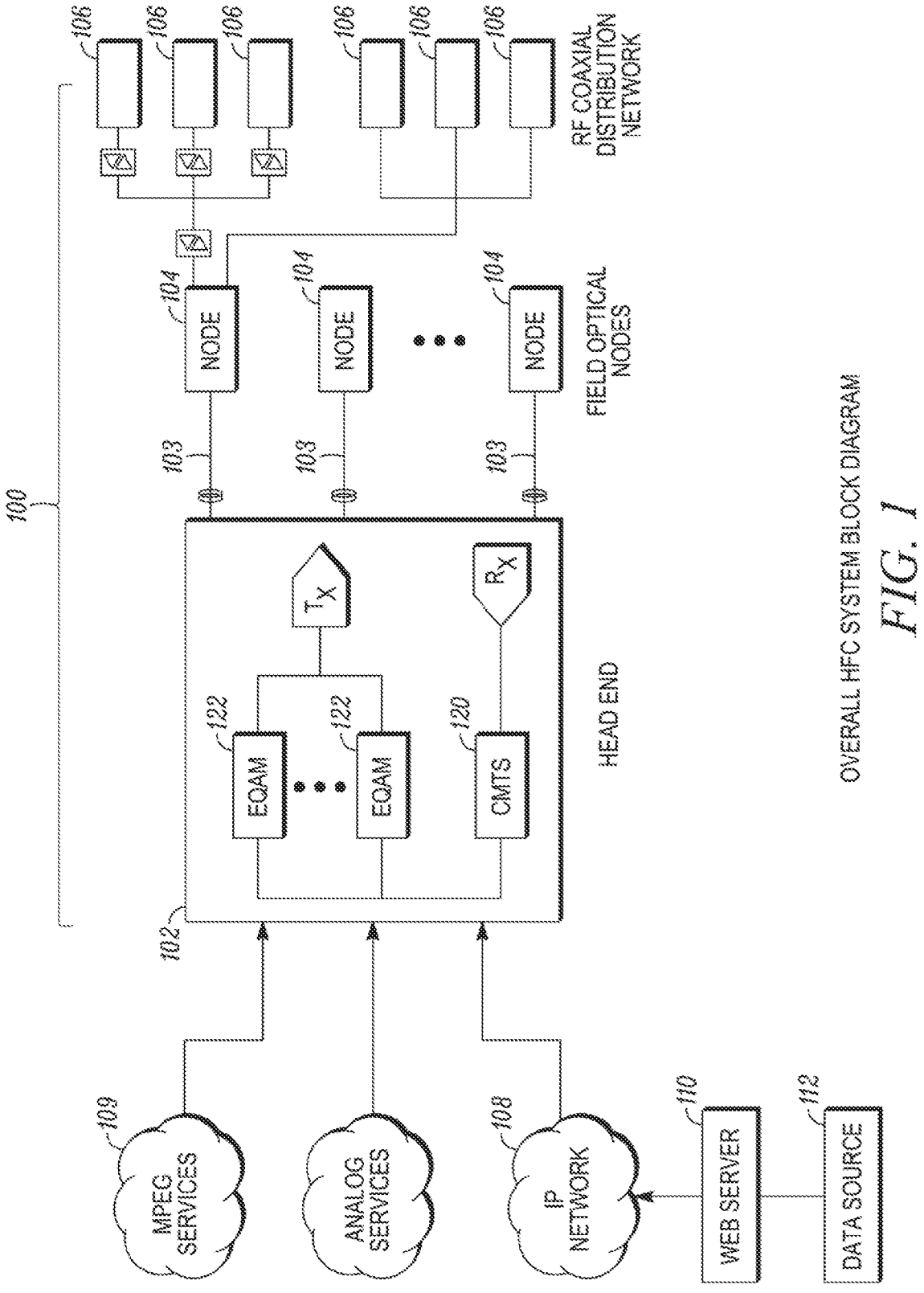
21. A system within a CATV network, said system comprising:

(a) a processor that generates a first signal and a second signal each including a first component to be amplified, said first signal including a first predistortion component and said second signal including a second predistortion component; and

(b) an amplifier comprising a first transistor and a second transistor that each simultaneously amplifies a respective one of the first signal and the second signal such that the first predistortion component and the second predistortion component jointly modulates the bias of the amplifier.

22. The system of claim 21 where the first predistortion component and the second predistortion component that jointly modulate the bias of the amplifier cancel each other at the output of the amplifier.

23. The system of claim 21 where the predistortion components carry a component that reduces amplifier distortion without cancellation of each other at the output of the amplifier.



OVERALL HFC SYSTEM BLOCK DIAGRAM

FIG. 1

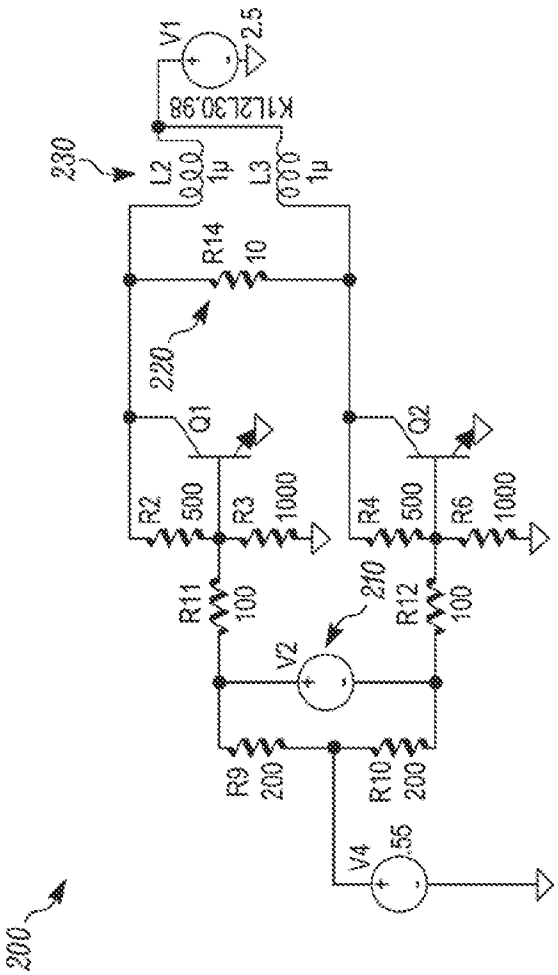

V1
2.5
K1L2L3 0.98
230
L2
0.0 0
1µ
L3
0.0 0
1µ
R14
10
220
Q1
Q2
R2
500
R3
1000
R4
500
R6
1000
R11
100
210
R12
100
V2
R9
200
R10
200
V4
.55
200

FIG. 2

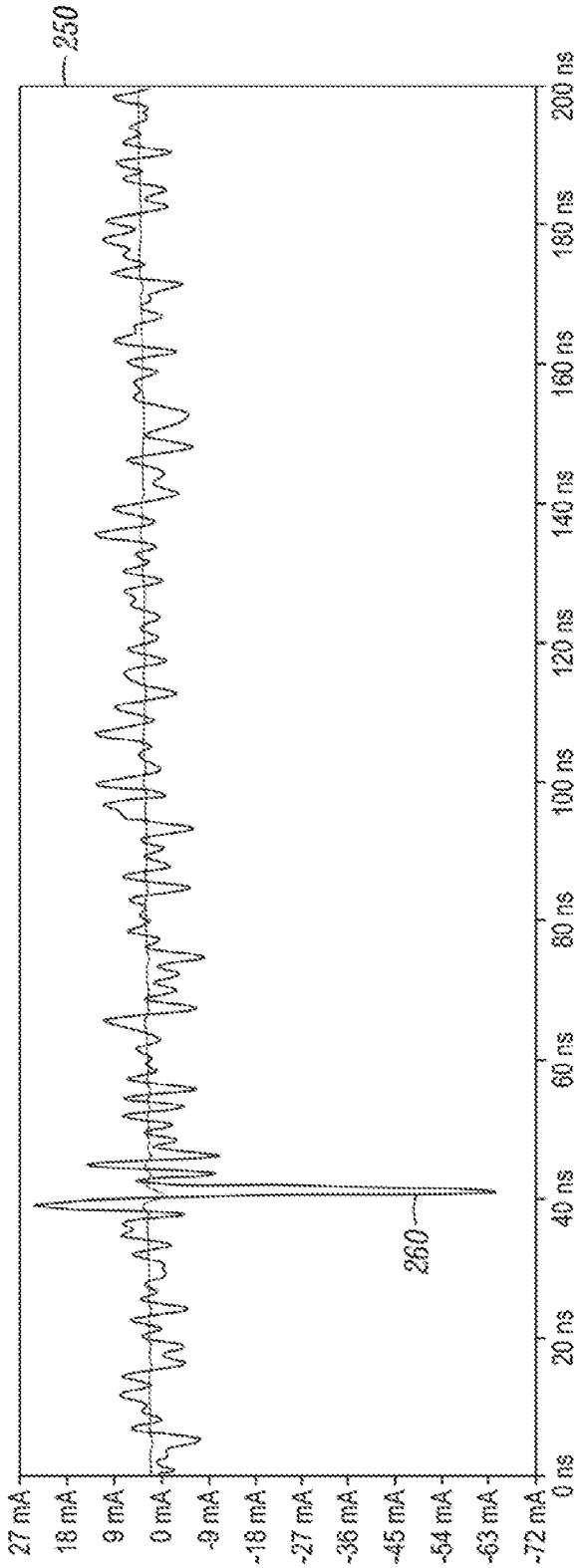

250
260
27 mA
18 mA
9 mA
0 mA
-9 mA
-18 mA
-27 mA
-36 mA
-45 mA
-54 mA
-63 mA
-72 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 3

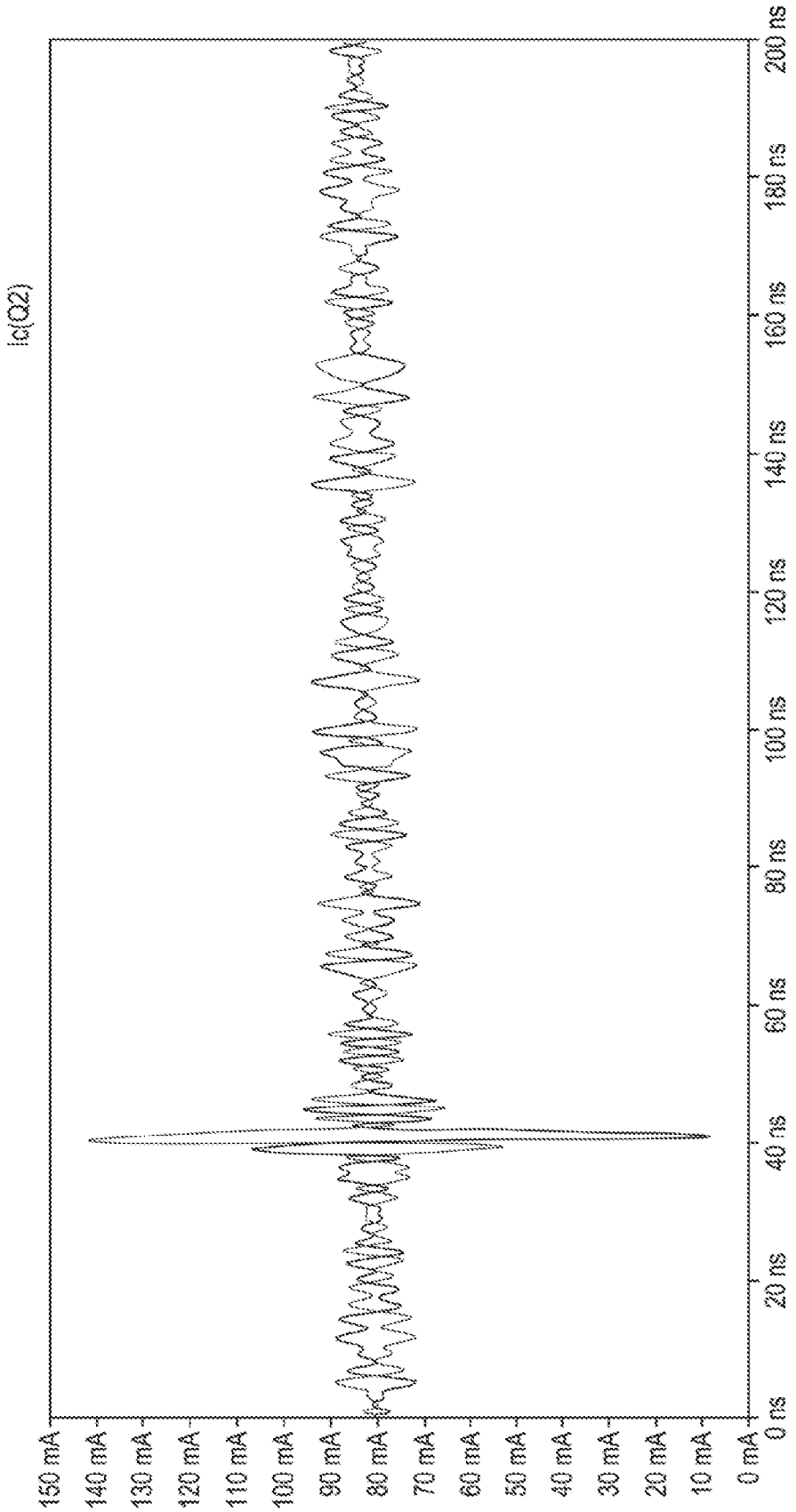

Ic(O2)
150 mA
140 mA
130 mA
120 mA
110 mA
100 mA
90 mA
80 mA
70 mA
60 mA
50 mA
40 mA
30 mA
20 mA
10 mA
0 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 4

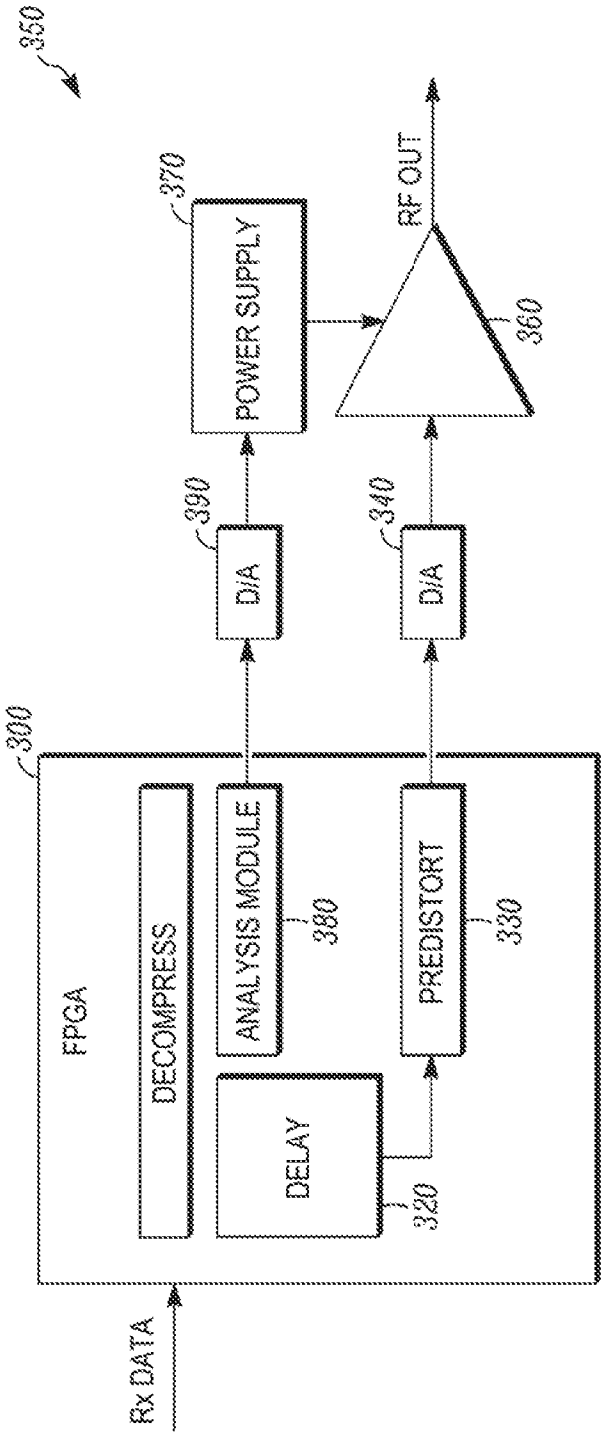

350
370
POWER SUPPLY
RF OUT
360
390
D/A
340
D/A
300
FPGA
DECOMPRESS
ANALYSIS MODULE
380
PREDISTORT
330
DELAY
320
Rx DATA

FIG. 5

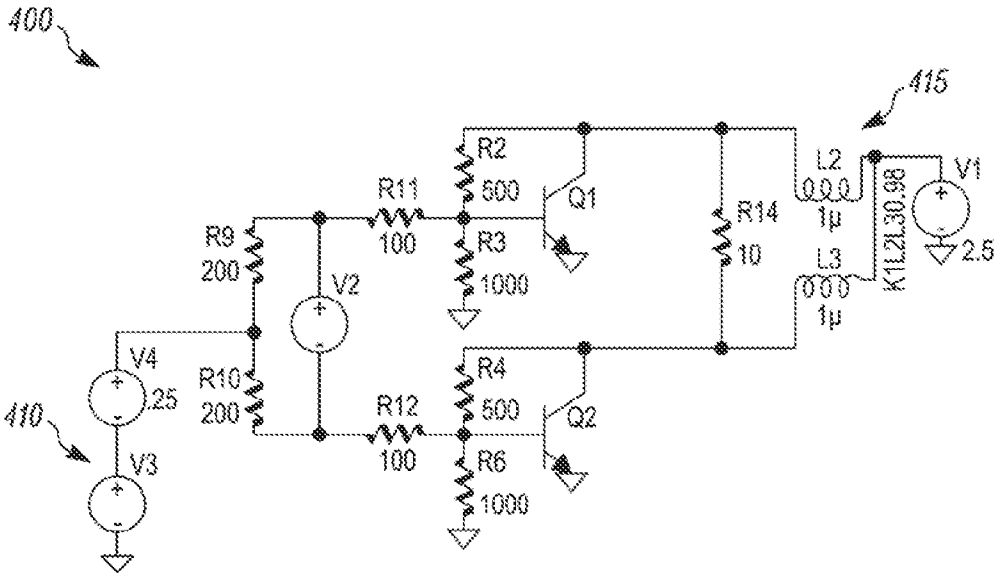

400
415
410
R2
500
Q1
R11
100
R3
1000
R9
200
V2
R14
10
L2
0 0 0
1µ
L3
0 0 0
1µ
K1 L2L3 0.98
V1
2.5
V4
25
V3
R10
200
R12
100
R4
500
Q2
R6
1000

FIG. 6

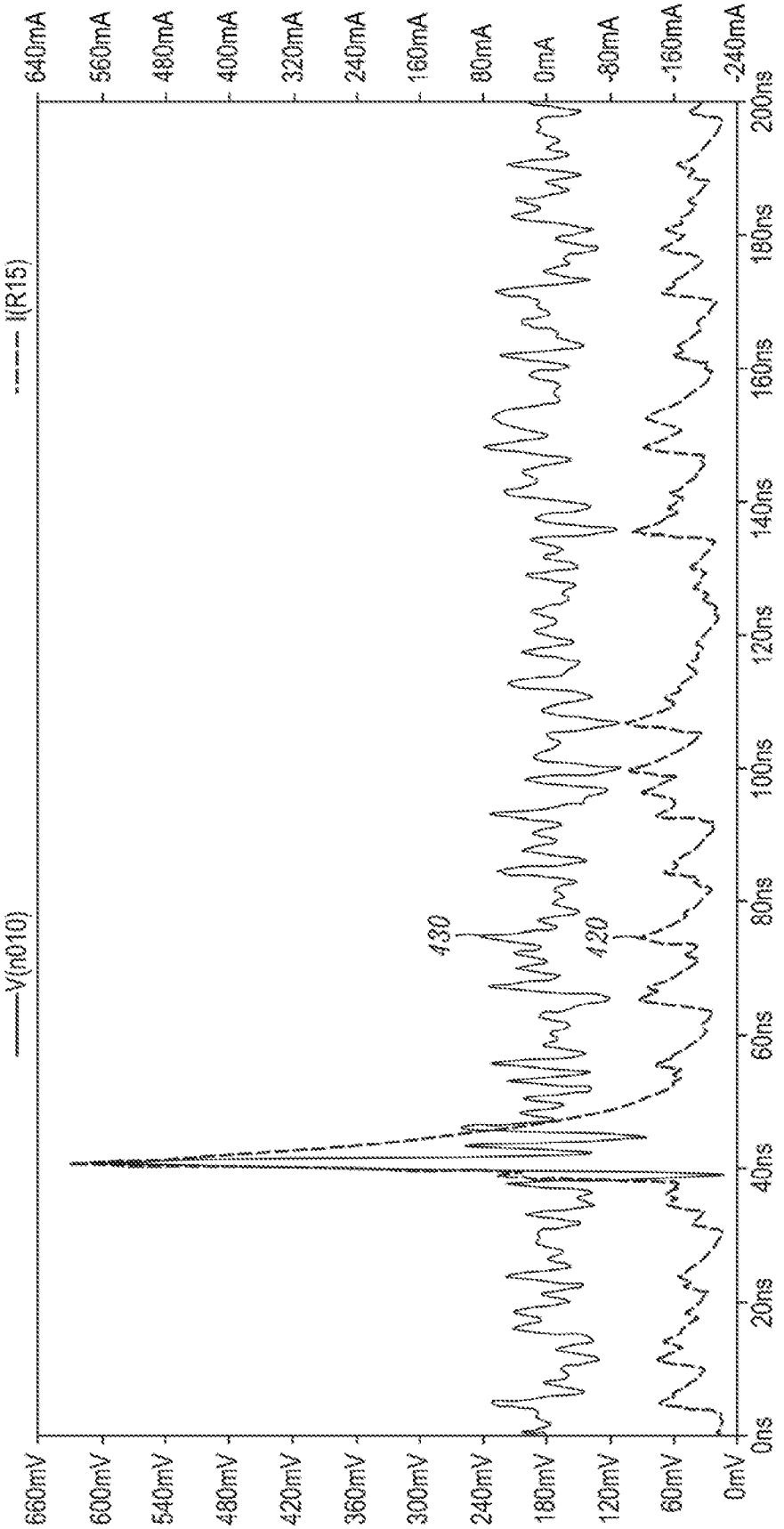

V(n010)
I(R15)
640mA
560mA
480mA
400mA
320mA
240mA
160mA
80mA
0mA
-80mA
-160mA
-240mA
660mV
600mV
540mV
480mV
420mV
360mV
300mV
240mV
180mV
120mV
60mV
0mV
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns
430
420

FIG. 7

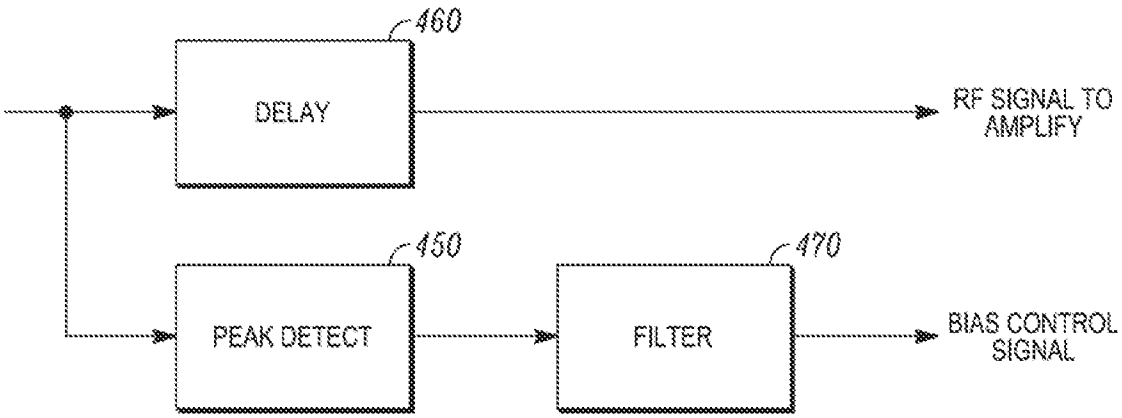

460
DELAY
RF SIGNAL TO AMPLIFY
450
PEAK DETECT
470
FILTER
BIAS CONTROL SIGNAL

FIG. 8

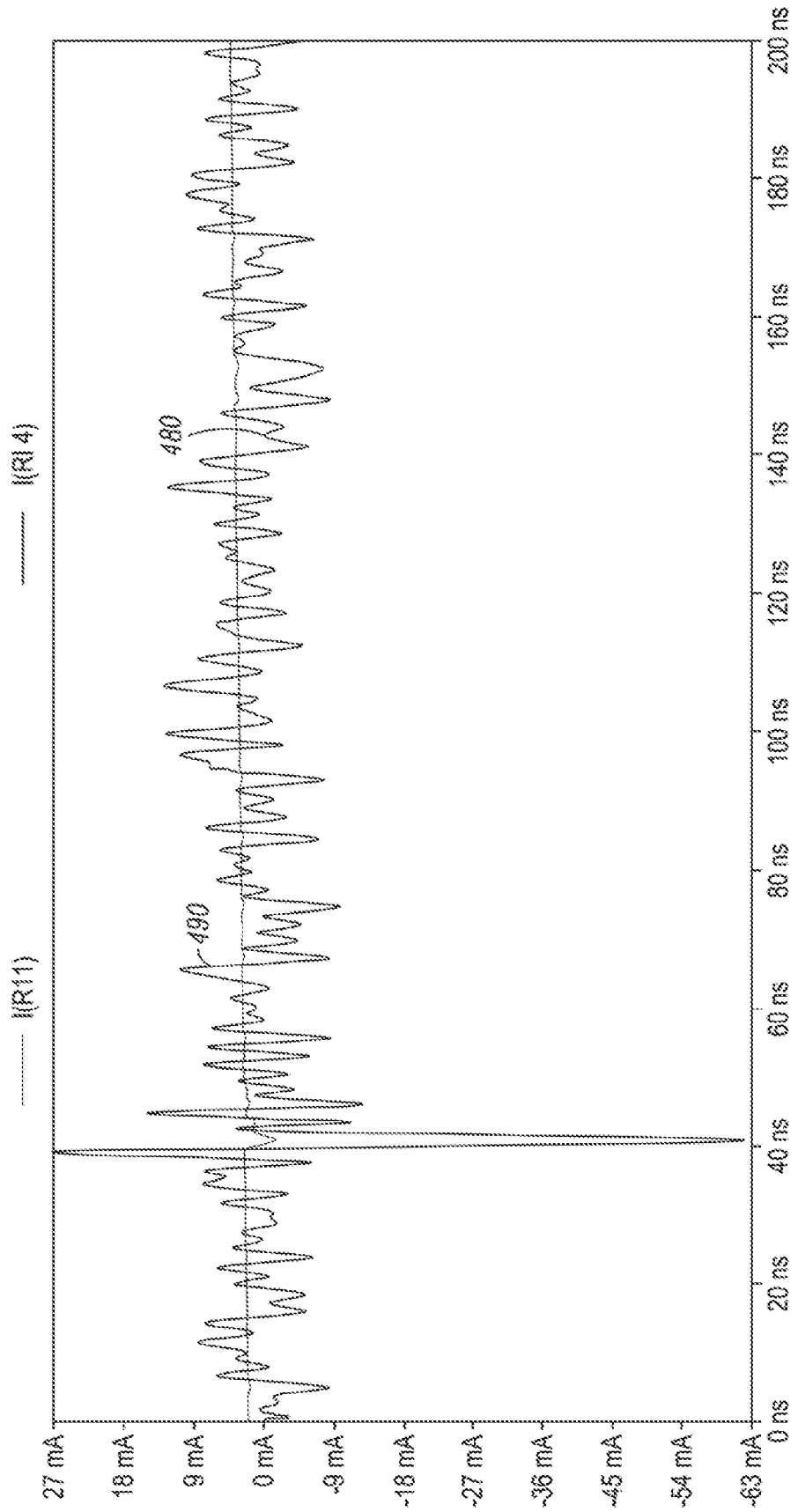

I(R11)
I(RI 4)
480
490
27 mA
18 mA
9 mA
0 mA
-9 mA
-18 mA
-27 mA
-36 mA
-45 mA
-54 mA
-63 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 9

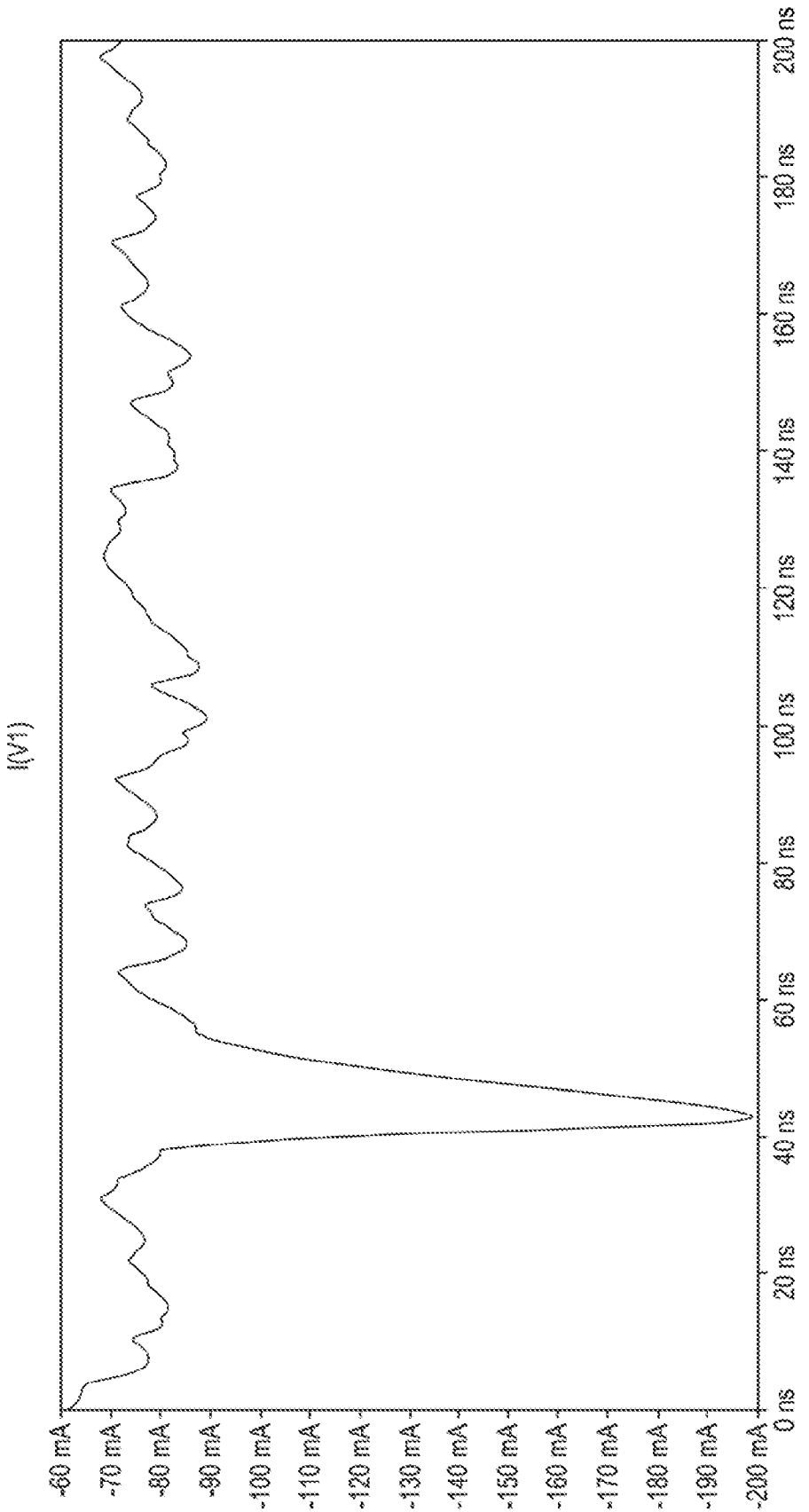

I(V1)
-60 mA
-70 mA
-80 mA
-90 mA
-100 mA
-110 mA
-120 mA
-130 mA
-140 mA
-150 mA
-160 mA
-170 mA
-180 mA
-190 mA
-200 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 10

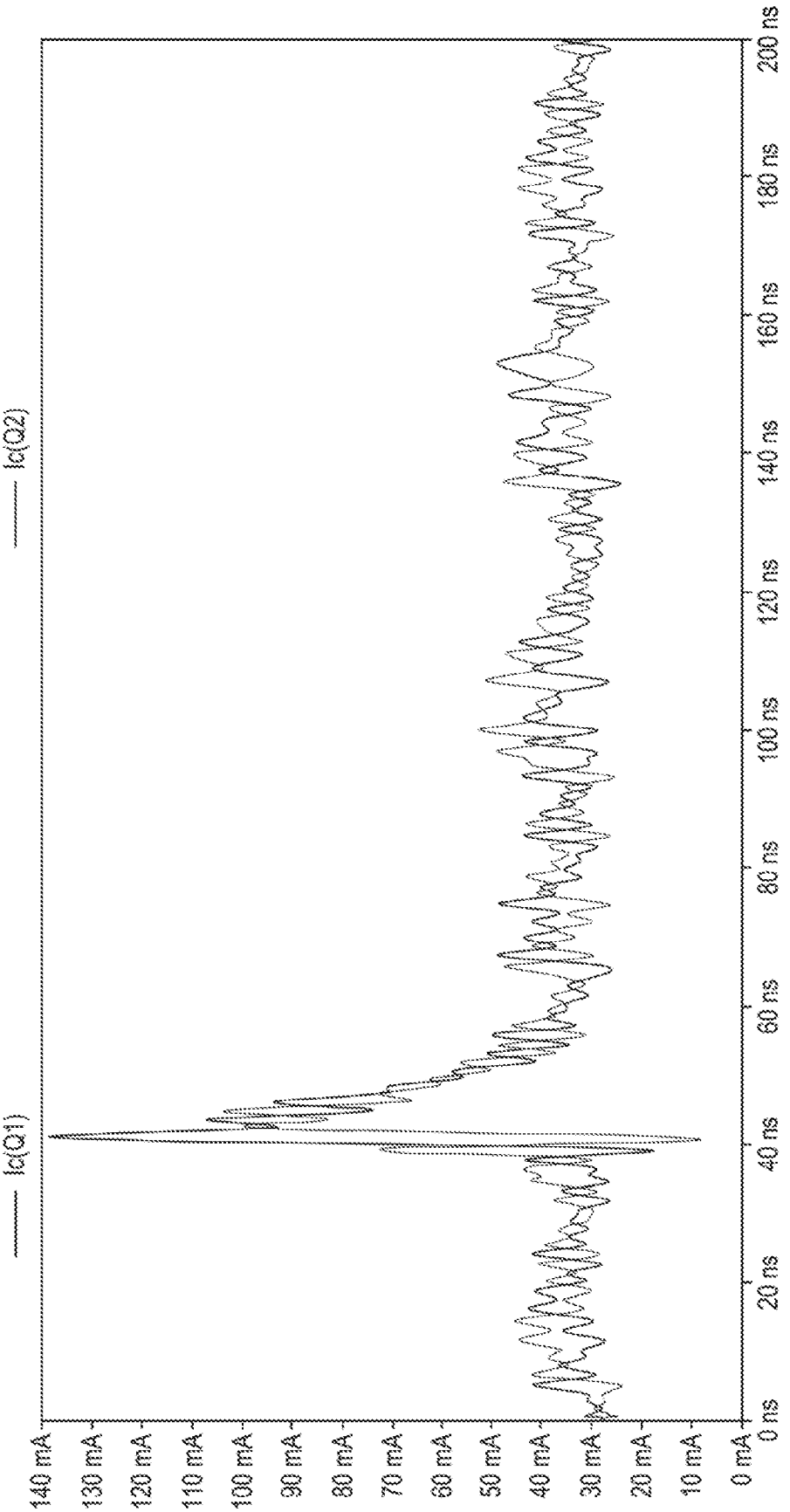

Ic(Q1)
Ic(Q2)
140 mA
130 mA
120 mA
110 mA
100 mA
90 mA
80 mA
70 mA
60 mA
50 mA
40 mA
30 mA
20 mA
10 mA
0 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 11

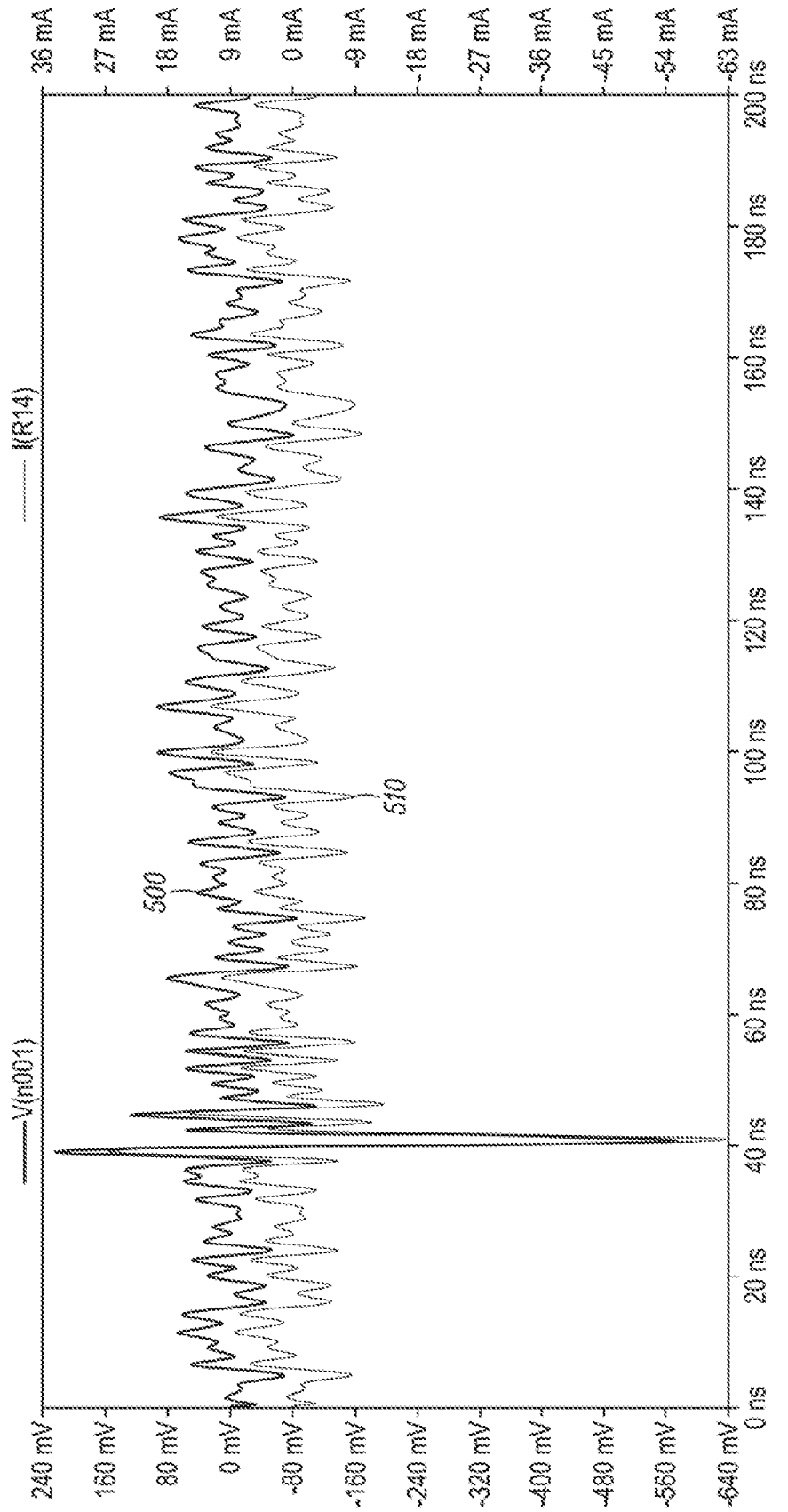

V(n001)
I(R14)
240 mV
160 mV
80 mV
0 mV
-80 mV
-160 mV
-240 mV
-320 mV
-400 mV
-480 mV
-560 mV
-640 mV
36 mA
27 mA
18 mA
9 mA
0 mA
-9 mA
-18 mA
-27 mA
-36 mA
-45 mA
-54 mA
-63 mA
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
500
510

FIG. 12

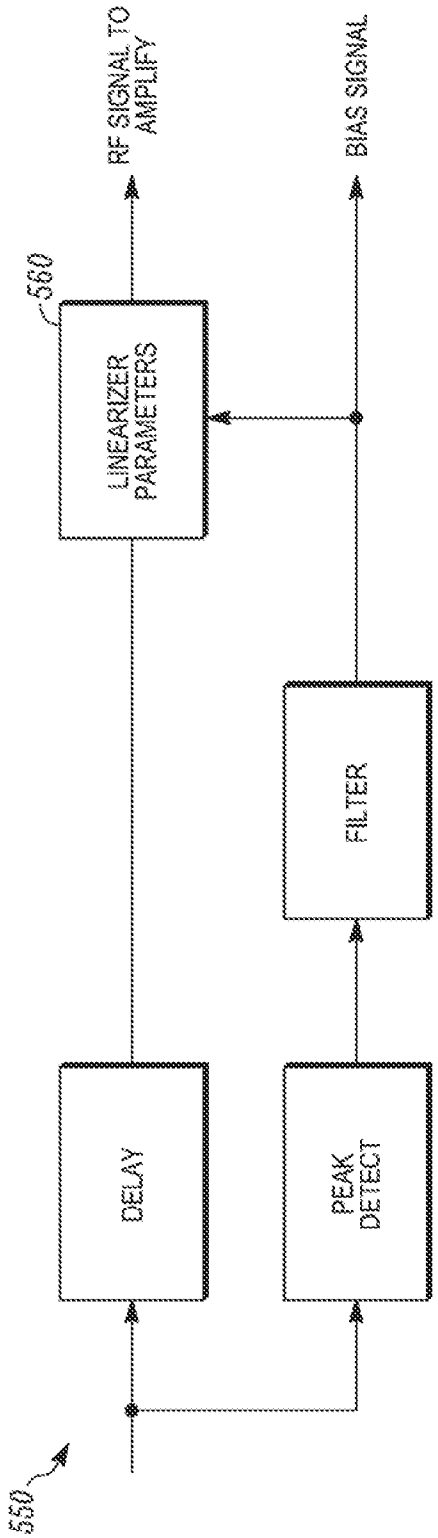

RF SIGNAL TO AMPLIFY
BIAS SIGNAL
560
LINEARIZER PARAMETERS
FILTER
DELAY
PEAK DETECT
550

FIG. 13

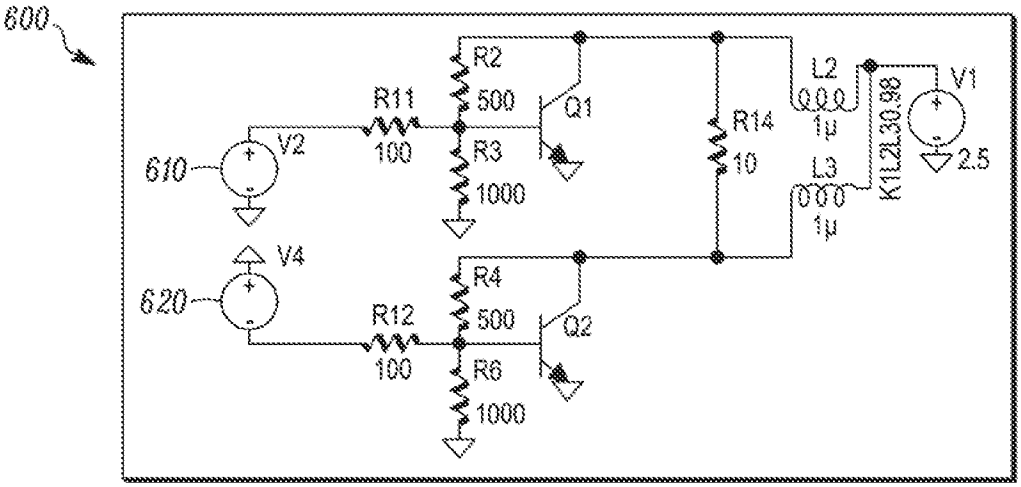

600
R2
500
Q1
R11
100
R3
1000
V2
610
R14
10
L2
1µ
L3
1µ
K1L2L3 0.98
V1
2.5
V4
620
R4
500
Q2
R12
100
R6
1000

FIG. 14

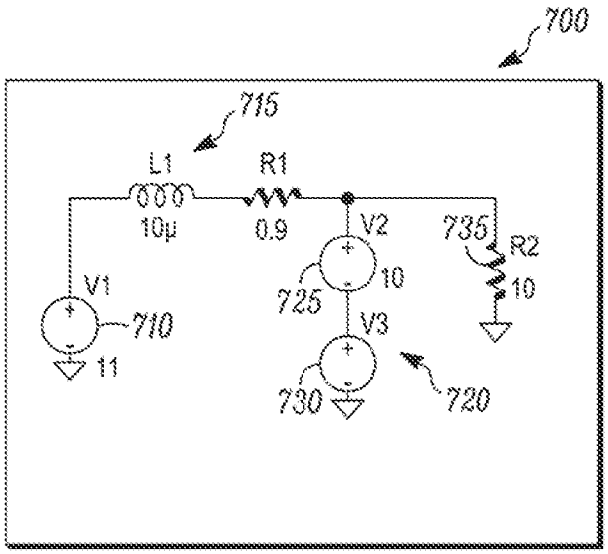

700
715
L1
10µ
R1
0.9
V2
10
735
R2
10
V1
710
11
725
V3
730
720

FIG. 15

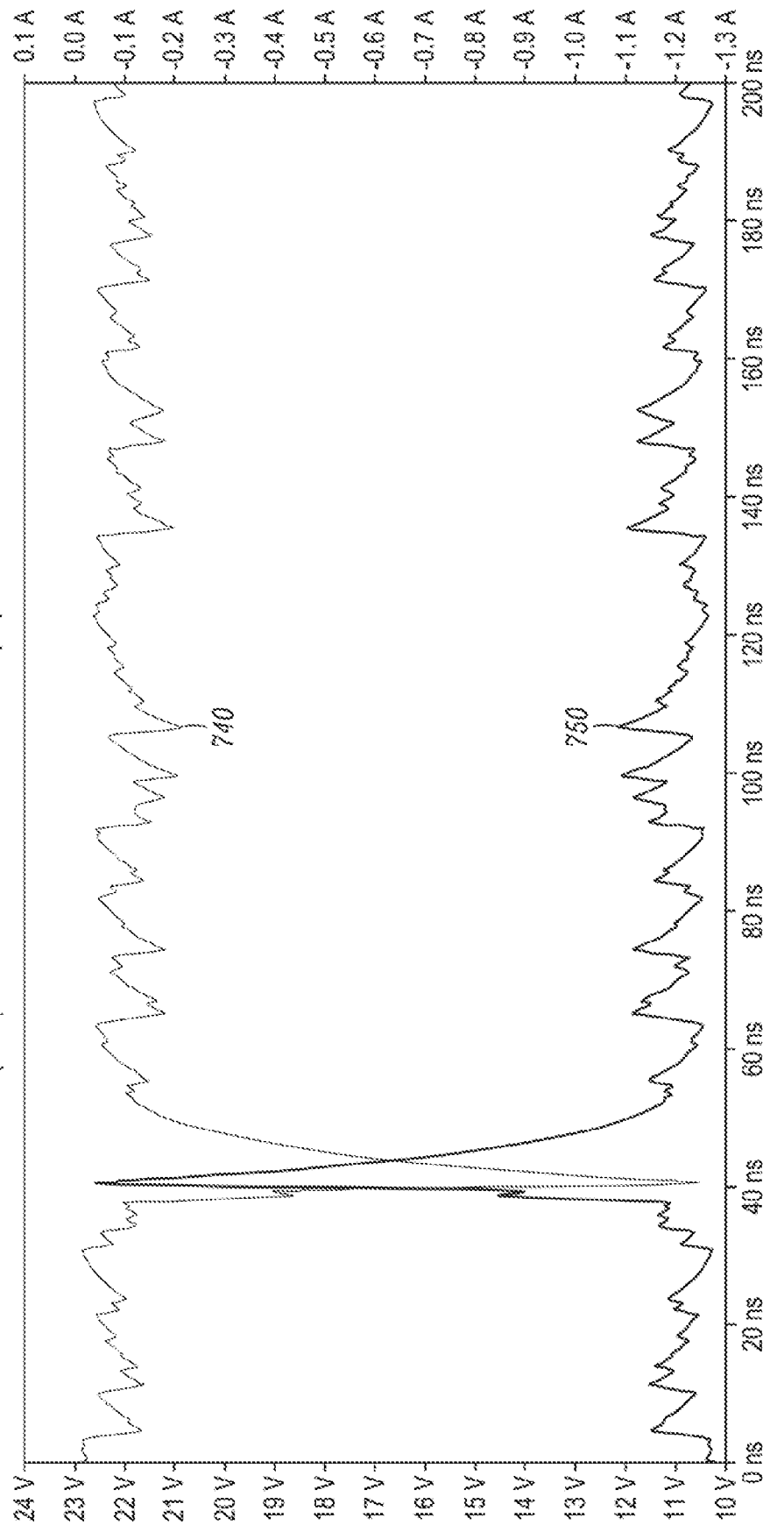

V(n003)
I(V3)
740
750
24 V
23 V
22 V
21 V
20 V
19 V
18 V
17 V
16 V
15 V
14 V
13 V
12 V
11 V
10 V
0.1 A
0.0 A
-0.1 A
-0.2 A
-0.3 A
-0.4 A
-0.5 A
-0.6 A
-0.7 A
-0.8 A
-0.9 A
-1.0 A
-1.1 A
-1.2 A
-1.3 A
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns

FIG. 16

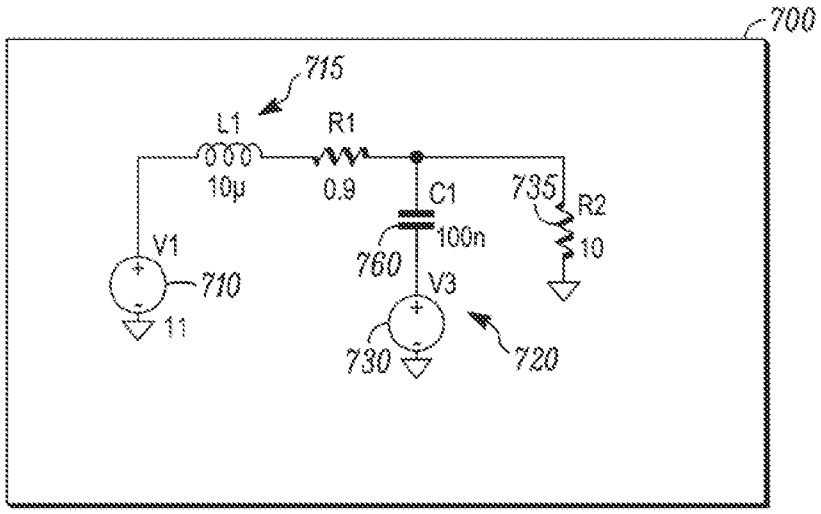


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/051663

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L12/28 H04N21/61 H04J14/02 H04N7/173 G02F1/01
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04J H04L H04N G02F H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/191877 A1 (RAKIB SHLOMO SELIM [US]) 25 July 2013 (2013-07-25) paragraph [0050] - paragraph [0056] paragraph [0176] - paragraph [0177] paragraph [0251] - paragraph [0260] -----	1-23
A	EP 0 768 765 A1 (PIRELLI CAVI SPA [IT] CORNING O T I INC [US]) 16 April 1997 (1997-04-16) column 1, line 1 - column 4, line 36 -----	1-23
A	EP 2 495 607 A2 (HUAWEI TECH CO LTD [CN]) 5 September 2012 (2012-09-05) paragraph [0003] paragraph [0006] - paragraph [0008] paragraph [0020] - paragraph [0030] paragraph [0037] - paragraph [0038] -----	1-23

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 December 2014	08/01/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Gleut, Ronan

1

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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