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Isaacs

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[54] **WIRELESS ALARM SYSTEM**

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[52] **U.S. Cl.** ..... **340/171 R**, 343/225

[51] **Int. Cl.** **H04b 7/00**

[58] **Field of Search** 340/164, 171, 167 A; 343/225; 328/111, 112; 307/234

[56] **References Cited**

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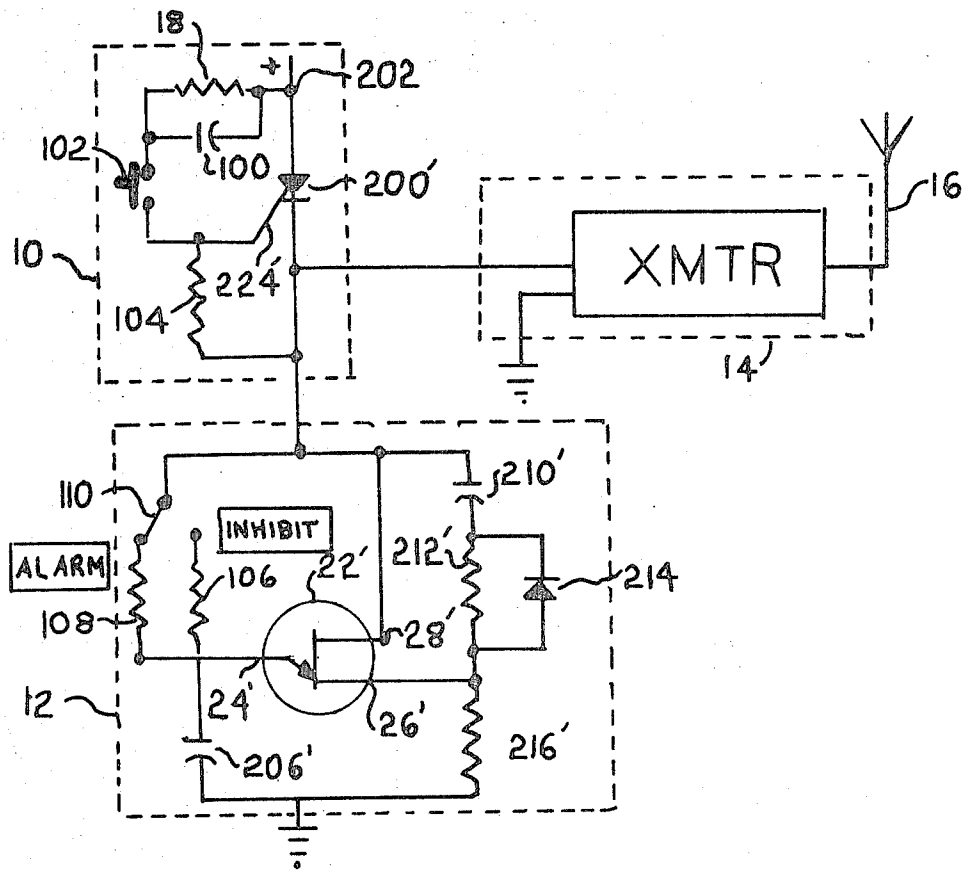
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[57] **ABSTRACT**

A wireless alarm system suitable for home and office use which includes transmitter and receiver assemblies. Two types of transmitters are includeable in this system, with one of said transmitters providing an alarm signal of a predetermined duration while the other of said transmitters selectively provides an alarm or an inhibit signal, each having different durations. The second of the transmitters may be portable, and both transmitters can send coded signals to the receiver which includes a decoder or detector means to provide a signal for operation of the receiver. An alarm is connected to the receiver and is actuated thereby upon receipt of a suitable alarm signal.

6 Claims, 11 Drawing Figures



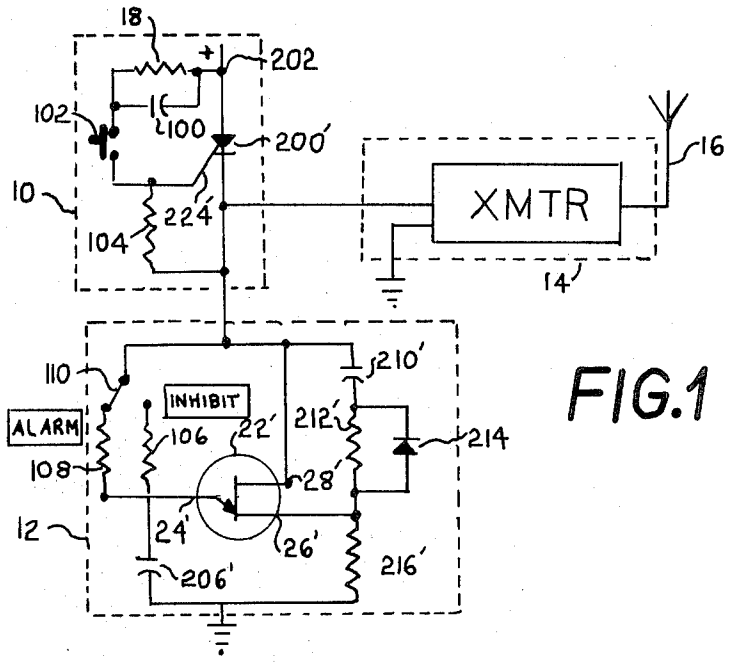

18
202
102
100
200'
16
10
224'
XMTR
104
14'
110
210'
INHIBIT
ALARM
106
22'
212'
214
108
28'
12
24'
26'
216'
206'

FIG.1

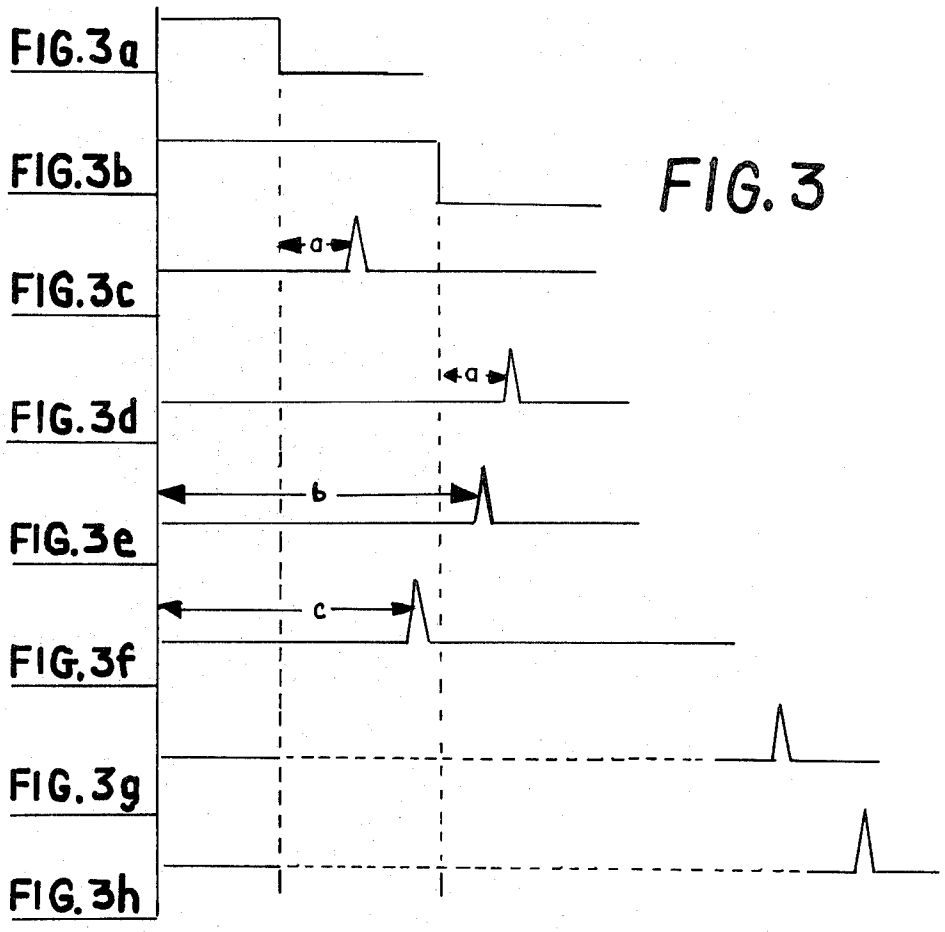

FIG.3a
FIG.3b
a
FIG.3c
a
FIG.3d
b
FIG.3e
c
FIG.3f
FIG.3g
FIG.3h

FIG. 3

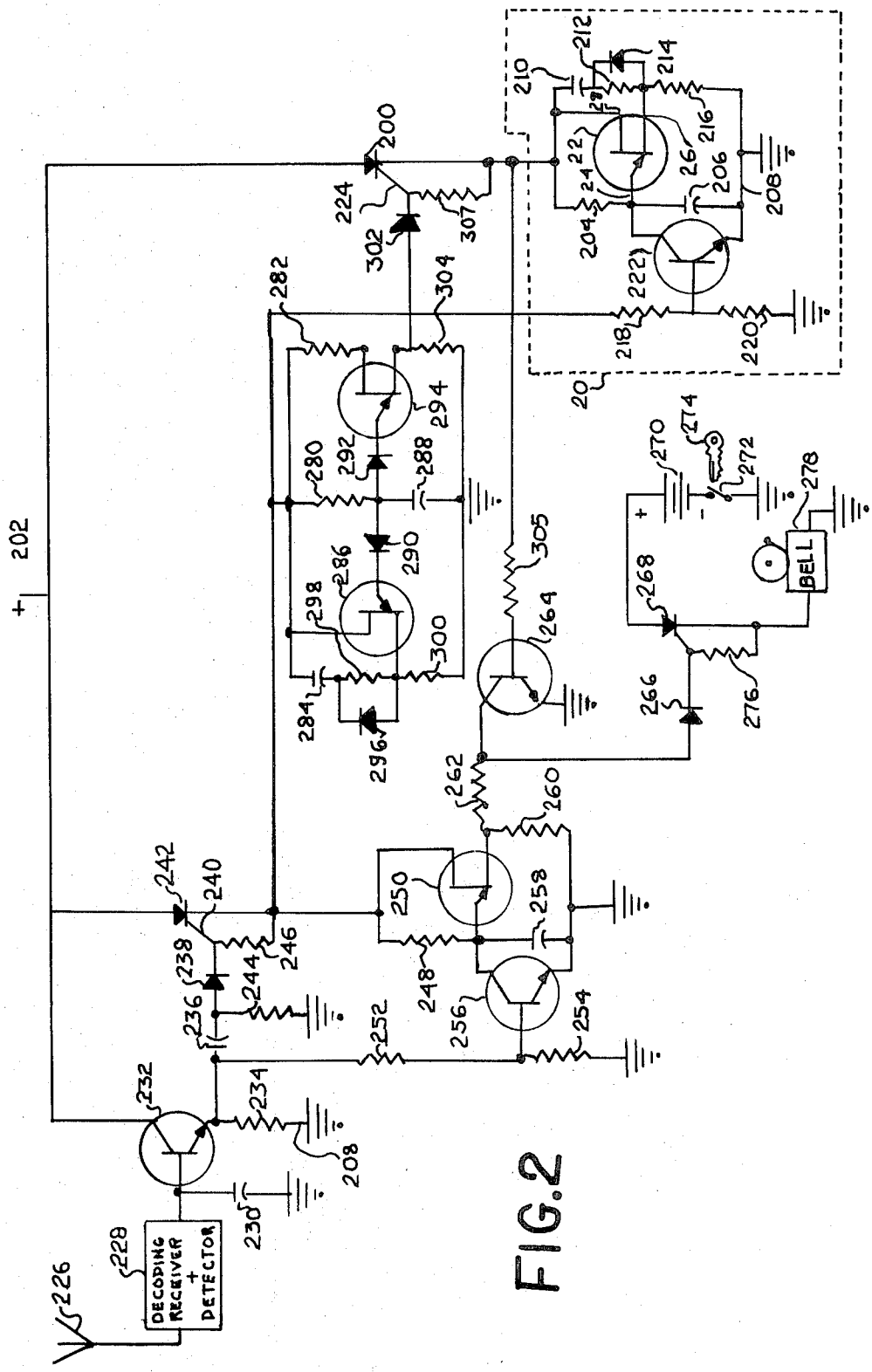

202
200
224
302
307
282
304
294
292
280
288
290
286
298
300
284
296
305
264
262
260
250
258
248
256
254
252
242
240
238
244
246
236
232
234
208
230
228
DECODING RECEIVER + DETECTOR
226
210
212
214
216
206
208
204
222
218
220
20
270
274
272
278
BELL
268
266
276

FIG. 2

WIRELESS ALARM SYSTEM

This invention relates to an alarm system, and more particularly, to a wireless alarm system.

Conventional burglar alarm systems for home and office use often require complex and cumbersome hand wiring techniques which are undesirable from many vantage points. Recently there have been developed wireless alarm systems but these systems suffer from being complex and expensive. In addition, these prior art wireless systems use only the most simple of wireless transmission techniques and are fairly easy to be overcome and bypassed by intruders.

Accordingly, this invention provides an improved wireless alarm system which seeks to remedy the above-mentioned problems and others that will become apparent hereinafter.

FIG. 1 is a schematic diagram of the transmitter assembly used with this invention;

FIG. 2 is a schematic diagram of the receiver and alarm assembly used with this invention; and

FIG. 3 (FIG. 3*a* – 3*h*) presents a plurality of timing signals illustrative of the operation of this invention.

Referring to the Figures and more particularly to FIG. 1, there is shown a schematic diagram of a transmitter assembly which comprises an actuation portion **10**, a timing portion **12**, a transmitter **14** and an antenna **16**.

Before describing the operation of FIG. 1, reference is made to FIG. 2 and to a timer circuit **20** which serves as a basic building block used in both the transmitter and receiver assemblies of FIGS. 1 and 2. The timer assembly is well known prior art and is found in the General Electric SCR Manual, 1964 Edition, on page 212. Briefly, the timer circuit comprises a unijunction transistor **22** having an emitter terminal **24**, B_1 terminal **26** and B_2 terminal **28**. For purposes of discussion herein, the B_2 terminal **28** is connected to the cathode of an SCR **200**, the anode thereof being connected to a source of voltage **202**. A resistor **204** is connected between B_2 **28** and emitter **24** while a capacitor **206** is connected between emitter **24** and a point of reference potential **208**. One end of a capacitor **210** is connected to B_2 terminal **28** while the other end is connected through a parallel combination of resistor **212** and diode **214** to B_1 terminal **26**. The anode of diode **214** is also is also connected to B_1 terminal **26**. A resistor **216** is connected between B_1 terminal **26** and the point of reference potential **208** which may be ground. A pair of resistors **218** and **220** form a voltage divider and are connected at their divider point to the base of a transistor **222** having its collector terminal connected to the emitter terminal **24** of unijunction transistor **22** and its emitter connected to ground **208**. In operation, the SCR **200** is triggered in the conventional manner by a pulse applied to its gate terminal **224** and voltage then is carried to the B_2 terminal **28**. The charge path formed by capacitor **210** and resistors **212** and **216** is much faster than the charge path formed by resistor **204** and capacitor **206** so that after a short period of time, capacitor **210** has assumed approximately the value of the positive supply voltage **202**. When capacitor **206** thereafter charges to a predetermined voltage level, the unijunction transistor **22** will turn on causing a trigger pulse to develop at B_1 terminal **26**. This positive trigger pulse is carried through the now forwardly biased diode **214** and through capacitor **210** to place a more positive voltage on the cathode of SCR **200** than on its anode thereby turning off the SCR and turning off the power previously carried therethrough to timer circuit **20**. In addition to that described above, transistor **222** when in a saturated condition serves as a reset means since it discharges or damps capacitor **206** and also prevents capacitor **206** from being charged and therefore, adds an additional amount of timing control to the timer **20**. Transistor **222** can be saturated by means of a sufficiently positive voltage occurring at its base terminal.

Referring again to FIG. 1, there is shown the timing control **12** which includes a timer circuit substantially similar to the timer circuit **20** described above except for the omission of transistor **222**. Therefore, the same numerals have been used with primed designations to illustrate the same components. The transmitter assembly includes the previously described SCR **200'** having its anode connected to the source of positive potential **202** with a parallel combination of a resistor **18** and a capacitor **100** connected between the source of positive potential **202** and one side of a push button switch **102** the other side of which is connected to the gate electrode **224'** of SCR **200'** and through a resistor **104** to the cathode of SCR **200'**. The transmitter **14** is conventional and is powered from the cathode side of SCR **200'** and will be so powered as long as the SCR is conducting.

As contemplated, the transmitter **14** provides a coded signal which may be coded in frequency or time domain to make the present system relatively foolproof.

There is shown in the timer control circuit **12** of FIG. 1 two selectively controlled resistors **106** and **108** connected between B_2 terminal **28'** and the emitter terminal **24'**. The selectivity of those resistors is controlled by means of a switch **110**. For purposes herein, it will be assumed that resistor **108** is permanently wired into the timer control **12** while hereinafter the description will include a resistor **106**. In operation, a push button switch **102** is depressed either by manual means or by a magnetic switch or sensor located at an entry point to the protected premises. Switch **102** may also be a fire sensor or other transducer responsive to certain environmental conditions. When the switch is closed, a surge of current flows through capacitor **100** to trigger SCR **200'** into its conducting condition. As soon as this occurs, transmitter **14** begins to send its coded signal. A predetermined period thereafter, the peak voltage developed when unijunction transistor **22'** begins to conduct which is carried through diode **214'** back biases SCR **200'** to cut off the supply of power to the transmitter thus terminating its operation. The duration of time during which transmitter **14** is sending its coded signal is controlled by the charging rate as determined by resistor **108** and capacitor **206'**. As indicated hereinabove, resistor **106** can be selectively utilized with capacitor **206'**, so that the charge time is changed in order to change the duration of time during which the transmitter **14** is operating. At this point, and for ease of identification, resistor **106** will be identified as setting a duration which is identifiable as an inhibit duration, while resistor **108** will control a time duration identifiable as an alarm duration. Other time durations can be utilized herein to control and identify additional conditions.

As contemplated herein, most transmitters connected at points of entry will only have resistor **108** permanently wired therein, while a portable hand carried transmitter usable by an operator will have both resistors **106** and **108** and switch **110** so that an alarm or an inhibit signal may be selectively sent.

Referring now to FIG. **2**, there is shown a schematic diagram of the receiver circuit and the alarm circuit responsive to the transmitter of FIG. **1**. There is shown an antenna **226** connected to a decoding receiver and detector **228** for receiving the coded signal generated by transmitter **14** and converting the same to a DC level. The capacitor **230** is connected between the output of detector **228** and ground to damp transients from reaching the remainder of the receiver circuitry illustrated in FIG. **2**.

The output of decoding receiver and detector **228** is also connected to the base of transistor **232**, the emitter of which is connected through a resistor **234** to the source of reference potential **208**. The collector of transistor **232** is connected to the source of positive potential **202**. The emitter of transistor **232** is connected through a capacitor **236** and a forwardly biased diode **238** to a trigger terminal **240** of SCR **242**, the anode of which is connected to the positive source of potential **202**. A resistor **244** is connected between the connection point of capacitor **236** and diode **238** and ground while another resistor **246** is connected between the gate and cathode terminals of SCR **242**. The cathode is also connected to a timing circuit relatively similar to that illustrated in block **20** except as to minor variations thereof. In particular, the cathode is connected to one side of a resistor **248**, the other side of which is connected to the emitter of a unijunction transistor **250**, and the cathode is also connected to the B_2 terminal of the unijunction transistor. Resistors **252** and **254** are connected in series from the emitter of transistor **232** to ground with the connection point of the resistors being joined to the base of a transistor **256**. A capacitor **258** is connected between the collector and emitter terminals of transistor **256** and the collector is also connected to the emitter terminal of unijunction transistor **250**. One side of a resistor **260** is connected to the B_1 terminal of the unijunction transistor while the other side is connected to ground as is the emitter of transistor **256**.

In operation, when transistor **256** is saturated, capacitor **258** is prevented from charging while when transistor **256** is not conducting, a charge path is formed of resistor **248** and capacitor **258** to cause a pulse to be generated across resistor **260** when unijunction transistor **250** begins to conduct. The time delay will be discussed in more detail below.

The B_1 terminal of transistor **250** is connected through a resistor **262** to the collector of a transistor **264** and through a forwardly biased diode **266** to the gate electrode of an SCR **268**. The anode of SCR **268** is connected to one side of a battery **270** while the other side is connected through a switch **272**, preferably operated by a key **274** to ground. A biasing resistor **276** is connected between the gate electrode of switch **268** and the cathode thereof with the cathode being connected through an alarm means such as a bell **278** to ground. The cathode of SCR **242** is connected to a twin timing circuit more fully described hereinafter. The cathode is connected to one side of a resistor **280**, a resistor **282**, a capacitor **284** and to the B_2 terminal of a unijunction transistor **286**. The other side of resistor **280** is connected through a capacitor **288** to ground and through forward biased diode **290** and **292** to the emitter terminal of unijunction transistor **286** and the emitter terminal of a unijunction transistor **294** respectively. The other side of capacitor **284** is connected through a parallel combination of diode **296** and resistor **298** to the B_1 terminal of unijunction transistor **286** and through a resistor **300** to ground. The other side of resistor **282** is connected to the B_2 terminal of unijunction transistor **294**, while its B_1 terminal is connected through a forward biased diode **302** to the gate electrode **224** of SCR **200** and the B_1 terminal is also connected through a resistor **304** to ground.

Referring now to FIG. **3** in which a plurality of timing diagrams are presented, the circuit of FIG. **2** will now be discussed in more detail. FIG. **3***a* represents the time duration for an alarm signal as generated by resistor **108** and capacitor **206'** of FIG. **1**, while FIG. **3***b* illustrates the time duration during which transmitter **14** is operating when an inhibit signal is sent under timing control of resistor **106** and capacitor **206'**. As can be seen therein, the inhibit signal lasts for a longer period than does the alarm signal. The wave forms illustrated in FIGS. **3***a* and **3***b* would appear at the output of decoding receiver and detector **228**, since it produces a DC level representative of the length of time transmitter **14** is operating. When either signal is present at the base of transistor **232**, it is caused to conduct which causes transistor **256** to saturate. In this condition, capacitor **258** is prevented from charging thus preventing the timing circuit in which unijunction transistor **250** is located from operating. The pulse signal present at the base of transistor **232** is also carried through capacitor **236** to trigger SCR **242** into a conducting state thereby placing a source of positive potential at its cathode. When the alarm signal is present, that is the signal of FIG. **3***a*, transistor **256** is saturated, while after it terminates, the timing circuit including unijunction transistor **250** is enabled to operate.

Referring now to FIG. **3***c*, there is shown a triggering pulse which begins a predetermined period of time "*a*" after the termination of the alarm signal in FIG. **3***a*, said triggering pulse occuring when unijunction transistor **250** becomes conducting. Similarly in FIG. **3***d*, there is shown a triggering pulse present at terminal B_1 of the unijunction transistor which is present a time period "*a*" after the termination of the inhibit signal illustrated in FIG. **3***b*.

When SCR **242** conducts, the timing circuit including unijunction transistor **286** causes the SCR to become back biased after a predetermined period of time as discussed above with reference to block **20**, thereby interrupting the power available for the remainder of the receiver circuit. The time duration or delay of this latter circuit is identified as "*b*" in FIG. **3***e* and is at least as long as the length of the wave form illustrated in FIG. **3***b*. FIG. **3***f* presents a time delay generated by the timing circuit including unijunction transistor **294** and its time delay or duration is designated by "*c*," said duration "*c*" being greater than the duration of the alarm signal in wave form **3***a* plus duration "*a*," but less than time duration "*b*."

Illustrated in FIGS. **3***g* and **3***h* are inhibit time period wave forms of relatively long duration as compared with the time durations illustrated above.

Referring now to FIG. 2, when an alarm signal is received, a triggering pulse illustrated in FIG. 3*c* is generated at the B_1 terminal of unijunction transistor **250** which is carried through diode **266** to trigger SCR **268** into its conducting condition. Assuming key switch **274** to have closed switch **272**, the bell **278** will then sound and will continue to sound until the key switch causes switch **272** to be opened, thereby interrupting the supply of power to the bell.

The transmitter illustrated in FIG. 1 having both resistors **106** and **108** is capable of generating not only the just described alarm signal but is also capable of generating an inhibit signal. When the inhibit signal is received, it should prevent the sounding of the alarm so that the person operating the inhibit signal can enter or leave the premises without sounding the alarm. The inhibit signal is of a predetermined duration so that the entry or exit procedure may be accomplished without undue fear that the warning will be inadvertently sounded.

When the inhibit signal is received, the wave form 3*b* is illustrative of the duration during which transmitter **14** has been operated. Wave form 3*f* generated by the timing circuit including unijunction transistor **294** causes SCR **200** to conduct which places transistor **264** into a saturated state. While SCR **200** is conducting, SCR **268** cannot be triggered because of the virtual ground on the output of unijunction transistor **250** through transistor **264.** At time delay period *b*, SCR **242** becomes back biased, as described above, and therefore all power to the receiver circuit is interrupted, although SCR **200** still remains conducting. When the pulse illustrated in FIG. 3*d* at the output of unijunction transistor **250** was to have occurred, the power therefor will have been interrupted, and transistor **264** is still saturated. Therefore, the pulse generated in FIG. 3d does not cause SCR **268** to conduct and the bell is not sounded.

Although FIG. 3*d* illustrates a pulse occurring time delay "*a*" after the end of the inhibit signal, it should now be apparent that because of the turn off signal generated at time duration "b" the pulse in FIG. 3*d* will never actually occur because the power for that timing circuit will have been interrupted. As discussed above, the inhibit signal which is generated prevents the sounding of the alarm for a predetermined period of time which is generally much greater than the time delay previously discussed. In particular, the timing control circuit illustrated in block **20** will cause SCR **200** to become back biased after the time delay illustrated in FIGS. 3*g* and 3*h* depending upon whether or not the received signal is an alarm or an inhibit signal. Prior to turning off SCR **200,** transistor **264** will always be maintained in a saturated state from time period "*c*" as illustrated in FIG. 3*f* until the time periods illustrated in FIGS. 3*g* and 3*h*.

If the inhibit signal has been transmitted and the operator wants to reinhibit the circuit for the full inhibit time duration, all he need do is reactivate the inhibit button after an inconsequential time period which will cause transistor **222** of timing control circuit **20** to become saturated thus dischargin capacitor **206.**

Capacitor **230** serves to damp transients and to ensure that the receiver circuit will be responsive not only to input signals lasting a predetermined duration but will be insensitive to signals of less than a predetermined duration.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above apparatus without departing from the scope of the invention, it is intended that all matter contained in the above description and shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

I claim:

1. A wireless alarm system comprising transmitter means and receiver means,

said transmitter means comprising means for transmitting at least two signals having different durations, the first of said two signals being an alarm signal and the second of said two signals being an inhibit signal,

said receiver means being capable of receiving said alarm and said inhibit signals and comprising means for sounding an alarm only if said alarm signal is received.

2. A wireless alarm system as set forth in claim **1,** wherein said receiver further comprises alarm means responsive to a received alarm signal to energize said alarm means, and inhibit means responsive to a received inhibit signal to prevent said alarm means from being energized.

3. A wireless alarm system as set forth in claim **2,** wherein said inhibit means comprises means for inhibiting said alarm means from being energized for a predetermined period of time.

4. A wireless alarm system as set forth in claim **3,** wherein said receiver means comprises trigger means responsive to the termination of the duration of said alarm signal for producing a trigger signal, said trigger signal being coupled to said alarm means to energize said alarm means, the time duration of said inhibit signal being greater than the time duration of said alarm signal and being greater than the time at which said trigger signal is produced, said alarm means being prevented from being energized if said inhibit signal is present when said trigger signal is produced.

5. A wireless alarm system as set forth in claim **4,** wherein said transmitter means further comprises a transmitter and timing means connected to said transmitter for controlling the length of time said transmitter operates, and switch means connected to said timing means for controlling the operation of said timing means to produce either an alarm or an inhibit signal.

6. A wireless alarm system as set forth in claim **4,** wherein said receiver includes capacitor means for rejecting signals having a duration less than the duration of said alarm signal.

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