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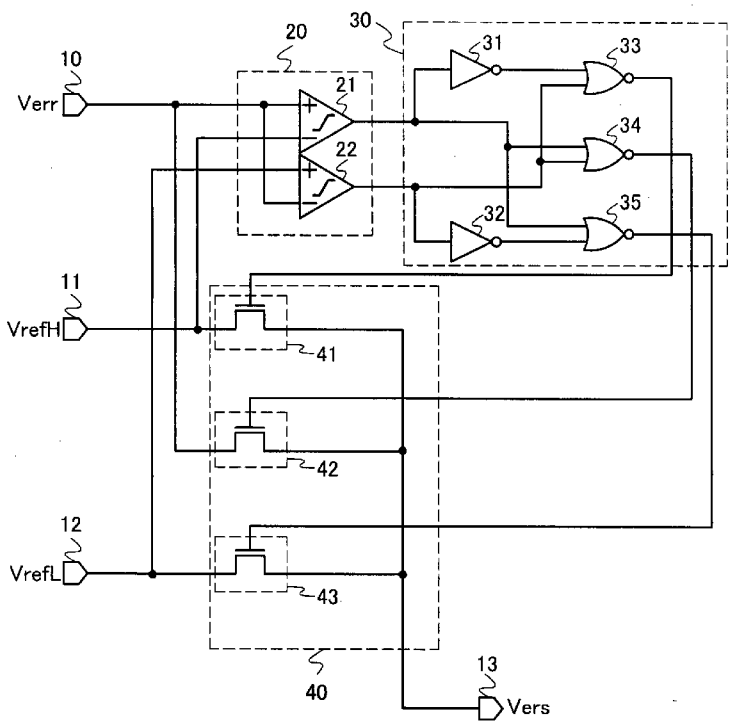
(54) **Title**: PWM LIMITER CIRCUIT

FIG. 1



(57) **Abstract**: The duty ratio of a PWM signal is prevented from being zero immediately after the start of PWM control, for example. A PWM limiter circuit has a structure with which a signal output from the PWM limiter circuit can be prevented from being higher than a certain value or lower than a certain value. The PWM limiter circuit includes a comparator circuit, a controller circuit, and a switch circuit. The highest duty ratio reference voltage V_{refH} is input to a first input terminal. The lowest duty ratio reference voltage V_{refL} is input to a second input terminal. Voltage V_{err} output from an error amplifier is input to a third input terminal.

WO 2011/052357 A1

DESCRIPTION

PWM LIMITER CIRCUIT

TECHNICAL FIELD

[0001]

The technical field of the present invention relates to a PWM limiter circuit applicable to a power supply circuit or the like (e.g., a switching regulator).

BACKGROUND ART

[0002]

Pulse width modulation (PWM) control used in a power supply circuit raises or lowers input voltage by a change in duty ratio of a PWM signal.

[0003]

FIG. 5 illustrates a structure example of a PWM control circuit. The PWM control circuit includes an error amplifier 50, a reference voltage generation circuit 60, a PWM limiter circuit 70, an oscillator 80 for generating a triangle wave, and a PWM comparator 90.

[0004]

The error amplifier 50 amplifies a difference between feedback voltage V_{fb} and reference voltage and outputs voltage V_{err}.

[0005]

The reference voltage generation circuit 60 generates the reference voltage and reference voltage V_{ref}.

[0006]

The PWM limiter circuit 70 controls its output voltage V_{ers} by comparing the voltage V_{err} output from the error amplifier 50 and the reference voltage V_{ref} with each other.

[0007]

The oscillator 80 generates a triangle wave V_{osc} that is a signal needed for generation of a PWM signal.

[0008]

The PWM comparator 90 outputs a PWM signal from the voltage V_{ers} output from the PWM limiter circuit 70 and the triangle wave V_{osc} generated in the oscillator 80.

[0009]

In PWM control, when a duty ratio represented by a ratio of the pulse width of a PWM signal to the cycle of the PWM signal is higher than or equal to a certain ratio (80 %), harmonic noise might be generated. Further, an element might be damaged by supply of excessive current.

[0010]

Therefore, in order to perform PWM control without the above problems, it is necessary to perform limiter control for preventing the duty ratio of a PWM signal from being higher than a certain ratio.

[0011]

Reference 1 discloses a method for controlling the duty ratio of a PWM signal by input of the highest duty ratio voltage to a comparator when voltage output from an error amplifier is higher than the highest duty ratio voltage as a method of limiter control.

[Reference]

[0012]

Reference 1: Japanese Published Patent Application No. H10-127047

DISCLOSURE OF INVENTION

[0013]

Even in the case where limiter control is performed in order to prevent the duty ratio of a PWM signal from being higher than a certain ratio, the duty ratio of the PWM signal is zero immediately after the start of PWM control, so that problems such as generation of noise due to ringing of current flowing through a coil and unstable operation of a constant voltage control circuit occur.

[0014]

Similarly, in the case where PWM control is performed using a device where input voltage greatly fluctuates, such as a solar cell, as a power source, the duty ratio of a PWM signal is zero.

[0015]

A PWM limiter circuit has a structure with which a signal output from the PWM limiter circuit can be prevented from being higher than a certain value or lower than a certain value.

[0016]

One embodiment of the present invention is a PWM limiter circuit. The PWM limiter circuit includes a first terminal to which the highest duty ratio reference voltage is input, a second terminal to which the lowest duty ratio reference voltage is input, a comparator for comparing a voltage input to a third terminal and the highest duty ratio reference voltage with each other, a comparator for comparing the voltage input to the third terminal and the lowest duty ratio reference voltage with each other, a first switch which is turned on when the voltage input to the third terminal is higher than the highest duty ratio reference voltage, a second switch which is turned on when the voltage input to the third terminal is lower than the lowest duty ratio reference voltage, a third switch which is turned on when the voltage input to the third terminal is higher than the lowest duty ratio reference voltage and lower than the highest duty ratio reference voltage, and an output terminal which is electrically connected to the first switch, the second switch, and the third switch.

[0017]

By control of a PWM signal so that the duty ratio of the PWM signal is prevented from being zero, generation of noise can be suppressed and unstable operation can be prevented.

BRIEF DESCRIPTION OF DRAWINGS

[0018]

In the accompanying drawings:

FIG. 1 is a circuit diagram of a PWM limiter circuit;

FIG. 2 is a circuit diagram of a PWM limiter circuit;

FIGS. 3A and 3B are graphs illustrating generation of a PWM signal when voltage V_{err} output from an error amplifier is sometimes lower than the lowest duty ratio reference voltage V_{refL};

FIGS. 4A and 4B are graphs illustrating generation of a PWM signal when

voltage V_{err} output from an error amplifier is sometimes higher than the highest duty ratio reference voltage V_{refH}; and

FIG. 5 is a circuit diagram illustrating a structure example of a PWM control circuit.

FIG. 6 is a circuit diagram illustrating a structure example of DC-DC converter including a PWM control circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

[0019]

Hereinafter, embodiments of the disclosed invention will be described with reference to the drawings. Note that the disclosed invention is not limited to the following description. It will be readily appreciated by those skilled in the art that modes and details of the disclosed invention can be changed in various ways without departing from the spirit and scope of the disclosed invention. Therefore, the disclosed invention should not be construed as being limited to the following description of the embodiments.

[0020]

(Embodiment 1)

FIG. 1 is a circuit diagram of a PWM limiter circuit in this embodiment. The PWM limiter circuit includes a comparator circuit 20, a controller circuit 30, and a switch circuit 40.

[0021]

Voltage V_{err} output from an error amplifier is input to an input terminal 10.

[0022]

The highest duty ratio reference voltage V_{refH} is input to an input terminal 11.

[0023]

The lowest duty ratio reference voltage V_{refL} is input to an input terminal 12.

[0024]

A circuit for outputting the highest duty ratio reference voltage V_{refH} and the lowest duty ratio reference voltage V_{refL} may be an operational amplifier.

[0025]

The comparator circuit 20 compares the voltage V_{err} output from the error

amplifier with the highest duty ratio reference voltage V_{refH} or the lowest duty ratio reference voltage V_{refL}.

[0026]

The comparator circuit 20 includes comparators 21 and 22.

[0027]

The voltage V_{err} output from the error amplifier is input to a noninversion input terminal of the comparator 21. The highest duty ratio reference voltage V_{refH} is input to an inversion input terminal of the comparator 21.

[0028]

The lowest duty ratio reference voltage V_{refL} is input to a noninversion input terminal of the comparator 22. The voltage V_{err} output from the error amplifier is input to an inversion input terminal of the comparator 22.

[0029]

The controller circuit 30 generates a signal for controlling a signal output from the comparator circuit 20 with the switch circuit 40.

[0030]

The controller circuit 30 includes NOT gates 31 and 32 and NOR gates 33 to 35.

[0031]

The switch circuit 40 includes switches 41 to 43. Here, the switches 41 to 43 are MOS switches including NMOS transistors.

[0032]

Here, the transistors included in the switch circuit 40 are thin film transistors including silicon in channel layers. Note that the transistors included in the switch circuit 40 are not limited to single-gate transistors. Multi-gate transistors such as double-gate transistors may be used.

[0033]

Further, the channel layers of the transistors included in the switch circuit 40 are not limited to silicon. An oxide semiconductor or the like may be used.

[0034]

Note that the switches 41 to 43 are not limited to having these structures as long as on states and off states of the switches 41 to 43 are switched in response to a

signal from the controller circuit 30.

[0035]

Voltage V_{ers} output from the PWM limiter circuit is output to an output terminal 13.

[0036]

Next, a method for controlling a PWM signal with the PWM limiter circuit is described.

[0037]

The duty ratio of a PWM signal is controlled in such a manner that the voltage V_{err} output from the error amplifier and a triangle wave V_{osc} are compared with each other in a PWM comparator and the difference therebetween is amplified.

[0038]

The PWM comparator compares the voltage V_{err} output from the error amplifier and the triangle wave V_{osc} with each other. In the case where the signal level of the triangle wave V_{osc} is higher than the voltage V_{err} output from the error amplifier, an H-level (a high-level) signal is output as a PWM signal. In contrast, in the case where the signal level of the triangle wave V_{osc} is lower than the voltage V_{err} output from the error amplifier, an L-level (a low-level) signal is output as the PWM signal.

[0039]

In the case where the voltage V_{err} output from the error amplifier is lower than the triangle wave V_{osc}, the PWM signal does not have a duty ratio. Similarly, in the case where the voltage V_{err} output from the error amplifier is higher than the triangle wave V_{osc}, the PWM signal does not have a duty ratio.

[0040]

First, the case where the voltage V_{err} output from the error amplifier is lower than the lowest duty ratio reference voltage V_{refL} is described.

[0041]

In this case, the switch 43 is turned on, and the lowest duty ratio reference voltage V_{refL} is output as the voltage V_{ers} output from the PWM limiter circuit.

[0042]

FIGS. 3A and 3B are graphs illustrating generation of a PWM signal when the voltage V_{err} output from the error amplifier is sometimes lower than the lowest duty

ratio reference voltage V_{refL}.

[0043]

In FIG. 3A, the vertical axis indicates voltage [V] and the horizontal axis indicates time [s]. A line 100 indicates the triangle wave V_{osc}. A line 110 indicates the voltage V_{err} output from the error amplifier. A line 120 indicates the lowest duty ratio reference voltage V_{refL}.

[0044]

In FIG. 3B, the vertical axis indicates voltage [V] and the horizontal axis indicates time [s]. A line 130 indicates a PWM signal generated from the triangle wave and the voltage output from the error amplifier or the lowest duty ratio reference voltage in FIG. 3A.

[0045]

In a region 125 in FIG. 3A, the voltage V_{err} output from the error amplifier is lower than the lowest duty ratio reference voltage V_{refL}. Therefore, the lowest duty ratio reference voltage V_{refL} is output as the voltage V_{ers} output from the PWM limiter circuit.

[0046]

Next, the case where the voltage V_{err} output from the error amplifier is higher than the highest duty ratio reference voltage V_{refH} is described.

[0047]

In this case, the switch 41 is turned on, and the highest duty ratio reference voltage V_{refH} is output as the voltage V_{ers} output from the PWM limiter circuit.

[0048]

FIGS. 4A and 4B are graphs illustrating generation of a PWM signal when the voltage V_{err} output from the error amplifier is sometimes higher than the highest duty ratio reference voltage V_{refH}.

[0049]

In FIG. 4A, the vertical axis indicates voltage [V] and the horizontal axis indicates time [s]. The line 100 indicates the triangle wave V_{osc}. The line 110 indicates the voltage V_{err} output from the error amplifier. A line 140 indicates the highest duty ratio reference voltage V_{refH}.

[0050]

In FIG. 4B, the vertical axis indicates voltage [V] and the horizontal axis indicates time [s]. The line 130 indicates a PWM signal generated from the triangle wave and the voltage output from the error amplifier or the highest duty ratio reference voltage in FIG. 4A.

[0051]

In a region 145 in FIG. 4A, the voltage V_{err} output from the error amplifier is higher than the highest duty ratio reference voltage V_{refH}. Therefore, the highest duty ratio reference voltage V_{refH} is output as the voltage V_{ers} output from the PWM limiter circuit.

[0052]

Finally, the case where the voltage V_{err} output from the error amplifier is higher than the lowest duty ratio reference voltage V_{refL} and lower than the highest duty ratio reference voltage V_{refH} is described.

[0053]

In this case, the switch 42 is turned on, and the voltage V_{err} output from the error amplifier is output as the voltage V_{ers} output from the PWM limiter circuit.

[0054]

Through the above control, the voltage V_{ers} output from the PWM limiter circuit always exists in the amplitude of the triangle wave V_{osc}, so that a PWM signal always has a duty ratio.

[0055]

(Embodiment 2)

FIG. 2 is a circuit diagram of a PWM limiter circuit in this embodiment. The PWM limiter circuit differs from the PWM limiter circuit in FIG. 1 in the structures of the switch circuit 40 and the controller circuit 30.

[0056]

A switch 44 is a MOS switch including a PMOS transistor Q1. A PMOS transistor Q2 whose source and drain are short-circuited is provided as a dummy switch for compensating feedthrough electric charge from a gate when the PMOS transistor Q1 is turned off.

[0057]

The PMOS transistor Q1 which is a MOS switch and the PMOS transistor Q2

which is a dummy switch are driven with pulses whose phases are opposite. Thus, a NOT gate 36 is provided in the controller circuit 30.

[0058]

A switch 45 is a MOS switch (a transmission gate) including a PMOS transistor Q3 and an NMOS transistor Q4. A NOT gate 37 is provided in the controller circuit 30 in order to drive the switch 45.

[0059]

A switch 46 is a MOS switch including an NMOS transistor Q5, to which an NMOS transistor Q6 is added as a dummy switch. A NOT gate 38 is provided in the controller circuit 30 in order to drive the switch 46.

[0060]

The polarities of the transistors used as the MOS switches are not limited to them; however, it is advantageous to connect the switch 44 which is the MOS switch including the PMOS transistor Q1 to the input terminal 11 to which the highest duty ratio reference voltage V_{refH} is input. The advantage of the above structure is that gate-source voltage (V_{gs}) of the PMOS transistor Q1 is raised and source-drain resistance (R_{ds}) is lowered.

[0061]

Similarly, when the switch 46 which is the MOS switch including the NMOS transistor Q5 is connected to the input terminal 12 to which the lowest duty ratio reference voltage V_{refL} is input, gate-source voltage (V_{gs}) of the NMOS transistor Q5 is raised and source-drain resistance (R_{ds}) is lowered, which is effective.

[0062]

Note that a method for controlling a PWM signal with the PWM limiter circuit in FIG. 2 is similar to a method for controlling a PWM signal with the PWM limiter circuit in FIG. 1.

[0063]

(Embodiment 3)

FIG. 6 is a circuit diagram of a DC-DC converter which includes a PWM control circuit having the PWM limiter circuit described in Embodiments 1 and 2.

[0064]

A DC-DC converter 200 described in this embodiment includes a power

transistor 210, a coil 220, a diode 230, a capacitor 240, a resistor 250, a resistor 260, and a PWM control circuit 270. In the DC-DC converter 200, voltage obtained by division of output voltage is monitored with the PWM control circuit 270, and the level of the output voltage is set to a desired level.

[0065]

The PWM control circuit 270 controls a PWM signal used for driving the power transistor 210. The structure of the PWM control circuit 270 is similar to that of the circuit illustrated in FIG. 5. The PWM limiter circuit included in the PWM control circuit 270 controls the upper and lower limits of the duty ratio of a PWM signal. The structure of the PWM limiter circuit in this embodiment is similar to those of FIG. 1 and FIG. 2. Further, a method for controlling a PWM signal with the PWM limiter circuit is similar to those of Embodiments 1 and 2; thus, description of such a method is omitted.

This application is based on Japanese Patent Application serial No. 2009-247700 filed with Japan Patent Office on October 28, 2009, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A PWM limiter circuit comprising:

a first terminal to which highest duty ratio reference voltage is input;

a second terminal to which lowest duty ratio reference voltage is input;

a comparator for comparing a voltage input to a third terminal with the highest duty ratio reference voltage or the lowest duty ratio reference voltage;

a first switch which is turned on when the voltage input to the third terminal is higher than the highest duty ratio reference voltage;

a second switch which is turned on when the voltage input to the third terminal is lower than the lowest duty ratio reference voltage;

a third switch which is turned on when the voltage input to the third terminal is higher than the lowest duty ratio reference voltage and lower than the highest duty ratio reference voltage; and

an output terminal electrically connected to the first switch, the second switch, and the third switch,

wherein the first switch is electrically connected to the first terminal, the second switch is electrically connected to the second terminal, and the third switch is electrically connected to the third terminal.

2. The PWM limiter circuit according to claim 1,

wherein the first switch is formed using a p-channel transistor, and

wherein the second switch is formed using an n-channel transistor.

3. A DC-DC converter comprising:

a PWM control circuit comprising:

a PWM limiter circuit comprising:

a first terminal to which highest duty ratio reference voltage is input;

a second terminal to which lowest duty ratio reference voltage is input;

a comparator for comparing a voltage input to a third terminal

with the highest duty ratio reference voltage or the lowest duty ratio reference voltage;

a first switch which is turned on when the voltage input to the third terminal is higher than the highest duty ratio reference voltage;

a second switch which is turned on when the voltage input to the third terminal is lower than the lowest duty ratio reference voltage;

a third switch which is turned on when the voltage input to the third terminal is higher than the lowest duty ratio reference voltage and lower than the highest duty ratio reference voltage; and

an output terminal electrically connected to the first switch, the second switch, and the third switch,

wherein the first switch is electrically connected to the first terminal, the second switch is electrically connected to the second terminal, and the third switch is electrically connected to the third terminal.

4. The PWM limiter circuit according to claim 3,

wherein the first switch is formed using a p-channel transistor, and

wherein the second switch is formed using an n-channel transistor.

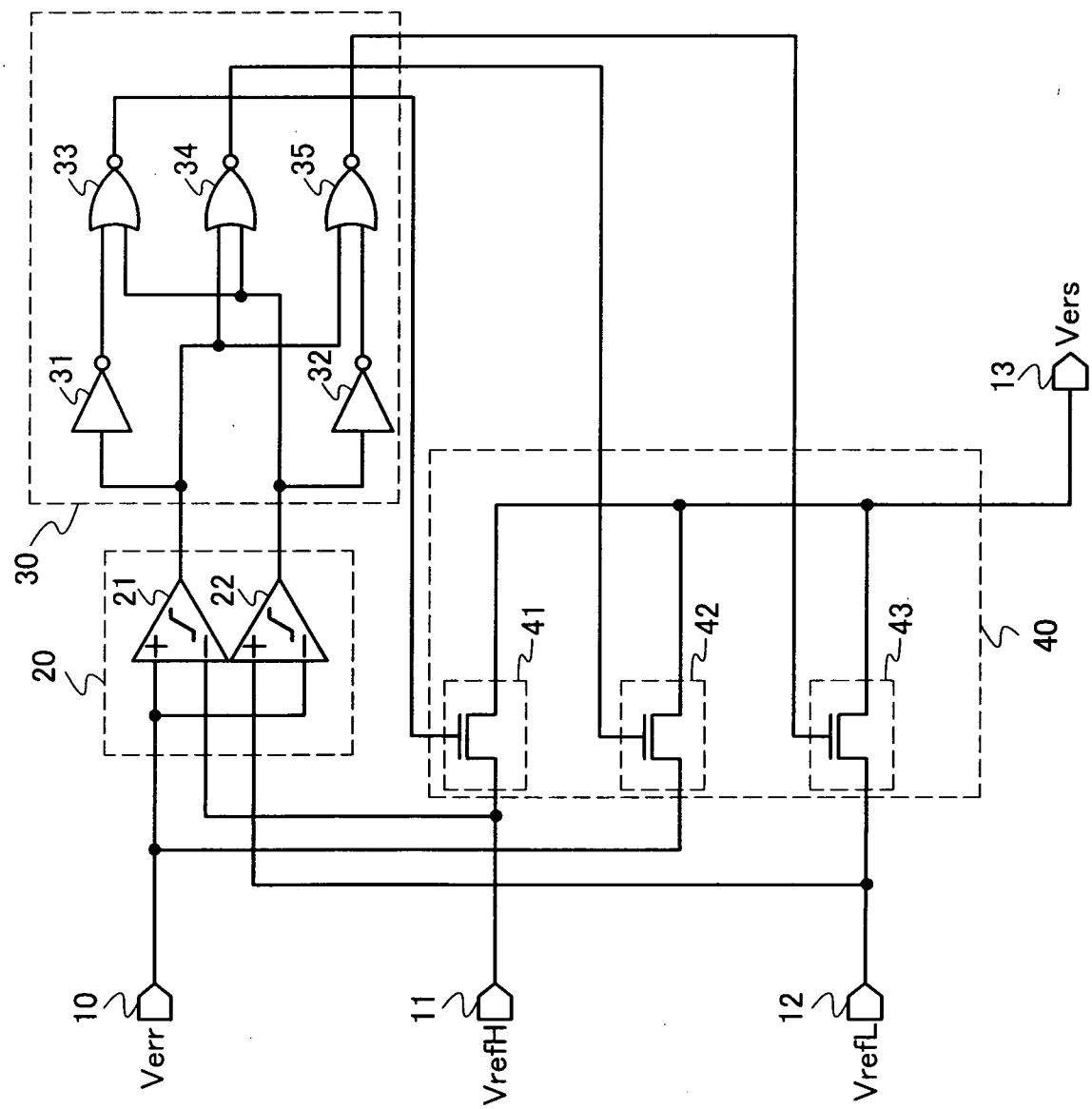

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FIG. 1

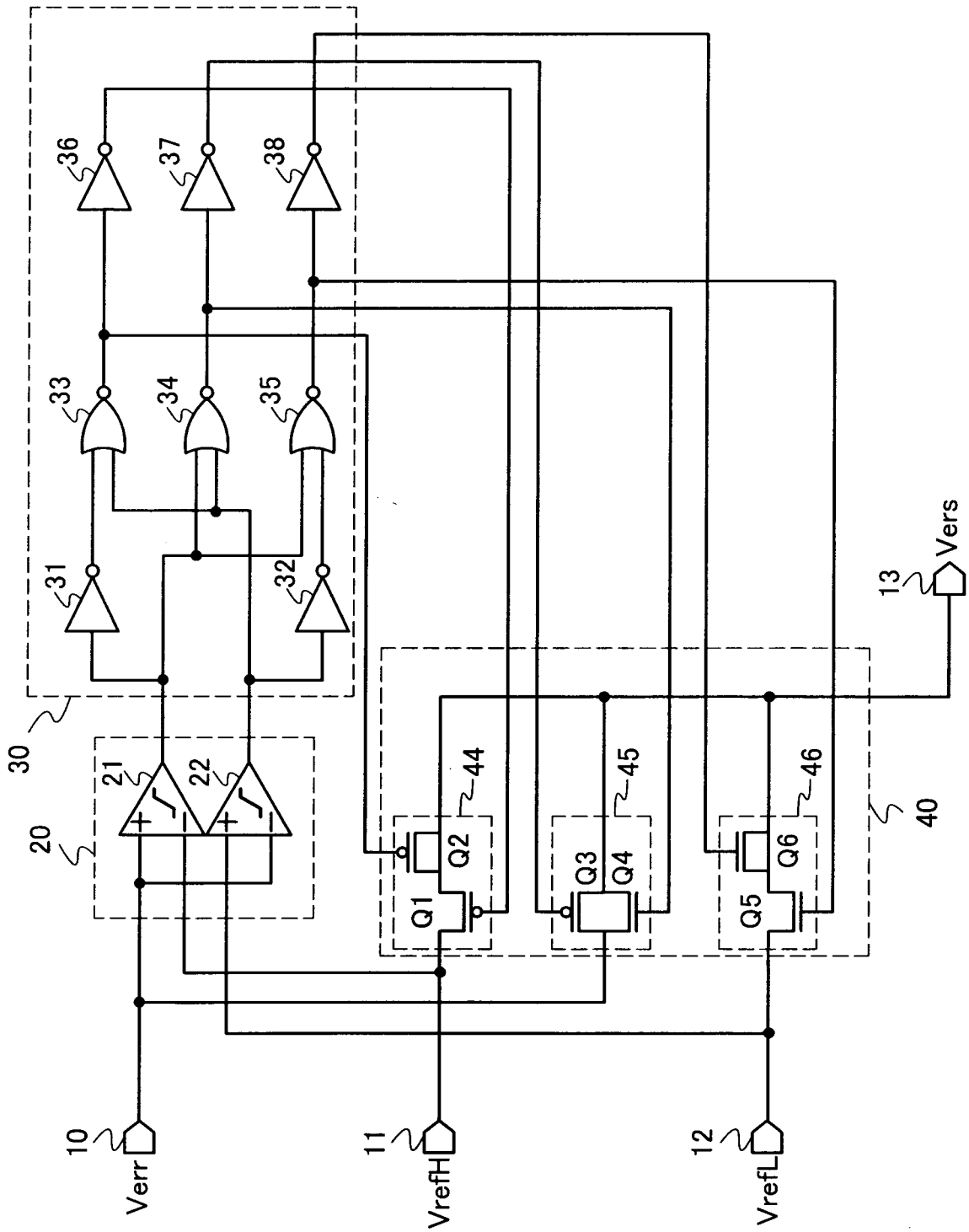
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FIG. 2

FIG. 3A

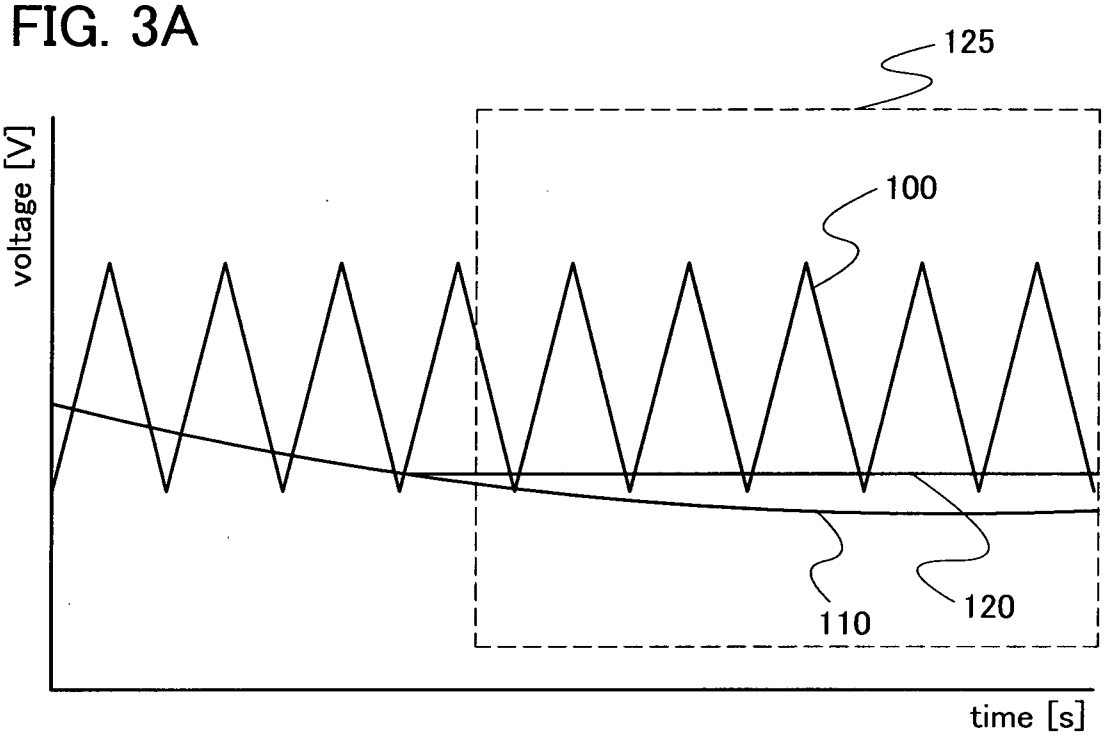


FIG. 3B

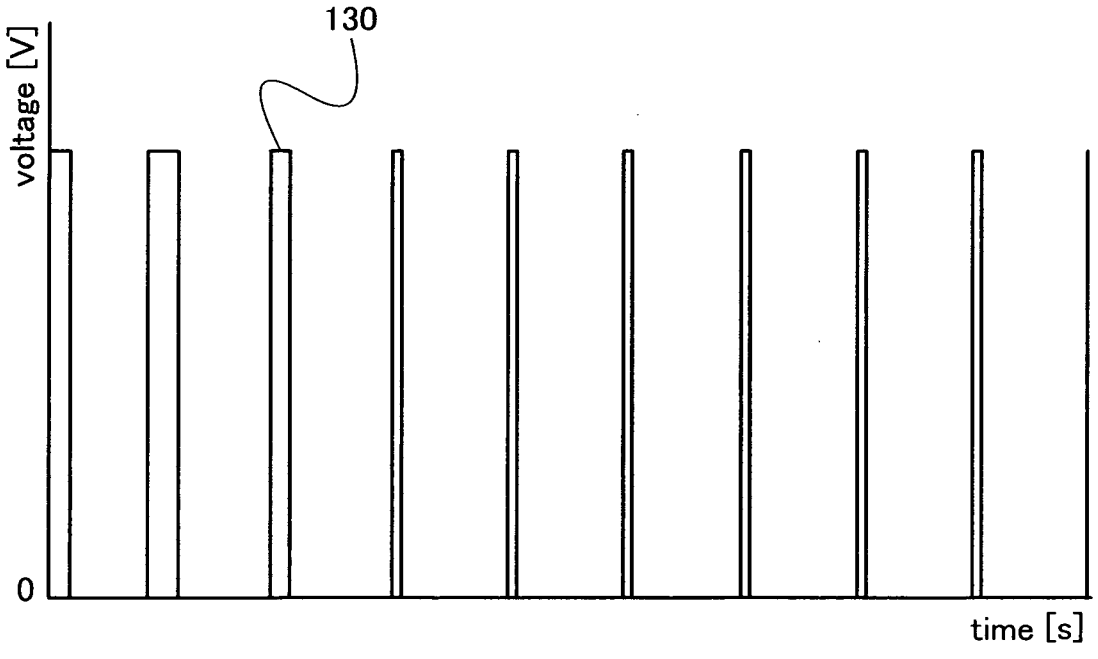


FIG. 4A

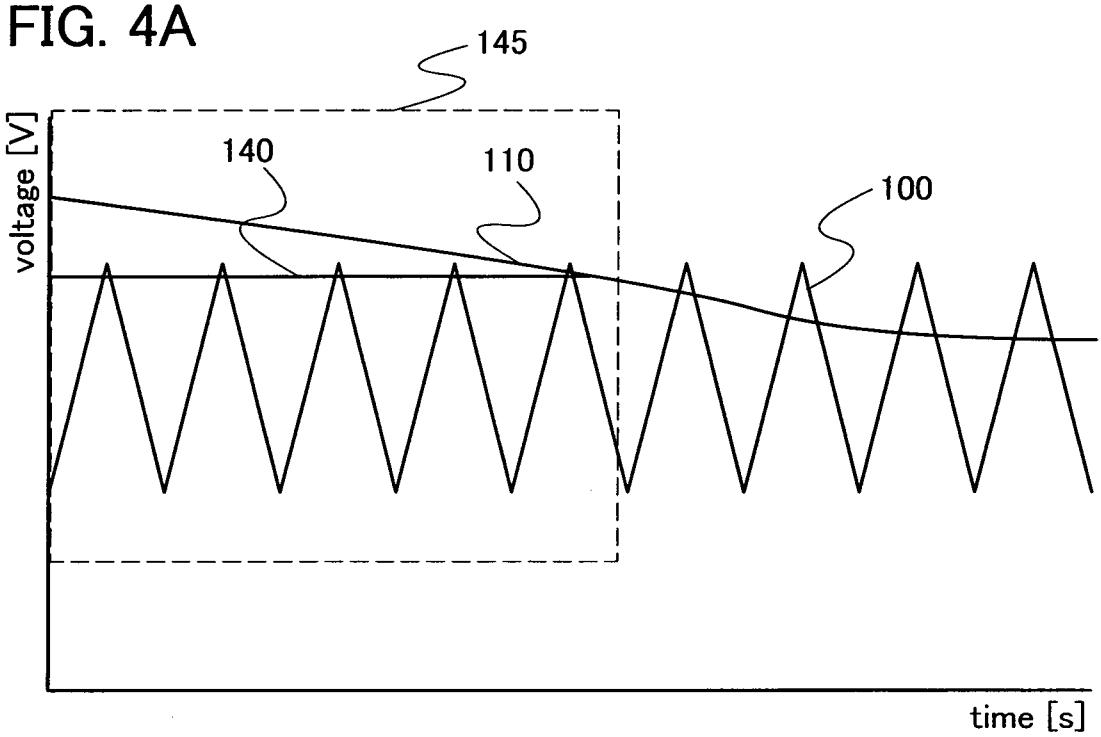
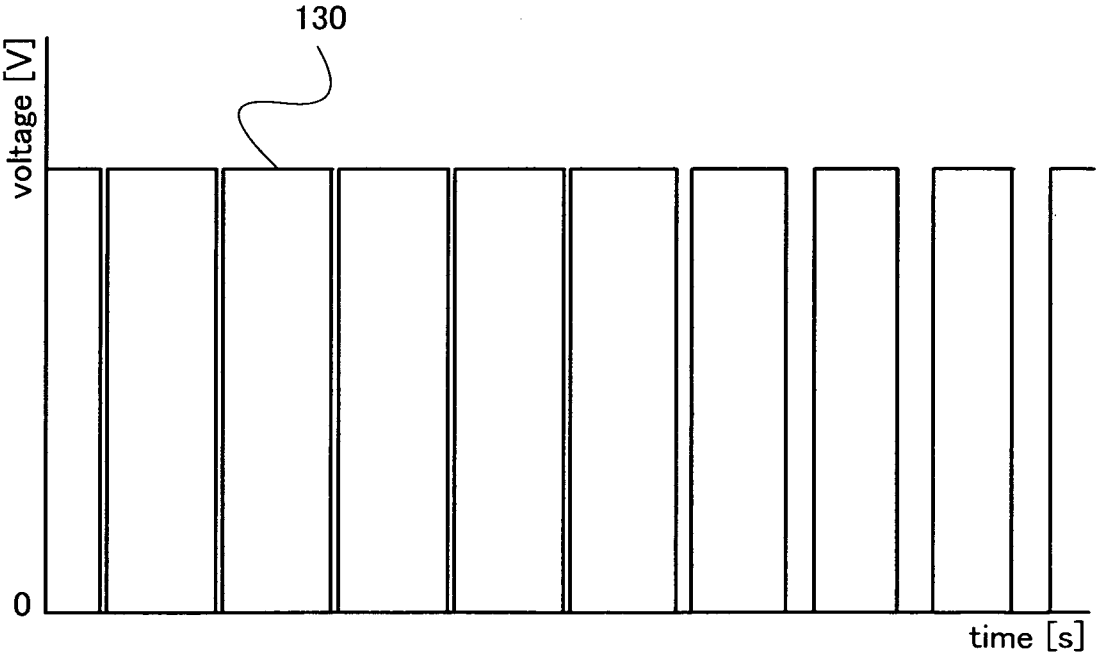


FIG. 4B



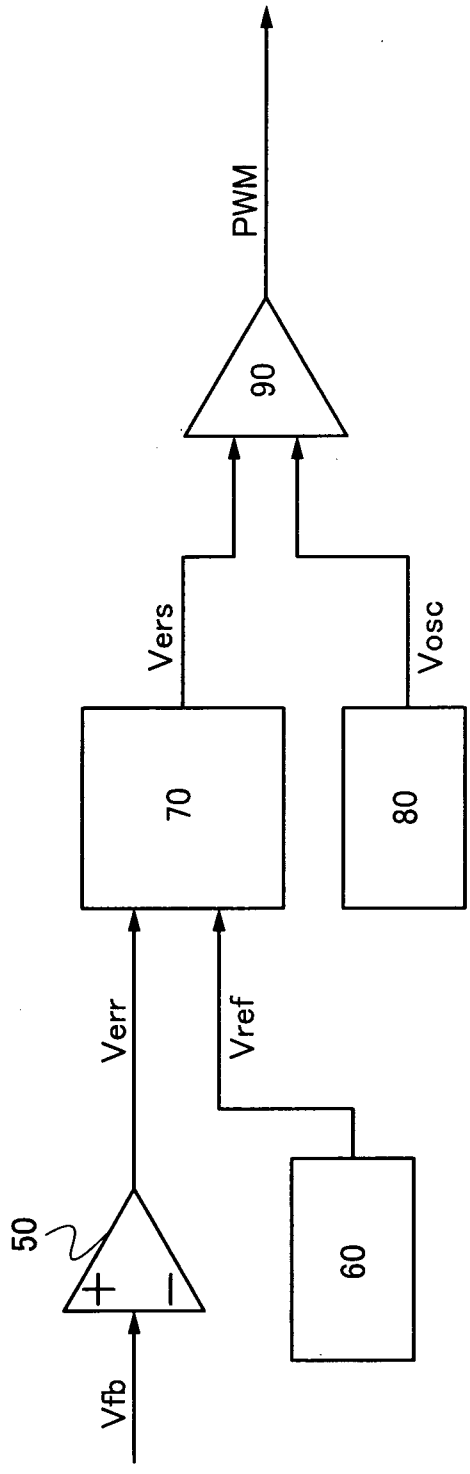
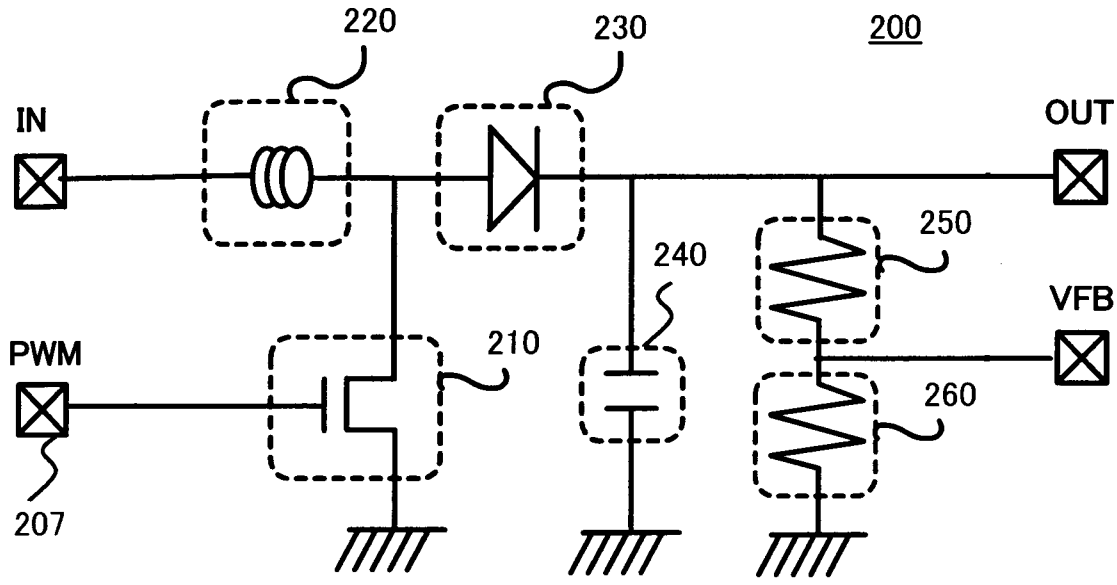


FIG. 5

FIG. 6



REFERENCE NUMERALS

10: input terminal, 11: input terminal, 12: input terminal, 13: output terminal, 20: comparator circuit, 21: comparator, 22: comparator, 30: controller circuit, 31: NOT gate, 32: NOT gate, 36: NOT gate, 37: NOT gate, 38: NOT gate, 33: NOR gate, 34: NOR gate, 35: NOR gate, 40: switch circuit, 41: switch, 42: switch, 43: switch, 44: switch, 45: switch, 46: switch, 50: error amplifier, 60: reference voltage generation circuit, 70: PWM limiter circuit, 80: oscillator, 90: PWM comparator, 100: line indicating triangle wave V_{osc}, 110: line indicating voltage V_{err} output from error amplifier, 120: line indicating lowest duty ratio reference voltage V_{refL}, 125: region, 130: line indicating PWM signal, 140: line indicating highest duty ratio reference voltage V_{refH}, 145: region, Q1: p-channel transistor, Q2: p-channel transistor, Q3 p-channel transistor, Q4: n-channel transistor, Q5: n-channel transistor, Q6: n-channel transistor, 200: DC-DC converter, 210: power transistor, 220: coil, 230: diode, 240: capacitor, 250: resistor, 260: resistor, and 270: PWM control circuit.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/067606

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H02M3/00(2006.01)i, H02M1/08(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H02M3/00, H02M1/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2010
Registered utility model specifications of Japan 1996-2010
Published registered utility model applications of Japan 1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2002-369505 A (Hitachi, Ltd.) 2002.12.20, [0015]-[0019], Fig 1 & US 2002/0185994 A1	1-4
Y	JP 8-44465 A (Seiko Epson Corp.) 1996.02.16, [0035]-[0039], Fig 3 & US 5727193 A	1-4

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
01.12.2010	14.12.2010

Name and mailing address of the ISA/JP	Authorized officer
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