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(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

(72) Inventor: **Ogawa, Kenji, c/o NEC Corporation**
7-1, Shiba 5-chome
Minato-ku, Tokyo 108-1(JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
W-8000 München 26(DE)

(54) **Insulated gate transistor operable at a low drain-source voltage.**

(57) A transistor comprising: A first region of a first conductivity type semiconductor having an upper surface portion and a bottom surface portion; a second region of a second conductivity type semiconductor formed in said upper surface portion; a third region of said first conductivity type semiconductor formed in said second region; a gate insulator film formed on said second region positioned between said third and first regions; a gate electrode formed on said gate insulator film; a source electrode connected with said third region; a fourth region of said second conductivity type semiconductor formed in a first limited area of said first region apart from said second region; a resistive layer formed in electrical contact with a second limited area of said first region apart from said second region and said first limited area; and a drain electrode contacting said fourth region and said resistive layer, said resistive layer presenting a predetermined value of resistance between said second limited area and said drain electrode, wherein said first limited area positions in said upper surface portion of said first region.

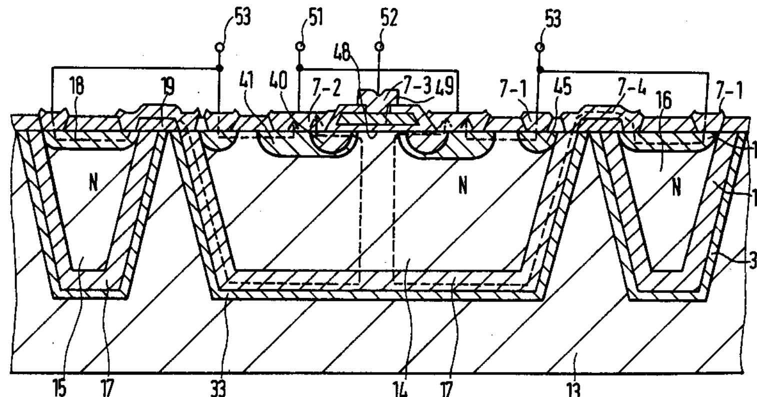

FIG. 2

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Background of the Invention

(Field of the Invention)

This invention relates to an insulated gate transistor (IGT) having a PN-junction region in a drain region of a MOS field effect transistor using a semiconductor substrate as the drain region and, more particularly, to an improvement for being operable at a low drain-source voltage (V_{DS}).

(Description of the Related Art)

As a high-power device, there has been widely used a vertical MOS field effect transistor in which a source region of one conductivity type is formed in a base region of the other conductivity type which is formed in a semiconductor substrate of the one conductivity type as a drain region. A gate electrode is formed on the base region locating between the source and drain regions via a gate insulator film. This kind of vertical MOS field effect transistor flows a drain current across the thickness of the semiconductor substrate to allow a large power consumption. This vertical MOS field effect transistor, however, has a drawback of a large ON-resistance due to the current flow across the thickness of the substrate. This drawback causes a large power loss.

For improving this large ON-resistance, an IGT has been proposed by M. F. Chang et al in IEDM83, pages 83 to 86. The IGT has a high impurity region of the other conductivity type in the drain region in contact with the drain electrode to interpose the other conductivity type region between the drain region and the drain electrode. According to this IGT,a carrier injection of other conductivity type carriers is generated from the high impurity region to the drain region as a reaction of the drain current flowing into the high impurity region. By the carrier injection, a conductivity modulation is generated to make the ON-resistance very small.

The carriers of the carrier injection are, however, majority carriers of the high impurity region. Therefore, the PN-junction between the drain region and the high impurity region is necessary to be forward biased. This required forward bias restricts the lower limit of the drain-source voltage to more than 0.5 or 0.6 volts. In a region of the drain-source voltage lower than this value, there flows little drain current to lose a transistor action. Thus, the proposed IGT has a drawback that it does not operate in a low drain-source voltage.

The proposed IGT has another drawback of a deteriorated operational speed. When the IGT turns off, a discharging path of the charges in the drain region does not exist due to the existance of the high impurity region. Therefore, the IGT does not turn off until the charges in the drain region disappear by recombination in the drain region.

As an IGT operable at a low drain-source voltage with a high speed, a lateral IGT has been proposed by M.R. Simpson in IEDM85, pages 740 to 743. In the lateral IGT, the high impurity region is formed in the same surface of the drain region as the base and source regions. The drain electrode is connected with the high impurity region and a portion of the drain region located on opposite side of the high impurity region to the source and drain regions. Drain current flows laterally along the surface of the drain region.

In a high drain-source voltage region, the PN-junction between the high impurity region and the drain region is forward biased to allow the carrier injection, while the resistance component of the drain region under the high impurity region restricts the drain current following directly to the drain electrode, resulted in the IGT operation. On the other hand, in a low drain-source voltage region, since the IGT operation does not function due to insufficient forward bias of the PN-junction between the high impurity region and the drain region, the drain current bypasses the high impurity region to flow directly to the drain electrode, resulted in a MOS field effect transistor action. Thus, the lateral IGT can operate in a low drain-source voltage region. Furthermore, if the lateral IGT turns off, the discharging path of the carriers in the drain region is kept by a route through the direct connection of the drain region and the drain electrode. Therefore, the lateral IGT can operate at a high speed.

This lateral IGT, however, has a large ON-resistance based on a drain current flowing along the surface of the drain region. By the same reason, it requires a large area on a semiconductor chip to lower a current capacity.

Another improvement of the IGT has been proposed by T. Goto et al in a Japanese Laid-open Patent No. 60-170263 published on September 3, 1985. This improved IGT has the high impurity region of a lattice shape or a comb shape in a bottom region of the drain region. This improvement has an improved high speed operation, a low ON-resistance and a large current capacity. It is, however, difficult to obtain a sufficient resistance component in the drain region positioning in adjacent to the high impurity region. Due to this insufficient resistance component, the MOS field effect transistor action is kept up to a large drain-source voltage. The low ON-resistance cannot be obtained until the drain-source voltage becomes fairly high voltage.

Summary of the Invention

It is, therefore, a primary object of the present invention to provide an IGT operable at a low drain-source voltage and at a high speed.

It is another object of the present invention to provide an IGT having a large current capacity and showing a low ON-resistance even at a low drain-source voltage.

This objects are achieved by a transistor as defined in claim 1; the dependent claims are related to further developments of the invention.

The present invention provides a transistor having a semiconductor substrate of one conductivity type and having an upper surface portion and a bottom surface portion, a base region of the other conductivity type formed in the upper surface portion of the semiconductor substrate, a source region of the one conductivity type formed in the base region, a source electrode connected to the source region, a gate insulator film covering the base region positioning between the source region and the semiconductor substrate, a gate electrode formed on the gate insulator film, an additional region of the other conductivity type formed in the semiconductor substrate apart from the base region, a resistance region formed in electrical contact with the bottom surface portion, and a drain electrode formed in contact with the additional region and the resistance region. The resistance region may be formed by resistive material deposited by a resistance region formed in a semiconductor region formed outside but combined with the semiconductor substrate and connected to the additional region.

According to the present invention, the additional region is formed in the semiconductor substrate apart from the base region and drain electrode is connected through the resistance region and the additional region. Therefore, although the transistor operates as an IGT when the drain-source voltage is large, it operates as a vertical MOS field effect transistor when the drain-source voltage is small. Furthermore, since the charges in the semiconductor substrate which operates as a drain region can be discharged to the drain electrode through the bottom surface portion and the resistance region, the transistor according to the present invention can operate at a high speed. The drain current flows vertically across the thickness of the semiconductor substrate. Therefore, the transistor has a small ON-resistance and may have a large current capacity. Although the resistive component of the bottom surface portion at the remaining part is not enough for making the transistor operate at the IGT with a small drain-source voltage, this drawback is improved by using the resistance region. Thus, the transistor of the present invention operates to show a small ON-resistance for a small drain-source voltage.

Brief Description of the Drawings

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a sectional view showing a transistor according to the co-pending application EP 88 116 192;

Fig. 2 is a sectional view showing a preferred embodiment of the present invention;

Fig. 3 is a plane view showing the preferred embodiment of the present invention;

Fig. 4 is a graph showing a relationship between drain current and drain-source voltage of the IGT in the prior art;

Figs. 5, 6 and 7 are graphs showing a relationship between drain current and drain-source voltage of the transistors according to the preferred embodiment having various resistances of the used resistance regions;

Figs. 8(a) and 9(b) are graphs showing input and output waveforms of the IGT in the prior art; and

Figs. 9(a) and 9(b) are graphs showing input and output waveforms of the transistor according to the preferred embodiment of the present invention.

Description of the Preferred Embodiments

Referring to Fig. 1, the transistor uses an N-type Si substrate 12 having an impurity concentration of 2.5 x 10^{14} cm^{-3} and a thickness of 100 μm. A plurality of stripes of P-type base regions 21 having an impurity concentration of 9 x 10^{16} cm^{-3} and having a depth of 6 μm are formed in an upper surface portion of the substrate 12. In each stripe of base region 21, two stripes of N^+-type source regions 30 are formed with separated from each other. Each stripe of the source region 30 has an impurity concentration of 2.5 x 10^{18} cm^{-3} and a depth of 3 μm. A gate insulator film 8 of SiO_2 having a thickness of 1,000 Å are thermally grown on the whole upper surface of the substrate 12 and then etched away from the base regions 21 interposed between the two stripes of source regions 30 which are formed in the same base region 21. and from parts of the source regions 30 adjacent to the exposed region of the base region 21. On the remaining gate insulator film 8, gate electrodes 9 are formed with polycrystalline silicon to have a thickness of 5,000 Å. The gate electrodes 9 are covered with SiO_2 film having a stripe of aperture. The exposed base and source regions are covered with a comb-shape source electrode 7-2 of aluminum and connected to a source terminal 1. The exposed portions of the gate electrodes 9 are also

covered with a comb-shape gate wiring 7-3 of aluminum and connected to a gate terminal 2.

The bottom surface portion of the substrate 12 has a plurality of stripes of N^+-type regions 6 having an impurity concentration of 4 x 10^{17} cm^{-3} and a depth of 2 μm and a plurality of stripes of P^+-type regions 5 having an impurity concentration of 3.5 x 10^{18} cm^{-3} and a depth of 3 μm. The stripes of the N^+-type regions 6 and the stripes of the P^+-type regions 5 are alternately formed. On the N^+-type regions 6, resistance regions 4 of Ni-Cr layer having a thickness of 5,000 Å. This resistance regions 4 may be formed with epitaxially grown impurity-doped Si. The resistance across the thickness of the resistance regions is selected to have a resistance in a range from 1/10 to 10 times of ON-resistance of the obtained transistor at a MOS field effect transistor operation. The typical value of the resistance of the resistance region is from 10 to 50 ohms. A drain electrode 7-1 of aluminum is formed to cover all the P^+-type regions 5 and the resistance regions 4. The drain electrode 7-1 is connected to a drain terminal 3.

According to this transistor, if the drain-source voltage V_{DS} is small, the PN-junctions between the N-type substrate 12 and the P^+-type regions 5 are not biased forward to produce no current 11 flowing through the PN-junction but to make current 10 flow through the N^+-type region 6 and the resistance regions 4. Thus, the transistor operates as a MOS field effect transistor in an operational condition of a small drain-source voltage V_{DS}. As the drain-source voltage V_{DS} increases, the drain current becomes large to raise voltage drop across the N^+-type region 6 and the resistance region 4. When the voltage drop becomes larger than a forward-biasing voltage of PN-junction, that is, larger than 0.6 volts, electrons in the substrate 12 are allowed to flow into the P^+-type regions 5 and to inject holes in the P^+-type regions 5 into the substrate 12. This hole-injection produces a conductivity-modulation in the substrate 12 to operate the transistor as the IGT. By the IGT-operation, ON-resistance of the current flow 11 becomes very small. Majority of current flows through the P^+-type regions 5 with small ON-resistance. Thus, the transistor operates in a wide range of drain-source voltage with a small ON-resistance. Regarding the ON-resistance, that at the MOS field effect transistor operation is small compared to the lateral IGT in the prior art.

Furthermore, the transistor uses additional resistance regions 4, a sufficient resistance can be applied in parallel with the P^+-type region 5 in vertical direction. The applied resistance is easily controlled. Therefore, in spite of the vertical action, the IGT operation can be maintain to a sufficiently low drain-source voltage.

Referring now to Figs. 2 and 3, a preferred embodiment according to the present invention will be described. The transistor is formed in Si islands 14, 15 and 16 which are supported by polycrystalline silicon 13 via silicon oxide layers 33. Each Si island is formed of N-type monocrystalline silicon having an impurity concentration of 2.5 x 10^{14} cm^{-3} and a thickness of 45 μm and has an N^+-type layer 17 having an impurity concentration of 4 x 10^{17} cm^{-3} and a thickness of 8 μm on side and bottom surfaces. A P-type ring-shape base region 41 having an impurity concentration of 9 x 10^{16} cm^{-3} and a depth of 6 μm is formed in the Si island 14. An N^+-type ring-shape source region 40 having an impurity concentration of 2.5 x 10^{18} cm^{-3} and a depth of 3 μm is formed in the base region 41. A gate insulator film 48 of SiO_2 having a thickness of 1,000 Å is formed to cover portion surrounded by the ring-shape source region 40 with some coverage over the source region 40. A gate electrode 49 of polycrystalline silicon having a thickness of 5,000 Å is formed on the gate insulator film 48 and is covered with SiO_2 layer having an aperture to expose a part of the gate electrode 49. A gate wiring 7-3 of aluminum is connected to the exposed part of the gate electrode 49 to connect with a gate terminal 52. Aluminum source electrode 7-2 contacts both of source and base regions 40 and 41 to connect with a source terminal 1. A ring-shape P^+-type region 45 having an impurity concentration of 3.5 x 10^{18} cm^{-3} and a depth of 4 μm is formed in the island 14 so as to surround but isolated from the base region 41.

P-type resistance regions 18 having an impurity concentration of 1.5 x 10^{18} cm^{-3} are respectively formed in the islands 15 and 16 by impurity diffusion. One end of each resistance region 18 is connected to the N^+-type region 17 in the island 14 by an aluminum wiring 7-4 which is isolated from the N^+-type regions 17 in the islands 15 and 16 by silicon oxide layer 19. The other end of each resistance region 18 is connected to the P^+-type region 45 with aluminum drain electrode 7-1 which is connected to drain terminal 3. It is noted that, although two drain terminals 3 are shown, those two drain terminals 3 are used in an application by electrically connecting with each other.

When the drain-source voltage V_{DS} is small, since the PN-junction between the P^+-type region 5 and the N-type island 14 is not biased forward, drain current flows through a route of the drain electrode 7-1-the resistance region 18-the aluminum wiring 7-4-the N^+-type region 17 in the island 14-the island 14-the base region 41 under the gate electrode 49-the source region 40-the source electrode 72. Therefore, the transistor operates as a MOS field effect transistor. As the drain-source voltage V_{DS} increases, the drain current rises to

increase the voltage drop across the resistance region 18. When the voltage drop rises to forward bias the PN-junction between the P^+-type region 45 and the N-type island 14, electrons supplied from the source region 40 to the island 14 through the base region 41 under the gate electrode 49 flows into the P^+-type region 45. In response thereto, holes are injected into the island 14 from the P^+-type region 45 and then drawn to the drain region 41 to produce a current flowing through the P^+-type region 45-the island 14-the base region 41-the source electrode 7-2. Therefore, the transistor operates as an IGT.

The effect of the resistance of the resistance region 18 will be explained. Fig. 4 shows a relationship between the drain current I_D and the drain-source voltage V_{DS} of the prior art IGT in which a one conductivity-type Si substrate has another conductivity-type region on all over the bottom surface as disclosed in IEDM83, pages 83 to 86. The drain current I_D stops flowing in the drain-source voltage range below 0.7 volts. In contrast, the drain current I_D of the transistor shown in Figs. 2 and 3 flows at the drain-source voltage range below 0.7 volts, as shown in Figs. 5, 6 and 7. Fig. 5 is a case of the transistor having the resistance region 18 of 15 ohms and shows a turning point between MOS and IGT operations at the drain-source voltage V_{DS} of about 2.8 volts. Fig. 6 is a case having the resistance region 18 of 20 ohms and shows the turning point at about 2.4 volts. Fig. 7 is a case having the resistance region 18 of 39 ohms and shows the turning point at about 1.5 volts. As apparent from those Figs. 5, 6 and 7, the turning point between MOS and IGT operations lowers with increment of the resistance of the resistance region 18. This means the turning point may be arbitrarily controlled by adjusting the resistance of the resistance region 18. The resistance of the resistance region 18, however, should be selected in a range from 1/10 to 10 times of ON-resistance of the transistor operating as the MOS field effect transistor.

Figs. 8(a) and 8(b) are input and output waveforms of the prior art IGT as disclosed in IEDM 83 pages 83 to 86. The output waveform is deformed at its leading edges corresponding to the off-condition of the IGT just after changed from on-condition. This is because, when the IGT turns off, charges in the island 14 lose their discharging path and disappear by recombination in the island 14. On the contrast, the transistor according to the preferred embodiment shows input and output waveforms shown in Figs. 9(a) and 9(b). The output waveform has a sharp leading edges. This result shows a high speed operation. More specifically, the drain electrode 7-1 is connected to the N^+-type region 17 in the island 14 through the resistance region 18. Therefore, if the transistor turns off, the charges in the island 14 can quickly discharge through the N^+-type region 17 in the island 14 and the resistance region 18, resulted in a quick risinging of the output signal.

Many modifications can be applied. The preferred embodiment can be formed in a single monocrystalline silicon chip with using islands isolated from each other by means of PN-junction isolation. The resistance regions 18 in the second preferred embodiment may be formed with resistive metal deposited on the field oxide layer.

Claims

1. A transistor comprising:

   A first region of a first conductivity type semiconductor having an upper surface portion and a bottom surface portion;

   a second region of a second conductivity type semiconductor formed in said upper surface portion;

   a third region of said first conductivity type semiconductor formed in said second region;

   a gate insulator film (43) formed on said second region positioned between said third and first regions;

   a gate electrode (49) formed on said gate insulator film (48);

   a source electrode (7-2) connected with said third region;

   a fourth region of said second conductivity type semiconductor formed in a first limited area of said first region apart from said second region;

   a resistive layer (18) formed in electrical contact with a second limited area of said first region apart from said second region and said first limited area; and

   a drain electrode (7-1) contacting said fourth region and said resistive layer (18), said resistive layer presenting a predetermined value of resistance between said second limited area and said drain electrode (7-1), wherein said first limited area positions in said upper surface portion of said first region.

2. The transistor as claimed in claim 1, further comprising a sixth region of said first conductivity type semiconductor physically combined with but electrically isolated from said first region, said resistive layer being an impurity region of said second conductivity type semiconductor formed in said sixth region, said second limited area being said bottom surface portion and side surface portion of said first region, one part of said impurity region being electrically connected with said side sur-

face portion at said upper surface portion and another one part of said impurity region being connected with said drain electrode (7-1) together with said fourth region.

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3. The transistor as claimed in claim 2, wherein said first and sixth regions are physically combined with polycrystalline semiconductor.

4. A transistor comprising:

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A first semiconductor region of one conductivity type having an upper surface;

a second semiconductor region of said one conductivity type, said first and second semiconductor regions being physically supported by polycrystalline semiconductor and being electrically isolated from each other;

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a base semiconductor region (41) of said other conductivity type formed in said upper surface of said first region;

20

a source semiconductor region (40) of said one conductivity type formed in said drain semiconductor region;

a gate insulator film (48) formed on said base semiconductor region positioning between said source and first semiconductor regions;

25

a gate electrode (49) formed on said gate insulator film;

a third semiconductor region of said other conductivity type formed in said upper surface of said first region but separated from said base semiconductor region (41);

30

a fourth semiconductor region of said one conductivity type formed in said first semiconductor region along its surfaces except for said upper surface, said fourth semiconductor region having an impurity concentration higher than said first semiconductor region;

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a fifth semiconductor region of said other conductivity type formed in said second semiconductor region, said fifth semiconductor region having first and second contact portions to present a predetermined value of resistance therebetween;

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a wiring connecting said fourth semiconductor region and said first contact portion of said fifth semiconductor region; and

a drain electrode (7-1) connected with said fourth semiconductor region and said second contact portion of said fifth semiconductor region.

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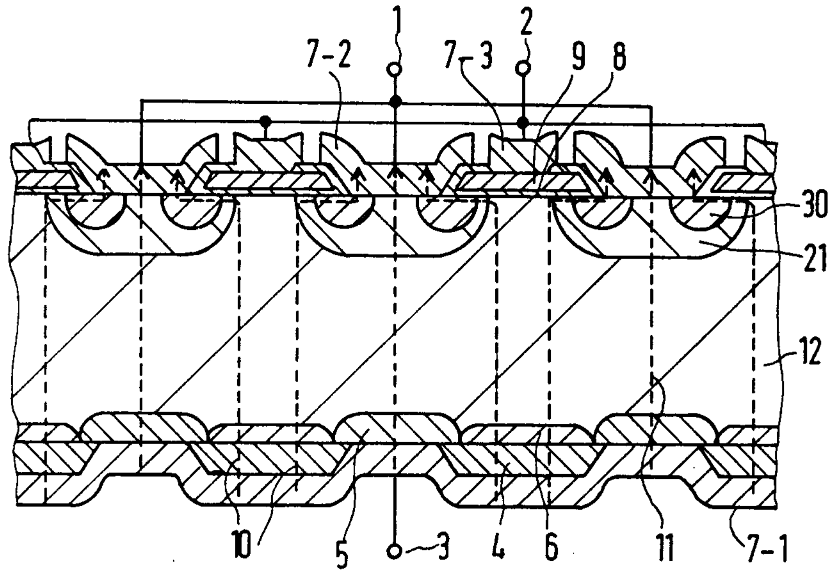


FIG.1

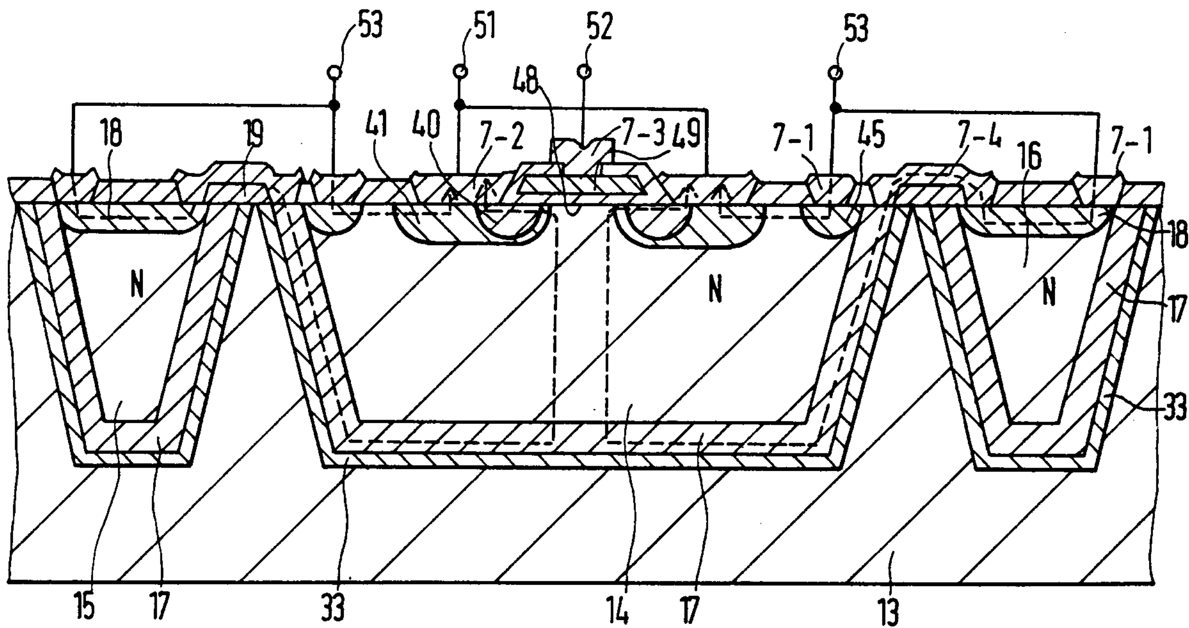


FIG. 2

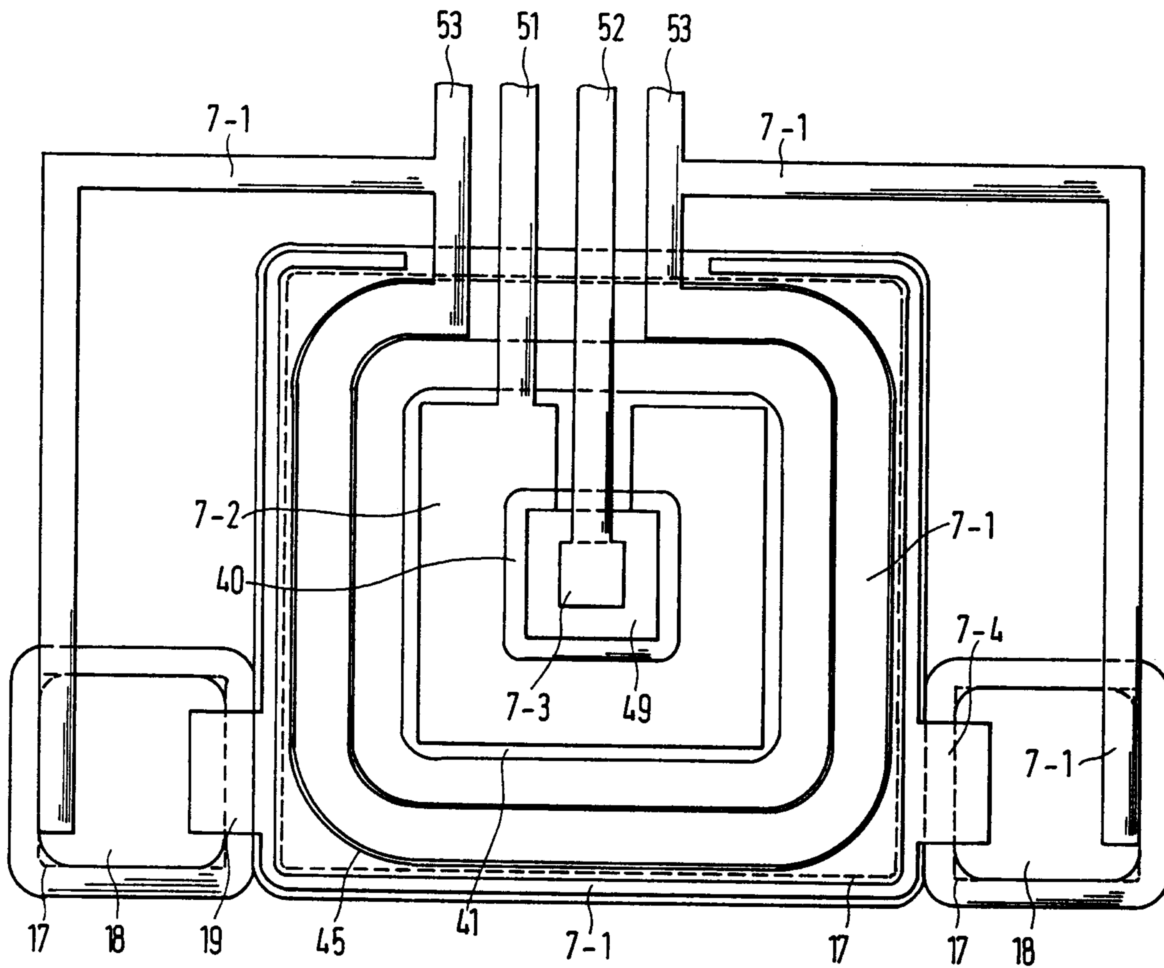


FIG.3

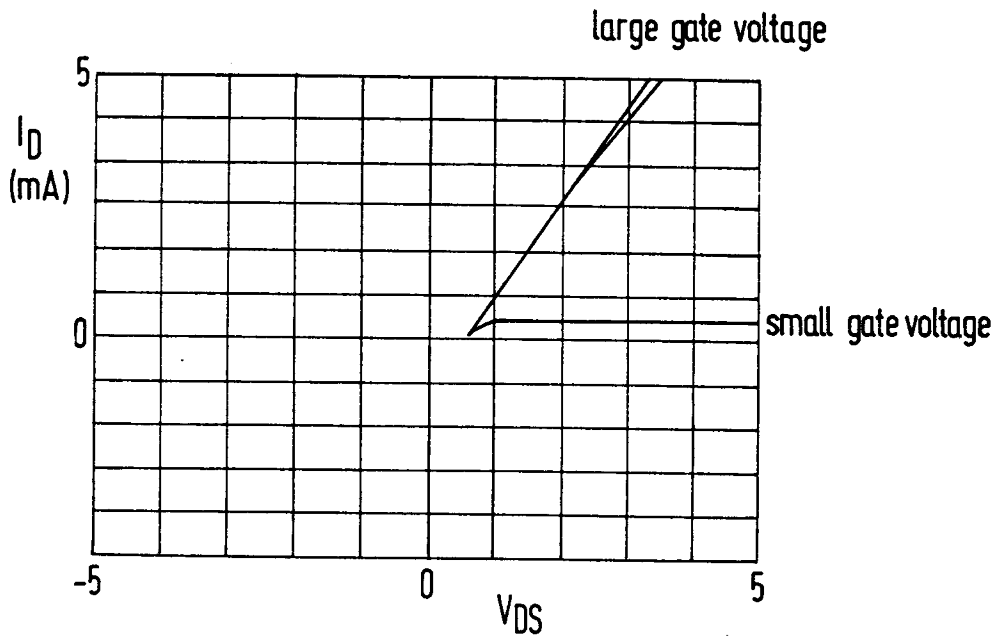
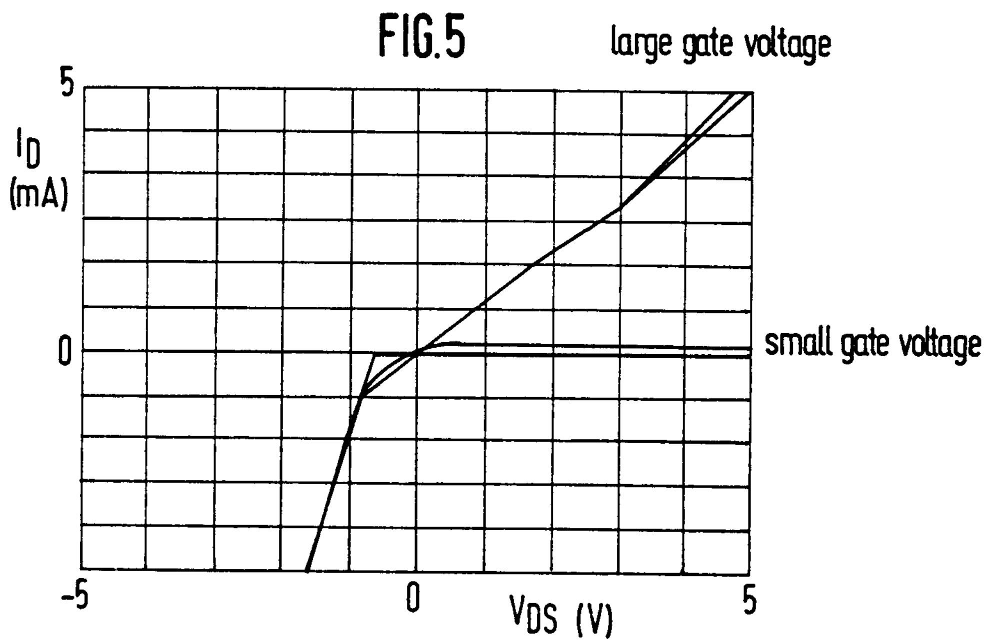


FIG.4

FIG.5



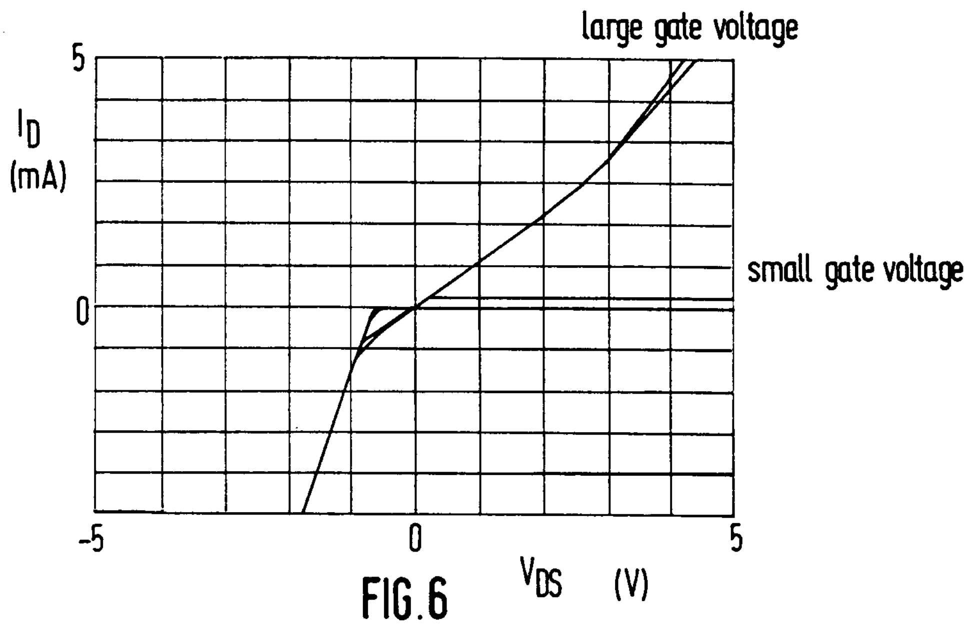
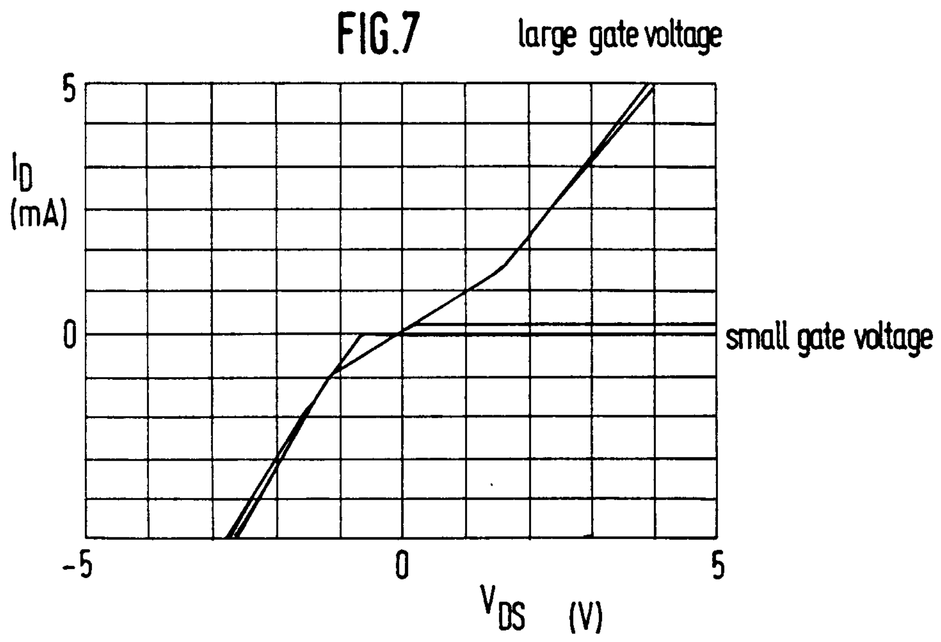


FIG.6

FIG.7



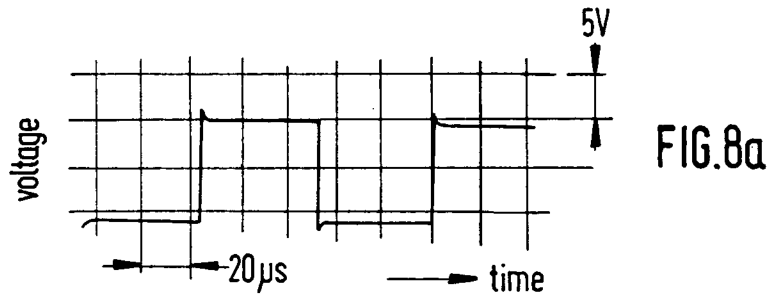


FIG.8a

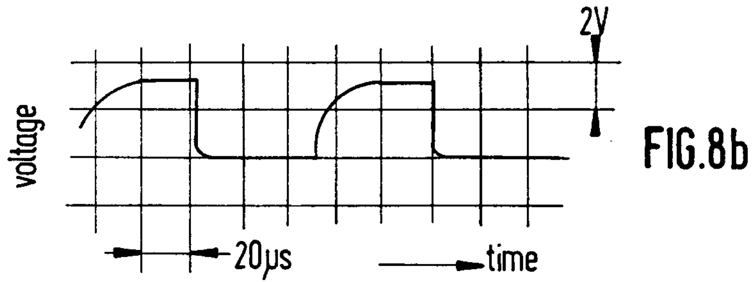


FIG.8b

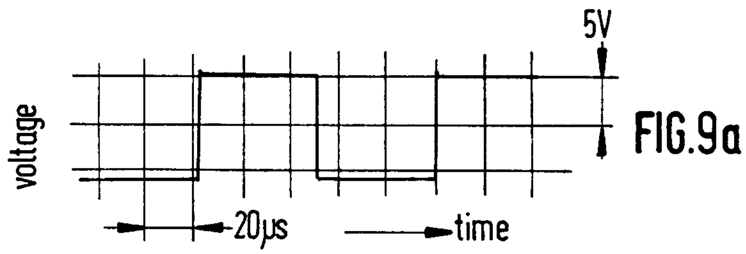


FIG.9a

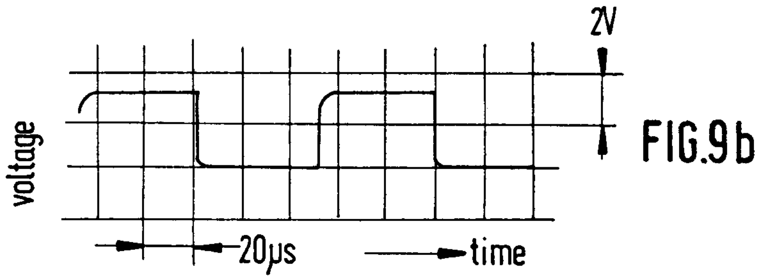


FIG.9b