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[Continued on next page]

(54) Title: THREE-DIMENSIONAL PATTERNING METHODS AND RELATED DEVICES

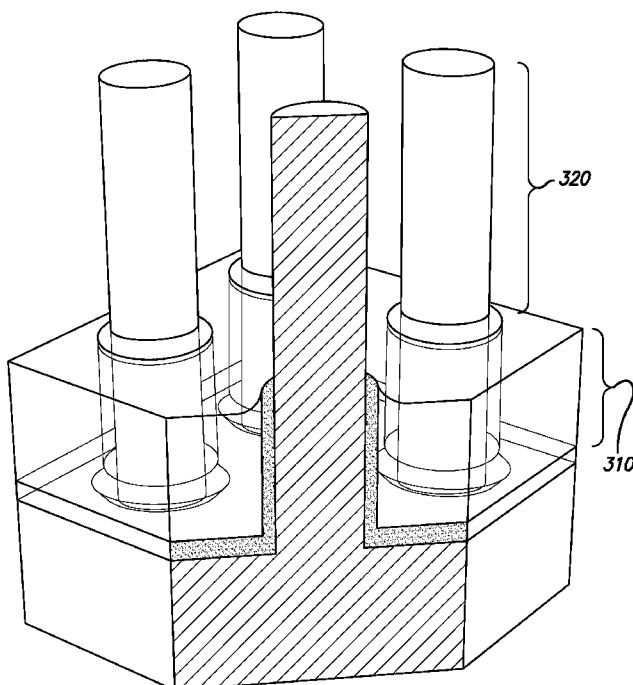


FIG. 3

(57) Abstract: Three-dimensional patterning methods of a three-dimensional microstructure, such as a semiconductor wire array, are described, in conjunction with etching and/or deposition steps to pattern the three-dimensional microstructure.

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Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: patterning, three-dimensional, nano silicon, wire, embedded portion, dopant

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2009-032412 A1 (CALIFORNIA INSTITUTE OF TECHNOLOGY et al.) 12 March 2009 See abstract, paragraphs [0036]-[0044],[0057]-[0062], figure 1, claim 1.	1-31
A	US 2008-0047604 A1 (BASTIAAN ARIE KOREVAAR et al.) 28 February 2008 See abstract, paragraphs [0044]-[0047], figures 1-3.	1-31
A	US 2009-0165844 A1 (ACHYUT KUMAR DUTTA) 02 July 2009 See abstract, paragraphs [0046]-[0061], figures 3 and 4.	1-31

 Further documents are listed in the continuation of Box C. See patent family annex.

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