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(71) Applicant: **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** [US/US]; 77 Massachusetts Avenue, Cambridge, MA 02139 (US).

(72) Inventor: **MURPHY, Robert, J.**; 421 High Street, Westwood, MA 02090 (US).

(74) Agent: **SICARD, Keri, E.** et al.; Daly, Crowley, Mofford & Durkee, LLP, One University Avenue, Suite 201B, Westwood, Massachusetts 02090 (US).

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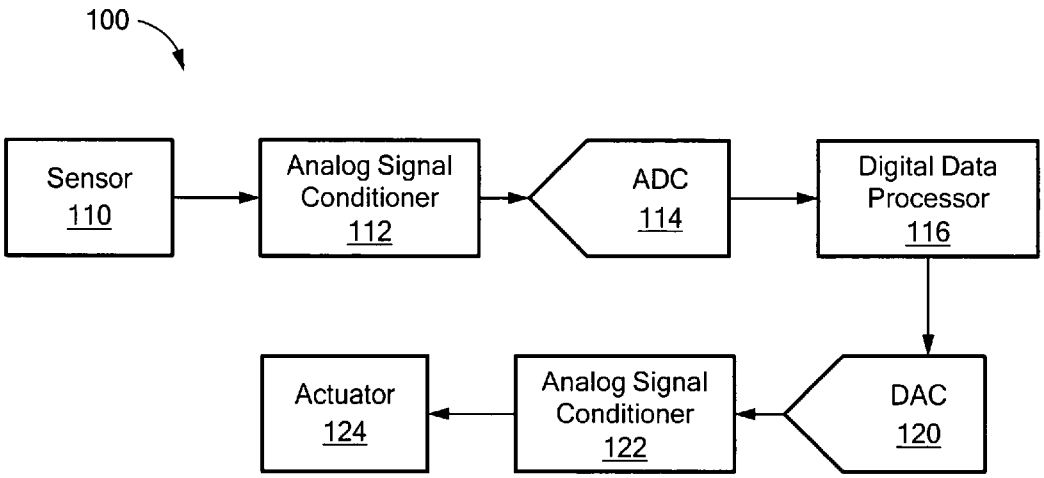

FIG. 1

(57) Abstract: Spectrally-efficient digital logic (SEDL) techniques implement spectrally-efficient pulses (e.g., Gaussian-shaped pulses) in lieu of conventional square waveforms to improve electromagnetic, radio frequency, and other unwanted emissions. The SEDL techniques can be used for combinatorial or sequential logic elements and circuits. A SEDL circuit includes a multiplier circuit configured to receive a clock signal and provide a product of the input signal and a clock signal, an integrator circuit to integrate the product signal over a first portion of a clock period to determine the logic state of the input signal, a limit circuit configured to apply limits to a state result provided to the integrator circuit, and a pulse generator configured to receive the logic state from the limit circuit and provide and output signal having a Gaussian-shaped output pulse that represents that logic value corresponding to the logic value of the input signal.

WO 2020/005223 A1

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SPECTRALLY EFFICIENT DIGITAL LOGIC

FIELD

[0001] The concepts, systems, configurations, devices and techniques described herein relate generally to combinatorial and sequential circuits that implement digital logic.

BACKGROUND

[0002] Consumer products are required to adhere to EMI/RFI (electromagnetic interference/radio frequency interference) regulations to reduce emissions and interferences from electromagnetic and RF (radio frequency) sources. EMI/RFI may be any disturbance generated by an external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction. There is a very large industry involving EMI/RFI regulations compliance testing and/or mitigation. There is also some concern among consumers about potential health hazards associated with electromagnetic and radio frequency emissions from electronic products. Electronic products and systems are typically required to pass EMI/RFI testing to ensure that they do not pollute any components, devices, or persons in their vicinity. For example, EMI/RFI must be mitigated for cellular technology manufacturers, data service providers, computer manufacturers, aerospace systems, automotive industry, military electronics, appliance manufacturers, medical devices, and toy/video game manufacturers, among many others.

[0003] Digital circuits (e.g. a digital processor or other logic element) generally operate on signal waveforms having a square shape (e.g. a sequence of pulses having rising and falling edges which are generally square or rectangular in shape). When such square waveforms are generated, transmitted, received or otherwise used by a digital processor or other logic element, the square edges may produce spurious signals over a wide range of frequencies. Such broadband spectral content can make its way back to other components, such as sensors, actuators, and analog signal conditioners. This extraneous and unwanted spectral content often limits or degrades sensor/actuator performance. Extraneous content can make its way to sensitive electronics generally in at least two ways. First, via

conducted paths, such as power supplies, grounds, etc., and second, via radiated paths, such as crosstalk, EMI, etc. Safeguarding against these sources of ingress can often be very challenging.

[0004] Systems containing sensors (of any type) are particularly susceptible to EMI/RFI emissions, for example from conductive paths or radiative paths. Even systems not containing sensors are usually required to pass EMI/RFI testing to ensure that such systems do not pollute other systems or subsystems through electromagnetic or radio frequency emissions. Electrical interference from one sub-system (often digital) can degrade the performance of another (often a sensor or an analog component).

[0005] It would, therefore, be desirable to provide a digital logic family with intrinsically low EMI/RFI emissions.

SUMMARY

[0006] In a circuit, a method to assess a state of an incoming bit comprises receiving an input signal; receiving a clock signal; obtaining a product signal from the product of the input and clock signals; integrating the product signal over a clock period to determine a logic state of the input signal; providing the determined logic state to a pulse generator; and providing an output signal having a spectrally-efficient-shape at an output of the pulse generator, wherein the spectrally-efficient-shaped output signal represents a logic value corresponding to the logic value of the input signal. The product signal can be integrated over a first-half of the clock period and the output signal is output by the pulse generator over a second-half of the clock period. The product signal can be integrated over a first portion of the clock period and the output signal is output by the pulse generator over a second portion of the clock period. The spectrally-efficient-shaped pulses can be Gaussian-shaped pulses. Integrating the product signal over one-half of a clock period can comprise obtaining an average value; slowly discharging the average over the second half of the clock period; and determining the logic state (State(k)) of the input signal according to:

[0007] State(k) = $\int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k)dt$

in which:

State(k) is the logic state of the input signal;

Input(tk) is the input signal at time t = tk;

Clk(tk) is the clock signal at time t = tk.

[0008] The method of claim 1 can provide the determined logic state to a pulse generator by applying limits to state result; formulating the pulses from the incoming clock; and State steers a 0 to Q and a 1 to Qbar or vise-versa. The spectrally efficient waveform can be formed by EXP -0.5*(t/σ)^2 Fourier Transform -> σ*sqrt(2*π)*EXP -0.5*(ω*σ)^2. The circuit can comprise a combinatorial circuit. The circuit can comprise a sequential circuit.

[0009] A circuit comprises a multiplier circuit having a first input configured to receive an input signal and having a second input configured to receive a clock signal and having an output configured to provide a product signal corresponding to the product of an input signal and a clock signal; an integrator circuit having an input coupled to the output of said multiplier circuit and having an output, said integrator configured to integrate the product signal over a clock period to determine a logic state of the input signal; a limit circuit having an input coupled to the output of said integrator circuit and having an output, said limit circuit configured to apply limits to a state result provided to the input thereof from said integrator circuit; and a pulse generator having an input coupled to the output of said limit circuit and having an output, said pulse generator configured to receive the logic state from said limit circuit and to provide over the clock period at the output thereof an output signal having a Gaussian-shape output signal pulse, wherein the Gaussian-shaped output signal pulse represents a logic value corresponding to the logic value of the input signal. The product signal can be integrated over a first-half of the clock period and the output signal is output by the pulse generator over a second-half of the clock period. The product signal can be integrated over a first portion of the clock period and the output signal is output by the pulse generator over a second portion of the clock period. The spectrally-efficient-shaped pulses

can be Gaussian-shaped pulses. The integrator is configured to determine during a first-half of a clock period, a logic state of the input signal according to:

[0010] State(k) = $\int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k)dt$

in which:

State(k) is the logic state of the input signal;

Input(tk) is the input signal at time t = tk; and

Clk(tk) is the clock signal at time t = tk.

[0011] The spectrally efficient waveform can be formed by EXP -0.5*(t/σ)^2 Fourier Transform -> σ*sqrt(2*π)*EXP -0.5*(ω*σ)^2.

[0012] In a circuit, a method comprising receiving a spectrally-efficient signal comprising a plurality of spectrally-efficient pulses; receiving a complementary spectrally-efficient signal; comparing the spectrally-efficient signal to the complementary spectrally-efficient signal; and determining a logical value corresponding to the spectrally-efficient signal. The spectrally-efficient signal comprises a plurality of Gaussian shaped pulses. The circuit comprises at least one of a combinatorial circuit and a sequential circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing features may be more fully understood from the following description of the drawings in which:

[0014] Fig. 1 is a block diagram of an illustrative system containing one or more sensors and operable with spectrally efficient digital logic (SEDL);

[0015] Fig. 2 is a graphical diagram in the time domain (i.e. a plot of voltage vs. time) showing an example of a conventional logic waveform and an example of a spectrally efficient example waveform;

[0016] Fig. 3 is a schematic circuit diagram showing an example combinatorial circuit for an address decoder operable with SEDL;

[0017] Fig. 4 is a graphical diagram in the time domain showing example conventional logic waveforms and example SEDL waveforms for the combinatorial circuit of Fig. 3;

[0018] Fig. 5 is a schematic diagram showing an example combinatorial buffer circuit operable with SEDL;

[0019] Fig. 6 is a block diagram showing an example sequential circuit to implement the SEDL techniques of the present disclosure;

[0020] Fig. 7 is a graphical diagram showing various signals of the example sequential circuit of Fig. 6, illustrating an integrating portion and a discharging portion of the signal processing;

[0021] Fig. 8 is a graphical diagram showing various signals of the example sequential circuit of Fig. 6, showing the data in, data out, and clock cycle delay;

[0022] Fig. 9 is a block diagram showing an example sequential state retention circuit having a master flip-flop and a slave flip-flop;

[0023] Fig. 10 is a graphical diagram showing the waveforms of the example sequential state retention circuit of Fig. 9; and

[0024] Fig. 11 is a block diagram showing a combined circuit including both combinatorial logic elements and sequential logic elements, using the SEDL techniques in accordance with the present disclosure.

[0025] It should be appreciated that the drawings are not necessarily to scale, or inclusive of all elements of a system, emphasis instead generally being placed upon illustrating the concepts, structures, and techniques sought to be protected herein.

DETAILED DESCRIPTION

[0026] Before proceeding with a discussion of illustrative embodiments of spectrally efficient digital logic (SEDL) techniques (referred to herein as “SEDL” or “spectrally-efficient” techniques), some introductory concepts and terminology are explained.

[0027] In general overview, the term “digital logic circuit” (or more simply “logic circuit” or “logic element”) refers to a circuit or device capable of receiving one or more input signals (or more simply “inputs”) and in response thereto, providing one or more output signals (or more simply “outputs”) with the output signal having a Boolean logic relationship to the input signal. One type of logic circuit is a logic gate (such as an AND gate). Digital logic circuits may have one or more inputs, and one or more outputs. Individual logic circuits can be connected together to form combinatorial or sequential circuits, or relatively complicated logical functions that can include both combinatorial (e.g., gate) and sequential (e.g., flip-flop) components. Known digital logic families include, but are not limited to, transistor-transistor logic (TTL), complementary-metal-oxide semiconductor (CMOS) logic, and emitter-coupled logic (ECL), for example.

[0028] The spectrally efficient techniques disclosed herein are applicable to both CMOS and bipolar technologies, as well as optical transceivers, and more generally any system that receives signals and performs digital logic or processing.

[0029] In accordance with an embodiment of concepts, systems, methods and devices described herein, rather than providing or otherwise utilizing conventional square waves to represent an incoming bit (or to output a logical 1 or 0 from a spectrally efficient waveform), in accordance with the techniques described herein, spectrally efficient waveforms (e. g., waveforms which include pulses having a Gaussian or other spectrally efficient shape) may be provided to a digital circuit such as a digital processor. The spectrally efficient waveforms reduce spectral content and, thus, reduce EMI/RFI produced by the associated circuit(s).

[0030] One advantage of using spectrally efficient pulses as compared to a conventional square wave, for example, is that spectrally efficient pulses do not make use of fast-edge switching. Waveforms which include square edges needed for fast edge switching produce a relatively large number of “harmonic signals” (or more simply “harmonics”). Such undesired harmonic signals can be a source of undesired bit errors (sometimes referred to as “logic glitches” or more simply “glitches”) in digital circuits. Thus, conventional logic systems which operate with square shaped waveforms are susceptible to logic glitches.

A spectrally efficient waveform is a waveform which produces relatively few "harmonic signals" (or more simply "harmonics"). Thus, the spectrally efficient logic concepts, techniques, systems and devices described herein are tolerant of noise, distortion, and logic glitches as compared to conventional logic systems and techniques.

[0031] The SEDL architecture of the present disclosure is more resilient than conventional logic. Furthermore, the spectrally efficient signals also contain a strong clock component, rendering clock recovery easy. Further still, the spectrally efficient techniques also potentially allow the digital portion of an integrated circuit (IC) to be developed using a similar process that is used for the analog/RF portion of the IC, which can simplify development and manufacturing of the IC.

[0032] As will be described herein, the spectrally efficient waveforms in accordance with the concepts described herein can be implemented in both combinatorial logic circuits and sequential logic circuits as well as in circuits which include both combinatorial logic and sequential logic in a same circuit.

[0033] Using spectrally efficient pulses in combinatorial and/or sequential logic circuits reduces emissions while achieving the same functionality as conventional square waveforms. Additional advantages of the spectrally efficient pulses described herein include reduced supply/ground "bounce" at the signal transitions (bounce in the signal is greatly reduced at signal state transitions), reduced distortion present on imperfect interconnect transmission line, and reduced EMI/EMC (electromagnetic interference / electromagnetic compatibility) crosstalk, which scales with frequency due to the reduced high frequency content at the same data rate. The emissions are reduced in at least conducted and radiated emissions. Enhanced determination of logic state is achieved through the spectrally efficient pulses, which are noise and distortion tolerant and compatible with standard logic families. The spectrally efficient pulses and concepts described herein can be applied to build an entire logic system or certain desired portions of an overall system. Thus, after reading the disclosure provided herein, it will be appreciated that the SEDL waveforms can be used for either the combinatorial or the sequential circuits, or in circuits including both combinatorial and sequential components, to achieve low EMI/RFI in accordance with the present disclosure.

[0034] It should thus be appreciated that the broad concepts described herein are not limited to any particular implementation details such as a specific arrangement of circuits. Rather the broad concepts described herein may be applied to a wide variety of different arrangement of combinatorial and/or sequential circuits while maintaining structural relationships to provide a spectrally efficient system.

[0035] As used herein, "and/or" means "and" or "or", as well as "and" and "or." Also, “at least one of X and Y” means “X or Y” as well as “X and Y.” Moreover, all patent and non-patent literature cited herein is hereby incorporated by references in its entirety for all purposes.

[0036] Turning now to Fig. 1, a system 100, which may be any appropriate instrumentation or device, such as a cell phone or other system having one or more sensor(s) and in some cases actuators as well, includes at least one sensor 110 coupled to an analog signal conditioner 112. The analog signal conditioner 112 conditions (e.g. filters, amplifies, or otherwise processes) the signal received from the sensor 110 and provides the conditioned signal to an analog-to-digital converter (ADC) 114. The ADC receives the signal provided there to and converts the analog signals from signal conditioner 112 into a stream of digital bits. The stream of digital bits produced by ADC 114 are provided to an input of a digital data processor 116 for subsequent processing. In some cases, the resulting process is used to drive actuators via a path including a digital-to-analog converter (DAC) 120, an analog signal conditioner 122, and an actuator 124.

[0037] The concepts of the present disclosure output spectrally efficient pulses at the output of the ADC 114 and receive spectrally efficient pulses at the DAC 120, which determines the logic state using pulses, as will be appreciated upon reading the present disclosure. Refer to Figs. 3 and 5 showing example combinatorial circuits using SEDL concepts and refer to Fig. 6 showing an example sequential circuit using the SEDL concepts.

[0038] It should be appreciated that although only one sensor and one actuator are shown in Fig. 1, the concepts described herein are applicable to systems which include one or more sensors and one or more actuators, as well as

to complex systems having multiple instances of system 100 as shown in Fig. 1 connected together to provide multiple sensors and multiple actuators under control of multiple processors or a single processor.

[0039] Example sensors for the sensor 110 include magnetic field sensors, motion sensors, microphones, acoustic sensors, optical receivers, RF sensors, electromagnetic sensors, or any other sensor that senses a parameter or other feature of an object or incoming signal (such as an optical or RF signal) and generates an analog or digital signal or otherwise uses digital logic. It will be appreciated that some sensors may be coupled to an ADC and may generate an analog signal that is digitized by the ADC, or may have an integrated ADC to produce a digital signal. The spectrally efficient techniques herein are applicable to both types of sensors to evaluate an incoming bit and output a Gaussian pulse as opposed to a conventional square waveform.

[0040] Referring now to Fig. 2, a conventional waveform 210 has rising and falling edges having a substantially square shape. See, for example, rising edges 210a, 210c, 210e of the square waveform 210 and falling edges 210b, 210d of the square waveform 210. As noted above, such square edges can generate undesired spectral content. The square signals contain two levels representing binary states 0 and 1, with the transition between logic states (e.g. a “0” state and a “1” state) occurring in a short period of time (generally referred to as a “narrow transition” between logic states). When such narrow transitions are combined with a relatively high I/O count (due to a circuit receiving or transmitting a large number of signals) a relatively high level of emissions may result. This is undesirable.

[0041] Waveform 220, on the other hand, corresponds to a spectrally efficient digital logic (SEDL) waveform which includes the same information (bits of data) as waveform 210. In an embodiment, the pulses which exist in the SEDL waveform 220 are formed using one or more Gaussian shaped pulses.

[0042] As illustrated in Fig. 2, each bit of data in the square waveform 210 has a corresponding set of Gaussian pulses (with a set of pulses defined herein as one or more pulses) in the spectrally efficient waveform 220. Note that the transition between logic states in a spectrally efficient waveform takes a longer

period of time as compared to such a transition in a conventional square waveform. Thus, the spectrally efficient waveform is said to have a slower transition timing than a conventional waveform having rectangular or square-shaped pulses. With each bit is represented by one Gaussian-shaped pulses producing a corresponding Gauss shaped frequency spectrum and is more spectrally efficient (i.e., has fewer harmonics and/or occupies a smaller portion of the frequency spectrum) than a conventional rectangular (square-shaped) pulse.

[0043] A Gaussian-shaped pulse can be expressed as EXP -0.5*(t/σ)^2 Fourier Transform -> σ*sqrt(2*π)*EXP -0.5*(ω*σ)^2, where t is time, ω is angular frequency, and σ is 14.74% of a bit period. Another useful property of a Gaussian-shaped pulse is that it survives integration and/or differentiation as occurs in filtering operations. Gaussian pulse also eliminate the need for an associated clock to the square wave, as each bit is represented by a Gauss shaped pulse.

[0044] Note that by replacing the conventional square waveform with a spectrally efficient waveform having a plurality of pulses, the pulses not only provide the logic value (high or low), but also provide the number of instances of that logic value (e.g., the number of bits). So rather than providing a logical high or low, the spectrally efficient waveform provides separate pulses for each logic value that correspond to each bit of the waveform.

[0045] When receiving an incoming SEDL waveform, in order to derive the logical value associated with each of the SEDL pulses, a complementary SEDL signal is compared to the original SEDL signal. The Gauss pulse data is differential so that the data signal is actually the signal minus its complement. The original SEDL signal minus its complementary signal has a value comparable to the conventional square wave peak to peak value.

[0046] Although described in some instances as being a Gaussian Pulse shaped waveform, it should of course, be appreciated that any spectrally efficient waveform can be implemented in accordance with the present disclosure. Other examples of spectrally efficient waveforms include (1) approximations to Gaussian pulses, (2) sinusoidal waveforms, (3) a non-return-to-zero (NRZ) waveform (e.g., formed by summing the outputs of two cascaded SEDL flip-flops) which appears to

be similar to traditional square waves, but it is spectrally efficient due to the slow edges on bit transitions.

[0047] Reference is now made to Figs. 3-4 showing an example combinatorial circuit for an address decoder and the various signals associated therewith, in accordance with an embodiment of the present disclosure. Fig. 3 is a schematic circuit diagram showing an example combinatorial circuit 300 for an address decoder, and Fig. 4 is a graphical diagram 400 showing both conventional logic example waveforms and spectrally efficient example waveforms for the combinatorial circuit of Fig. 3.

[0048] Referring first to Fig. 3, an illustrative address decoder circuit 300 is an example combinatorial circuit capable of receiving a 2 bit address (A, B) and has four (4) corresponding device select lines (Y0, Y1, Y2, Y3). The address decoder circuit 300 is operable with SEDL pulses (i.e. spectrally-efficient waveforms) to implement the digital logic without any modifications required to the circuit design.

[0049] Thus, in response to one or more spectrally-efficient pulses corresponding to an address for a particular device provided to the decoder circuit address inputs A, B the decoder provides an output signal on a selected one of outputs Y0, Y1, Y2, Y3 for the particular device. It should be appreciated that although Fig. 3 illustrates a single address decoder capable of serving multiple devices coupled to an address bus (i.e. each device coupled to one of outputs Y0, Y1, Y2, Y3), the SEDL pulses described herein are also useful when used with a dedicated, single-output address decoder which may be incorporated into each device on an address bus.

[0050] Various input and output waveforms are shown in FIG. 4 as both square waveforms and Gaussian pulse-shaped waveforms to illustrate use of both types of waveforms in the combinatorial circuit. The waveforms show the same information, with each bit in the conventional square wave being represented by either a logical high or low value, and each bit in the SEDL waveform being represented by a pulse.

[0051] As shown in Fig. 3, the input of the OR gate 310 is coupled to input signal “B”. Similarly, the first input of the OR gate 312 is coupled to the input signal

"A". The output of the OR gate 310 is coupled to each of the AND (or NAND) gates 320, 322, 324, 326. The output of the OR gate 312 is coupled to the other input for each of the AND (or NAND) gates 320, 322, 324, 326. The output of the AND gates 320, 322, 324, 326 are the select lines Y0, Y1, Y2, Y3, respectively.

[0052] As shown in FIG. 4, input signals A and B (and identified with reference numerals 426, 430) are used to select lines Y0, Y1, Y2, or Y3 on the decoder. Significantly, inputs A and B are spectrally-efficient waveforms 430, 426.

[0053] For comparison, corresponding conventional square waveforms 432, 428 are also shown.

[0054] As shown, when A is 0 and B is 0 the output is Y0; when A is 1 and B is 0, the output is Y1; when A is 0 and B is 1 the output is Y2; and when A is 1 and B is 1 the output is Y3. This provides four select lines using two inputs and same result using square and Gaussian-shaped pulse waveforms. Note that the spectrally-efficient waveforms provide the same output without emissions concerns associated with conventional square waveforms. The Gaussian pulse can nominally have a fixed value within a given logic family. For example, the Gaussian pulse can have a 0.25 volts peak for this implementation of a CML/ECL type of cases. Other values can be used, however, for different implementations. For example, TTL can be 0V for a logic 0 ("low") and 5V or 3.3V for a logic 1 ("high"). Different voltage values can be used for different SEDL families.

[0055] Fig. 5 is a schematic diagram showing an example combinatorial buffer circuit 510, in accordance with an embodiment of the present disclosure. The combinatorial buffer circuit 510 includes a unity gain, current source fed, differential buffer. This provides the signal in true and complementary form. The logic element is an ECL-like "OR" structure (not shown). The potential at the emitter coupled junction of the logic element, is the logical "OR" of its inputs. When using conventional square-shaped waveforms, it is desired to have as much gain as possible to force the signal into a square waveform shape. However, it is not desired to have this same gain when using spectrally-efficient pulses. In fact, the opposite (a reduction in gain) is desired to ensure that the signal does not try to lock into square shape. Thus, resistors (R5, R6, R15, R16) are added to the logic

element to reduce gain, so it does not try to force the signal into a square-shaped waveform and thus retains the spectrally-efficient waveform pulses.

[0056] Reference is now made to Figs. 6-8 showing an example sequential circuit 600 and graphical diagrams 700 and 800 of the various signals associated therewith, in accordance with an embodiment of the present disclosure. Fig. 6 is a block diagram showing an example sequential circuit 600 to implement the SEDL techniques of the present disclosure. Fig. 7 is a graphical diagram 700 showing various signals of the example sequential circuit of Fig. 6, showing an integrating portion and a discharging portion of the signal processing. Fig. 8 is a graphical diagram 800 showing various signals of the example sequential circuit of Fig. 6, showing the data in, data out, and clock cycle delay.

[0057] With reference to Fig. 6, the SEDL sequential device 600 assesses the state of an incoming bit on the data input 610 by integrating over a first portion of the clock period and then discharging over the second portion. The data input 610 and clock signal 612 are received at the multiplier circuit 614 of the SEDL sequential circuit 600. The multiplier circuit 614 is configured to provide a product signal corresponding to the product of the data input signal 610 multiplied the clock signal 612. An integrator circuit 616 has an input coupled to the output of the multiplier circuit 614 and an output coupled to a limit circuit 618. The integrator circuit 616 is configured to integrate the product signal over a first portion of a clock period to determine a logic state of the input signal 610. The limit circuit 618 has an input coupled to the output of the integrator circuit 616 and has a pulse generator output. The limit circuit 618 is configured to apply limits to a state result provided to the input of the limit circuit 618 from said integrator circuit 616. The SEDL sequential device 600 includes a pulse generator 622 having an input coupled to the output of the limit circuit 618 and has an output. The pulse generator 622 is configured to receive the logic state from the limit circuit 618 and to provide an output signal (i.e., discharge) over a second portion (e.g., a second-half) of the clock period at the output thereof having a spectrally-efficient shaped output signal pulse, wherein the spectrally-efficient shaped output signal pulse represents a logic value corresponding to the logic value of the input signal 610.

[0058] The integrator circuit is configured to determine the logic state of the input signal during a first period (e.g., a first-half) of a clock period according to:

$$\text{State(k)} = \int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k)dt$$

[0059] in which:

State(k) is the logic state of the input signal;

Input(t_k) is the input signal at time t = t_k; and

Clk(t_k) is the clock signal at time t = t_k.

[0060] Integrating by the integrator circuit 616 over a first portion (e.g., first-half) of a clock period provides the "average" value of the bit, which is provided to the filter 618. The average is then slowly discharged over the second portion (e.g., second-half) of the clock period. The aggregate "integrate-discharge" operation reflects the logic state of the input signal.

[0061] Providing the determined logic state to the pulse generator 622 comprises applying limits to the state result, formulating the pulses from the incoming clock, and the output state of the integrator determines the polarity of the pulse generator output circuit.

[0062] Fig. 7 shows the various signals corresponding to the example sequential circuit of Fig. 6 and illustrates the integrating portion during a first time period T1 and the discharge portion during the second time period T2, which are used to determine the logic state of the input signal. The first time period T1 can be a first-half of the clock cycle, and the second time period T2 can be a second-half of the clock cycle. The first time period T1 and the second time period T2 do not overlap with each other and can be the same duration or one period can be longer or shorter than the other. As will be appreciated in light of the present disclosure, the state is then fed to a pulse generator arrangement 622 which generates a new pulse with every clock cycle. Limits to the state are applied to the logic state by the limit circuit 618.

[0063] The various waveforms shown in Figs. 7 and 8 include (i) the data-in waveform 710 which can be the value input at data 610 to the multiplier circuit 614 in Fig. 6, (ii) data-in bar waveform 712, (iii) the clock signal waveform 714, (iv) the data*clock waveform 716 which can be the output of the multiplier circuit 614 of Fig. 6, (v) the data*clock bar waveform 718, (vi) the integrator output waveform 720 which can be the output of the integrator circuit 616 of Fig. 6, (vii) the integrator output bar waveform 722, (viii) the data out waveform 724 which can be Q output 626 in Fig. 6, and (ix) the data out bar waveform 726 which can be Qbar output 628 in Fig. 6.

[0064] As shown in Fig. 8, the output is delivered one-half of a clock cycle later than the input. The state is held for one clock cycle. Note that the output data 832 matches the input data 830 with a half clock cycle delay, as is similarly observed with the conventional flip-flop logic gate.

[0065] Reference is now made to Figs. 9-10 showing an example sequential state retention circuit 900 and a graphical diagram 1000 of the corresponding various input and output waveforms, according to an embodiment of the present disclosure. Fig. 9 is a block diagram 900 showing an example sequential state retention circuit having a master flip-flop and a slave flip-flop. Fig. 10 is a graphical diagram 1000 showing the waveforms of the D flip-flop circuit.

[0066] As shown in Fig. 9, a state retention device 900 is provided by using two D flip-flops in a master-slave arrangement and implementing the spectrally-efficient techniques of the present disclosure. As will be appreciated upon reading the present disclosure, to implement the spectrally-efficient pulses, each flip-flop 920, 942 includes, respectively, a multiplier circuit 924, 944; an integrator circuit 926, 946; a limit circuit 928, 948; and a pulse generator/selector arrangement 930/932, 910/942. A conventional D-type flip-flop typically holds a state for one clock cycle and is capable of holding the state indefinitely. SEDL flip-flops can also hold the state indefinitely.

[0067] The input of the first (master) flip-flop 920 can be switched from new data 910 to the output of the second (slave) flip-flop 942 for previously read data. The state can now be held indefinitely by including the second flip-flop. When the master 920 is listening to the slave 942, it holds the save until the master 920 is

switched back to listening to data input 910. Operating a device whose input is listening to its output can often create stability issues. The integration and regeneration topology used with the spectrally-efficient techniques of the present disclosure facilitates indefinite state retention, without producing a stability problem. The integrate/regenerate topology:

$$\text{State(k)} = \int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k) dt$$

GPdataOut = Limit [State(k)]*{ cos(2*pi*f) +1}^2

[0068] The matched filter output is "limited" (by the limit circuit 928) before driving the pulse generator which, in effect, holds the poles of the system on the jw axis at the clock frequency. The poles do not lie in either the right or left half plane which would cause an exponential increase or decay of the data being held indefinitely.

[0069] As shown in Fig. 10, the logic state can be saved for on clock cycle within a flip flop. The output is one-half clock cycle delayed from the input. A second flip-flop (slave) 942 can be attached to the output of the master 920. This saves the data for another clock cycle. The data out of the master 920 is delayed by one-half of a clock cycle with respect to its input 910. The data out of the slave 942 is delayed by one-half of a clock cycle with respect to its input, which is 1 full clock cycle delayed with respect to the Master input. The slave output is in phase with the master data in 910, but with a full clock cycle of delay. The output of the slave is 1 clock cycle delayed from the input of Master flip-flop 920.

[0070] The various waveforms shown in Fig. 10 include (i) the data-in waveform 1020 which can be the value input at data 910 to the multiplier circuit 914 of Fig. 9, (ii) the data-in bar waveform 1022, (iii) the clock signal waveform 1024 which can be the clock (clk) of Fig. 9, (iv) the latch waveform 1025 which can be latch command controlling the data in 910 of Fig. 9, (v) the latch bar waveform 1026, (vi) the master data out / salve data in waveform 1027 which can be the output of the pulse generator 930 and selector 932 as well as the input to the multiplier circuit 944 of the second flip-flop 942, (vii) the master data out / slave data in bar waveform 1038, (viii) the slave data out waveform 1030 which can be the Q output of pulse generator 940 and selector 950 of the slave flip-flop 942, and (ix)

the slave data out bar waveform 1030, which can be the Q bar output of the pulse generator 940 and selector 950 of the slave flip-flop 942 of Fig. 9. When the latch command is asserted 1040, the master input waveform 1020 is fed by the salve output waveform 1030, and whatever logic state is present at the output is held for as long as the latch remains asserted (period "TA").

[0071] Fig. 11 is a block diagram showing a circuit including combinatorial logic and sequential logic, and operable using the SEDL techniques in accordance with the present disclosure. It will be appreciated in light of the present disclosure that the SEDL techniques can be implemented in combinatorial logic circuits and in sequential logic circuits, as well as in circuits having both combinatorial logic and sequential logic, as shown in Fig. 11. As shown, the combinatorial logic circuit 1101 includes a AND/NAND gate 1110, OR/NOR gate 1112, and XOR/XNOR gate 1114. Using the spectrally-efficient waveforms of the present disclosure, the output of any of the appropriate gates 1110, 1112, or 1114 can be input as data to the sequential circuit 1102. The sequential circuit 1102 is similar to those described herein, including a multiplier circuit that multiplies the data-in 1120 by the clock 1122, an integrator circuit 1126, a limit circuit 1128, a pulse generator 1132 and a selector 1134 to select between Q 1136 and Qbar 1138.

[0072] As is known, combinatorial circuits implement Boolean functions and are functions of their inputs only and are not based on clocks or states, whereas sequential circuits compute their output based on the output and the state, with the state being updated based on a clock input. Thus, the sequential circuits have state and memory, whereas the combinatorial circuits do not have state or memory.

[0073] It will be appreciated upon reading the present disclosure that the spectrally efficient techniques assume that the shortest data pulse is one clock cycle wide. Meaning, the fastest data transition is not longer than one clock cycle.

[0074] Having described preferred embodiments which serve to illustrate various concepts, structures and techniques which are the subject of this patent, it will now become apparent to those of ordinary skill in the art that other embodiments incorporating these concepts, structures and techniques may be used. Accordingly, it is submitted that that scope of the patent should not be limited

to the described embodiments but rather should be limited only by the spirit and scope of the following claims.

[0075] All publications and references cited herein are expressly incorporated herein by reference in their entirety.

Claims

1. In a circuit, a method to assess a state of an incoming bit, the method comprising:

receiving an input signal;

receiving a clock signal;

obtaining a product signal from the product of the input and clock signals;

integrating the product signal over a clock period to determine a logic state of the input signal;

providing the determined logic state to a pulse generator; and

providing an output signal having a spectrally-efficient-shape at an output of the pulse generator, wherein the spectrally-efficient-shaped output signal represents a logic value corresponding to the logic value of the input signal.

2. The method of claim 1, wherein the product signal is integrated over a first-half of the clock period and the output signal is output by the pulse generator over a second-half of the clock period.

3. The method of claim 1, wherein the product signal is integrated over a first portion of the clock period and the output signal is output by the pulse generator over a second portion of the clock period.

4. The method of claim 1, wherein the spectrally-efficient-shaped pulses are Gaussian-shaped pulses.

5. The method of claim 1 wherein integrating the product signal over one-half of a clock period comprises:

obtaining an average value;

slowly discharging the average over the second half of the clock period; and

determining the logic state (State(k)) of the input signal according to:

$$\text{State}(k) = \int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k) dt$$

in which:

State(k) is the logic state of the input signal;

Input(t_k) is the input signal at time t = t_k;

Clk(t_k) is the clock signal at time t = t_k.

6. The method of claim 1 wherein providing the determined logic state to a pulse generator comprises:

applying limits to state result;

formulating the pulses from the incoming clock; and

State steers a 0 to Q and a 1 to Qbar or vise-versa.

7. The method of claim 1, wherein the spectrally efficient waveform is formed by EXP -0.5*(t/σ)^2 Fourier Transform -> σ*sqrt(2*π)*EXP -0.5*(ω*σ)^2.

8. The method of claim 1, wherein the circuit comprises a combinatorial circuit.

9. The method of claim 1, wherein the circuit comprises a sequential circuit.

10. A circuit comprising:

a multiplier circuit having a first input configured to receive an input signal and having a second input configured to receive a clock signal and having an output configured to provide a product signal corresponding to the product of an input signal and a clock signal;

an integrator circuit having an input coupled to the output of said multiplier circuit and having an output, said integrator configured to integrate the product signal over a clock period to determine a logic state of the input signal;

a limit circuit having an input coupled to the output of said integrator circuit and having an output, said limit circuit configured to apply limits to a state result provided to the input thereof from said integrator circuit; and

a pulse generator having an input coupled to the output of said limit circuit and having an output, said pulse generator configured to receive the logic state from said limit circuit and to provide over the clock period at the output thereof an output signal having a Gaussian-shape output signal pulse, wherein the Gaussian-shaped output signal pulse represents a logic value corresponding to the logic value of the input signal.

11. The circuit of claim 10, wherein the product signal is integrated over a first-half of the clock period and the output signal is output by the pulse generator over a second-half of the clock period.

12. The circuit of claim 10, wherein the product signal is integrated over a first portion of the clock period and the output signal is output by the pulse generator over a second portion of the clock period.

13. The method of claim 10, wherein the spectrally-efficient-shaped pulses are Gaussian-shaped pulses.

14. The circuit of claim 10 wherein:

said integrator is configured to determine during a first-half of a clock period, a logic state of the input signal according to:

$$\text{State}(k) = \int_{t_k}^{t_k+T/2} Input(t_k) * Clk(t_k)dt$$

in which:

State(k) is the logic state of the input signal;

Input(t_k) is the input signal at time t = t_k; and

Clk(t_k) is the clock signal at time t = t_k.

15. The circuit of claim 10, wherein the spectrally efficient waveform is formed by EXP -0.5*(t/σ)^2 Fourier Transform -> σ*sqrt(2*π)*EXP -0.5*(ω*σ)^2.

16. In a circuit, a method comprising:

receiving a spectrally-efficient signal comprising a plurality of spectrally-efficient pulses;

receiving a complementary spectrally-efficient signal;

comparing the spectrally-efficient signal to the complementary spectrally-efficient signal; and

determining a logical value corresponding to the spectrally-efficient signal.

17. The method of claim 16, wherein the spectrally-efficient signal comprises a plurality of Gaussian shaped pulses.

18. The method of claim 16, wherein the circuit comprises at least one of a combinatorial circuit and a sequential circuit.

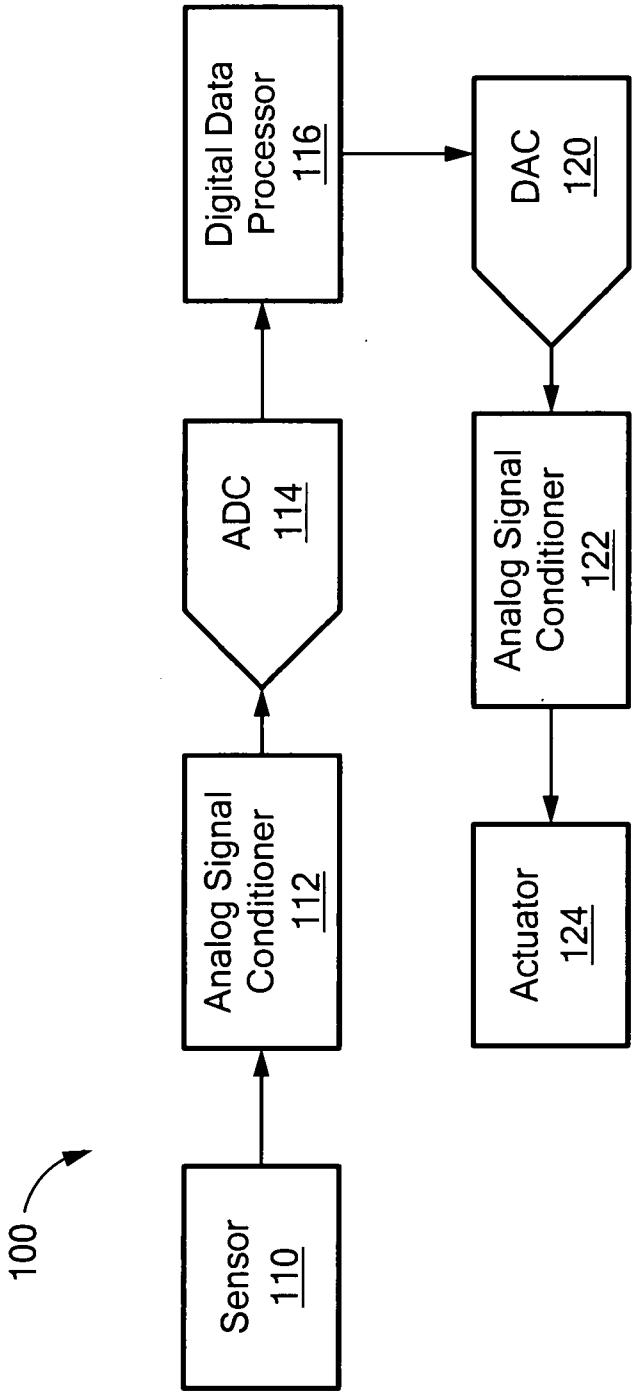
100
Sensor
110
Analog Signal
Conditioner
112
ADC
114
Digital Data
Processor
116
DAC
120
Analog Signal
Conditioner
122
Actuator
124

FIG. 1

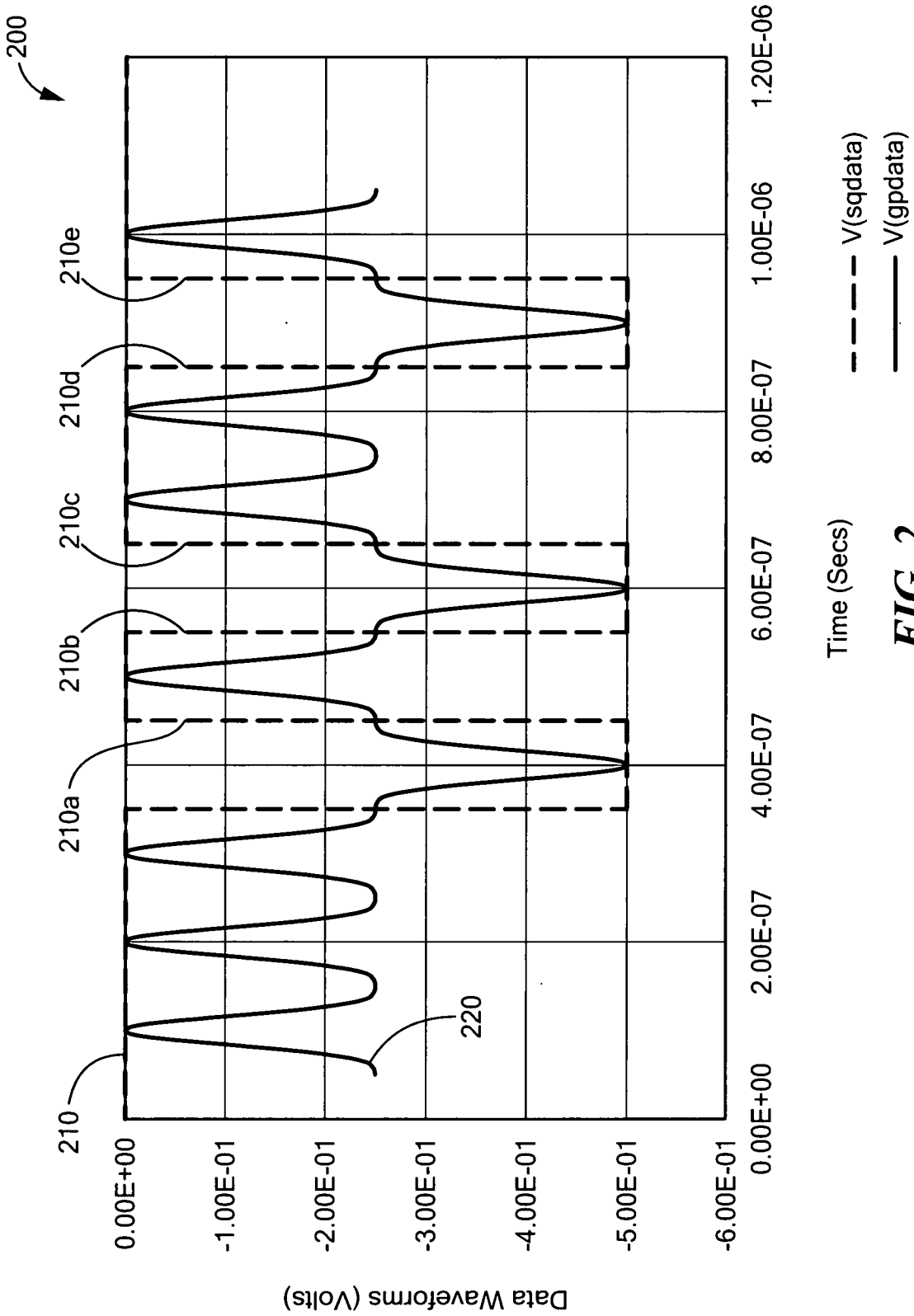
200
210
210a
210b
210c
210d
210e
220
0.00E+00
-1.00E-01
-2.00E-01
-3.00E-01
-4.00E-01
-5.00E-01
-6.00E-01
Data Waveforms (Volts)
0.00E+00
2.00E-07
4.00E-07
6.00E-07
8.00E-07
1.00E-06
1.20E-06
Time (Secs)
V(sqdata)
V(gpdata)

FIG. 2

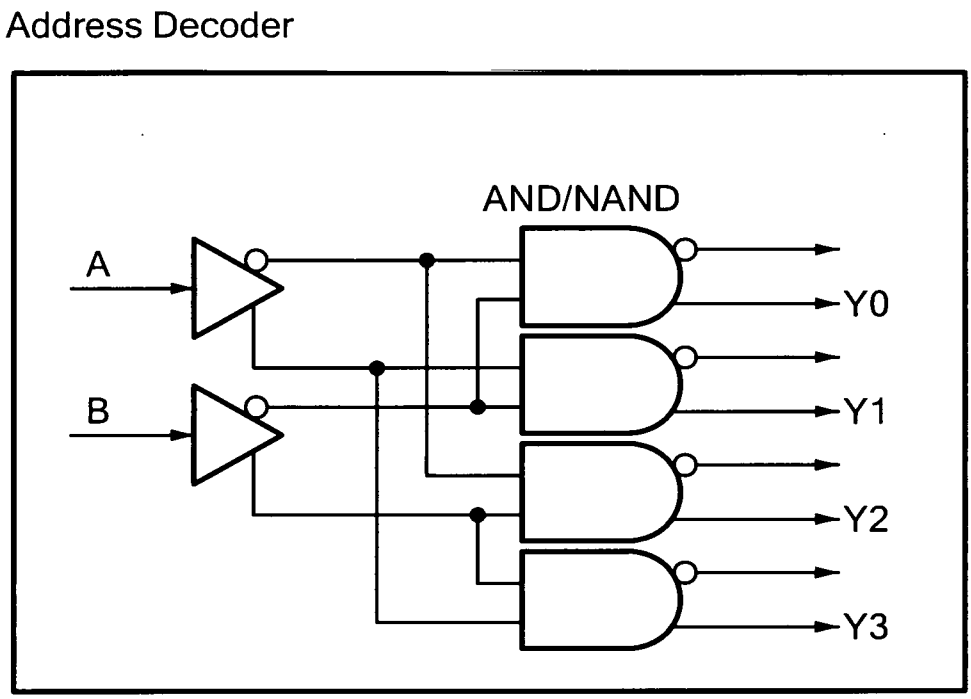

FIG. 3

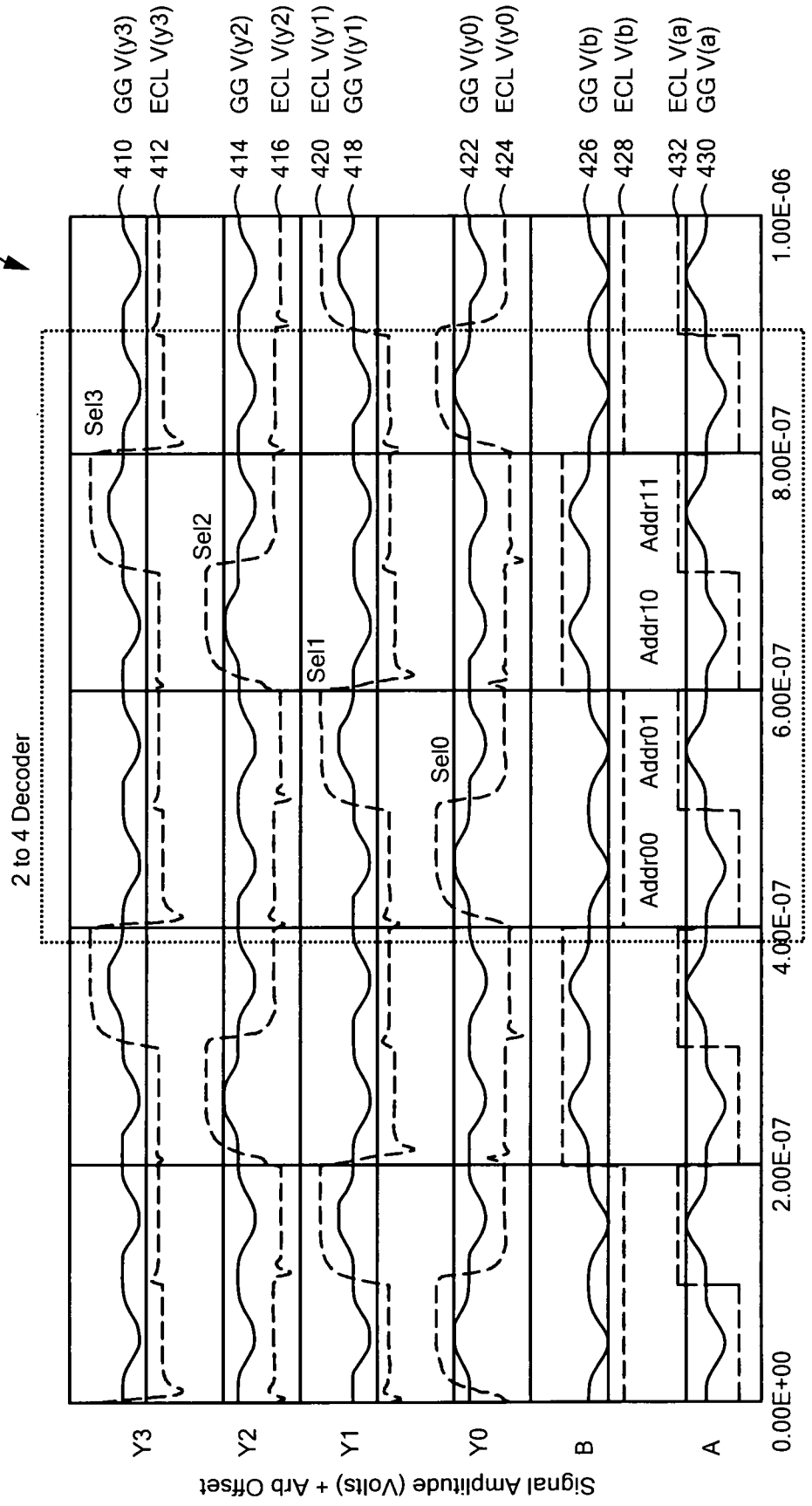
400
2 to 4 Decoder
GG V(y3)
ECL V(y3)
GG V(y2)
ECL V(y2)
ECL V(y1)
GG V(y1)
GG V(y0)
ECL V(y0)
GG V(b)
ECL V(b)
ECL V(a)
GG V(a)
410
412
414
416
420
418
422
424
426
428
432
430
Sel3
Sel2
Sel1
Sel0
Addr00
Addr01
Addr10
Addr11
Y3
Y2
Y1
Y0
B
A
Signal Amplitude (Volts) + Arb Offset
0.00E+00
2.00E-07
4.00E-07
6.00E-07
8.00E-07
1.00E-06
Elapsed Time (Sec)

FIG. 4

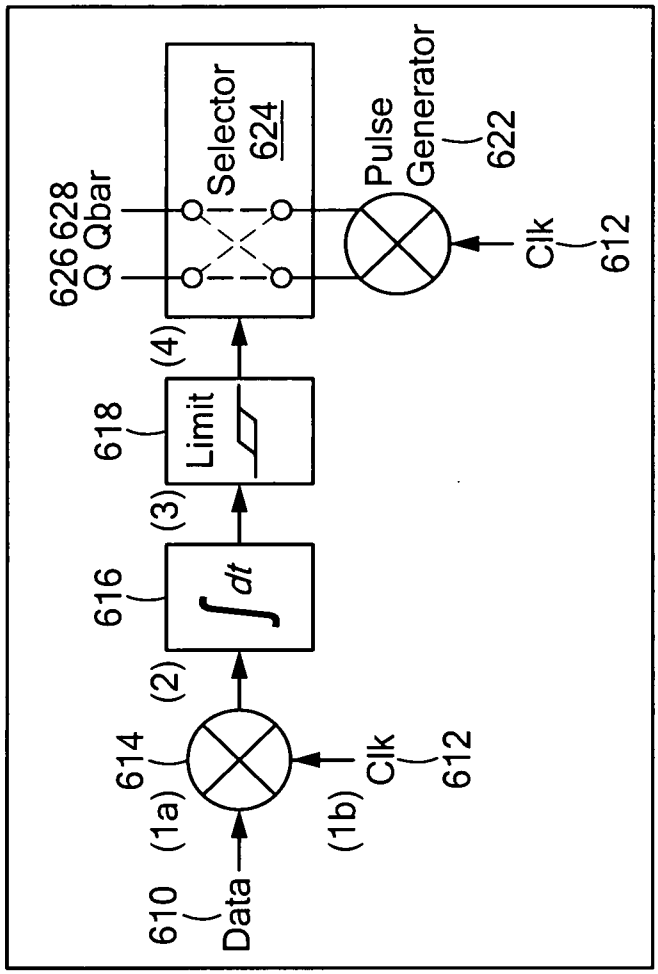
600
626 628
Q Qbar
Selector
624
Pulse
Generator
622
Clk
612
618
Limit
(4)
(3)
616
$\int dt$
(2)
614
(1a)
(1b)
Clk
612
610
Data

FIG. 6

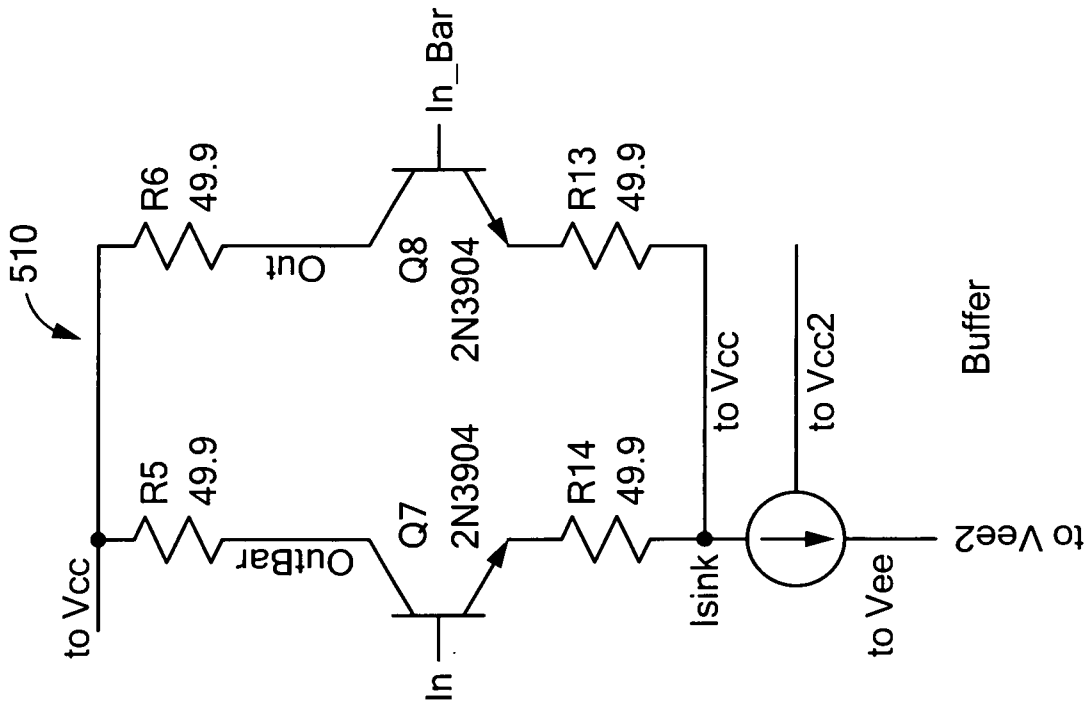
510
R6
49.9
Out
Q8
2N3904
In_Bar
R13
49.9
R5
49.9
OutBar
Q7
2N3904
R14
49.9
to Vcc
to Vcc2
Buffer
to Vcc
In
Isink
to Vee
to Vee2

FIG. 5

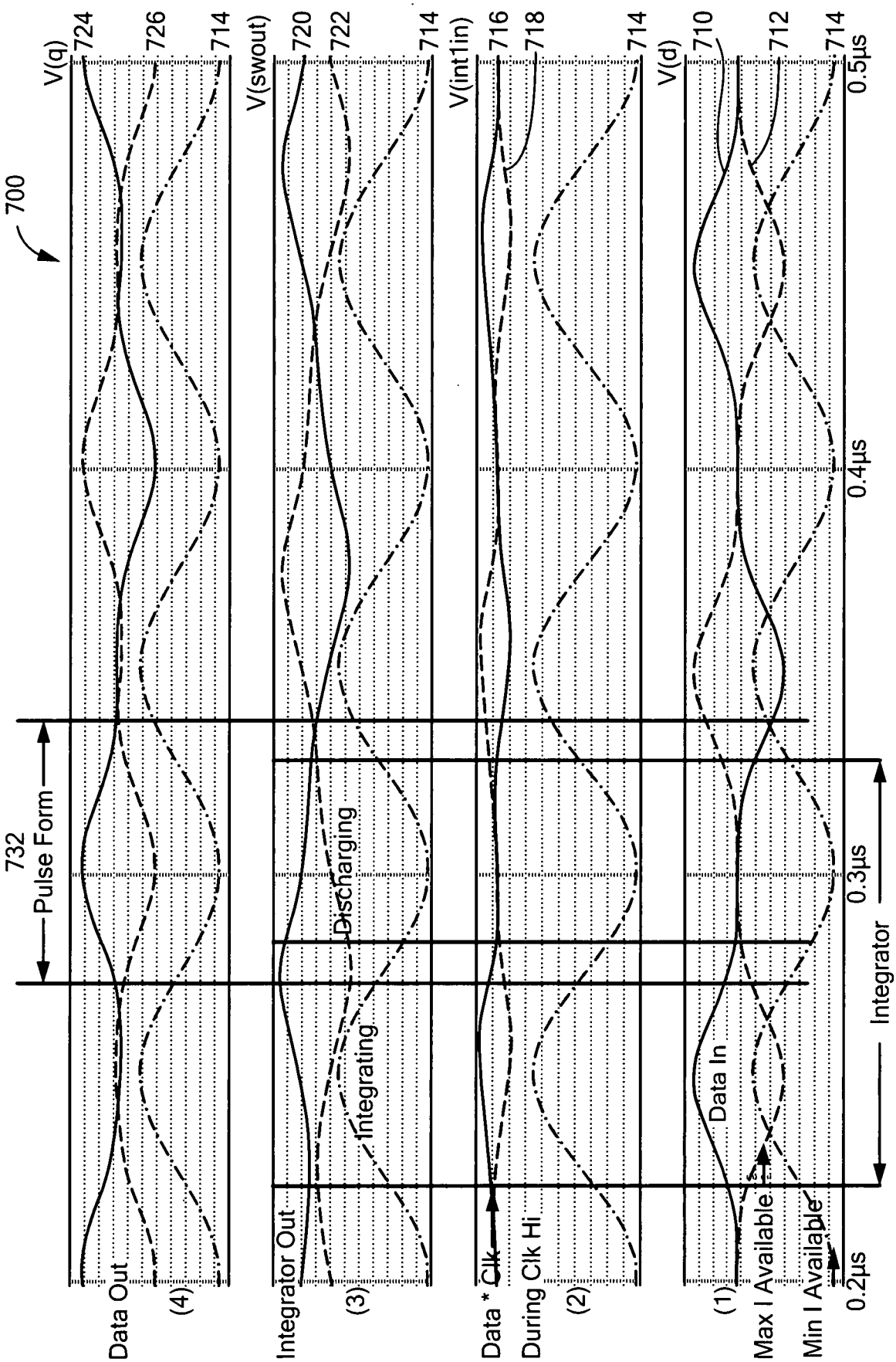
700
V(q)
724
726
714
V(swout)
720
722
714
V(int1in)
716
718
714
V(d)
710
712
714
0.5µs
0.4µs
0.3µs
0.2µs
732
Pulse Form
Integrator
730
T1
T2
Data Out
(4)
Integrator Out
(3)
Discharging
Integrating
Data * Clk
During Clk Hi
(2)
(1)
Data In
Max I Available
Min I Available

FIG. 7

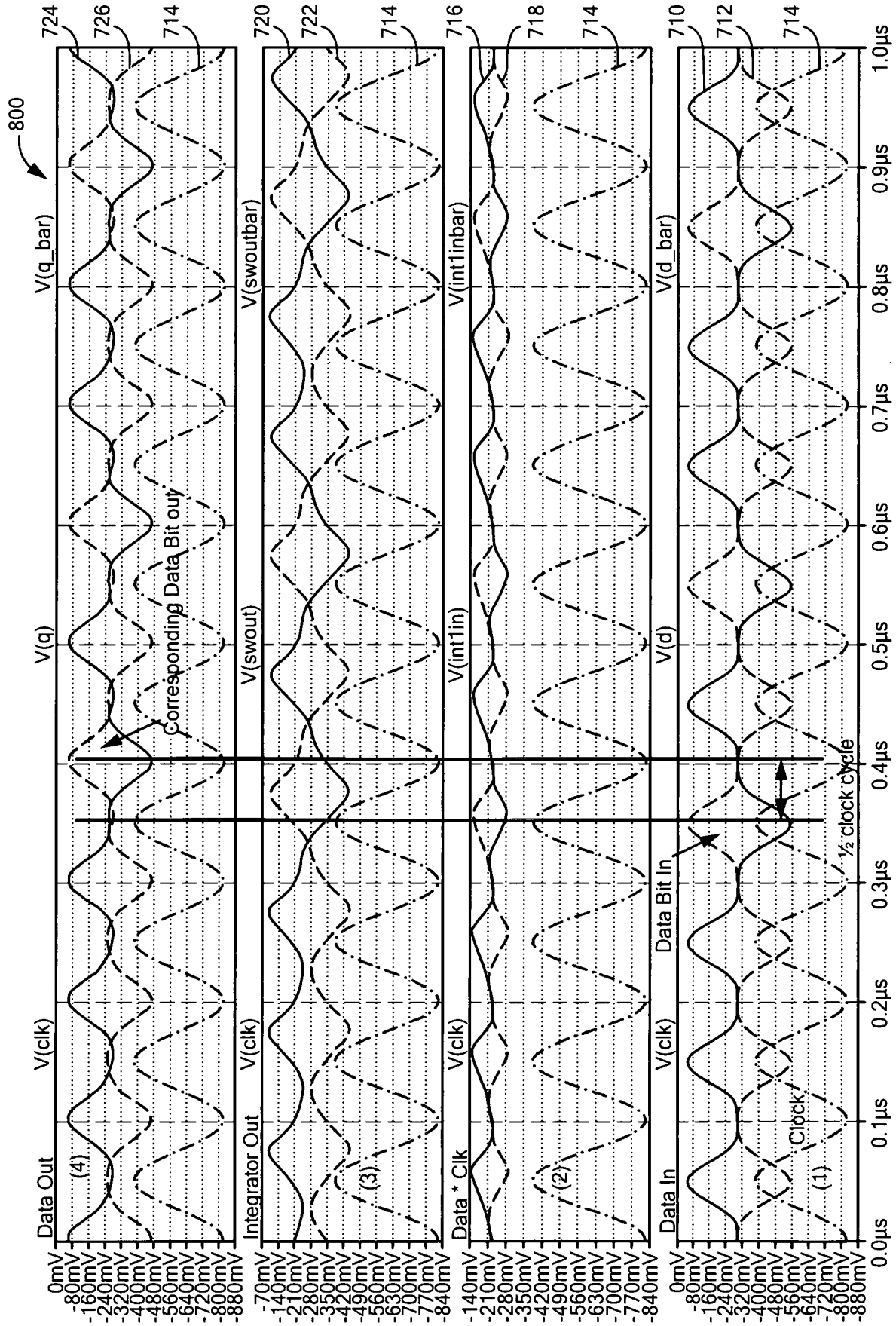
800
724
726
714
720
722
716
718
710
712
V(q_bar)
V(q)
V(swoutbar)
V(swout)
V(int1inbar)
V(int1in)
V(d_bar)
V(d)
V(clk)
Data Out
Integrator Out
Data * Clk
Data In
Data Bit In
Corresponding Data Bit out
Clock
½ clock cycle
(1)
(2)
(3)
(4)
0.0µs
0.1µs
0.2µs
0.3µs
0.4µs
0.5µs
0.6µs
0.7µs
0.8µs
0.9µs
1.0µs
0mV
-80mV
-160mV
-240mV
-320mV
-400mV
-480mV
-560mV
-640mV
-720mV
-800mV
-880mV
-70mV
-140mV
-210mV
-280mV
-350mV
-420mV
-490mV
-560mV
-630mV
-700mV
-770mV
-840mV

FIG. 8

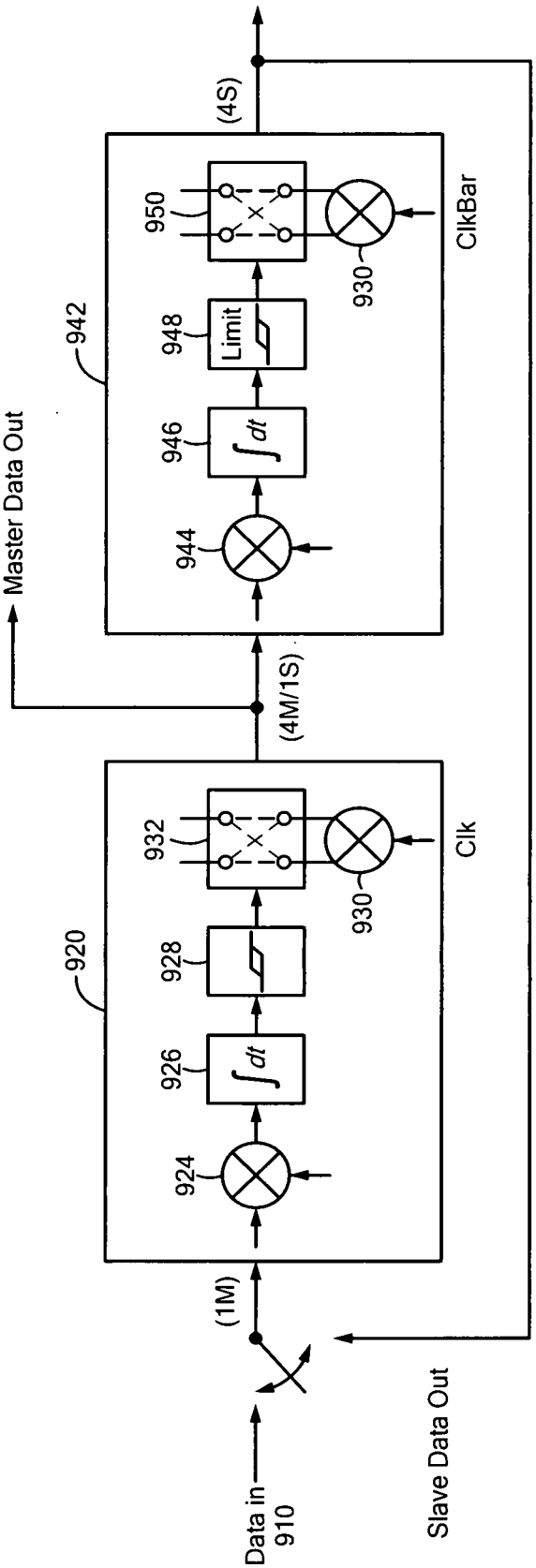
(4S)
950
930
ClkBar
942
948
Limit
946
∫dt
944
Master Data Out
(4M/1S)
932
930
Clk
920
928
926
∫dt
924
(1M)
Data in
910
Slave Data Out

FIG. 9

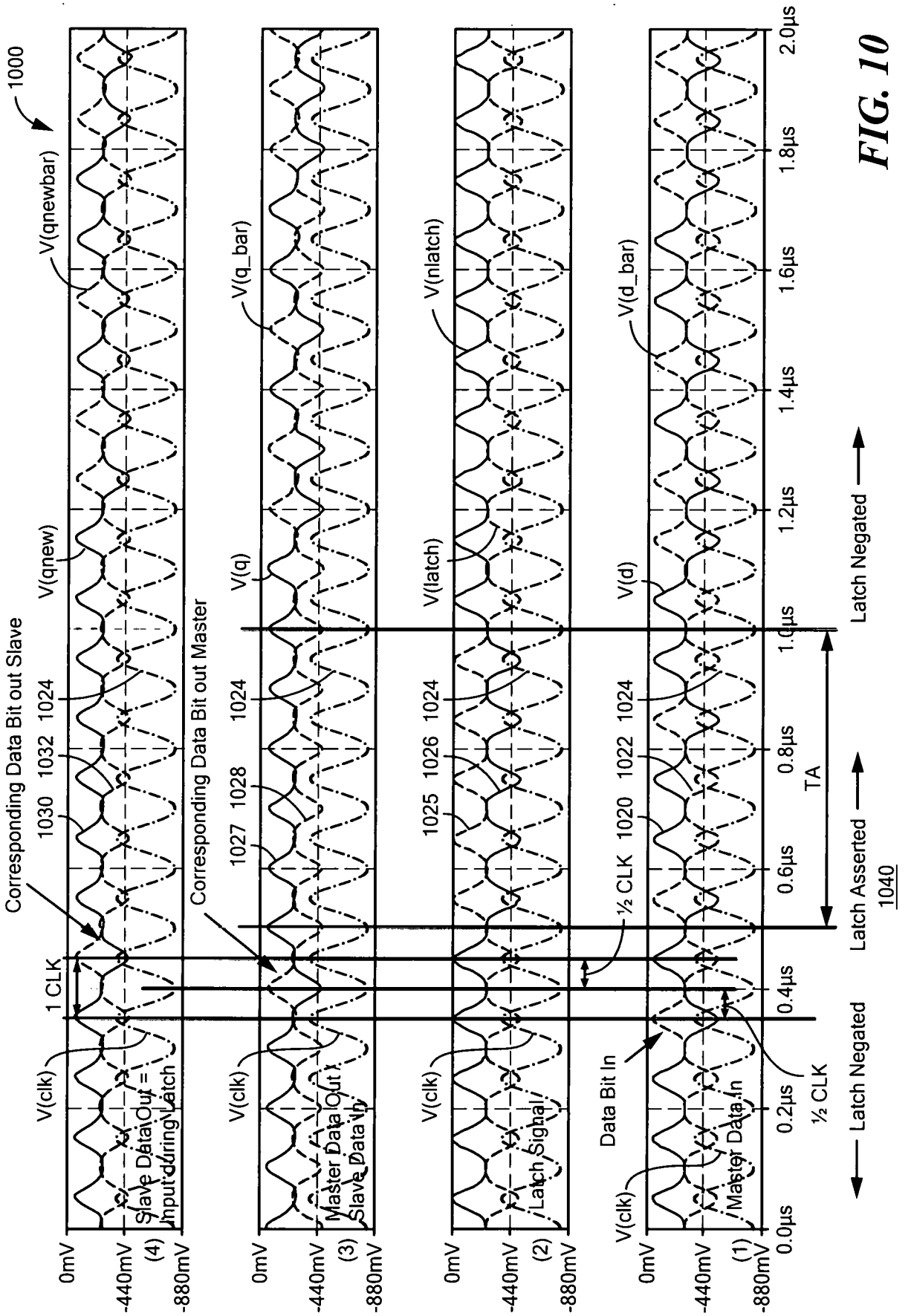
1000
V(qnewbar)
V(qnew)
Corresponding Data Bit out Slave
1 CLK
1030 1032 1024
V(clk)
Slave Data Out = Input during Latch
(4)
0mV
-440mV
-880mV
V(q_bar)
V(q)
Corresponding Data Bit out Master
1027 1028 1024
V(clk)
Master Data Out / Slave Data In
(3)
0mV
-440mV
-880mV
V(nlatch)
V(latch)
1025 1026 1024
V(clk)
Latch Signal
(2)
0mV
-440mV
-880mV
V(d_bar)
V(d)
½ CLK 1020 1022 1024
Data Bit In
V(clk)
Master Data In
(1)
0mV
-440mV
-880mV
0.0µs
0.2µs
½ CLK
0.4µs
0.6µs
0.8µs
1.0µs
1.2µs
1.4µs
1.6µs
1.8µs
2.0µs
TA
Latch Negated
Latch Asserted
Latch Negated
1040

FIG. 10

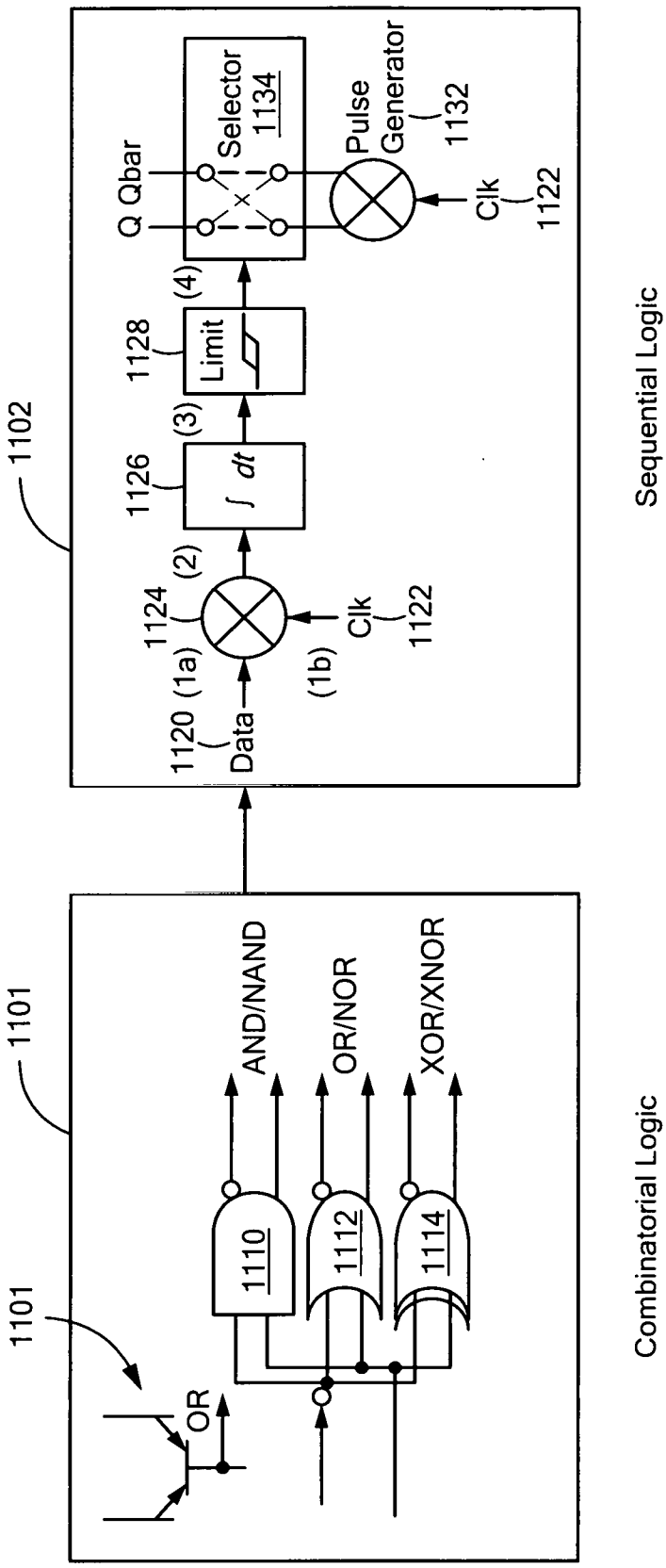
1102
1101
1101
Sequential Logic
Combinatorial Logic
1120 (1a)
Data
1124
(2)
(1b)
Clk
1122
1126
(3)
∫ dt
1128
Limit
(4)
Q Qbar
Selector
1134
Pulse
Generator
1132
Clk
1122
AND/NAND
OR/NOR
XOR/XNOR
1110
1112
1114
OR

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/039704

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K19/0175
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP H08 242173 A (SONY CORP) 17 September 1996 (1996-09-17) abstract; figures 1,2	1-15
A	WO 2006/071197 A1 (AGENCY SCIENCE TECH & RES [SG]; ZHENG YUAN JIN [SG]) 6 July 2006 (2006-07-06) paragraph [0033] - paragraph [0041]; claim 1; figures 1,2,3B	1-15
A	US 2006/098713 A1 (TIAN TONG [SG]) 11 May 2006 (2006-05-11) paragraph [0032] - paragraph [0039]; figures 1,3a	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2019	23/04/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Riccio, Ettore

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/039704

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/039704

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP H08242173 A	17-09-1996	JP 3303585 B2	22-07-2002
		JP H08242173 A	17-09-1996
WO 2006071197 A1	06-07-2006	JP 4560552 B2	13-10-2010
		JP 2008527797 A	24-07-2008
		US 2009021309 A1	22-01-2009
		WO 2006071197 A1	06-07-2006
US 2006098713 A1	11-05-2006	SG 122951 A1	29-06-2006
		US 2006098713 A1	11-05-2006

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15

In a circuit, a method to assess a state of an incoming bit, the method comprising:receiving an input signal;receiving a clock signal;obtaining a product signal from the product of the input and clock signals;integrating the product signal over a clock period to determine a logic state of the input signal;providing the determined logic state to a pulse generator; andproviding an output signal having a spectrally-efficient-shape at an output of the pulse generator, wherein the spectrally-efficient-shaped output signal represents a logic value corresponding to the logic value of the input signal.

---

2. claims: 16-18

n a circuit, a method comprising:receiving a spectrally-efficient signal comprising a plurality of spectrally-efficient pulses;receiving a complementary spectrally-efficient signal;comparing the spectrally-efficient signal to the complementary spectrally-efficient signal; anddetermining a logical value corresponding to the spectrally-efficient signal.
