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(54) **Title:** SIGNAL POWER SPLITTER/COMBINER WITH RESISTANCE AND IMPEDANCE TRANSFORMER LOADING

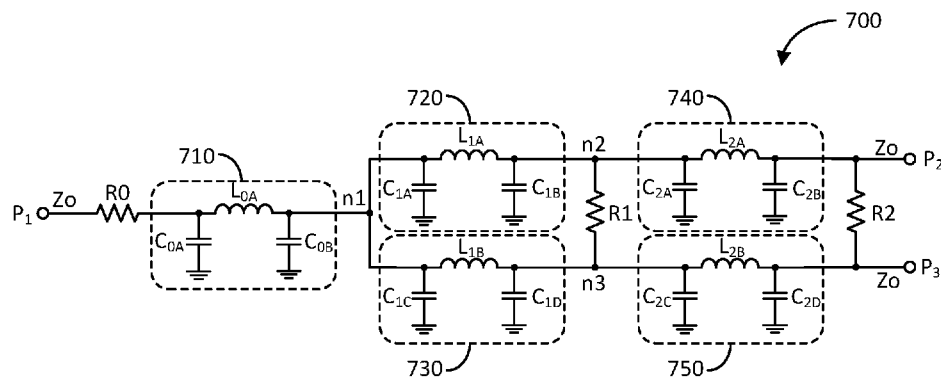


FIG. 7

(57) **Abstract:** An aspect relates to a signal power splitter/combiner (700) including a first signal port (P1); a first resistor (RO); a first impedance transformer (710) coupled in series with the first resistor between the first signal port and a first intermediate node (n1); a second impedance transformer (720) coupled between the first intermediate node (n1) and a second signal port (P2); a third impedance transformer (730) coupled between the first intermediate (n1) node and a third signal port (P3); and a second resistor (R2) coupled between the second and third signal ports. The signal power splitter/ combiner may further include a fourth impedance transformer (740) coupled between the second impedance (720) transformer and the second signal port, a fifth impedance transformer (750) coupled between the third impedance transformer (730) and the third signal port; and a third resistor (R1) coupled between a third intermediate node (n3) and a second intermediate node (n2); the second intermediate node (n2) between the second and fourth impedance transformers (720,740) and the third intermediate node (n3) between the third and fifth impedance transformers (730,750).



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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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SIGNAL POWER SPLITTER/COMBINER WITH RESISTANCE AND IMPEDANCE TRANSFORMER LOADING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present Application for Patent claims priority to pending U.S. Non-Provisional Application no. 17/392,005, filed August 2, 2021, and assigned to the assignee hereof and hereby expressly incorporated by reference herein as if fully set forth below and for all applicable purposes.

FIELD

[0002] Aspects of the present disclosure relate generally to signal power splitters/combiners, and in particular, to a signal power splitter/combiner with resistance and impedance transformer loading for improved performance over a wider bandwidth.

BACKGROUND

[0003] A signal power splitter is configured to receive an input signal, and power split the input signal to generate a set of output signals. Conversely, a signal power combiner is configured to receive a set of input signals, and power combiner the input signals to generate an output signal. Generally, a signal power splitter or combiner has reciprocity property, where the same device may be used as a power splitter or combiner depending on if the input signal is received at a single port on one side of the device, or a set of input signals are received at a set of input ports on another side of the device.

[0004] Other properties of interests of signal power splitters/combiners include insertion loss between an input port and an output port, isolation between two or more input or output ports, and impedance matching or return loss at any of the ports.

SUMMARY

[0005] The following presents a simplified summary of one or more implementations in order to provide a basic understanding of such implementations. This summary is not an extensive overview of all contemplated implementations, and is intended to neither identify key or critical elements of all implementations nor delineate the scope of any or all implementations. Its sole purpose is to present some concepts of one or more implementations in a simplified form as a prelude to the more detailed description that is presented later.

- [0006] An aspect of the disclosure relates to an apparatus. The apparatus includes a first signal port; a first resistor; a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node; a second impedance transformer coupled between the first intermediate node and a second signal port; a third impedance transformer coupled between the first intermediate node and a third signal port; and a second resistor coupled between the second and third signal ports.
- [0007] Another aspect of the disclosure relates to a method. The method includes receiving a first signal at a first signal port; propagating the first signal through a first resistor and a first transformer to generate a second signal at a first intermediate node; splitting the second signal at the first intermediate node to generate third and fourth signals; propagating the third signal through a second impedance transformer towards a second signal port; propagating the fourth signal through a third impedance transformer towards a third signal port; and electrically coupling the second signal port to the third signal port via a second resistor.
- [0008] Another aspect of the disclosure relates to an apparatus. The apparatus includes means for receiving a first signal at a first signal port; means for propagating the first signal through a first resistor and a first transformer to generate a second signal at a first intermediate node; means for splitting the second signal at the first intermediate node to generate third and fourth signals; means for propagating the third signal through a second impedance transformer towards a second signal port; means for propagating the fourth signal through a third impedance transformer towards a third signal port; and means for electrically coupling the second signal port to the third signal port via a second resistor.
- [0009] Another aspect of the disclosure relates to a method. The method includes receiving a first signal at a first signal port; receiving a second signal at a second signal port; electrically coupling the first signal port to the second signal port via a first resistor; propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer; propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer; combining the first and second signals at the first intermediate node to generate a third signal; and propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor.
- [0010] Another aspect of the disclosure relates to an apparatus. The apparatus includes means for receiving a first signal at a first signal port; means for receiving a second signal at a second signal port; means for electrically coupling the first signal port to the second signal

port via a first resistor; means for propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer; means for propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer; means for combining the first and second signals at the first intermediate node to generate a third signal; and means for propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor.

[0011] Another aspect of the disclosure relates to a wireless communication device. The wireless communication device includes at least one antenna; a set of transceiver chains coupled to the at least one antenna; and a signal power splitter or combiner coupled to the set of transceiver chains, wherein the signal power splitter or combiner includes: a first signal port; a first resistor; a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node; a second impedance transformer coupled between the first intermediate node and a second signal port; a third impedance transformer coupled between the first intermediate node and a third signal port; and a second resistor coupled between the second and third signal ports.

[0012] To the accomplishment of the foregoing and related ends, the one or more implementations include the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative aspects of the one or more implementations. These aspects are indicative, however, of but a few of the various ways in which the principles of various implementations may be employed and the description implementations are intended to include all such aspects and their equivalents.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1A illustrates a schematic diagram of an example signal power splitter in accordance with an aspect of the disclosure.

[0014] FIG. 1B illustrates a schematic diagram of an example signal power combiner in accordance with another aspect of the disclosure.

[0015] FIGs. 2A-2C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner of FIG. 1A or 1B in accordance with another aspect of the disclosure.

[0016] FIG. 3 illustrates a schematic diagram of another example signal power splitter/combiner in accordance with another aspect of the disclosure.

- [0017] FIG. 4 illustrates a schematic diagram of another example signal power splitter/combiner in accordance with another aspect of the disclosure.
- [0018] FIGs. 5A-5C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner of FIG. 3 or 4 in accordance with another aspect of the disclosure.
- [0019] FIG. 6 illustrates a schematic diagram of another example signal power splitter/combiner in accordance with another aspect of the disclosure.
- [0020] FIG. 7 illustrates a schematic diagram of another example signal power splitter/combiner in accordance with another aspect of the disclosure.
- [0021] FIG. 8 illustrates an example Smith chart of an impedance at a signal port of the signal power splitter/combiner of FIG. 3 or 4 in accordance with another aspect of the disclosure.
- [0022] FIG. 9 illustrates an example Smith chart of an impedance at a signal port of the signal power splitter/combiner of FIG. 6 or 7 in accordance with another aspect of the disclosure.
- [0023] FIGs. 10A-10C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner of FIG. 6 or 7 in accordance with another aspect of the disclosure.
- [0024] FIG. 11 illustrates a layout diagram of an example signal power splitter/combiner in accordance with another aspect of the disclosure.
- [0025] FIG. 12 illustrates a flow diagram of an example method of power splitting a signal in accordance with another aspect of the disclosure.
- [0026] FIG. 13 illustrates a flow diagram of an example method of power combining signals in accordance with another aspect of the disclosure.
- [0027] FIG. 14 illustrates a block diagram of an example wireless communication device in accordance with another aspect of the disclosure.
- [0028] FIG. 15 illustrates a block diagram of another example signal power splitter/combiner in accordance with another aspect of the disclosure.

DETAILED DESCRIPTION

- [0029] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some

instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts.

[0030] FIG. 1A illustrates a schematic diagram of an example signal power splitter 100 in accordance with an aspect of the disclosure. The signal power splitter 100 is configured to receive an input signal P_{in} , and power split the input signal P_{in} to generate first and second output signals P_{out1} and P_{out2} . In this example, the power splitting is equal or balanced, i.e., meaning that the power level of the first output signal P_{out1} is substantially the same as the power level of the second output signal P_{out2} . Assuming there is no insertion loss between the input and outputs of the signal power splitter 100, the signal power of each of the first and second output signals P_{out1} and P_{out2} is substantially three (3) decibels (dB) lower than the signal power of the input signal P_{in} .

[0031] The signal power splitter 100 includes an input signal port 110, a first transmission line 112 coupled between the input signal port 110 and a first output signal port 116, a second transmission line 114 coupled between the input signal port 110 and a second output signal port 118, and a resistor R coupled between the first and second output signal ports 116 and 118. As discussed, an input signal P_{in} is received at the input signal port 110, and the first and second output signals P_{out1} and P_{out2} are produced at the first and second output ports 116 and 118, respectively.

[0032] If the input signal port 110 and output signal ports 116 and 118 have a particular characteristic impedance Z_0 at a particular wavelength λ or frequency, the transmission lines 112 and 114 each have substantially the same impedance of Z_1 , which may be set to substantially $\sqrt{2} \cdot Z_0$. Additionally, the transmission lines 112 and 114 each have substantially the same length L_1 , which may be set to substantially a quarter wavelength ($\lambda/4$) at a particular frequency. Further, the resistance of the resistor R may be set to substantially $2 \cdot Z_0$.

[0033] The transmission lines 112 and 114 may be implemented as a microstrip, stripline, coplanar microstrip, suspended microstrip, or other, where the transmission lines 112 and 114 are each implemented as a metallization strips disposed on a dielectric or semiconductor substrate. The resistor R may also be implemented as suitably dimensioned thin film material, such as titanium nitride (TiN), disposed on the dielectric or semiconductor substrate.

[0034] FIG. 1B illustrates a schematic diagram of an example signal power combiner 150 in accordance with another aspect of the disclosure. The signal power splitter 100 previously discussed has a reciprocity property. That is, the signal power splitter 100

may be configured as a signal power combiner by receiving respective input signals at the ports 116 and 118, and generating a combined signal at port 110. The signal power combiner 150 is an example of the signal power splitter 100 being used as a power combiner. Because of its reciprocity property, the signal power splitter 100 and combiner 150 are generally referred to herein as a signal power splitter/combiner.

- [0035]** The signal power combiner 150 is configured to receive first and second input signals P_{in1} and P_{in2} , and power combine the input signals P_{in1} and P_{in2} to generate an output signal P_{out} . In this example, the power combining is equal or balanced, i.e., meaning that the power level of the output signal P_{out} is substantially the sum of the power levels of the input signals P_{in1} and P_{in2} . Assuming there is no insertion loss between the inputs and output of the signal power combiner 150, and the input signals P_{in1} and P_{in2} have substantially the same power, the power of the output signal P_{out} is substantially 3dB higher than the signal power of each of the input signals P_{in1} and P_{in2} .
- [0036]** The signal power combiner 150 includes a first input signal port 162, a second input signal port 164, a resistor R coupled between the first and second input signal ports 162 and 164, a first transmission line 166 coupled between the first input signal port 162 and an output signal port 170, and a second transmission line 168 coupled between the second input signal port 164 and the output signal port 170. As discussed, first and second input signal P_{in1} and P_{in2} are received at the first and second input signal port 162 and 164, respectively, and the output signal P_{out} is produced at the output signal port 170.
- [0037]** If the input signal ports 162 and 164 and output signal port 170 each have a particular characteristic impedance Z_0 at a particular wavelength λ or frequency, the transmission lines 166 and 168 each have substantially the same impedance of Z_1 , which may be set to substantially $\sqrt{2} \cdot Z_0$. Additionally, the transmission lines 166 and 168 each have substantially the same length L_1 , which may be set to substantially quarter wavelength ($\lambda/4$) at a particular frequency. Further, the resistance of the resistor R may be set to substantially $2 \cdot Z_0$.
- [0038]** Similarly, the transmission lines 166 and 168 may be implemented as a microstrip, stripline, coplanar microstrip, suspended microstrip, or other, where the transmission lines 166 and 168 are each implemented as a metallization strip disposed on a dielectric or semiconductor substrate. The resistor R may also be implemented as a suitably dimensioned thin film material, such as titanium nitride (TiN), disposed on the dielectric or semiconductor substrate.

- [0039] FIGs. 2A-2C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner 100/150 in accordance with another aspect of the disclosure. In each of the graphs, the x- or horizontal-axis represents frequency from 0 Hertz at the left end to 20 giga Hertz (GHz) at the right end. The y- or vertical-axis of the graph depicted in FIG. 2A represents insertion loss in dB between port 110/170 and port 116/162 (or port 110/170 and port 118/164) from -2dB at the top to -14dB at the bottom. The y- or vertical-axis of the graph depicted in FIG. 2B represents isolation in dB between the ports 116/162 and 118/164 from 0dB at the top to -30dB at the bottom. The y- or vertical-axis of the graph depicted in FIG. 2C represents the return loss dB at port 110/170 from 0dB at the top to -30dB at the bottom.
- [0040] With specific reference to FIG. 2A, the graph includes a shaded region indicating an example specification for the insertion loss for a particular application. In particular, the specification indicates an insertion loss of -5dB or less between frequencies 0 to 15GHz, but ideally should be -3dB across the whole frequency band. Additionally, as discussed, the graph also shows the insertion loss in dB between port 110/170 and port 116/162 (or port 110/170 and port 118/164). Note that the insertion loss varies between -3dB and -4dB between frequencies 0 to 15GHz, which meets the example specification for insertion loss.
- [0041] With specific reference to FIG. 2B, the graph includes a shaded region indicating an example specification for the isolation between ports 116/162 and 118/164 for a particular application. In particular, the specification indicates an isolation of -15dB or more between frequencies 7 to 15GHz. Additionally, as discussed, the graph also shows the isolation between ports 116/162 and 118/164. Note that the isolation varies between -13dB and -29dB within frequency band 7 to 15GHz. Thus, in the lower part of the frequency band 7 to 15GHz (e.g., between 7-8GHz), the isolation between ports 116/162 and 118/164 fails to meet the specification. This is because the length L_1 of the transmission lines 112/166 and 114/168 are each set for a particular frequency such as, in this example, 13GHz, where the isolation peaks at -29dB. The isolation decreases for frequencies farther away from the particular frequency where, in this example, the isolation does not meet specification below 8.2 GHz.
- [0042] With specific reference to FIG. 2C, the graph includes shaded regions indicating an example specification for the return loss at port 110/170 for a particular application. In particular, the specification indicates a return loss of -15dB or less within a lower frequency band 0 to 1GHz and within a higher frequency band 7-15GHz. Additionally,

as discussed, the graph also shows the return loss at such port 110/170. Note that the return loss varies between -12dB and -27dB within the higher frequency band 7 to 15GHz. Thus, especially in the lower part of the higher frequency band 7 to 15GHz (e.g., between 7-9GHz), the return loss fails to meet specification. Additionally, for the entire lower frequency band 0 to 1GHz, the return loss is greater than -5dB, which significantly fails to meet specification. Again, this is because the length L_1 of the transmission lines 112/166 and 114/168 are each set for a particular frequency such as, in this example, 13GHz, where the return loss is best at -29dB. The return loss increases for frequencies farther away from the particular frequency where, in this example, the return loss does not meet specification below 9GHz for the higher frequency band, and does not meet specification for the entire lower frequency band.

[0043] FIG. 3 illustrates a schematic diagram of another example signal power splitter/combiner 300 in accordance with another aspect of the disclosure. An approach to improve the bandwidth over which a signal power splitter/combiner may be able to meet specification in terms of insertion loss, isolation, and return loss is to add more stages to the signal power splitter/combiner. The power splitter/combiner 300 is an example of a multi-stage signal power splitter/combiner.

[0044] In particular, the signal power splitter/combiner 300 includes a first signal port P_1 , a first transmission line 312 coupled between the first signal port P_1 and a first intermediate node n_1 , a second transmission line 314 coupled between the first signal port P_1 and a second intermediate node n_2 , and a first resistor R_1 coupled between the first and second intermediate nodes n_1 and n_2 . The signal power splitter/combiner 300 further includes a third transmission line 316 coupled between the first intermediate node n_1 and a second signal port P_2 , a fourth transmission line 318 coupled between the second intermediate node n_2 and a third signal port P_3 , and a second resistor R_2 coupled between the second and third signal ports P_2 and P_3 .

[0045] If the signal power splitter/combiner 300 is used as a power splitter, the signal power splitter/combiner 300 receives an input signal P_{in} at port P_1 , and generates output signals P_{out1} and P_{out2} at ports P_2 and P_3 , respectively. If the signal power splitter/combiner 300 is used as a power combiner, the signal power splitter/combiner 300 receives input signals P_{in1} and P_{in2} at ports P_2 and P_3 , respectively, and generates an output signal P_{out} at port P_1 .

[0046] If the ports P_1 , P_2 , and P_3 each has a characteristic impedance Z_0 at a particular wavelength λ or frequency, the first and second transmission lines 312 and 314 may each have substantially the same impedance Z_1 (e.g., $Z_1=1.32 \cdot Z_0$) and substantially the same

length L_1 (e.g., $\lambda/4$ at a particular frequency (e.g., 13GHz)). Further, the resistance of the first resistor R1 may be set to substantially $1.87 \cdot Z_0$. Additionally, the third and fourth transmission lines 316 and 318 may each have substantially the same impedance of Z_2 (e.g., $Z_2=1.13 \cdot Z_0$) and substantially the same length L_2 (e.g., $\lambda/4$ at the particular frequency (e.g., 13GHz)). Further, the resistance of the second resistor R2 may be set to substantially $3.11 \cdot Z_0$.

[0047] The transmission lines 312, 314, 316, and 318 may be implemented as a microstrip, stripline, coplanar microstrip, suspended microstrip, or other, where the transmission lines 312, 314, 316, and 318 are each implemented as a metallization strip disposed on a dielectric or semiconductor substrate. The resistors R1 and R2 may also be implemented as suitably dimensioned thin film material, such as titanium nitride (TiN), disposed on the dielectric or semiconductor substrate.

[0048] FIG. 4 illustrates a schematic diagram of another example signal power splitter/combiner 400 in accordance with another aspect of the disclosure. The signal power splitter/combiner 400 may be an alternative implementation of signal power splitter/combiner 300 previously discussed. That is, the transmission lines 312, 314, 316, and 318 of signal power splitter/combiner 300 each operate as an impedance transformer. However, another circuit to implement an equivalent impedance transformer uses discrete devices, such as a pi-network including shunt capacitors coupled to opposite ends of a series inductor, respectively. By using discrete components instead of transmission lines, the signal power splitter/combiner 400 may be made smaller or more compact compared to signal power splitter/combiner 300.

[0049] The signal power splitter/combiner 400 includes a first signal port P_1 , a first impedance transformer 420, a second impedance transformer 430, a first resistor R1, a third impedance transformer 440, a fourth impedance transformer 450, a second resistor R2, a second signal port P_2 , and a third signal port P_3 . The first impedance transformer 420 is coupled between the first signal port P_1 and a first intermediate node n_1 . The first impedance transformer 420 includes a first shunt capacitor C_{1A} coupled between the first signal port P_1 and a lower voltage rail (e.g., ground), a series inductor L_{1A} coupled between the first signal port P_1 and the first intermediate node n_1 , and a second shunt capacitor C_{1B} coupled between the first intermediate node n_1 and the lower voltage rail (e.g., ground).

[0050] The second impedance transformer 430 is coupled between the first signal port P_1 and a second intermediate node n_2 . The second impedance transformer 430 includes a first

shunt capacitor C_{1C} coupled between the first signal port P_1 and the lower voltage rail (e.g., ground), a series inductor L_{1B} coupled between the first signal port P_1 and the second intermediate node n_2 , and a second shunt capacitor C_{1D} coupled between the second intermediate node n_2 and the lower voltage rail (e.g., ground). The first resistor R_1 is coupled between the first and second intermediate nodes n_1 and n_2 .

[0051] The third impedance transformer 440 is coupled between the first intermediate node n_1 and the second signal port P_2 . The third impedance transformer 440 includes a first shunt capacitor C_{2A} coupled between the first intermediate node n_1 and the lower voltage rail (e.g., ground), a series inductor L_{2A} coupled between the first intermediate node n_1 and the second signal port P_2 , and a second shunt capacitor C_{2B} coupled between the second signal port P_2 and the lower voltage rail (e.g., ground).

[0052] The fourth impedance transformer 450 is coupled between the second intermediate node n_2 and the third signal port P_3 . The fourth impedance transformer 450 includes a first shunt capacitor C_{2C} coupled between the second intermediate node n_2 and the lower voltage rail (e.g., ground), a series inductor L_{2B} coupled between the second intermediate node n_2 and the third signal port P_3 , and a second shunt capacitor C_{2D} coupled between the third signal port P_3 and the lower voltage rail (e.g., ground).

[0053] If the signal power splitter/combiner 400 is used as a power splitter, the signal power splitter/combiner 400 receives an input signal P_{in} at port P_1 , and generates output signals P_{out1} and P_{out2} at ports P_2 and P_3 , respectively. If the signal power splitter/combiner 400 is used as a power combiner, the signal power splitter/combiner 400 receives input signals P_{in1} and P_{in2} at ports P_2 and P_3 , respectively, and generates an output signal P_{out} at port P_1 .

[0054] If the ports P_1 , P_2 , and P_3 each have a characteristic impedance Z_0 at a particular wavelength λ or frequency, the first and second impedance transformers 420 and 430 may be configured to perform substantially the same impedance transformation as the first and second transmission lines 312 and 314, respectively. This may be accomplished by setting the capacitance and inductance of capacitors C_{1A} , C_{1B} , C_{1C} , and C_{1D} and inductors L_{1A} and L_{1B} , respectively. For example, the capacitance of the capacitors C_{1A} , C_{1B} , C_{1C} , and C_{1D} may be substantially the same, and the inductance of the inductors L_{1A} and L_{1B} may be substantially the same.

[0055] Similarly, the third and fourth impedance transformers 440 and 450 may be configured to perform substantially the same impedance transformation as the third and fourth transmission lines 316 and 318, respectively. This may be accomplished by setting the capacitance and inductance of capacitors C_{2A} , C_{2B} , C_{2C} , and C_{2D} and inductors L_{2A} and

L_{2B} , respectively. For example, the capacitance of the capacitors C_{2A} , C_{2B} , C_{2C} , and C_{2D} may be substantially the same, and the inductance of the inductors L_{2A} and L_{2B} may be substantially the same.

[0056] The resistors R1 and R2 of signal power splitter/combiner 400 may be implemented to have substantially the same resistances as resistors R1 and R2 of power splitter/combiner 300, respectively.

[0057] FIGs. 5A-5C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner 300 or 400 in accordance with another aspect of the disclosure. The dimensions, units, and scales of the graphs are the same as those depicted in FIGs. 2A-2C, previously discussed. The graphs also depict the same specification shaded regions for the insertion loss, isolation, and return loss, respectively.

[0058] With regard to insertion loss as depicted in FIG. 5A, the graph shows that the insertion loss in dB between port P_1 and port P_2 (or P_1 and P_3) is still within -3dB and -4dB between frequencies 0 to 15GHz, which meets the example specification for insertion loss. However, due to the power splitter/combiner 300 or 400 having two-stages compared to one-stage in power splitter/combiner 100 or 150, the power splitter/combiner 300 or 400 has a roll-off at a higher frequency compared to the roll-off associated with power splitter/combiner 100 or 150. For example, in the one-stage power splitter/combiner 100 or 150, the roll-off begins around 14GHz, whereas in the two-stage power splitter/combiner 300 or 400, the roll-off begins at 15GHz.

[0059] With regard to isolation as depicted in FIG. 5B, the graph shows the isolation between ports P_2 and P_3 is greater than -17dB between frequencies 7 to 15GHz, which meets the specification. Thus, due to the two-stages of power splitter/combiner 300 or 400, the bandwidth or frequency range for which the isolation meets specification is widened because the two-stages introduce another isolation peak within the frequency range of interest (e.g., 7-15GHz). For example, the isolation has peaks at 9.5GHz and 14GHz.

[0060] With regard to return loss as depicted in FIG. 5C, the graph shows that the return loss is wider within the upper frequency range of interest (7-15GHz). However, even within this frequency band, the return loss does not meet specification for frequencies between 7-9.5GHz. With regard to the lower frequency range of interest (e.g., 0-1GHz), the return loss does not meet specification. Thus, a two-stage signal power splitter/combiner 300 or 400 may be able to improve the return loss within the upper frequency band by frequency widening the return loss therein. However, the signal power splitter/combiner

300 or 400 still falls short of meeting specification for a portion of the upper frequency band and the entire lower frequency band.

[0061] FIG. 6 illustrates a schematic diagram of another example signal power splitter/combiner 600 in accordance with another aspect of the disclosure. In summary, to improve the return loss specification within the lower frequency band (e.g., 0-1GHz) and the lower portion of the upper frequency band (e.g., 7-15GHz), the signal power splitter/combiner 600 includes a loading resistor R0 and an additional impedance transformer 610 coupled in series between a signal port P₁ and first and second impedance transformers 612 and 614. As discussed in more detail herein, the loading resistor R0 improves the return loss within the lower frequency band so that it meets specification within that frequency band. The additional impedance transformer 610 improves the return loss within the lower portion of the upper frequency band so that the return loss across the upper frequency band meets specification.

[0062] In particular, the signal power splitter/combiner 600 includes a first signal port P₁, a loading resistor R0, a series transmission line 610, first and second parallel transmission lines 612 and 614, a first resistor R1, third and fourth parallel transmission lines 616 and 618, a second resistor R2, and second and third signal ports P₂ and P₃. The loading resistor R0 and the series transmission line 610 are coupled in series between the first signal port P₁ and a first intermediate node n1. The first parallel transmission line 612 is coupled between the first intermediate node n1 and a second intermediate node n2. The second parallel transmission line 614 is coupled between the first intermediate node n1 and a third intermediate node n3. The first resistor R1 is coupled between the second and third intermediate nodes n2 and n3. The third parallel transmission line 616 is coupled between the second intermediate node n2 and the second signal port P₂. The fourth parallel transmission line 618 is coupled between the third intermediate node n3 and the third signal port P₃. The second resistor R2 is coupled between the second and third signal ports P₂ and P₃.

[0063] Similarly, if the signal power splitter/combiner 600 is used as a power splitter, the signal power splitter/combiner 600 receives an input signal P_{in} at port P₁, and generates output signals P_{out1} and P_{out2} at ports P₂ and P₃, respectively. If the signal power splitter/combiner 600 is used as a power combiner, the signal power splitter/combiner 600 receives input signals P_{in1} and P_{in2} at ports P₂ and P₃, respectively, and generates an output signal P_{out} at port P₁. The resistances of the resistors R0, R1, and R2, the impedances Z₀, Z₁, and Z₂ and lengths L₁, L₂, and L₃ of the transmission lines 610, 612/614, and 616/618 may be

optimized so that the insertion loss, isolation, and return loss across one or more frequency bands of interests meet specification, such as those described with reference to FIGs. 2A-2C.

- [0064] Similarly, the transmission lines 610, 612, 614, 616, and 618 may be implemented as a microstrip, stripline, coplanar microstrip, suspended microstrip, or other, where the transmission lines 610, 612, 614, 616, and 618 are each implemented as a metallization strip disposed on a dielectric or semiconductor substrate. The resistors R0, R1 and R2 may also be implemented as suitably dimensioned thin film material, such as titanium nitride (TiN), disposed on the dielectric or semiconductor substrate.
- [0065] FIG. 7 illustrates a schematic diagram of another example signal power splitter/combiner 700 in accordance with another aspect of the disclosure. The signal power splitter/combiner 700 may be an alternative discrete component implementation of signal power splitter/combiner 600 previously discussed.
- [0066] The signal power splitter/combiner 700 includes a signal port P_1 , a loading resistor R0, a series impedance transformer 710, a first parallel impedance transformer 720, a second parallel impedance transformer 730, a first resistor R1, a third parallel impedance transformer 740, a fourth parallel impedance transformer 750, a second resistor R2, a second signal port P_2 , and a third signal port P_3 . The loading resistor R0 and the series impedance transformer 710 are coupled in series between the first port P_1 and a first intermediate node n1. The series impedance transformer 710 includes a first shunt capacitor C_{0A} coupled between the first port P_1 and a lower voltage rail (e.g., ground), a series inductor L_{0A} coupled between the first port P_1 and the first intermediate node n1, and a second shunt capacitor C_{0B} coupled between the first intermediate node n1 and the lower voltage rail (e.g., ground).
- [0067] The first parallel impedance transformer 720 is coupled between the first intermediate node n1 and a second intermediate node n2. The first parallel impedance transformer 720 includes a first shunt capacitor C_{1A} coupled between the first intermediate node n1 and the lower voltage rail (e.g., ground), a series inductor L_{1A} coupled between the first intermediate node n1 and the second intermediate node n2, and a second shunt capacitor C_{1B} coupled between the second intermediate node n2 and the lower voltage rail (e.g., ground).
- [0068] The second parallel impedance transformer 730 is coupled between the first intermediate node n1 and a third intermediate node n3. The second parallel impedance transformer 730 includes a first shunt capacitor C_{1C} coupled between the first intermediate node n1

and the lower voltage rail (e.g., ground), a series inductor L_{1B} coupled between the first intermediate node $n1$ and the third intermediate node $n3$, and a second shunt capacitor C_{1D} coupled between the third intermediate node $n3$ and the lower voltage rail (e.g., ground). The first resistor $R1$ is coupled between the second and third intermediate nodes $n2$ and $n3$.

- [0069]** The third parallel impedance transformer 740 is coupled between the second intermediate node $n2$ and the second port P_2 . The third parallel impedance transformer 740 includes a first shunt capacitor C_{2A} coupled between the second intermediate node $n2$ and the lower voltage rail (e.g., ground), a series inductor L_{2A} coupled between the second intermediate node $n2$ and the second port P_2 , and a second shunt capacitor C_{2B} coupled between the second port P_2 and the lower voltage rail (e.g., ground).
- [0070]** The fourth parallel impedance transformer 750 is coupled between the third intermediate node $n3$ and the third port P_3 . The fourth impedance transformer 750 includes a first shunt capacitor C_{2C} coupled between the third intermediate node $n3$ and the lower voltage rail (e.g., ground), a series inductor L_{2B} coupled between the third intermediate node $n3$ and the third port P_3 , and a second shunt capacitor C_{2D} coupled between the third port P_3 and the lower voltage rail (e.g., ground).
- [0071]** If the signal power splitter/combiner 700 is used as a power splitter, the signal power splitter/combiner 700 receives an input signal P_{in} at port P_1 , and generates output signals P_{out1} and P_{out2} at the ports P_2 and P_3 , respectively. If the signal power splitter/combiner 700 is used as a power combiner, the signal power splitter/combiner 700 receives input signals P_{in1} and P_{in2} at ports P_2 and P_3 , respectively, and generates an output signal P_{out} at the port P_1 .
- [0072]** If the ports P_1 , P_2 , and P_3 each have a characteristic impedance Z_0 at a particular wavelength λ or frequency, the loading resistor $R0$ and the series impedance transformer 710 may be configured to improve the return loss (and/or other characteristic(s)) of the signal power splitter/combiner 700 at one or more desired frequency bands, such as the lower frequency band (e.g., 0-1GHz) and a portion of an upper frequency band (e.g., 7-15GHz) previously discussed. This may be accomplished by setting the resistance of the loading resistor $R0$, and the capacitance and inductance of capacitors C_{0A} and C_{0B} and inductor L_{0A} of the series impedance transformer 710, respectively.
- [0073]** Similar to signal power splitter/combiner 600, the first and second parallel impedance transformers 720 and 730 may be configured to perform substantially the same impedance transformation as the first and second parallel transmission lines 612 and 614,

respectively. This may be accomplished by setting the capacitance and inductance of capacitors C_{1A} , C_{1B} , C_{1C} , and C_{1D} and inductors L_{1A} and L_{1B} , respectively. Similarly, the third and fourth parallel impedance transformers 740 and 750 may be configured to perform substantially the same impedance transformation as the third and fourth parallel transmission lines 616 and 618, respectively. This may be accomplished by setting the capacitance and inductance of capacitors C_{2A} , C_{2B} , C_{2C} , and C_{2D} and inductors L_{2A} and L_{2B} , respectively. The resistors R1 and R2 of power splitter/combiner 700 may be implemented to have substantially the same resistances as resistors R1 and R2 of power splitter/combiner 600, respectively.

[0074] FIG. 8 illustrates an example Smith chart of an impedance at a port of the signal power splitter/combiner 300 or 400 in accordance with another aspect of the disclosure. At low frequencies, such as within the lower frequency band (e.g., 0-1GHz), the impedance transformers 312, 314, 316, and 318 or 420, 430, 440, and 450 do not substantially affect the low frequency signal. This is because at low frequencies the transmission lines 312, 314, 316, and 318 essentially function as shorts. Similarly, at low frequencies, the capacitors of impedance transformers 420, 430, 440, and 450 essentially function as opens, and the inductors essentially function as shorts.

[0075] Thus, from the viewpoint of port P_1 , the impedance of the signal power splitter/combiner 300 or 400 is essentially R1 in parallel with R2. If, for example, R1 is $1.87 \cdot Z_0$ and R2 is $3.11 \cdot Z_0$, then the impedance presented to port P_1 by the power splitter/combiner 300 is $0.7 \cdot Z_0$, considering also Z_0 being present at ports P_2 and P_3 . Thus, as indicated in the Smith Chart, the impedance at such low frequencies is substantially resistive with a resistance less than Z_0 , as represented by the encircled number "1" on the Smith chart. This is the cause of the poor return loss at low frequencies. The region indicated within the square labeled number "2" is the impedance presented to port P_1 by the power splitter/combiner 300 at higher frequencies, such as the upper frequency band (e.g., 7-15GHz), where the return loss is better but may not meet the specification for the entire upper frequency band, as previously discussed.

[0076] FIG. 9 illustrates an example Smith chart of an impedance at a port of the signal power splitter/combiner 600 or 700 in accordance with another aspect of the disclosure. The addition of the loading resistor R0 in the power splitter/combiner 600 or 700 has the effect of increasing the resistance presented to port P_1 by the power splitter/combiner 600 or 700. Thus, the region indicated by the encircled number "3", representing the low frequency impedance, is closer to Z_0 than the encircled number "1" region of the Smith

chart associated with power splitter/combiner 300 or 400. Thus, the addition of the series loading resistor R0 improves the impedance matching or the return loss within the lower frequency band.

[0077] The addition of the series loading resistor R0 not only improves the impedance matching or return loss at lower frequencies, but may adversely affect the impedance matching within the upper frequency band. Thus, to compensate for any adverse effect to the impedance matching or return loss within the upper frequency band by the addition of the loading resistor R0, the series impedance transformer 610 or 710 improves the impedance matching or return loss within the upper frequency band. The Smith chart illustrates this with the square region labeled number "4" being compressed around Z_0 compared to the region "2" of the Smith chart pertaining to the power splitter/combiner 300 or 400. Thus, the addition of the series impedance transformer 610 or 710 improves the impedance matching or the return loss within the upper frequency band.

[0078] FIGs. 10A-10C illustrate graphs of example specifications and responses associated with the signal power splitter/combiner 600 or 700 in accordance with another aspect of the disclosure. The dimensions, units, and scales of the graphs are the same as those depicted in FIGs. 2A-2C, previously discussed. The graphs also depict the same specification shaded regions for the insertion loss, isolation, and return loss, respectively.

[0079] With regard to insertion loss as depicted in FIG. 10A, the graph shows that the insertion loss in dB between port P₁ and port P₂ (or P₁ and P₃) is about 1dB greater than the corresponding insertion loss of power splitter/combiner 300 or 400, but still less than the -5dB specification between frequencies 0 to 15GHz. Thus, the addition of the loading resistor R0 and the series impedance transformer 610 or 710 has minor effects on the insertion loss.

[0080] With regard to isolation as depicted in FIG. 10B, the graph shows that the isolation between ports P₂ and P₃ is greater than -15dB between frequencies 7 to 15GHz, which meets the specification. Thus, the addition of the loading resistor R0 and the series impedance transformer 610 or 710 to the two-stage signal power splitter/combiner 300 or 400 does not significantly impact the isolation within the upper frequency band (e.g., 7-15GHz).

[0081] With regard to return loss as depicted in FIG. 10C, the graph shows that the addition of the loading resistor R0 and the series impedance transformer 610 or 710 significantly improves the impedance match or return loss within the lower and the upper frequency

bands (e.g., 0-1GHz and 7-15GHz). Thus, the return loss within both bands meets the specification of less than -15dB.

[0082] FIG. 11 illustrates a layout diagram of an example signal power splitter/combiner 1100 in accordance with another aspect of the disclosure. The signal power splitter/combiner 1100 is an example layout implementation of the signal power splitter/combiner 700.

[0083] The signal power splitter/combiner 1100 includes a signal port P_1 , a loading resistor 1110, and a series impedance transformer including first and second shunt capacitors 1112 and series inductor 1114. The signal power splitter/combiner 1100 further includes a first parallel impedance transformer including shunt capacitors 1116 and 1124 and series inductor 1118. Note that the shunt capacitor 1116 is shared among the series impedance transformer and the first parallel impedance transformer. Similarly, the signal power splitter/combiner 1100 further includes a second parallel impedance transformer including shunt capacitors 1116 and 1126 and series inductor 1120. Also note that the shunt capacitor 1116 is shared among the series impedance transformer and the second parallel impedance transformer.

[0084] The signal power splitter/combiner 1100 further includes a third parallel impedance transformer including shunt capacitors 1124 and 1136, and series inductor 1130. Note that the shunt capacitor 1124 is shared among the first and third parallel impedance transformers. Additionally, the signal power splitter/combiner 1100 further includes a fourth parallel impedance transformer including shunt capacitors 1126 and 1138, and series inductor 1132. Note that the shunt capacitor 1126 is shared among the second and fourth parallel impedance transformers. The signal power splitter/combiner 1100 further includes first and second resistors 1128 and 1134, and second and third signal ports P_2 and P_3 .

[0085] The loading resistor 1110 and the series impedance transformer 1112/1114/1116 is coupled in series between the first port P_1 and a first intermediate node $n1$. The first parallel impedance transformer 1116/1118/1124 is coupled between the first intermediate node $n1$ and a second intermediate node $n2$. The second parallel impedance transformer 1116/1120/1126 is coupled between the first intermediate node $n1$ and a third intermediate node $n3$. The first resistor 1128 is coupled between the second and third intermediate nodes $n2$ and $n3$.

[0086] The third parallel impedance transformer 1124/1130/1136 is coupled between the second intermediate node $n2$ and the second port P_2 . The fourth parallel impedance transformer

1126/1132/1138 is coupled between the third intermediate node n_3 and the third port P_3 .

The second resistor 1134 is coupled between the second and third ports P_2 and P_3 .

[0087] As previously mentioned, the resistors 1110, 1128, and 1134 may be implemented as properly dimensioned sheets of resistive material, such as TiN. The capacitors 1112, 1116, 1124, 1126, 1136, and 1138 may be implemented as metal-insulator-metal (MIM) capacitors. The inductors 1114, 1118, 1120, 1130, and 1132 may be implemented as metallization coiled strip formed on one or more metallization layers.

[0088] If the signal power splitter/combiner 1100 is used as a power splitter, the signal power splitter/combiner 1100 receives an input signal P_{in} at port P_1 , and generates output signals P_{out1} and P_{out2} at the ports P_2 and P_3 , respectively. If the signal power splitter/combiner 1100 is used as a power combiner, the signal power splitter/combiner 1100 receives input signals P_{in1} and P_{in2} at ports P_2 and P_3 , respectively, and generates an output signal P_{out} at the port P_1 .

[0089] FIG. 12 illustrates a flow diagram of an example method 1200 of power splitting a signal in accordance with another aspect of the disclosure. The method 1200 includes receiving a first signal at a first signal port (block 1210). Examples of means for receiving a first signal at a first signal port include any of the signal ports P_1 , P_{11} , P_{21A} , and P_{21B} described herein.

[0090] The method 1200 further includes propagating the first signal through a first resistor and a first impedance transformer to generate a second signal at a first intermediate node (block 1220). Examples of means for propagating the first signal through a first resistor and a first transformer to generate a second signal at a first intermediate node include any of the loading resistors R_0 and 1110 and series impedance transformers 610, 710, and 1112/1114/1116 described herein.

[0091] The method 1200 also includes splitting the second signal at the first intermediate node to generate third and fourth signals (block 1230). Examples of means for splitting the second signal at the first intermediate node to generate third and fourth signals include any of the intermediate nodes n_1 described herein.

[0092] The method 1200 additionally includes propagating the third signal through a second impedance transformer towards a second signal port (block 1240). Examples of means for propagating the third signal through a second impedance transformer towards a second signal port include any of the impedance transformers 612, 720, and 1116/1118/1124 described herein.

- [0093] Further, the method 1200 includes propagating the fourth signal through a third impedance transformer towards a third signal port (block 1250). Examples of means for propagating the fourth signal through a third impedance transformer towards a third signal port include any of the impedance transformers 614, 730, and 1116/1120/1126 described herein.
- [0094] Also, the method 1200 includes electrically coupling the second signal port to the third signal port via a second resistor (block 1260). Examples of means for electrically coupling the second signal port to the third signal port via a second resistor include the coupling of the second resistor R2 or 1134 between the second and third ports P₂ and P₃.
- [0095] The method 1200 may further include propagating the third signal through a fourth impedance transformer from a second intermediate node to the second signal port, wherein the second impedance transformer is coupled between the first and second intermediate nodes, propagating the fourth signal through a fifth impedance transformer from a third intermediate node to the third signal port, wherein the third impedance transformer is coupled between the first and third intermediate nodes; and electrically coupling the second intermediate node to the third intermediate node via a third resistor.
- [0096] Examples of means for propagating the third signal through a fourth impedance transformer from a second intermediate node to the second signal port include any of the impedance transformers 616, 740, and 1124/1130/1136 described herein. Examples of means for propagating the fourth signal through a fifth impedance transformer from a third intermediate node to the third signal port include any of the impedance transformers 618, 750, and 1126/1132/1138 described herein. Examples of means for electrically coupling the second intermediate node to the third intermediate node via a third resistor include the coupling of the first resistor R1 or 1128 between the second and the third intermediate nodes n₂ and n₃.
- [0097] Additionally, the method 1200 may include splitting the third signal at the second signal port to generate fifth and sixth signals. Examples of means for splitting the third signal at the second signal port to generate fifth and sixth signals include any of the power splitters 1520 and 1530 described herein. In addition, the method 1200 may include splitting a fifth signal at the first signal port to generate the first signal and a sixth signal. Examples of means for splitting a fifth signal at the first signal port to generate the first signal and a sixth signal include any of the power splitters 1520 and 1530 as described herein.

- [0098] FIG. 13 illustrates a flow diagram of an example method 1300 of power combining signals in accordance with another aspect of the disclosure. The method 1300 includes receiving a first signal at a first signal port (block 1310). Examples of means for receiving a first signal at a first signal port include any of the signal ports P_2 described herein. The method 1300 further includes receiving a second signal at a second signal port (block 1320). Examples of means for receiving a second signal at a second signal port include any of the signal ports P_3 described herein.
- [0099] Additionally, the method 1300 includes electrically coupling the first signal port to the second signal port via a first resistor (block 1330). Examples of means for electrically coupling the first signal port to the second signal port via a first resistor include the coupling of the second resistor R_2 or 1134 between the second and third ports P_2 and P_3 described herein.
- [0100] The method 1300 also includes propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer (block 1340). Examples of means for propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer include any of the impedance transformers 612, 720, and 1124/1118/1116 described herein.
- [0101] Further, the method 1300 includes propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer (block 1350). Examples of means for propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer include any of the impedance transformers 614, 730, and 1126/1120/1116 described herein.
- [0102] The method 1300 also includes combining the first and second signals at the first intermediate node to generate a third signal (block 1360). Examples of means for combining the first and second signals at the first intermediate node to generate a third signal include any of the intermediate nodes n_1 described herein.
- [0103] And the method 1300 includes propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor (block 1370). Examples of means for propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor include any of the series impedance transformers 610, 710, and 1116/1114/1112, and loading resistors R_0 and 1110 described herein.
- [0104] The method 1300 may further include propagating the third signal from the second signal port to a second intermediate node via a fourth impedance transformer, wherein the first

impedance transformer is coupled between the first and second intermediate nodes; propagating the fourth signal from the third signal port to a third intermediate node via a fifth impedance transformer, wherein the second impedance transformer is coupled between the first and third intermediate nodes; and electrically coupling the second intermediate node to the third intermediate node via a third resistor.

[0105] Examples of means for propagating the third signal from the second signal port to a second intermediate node via a fourth impedance transformer include any of the impedance transformers 616, 740, and 1136/1130/1124 described herein. Examples of propagating the fourth signal from the third signal port to a third intermediate node via a fifth impedance transformer include any of the impedance transformers 618, 750, and 1138/1132/1126 described herein. And examples of means for electrically coupling the second intermediate node to the third intermediate node via a third resistor include the coupling of the first resistor R1 or 1128 between the second and the third intermediate nodes n2 and n3.

[0106] Additionally, the method 1300 may include combining the third signal with a fourth signal at the third signal port to generate a fifth signal. Means for combining the third signal with a fourth signal at the third signal port to generate a fifth signal include any of the power splitters 1520 and 1530 as described herein. In addition, the method 1300 may include combining fourth and fifth signals at the first signal port to generate the first signal. Examples of means for combining fourth and fifth signals at the first signal port to generate the first signal include any of the power splitters 1520 and 1530 as further described herein.

[0107] FIG. 14 illustrates a block diagram of an example wireless communication device 1400 in accordance with another aspect of the disclosure. The wireless communication device 1400 may be implemented as a smart phone, tablet device, laptop computer, desktop computer, wearable devices (e.g., a smart watch, activity monitoring device, health monitoring device, etc.), Internet of Things (IoT) device, and others.

[0108] The wireless communication device 1400 includes at least one antenna 1410 (e.g., a set of antennas, or one or more phase arrays antennas, etc.), a set of transceiver chains 1420, a signal power combiner 1440, a signal power splitter 1450, and a signal processing circuit 1460. Each of the set of transceiver chains 1420 may include a signal routing circuit 1422 configured to route signals to and from the at least one antenna 1410, a low noise amplifier (LNA) 1424, a phase shifter 1426, a down converting mixer 1428 (which receives a local oscillator (LO) signal), and an intermediate frequency (IF) or baseband (BB) filter 1430.

These devices are collectively configured to convert an RF signal received via the at least one antenna 1410 to a received IF or BB signal.

- [0109]** The signal power combiner 1440 includes inputs coupled to outputs of the set of transceivers chains 1420, respectively. For example, the inputs of the signal power combiner 1140 may be coupled to outputs of the corresponding received IF or BB filters 1430 of the set of transceivers chains 1420, respectively. The inputs of the signal power combiner 1140 are configured to receive IF or BB signals from the set of transceivers chains 1420. Considering the previous examples, one of the set of transceivers chains 1420 may be configured to generate an IF signal within the upper frequency band (e.g., 7-15GHz), and another one of the set of transceivers chains 1420 may be configured to generate an IF signal within the lower frequency band (e.g., 0-1GHz).
- [0110]** The signal power combiner 1440 is configured to combine the received IF or BB signals to generate a combined received IF or BB signal at its output. The signal power combiner 1440 may be implemented per any of the signal power combiners described herein. The output of the signal power combiner 1440 is coupled to an input of the signal processing circuit 1460. The signal processing circuit 1460 is configured to process the combined received IF or BB signal to recover data therefrom.
- [0111]** The signal processing circuit 1460 is configured to generate a combined transmit IF or BB signal including data. The signal processing circuit 1460 includes an output, at which the combined transmit IF or BB signal is generated, coupled to an input of the signal power splitter 1450. The signal power splitter 1450 is configured to power split the combined transmit IF or BB signal to generate a set of transmit IF or BB signals. The signal power splitter 1450 may be implemented per any of the signal power splitters described herein. The signal power splitter 1450 includes a set of outputs, at which the set of transmit IF or BB signals are generated, coupled to inputs of the set of transceivers chains 1420, respectively.
- [0112]** Each of the set of transceiver chains 1420 may further include an up converting mixer 1432 (which receives the LO signal), a radio frequency (RF) filter 1434, a phase shifter 1436, and a set of one or more amplifiers 1438 (e.g., a pre-amplifier, a power amplifier (PA), etc.). These devices are collectively configured to convert a transmit IF or BB signal received from the signal power splitter 1450 to generate a transmit RF signal, which is provided to the at least one antenna 1410 via the signal routing circuit 1422 for wireless transmission. The set of transmit IF or BB signals generated by the signal power splitter

1450 is provided to the corresponding up converting mixers 1432 of the set of transceivers chains 1420, respectively.

- [0113] FIG. 15 illustrates a block diagram of another example signal power splitter/combiner 1500 in accordance with another aspect of the disclosure. The power splitter/combiner 1500 may include a set of hierarchical signal power splitter/combiners, wherein each power splitter/combiner may be configured per any of the signal power splitter/combiner previously discussed.
- [0114] In particular, the signal power splitter/combiner 1500 includes a first hierarchical-level signal power splitter/combiner 1510 including signal ports P_{11} , P_{12} , and P_{13} . The first hierarchical-level signal power splitter/combiner 1510 may be implemented per any of signal power splitter/combiners 600, 700, and 1100 previously discussed, wherein signal ports P_{11} , P_{12} , and P_{13} correspond to signal ports P_1 , P_2 , and P_3 of signal power splitter/combiners 600, 700, and 1100, respectively.
- [0115] The signal power splitter/combiner 1500 includes a first, second hierarchical-level signal power splitter/combiner 1520 including signal ports P_{21A} , P_{22A} , and P_{23A} . The first, second hierarchical-level signal power splitter/combiner 1520 may be implemented per any of signal power splitter/combiners 600, 700, and 1100 previously discussed, wherein signal ports P_{21A} , P_{22A} , and P_{23A} correspond to signal ports P_1 , P_2 , and P_3 of signal power splitter/combiners 600, 700, and 1100, respectively.
- [0116] The signal power splitter/combiner 1500 includes a second, second hierarchical-level signal power splitter/combiner 1530 including signal ports P_{21B} , P_{22B} , and P_{23B} . The second, second hierarchical-level signal power splitter/combiner 1530 may be implemented per any of signal power splitter/combiners 600, 700, and 1100 previously discussed, wherein signal ports P_{21B} , P_{22B} , and P_{23B} correspond to signal ports P_1 , P_2 , and P_3 of signal power splitter/combiners 600, 700, and 1100, respectively.
- [0117] If the signal power splitter/combiner 1500 is used as a power splitter, the signal power splitter 1500 receives an input signal P_{in} at port P_{11} , and the first hierarchical-level splitter 1510 power splits the input signal P_{in} to generate first hierarchical-level output signals P_{out11} and P_{out12} at the ports P_{12} and P_{13} , respectively. The first, second hierarchical-level signal power splitter 1520 receives the first hierarchical-level output signal P_{out11} at port P_{21A} , and power splits the signal P_{out11} to generate second hierarchical-level output signals P_{out21} and P_{out22} at the ports P_{22A} and P_{23B} , respectively. The second, second hierarchical-level signal power splitter 1530 receives the second hierarchical-level output signal P_{out12} at port P_{21B} , and power splits the signal P_{out12} to generate second hierarchical-level output

signals P_{out23} and P_{out24} at the ports P_{22B} and P_{23B} , respectively. It shall be understood that there may be more than two hierarchical levels of signal power splitters.

[0118] If the signal power splitter/combiner 1500 is used as a power combiner, the signal power splitter 1500 receives input signals P_{in1} , P_{in2} , P_{in3} , and P_{in4} at ports P_{22A} , P_{23A} , P_{22B} , and P_{23B} , respectively. The first, second hierarchical-level signal power combiner 1520 power combines the input signals P_{in1} and P_{in2} to generate a first, first hierarchical-level input signal P_{in11} at port P_{21A} . Similarly, the second, second hierarchical-level signal power combiner 1530 power combines the input signals P_{in3} and P_{in4} to generate a second, first hierarchical-level input signal P_{in12} at port P_{21B} . The first hierarchical-level signal power combiner 1510 receives the first hierarchical-level input signals P_{in11} and P_{in12} at ports P_{12} and P_{13} , respectively, and power combines the signals P_{in11} and P_{in12} to generate output signal P_{out} at port P_{11} . It shall be understood that there may be more than two hierarchical levels of signal power combiners.

[0119] The example shown in FIG. 15 is a 1:4 power splitter or 4:1 power combiner. The maximum signal power splitting or combining is 2^n , where n is the number of hierarchical levels. For instance, in this example, $n=2$. Thus, the maximum number of signal splitting or combining is 2^2 or 4. An odd number or an even number other than the maximum 2^n of signal splitting or combining may be achieved by eliminating one or more power splitter/combiners at the highest hierarchical level. For example, a 1:3 power splitter or 3:1 power combiner may be achieved with power splitter/combiner 1500 by eliminating power splitter/combiner 1530. Another example is a three hierarchical level ($n=3$), where the highest hierarchical level has 6 power splitter/combiner instead of the maximum 8.

[0120] The following provides an overview of aspects of the present disclosure:

[0121] Aspect 1: An apparatus, including: a first signal port; a first resistor; a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node; a second impedance transformer coupled between the first intermediate node and a second signal port; a third impedance transformer coupled between the first intermediate node and a third signal port; and a second resistor coupled between the second and third signal ports.

[0122] Aspect 2: The apparatus of aspect 1, wherein the first impedance transformer includes a first transmission line with a first impedance and a first length.

[0123] Aspect 3: The apparatus of aspect 1 or 2, wherein the second impedance transformer includes a second transmission line with a second impedance and a second length.

- [0124] Aspect 4: The apparatus of any one of aspects 1-3, wherein the third impedance transformer includes a third transmission line with a third impedance and a third length.
- [0125] Aspect 5: The apparatus of aspect 4, wherein the second impedance is substantially the same as the third impedance, and wherein the second length is substantially the same as the third length.
- [0126] Aspect 6: The apparatus of any one of aspects 1-5, wherein the first impedance transformer includes a first shunt capacitor, a first series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the first series inductor, respectively.
- [0127] Aspect 7: The apparatus of any one of aspects 1-6, wherein the second impedance transformer includes a third shunt capacitor, a second series inductor, and a fourth shunt capacitor, wherein the third and fourth shunt capacitors are coupled to both ends of the second series inductor, respectively.
- [0128] Aspect 8: The apparatus of any one of aspects 1-7, wherein the third impedance transformer includes a fifth shunt capacitor, a third series inductor, and a sixth shunt capacitor, wherein the fifth and sixth shunt capacitors are coupled to both ends of the third series inductor, respectively.
- [0129] Aspect 9: The apparatus of aspect 9, wherein the third, fourth, fifth, and sixth shunt capacitors have substantially the same capacitance, and wherein the second and third series inductors have substantially the same inductance.
- [0130] Aspect 10: The apparatus of any one of aspects 6-9, wherein the second impedance transformer includes a second series inductor and a third shunt capacitor, wherein the second shunt capacitor is shared among the first and second impedance transformers, and wherein the second and third shunt capacitors are coupled to both ends of the second series inductor, respectively.
- [0131] Aspect 11: The apparatus of aspect 10, wherein the third impedance transformer includes a third series inductor and a fourth shunt capacitor, wherein the second shunt capacitor is shared among the first, second, and third impedance transformers, and wherein the second and fourth shunt capacitors are coupled to both ends of the third series inductor, respectively.
- [0132] Aspect 12: The apparatus of any one of aspects 1-11, further including: a fourth impedance transformer coupled between a second intermediate node and the second signal port, wherein the second impedance transformer is coupled between the first intermediate node and the second intermediate node; a fifth impedance transformer

coupled between a third intermediate node and the third signal port, wherein the third impedance transformer is coupled between the first intermediate node and the third intermediate node; and a third resistor coupled between the second and third intermediate nodes.

- [0133]** Aspect 13: The apparatus of aspect 12, wherein the fourth impedance transformer includes a first transmission line with a first impedance and a first length, wherein the fifth impedance transformer includes a second transmission line with a second impedance and a second length, wherein the first impedance is substantially the same as the second impedance, and wherein the first length is substantially the same as the second length.
- [0134]** Aspect 14: The apparatus of aspect 12, wherein: the fourth impedance transformer includes a first shunt capacitor, a first series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the first series inductor, respectively; the fifth impedance transformer includes a third shunt capacitor, a second series inductor, and a fourth shunt capacitor, wherein the third and fourth shunt capacitors are coupled to both ends of the second series inductor, respectively; and the first, second, third, and fourth shunt capacitors have substantially the same capacitance, and wherein the first and second series inductors have substantially the same inductance.
- [0135]** Aspect 15: A method, including: receiving a first signal at a first signal port; propagating the first signal through a first resistor and a first impedance transformer to generate a second signal at a first intermediate node; splitting the second signal at the first intermediate node to generate third and fourth signals; propagating the third signal through a second impedance transformer towards a second signal port; propagating the fourth signal through a third impedance transformer towards a third signal port; and electrically coupling the second signal port to the third signal port via a second resistor.
- [0136]** Aspect 16: The method of aspect 15, wherein the first, second, and third impedance transformers each includes a transmission line.
- [0137]** Aspect 17: The method of aspect 15, wherein the first, second, and third impedance transformers each includes a first shunt capacitor, a series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the series inductor, respectively.
- [0138]** Aspect 18: The method of any one of aspects 15-17, further including: propagating the third signal through a fourth impedance transformer from a second intermediate node to the second signal port, wherein the second impedance transformer is coupled between the first and second intermediate nodes; propagating the fourth signal through a fifth

impedance transformer from a third intermediate node to the third signal port, wherein the third impedance transformer is coupled between the first and third intermediate nodes; and electrically coupling the second intermediate node to the third intermediate node via a third resistor.

- [0139]** Aspect 19: The method of any one of aspects 15-18, further including splitting the third signal at the second signal port to generate fifth and sixth signals.
- [0140]** Aspect 20: The method of any one of aspects 15-19, further splitting a fifth signal to generate the first signal and a sixth signal.
- [0141]** Aspect 21: A method, including: receiving a first signal at a first signal port; receiving a second signal at a second signal port; electrically coupling the first signal port to the second signal port via a first resistor; propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer; propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer; combining the first and second signals at the first intermediate node to generate a third signal; and propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor.
- [0142]** Aspect 22: The method of aspect 21, wherein the first, second, and third impedance transformers each includes a transmission line.
- [0143]** Aspect 23: The method of aspect 21, wherein the first, second, and third impedance transformers each includes a first shunt capacitor, a series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the series inductor, respectively.
- [0144]** Aspect 24: The method of any one of aspects 21-23, further including: propagating the first signal from the first signal port to a second intermediate node via a fourth impedance transformer, wherein the first impedance transformer is coupled between the first and second intermediate nodes; propagating the second signal from the second signal port to a third intermediate node via a fifth impedance transformer, wherein the second impedance transformer is coupled between the first and third intermediate nodes; and electrically coupling the second intermediate node to the third intermediate node via a third resistor.
- [0145]** Aspect 25: The method of any one of aspects 21-24, further including combining the third signal with a fourth signal to generate a fifth signal.
- [0146]** Aspect 26: The method of any one of aspects 21-25, further including combining fourth and fifth signals to generate the first signal.

- [0147] Aspect 27: A wireless communication device, including: at least one antenna; a set of transceiver chains coupled to the at least one antenna; and a signal power splitter or combiner coupled to the set of transceiver chains, wherein the signal power splitter or combiner includes: a first signal port; a first resistor; a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node; a second impedance transformer coupled between the first intermediate node and a second signal port; a third impedance transformer coupled between the first intermediate node and a third signal port; and a second resistor coupled between the second and third signal ports.
- [0148] Aspect 28: The wireless communication device of aspect 27, wherein the first signal port is coupled to an input of a signal processing circuit, and wherein the second and third ports are coupled to inputs of the set of transceiver chains, respectively.
- [0149] Aspect 29: The wireless communication device of aspect 27, wherein the second and third signal ports are coupled to outputs of the set of transceiver chains, respectively, and wherein the first signal port is coupled to an input of a signal processing circuit.
- [0150] Aspect 30: The wireless communication device of any one of aspects 27-29, wherein the signal power splitter or combiner further comprises: a fourth impedance transformer coupled between a second intermediate node and the second signal port, wherein the second impedance transformer is coupled between the first intermediate node and the second intermediate node; a fifth impedance transformer coupled between a third intermediate node and the third signal port, wherein the third impedance transformer is coupled between the first intermediate node and the third intermediate node; and a third resistor coupled between the second and third intermediate nodes.
- [0151] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS**WHAT IS CLAIMED:**

1. An apparatus, comprising:
 - a first signal port;
 - a first resistor;
 - a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node;
 - a second impedance transformer coupled between the first intermediate node and a second signal port;
 - a third impedance transformer coupled between the first intermediate node and a third signal port; and
 - a second resistor coupled between the second and third signal ports.
2. The apparatus of claim 1, wherein the first impedance transformer comprises a first transmission line with a first impedance and a first length.
3. The apparatus of claim 2, wherein the second impedance transformer comprises a second transmission line with a second impedance and a second length.
4. The apparatus of claim 3, wherein the third impedance transformer comprises a third transmission line with a third impedance and a third length.
5. The apparatus of claim 4, wherein the second impedance is substantially the same as the third impedance, and wherein the second length is substantially the same as the third length.
6. The apparatus of claim 1, wherein the first impedance transformer comprises a first shunt capacitor, a first series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the first series inductor, respectively.
7. The apparatus of claim 6, wherein the second impedance transformer comprises a third shunt capacitor, a second series inductor, and a fourth shunt capacitor,

wherein the third and fourth shunt capacitors are coupled to both ends of the second series inductor, respectively.

8. The apparatus of claim 7, wherein the third impedance transformer comprises a fifth shunt capacitor, a third series inductor, and a sixth shunt capacitor, wherein the fifth and sixth shunt capacitors are coupled to both ends of the third series inductor, respectively.

9. The apparatus of claim 8, wherein the third, fourth, fifth, and sixth shunt capacitors have substantially the same capacitance, and wherein the second and third series inductors have substantially the same inductance.

10. The apparatus of claim 6, wherein the second impedance transformer comprises a second series inductor and a third shunt capacitor, wherein the second shunt capacitor is shared among the first and second impedance transformers, and wherein the second and third shunt capacitors are coupled to both ends of the second series inductor, respectively.

11. The apparatus of claim 10, wherein the third impedance transformer comprises a third series inductor and a fourth shunt capacitor, wherein the second shunt capacitor is shared among the first, second, and third impedance transformers, and wherein the second and fourth shunt capacitors are coupled to both ends of the third series inductor, respectively.

12. The apparatus of claim 1, further comprising:
a fourth impedance transformer coupled between a second intermediate node and the second signal port, wherein the second impedance transformer is coupled between the first intermediate node and the second intermediate node;

a fifth impedance transformer coupled between a third intermediate node and the third signal port, wherein the third impedance transformer is coupled between the first intermediate node and the third intermediate node; and

a third resistor coupled between the second and third intermediate nodes.

13. The apparatus of claim 12, wherein the fourth impedance transformer comprises a first transmission line with a first impedance and a first length, wherein the fifth impedance transformer comprises a second transmission line with a second impedance and a second length, wherein the first impedance is substantially the same as the second impedance, and wherein the first length is substantially the same as the second length.

14. The apparatus of claim 12, wherein:

the fourth impedance transformer comprises a first shunt capacitor, a first series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the first series inductor, respectively;

the fifth impedance transformer comprises a third shunt capacitor, a second series inductor, and a fourth shunt capacitor, wherein the third and fourth shunt capacitors are coupled to both ends of the second series inductor, respectively; and

the first, second, third, and fourth shunt capacitors have substantially the same capacitance, and wherein the first and second series inductors have substantially the same inductance.

15. A method, comprising:

receiving a first signal at a first signal port;

propagating the first signal through a first resistor and a first impedance transformer to generate a second signal at a first intermediate node;

splitting the second signal at the first intermediate node to generate third and fourth signals;

propagating the third signal through a second impedance transformer towards a second signal port;

propagating the fourth signal through a third impedance transformer towards a third signal port; and

electrically coupling the second signal port to the third signal port via a second resistor.

16. The method of claim 15, wherein the first, second, and third impedance transformers each comprises a transmission line.

17. The method of claim 15, wherein the first, second, and third impedance transformers each comprises a first shunt capacitor, a series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the series inductor, respectively.

18. The method of claim 15, further comprising:

propagating the third signal through a fourth impedance transformer from a second intermediate node to the second signal port, wherein the second impedance transformer is coupled between the first and second intermediate nodes;

propagating the fourth signal through a fifth impedance transformer from a third intermediate node to the third signal port, wherein the third impedance transformer is coupled between the first and third intermediate nodes; and

electrically coupling the second intermediate node to the third intermediate node via a third resistor.

19. The method of claim 15, further comprising splitting the third signal at the second signal port to generate fifth and sixth signals.

20. The method of claim 15, further splitting a fifth signal to generate the first signal and a sixth signal.

21. A method, comprising:

receiving a first signal at a first signal port;

receiving a second signal at a second signal port;

electrically coupling the first signal port to the second signal port via a first resistor;

propagating the first signal from the first signal port to a first intermediate node via a first impedance transformer;

propagating the second signal from the second signal port to the first intermediate node via a second impedance transformer;

combining the first and second signals at the first intermediate node to generate a third signal; and

propagating the third signal from the first intermediate node to a third signal port via a third impedance transformer and a second resistor.

22. The method of claim 21, wherein the first, second, and third impedance transformers each comprises a transmission line.

23. The method of claim 21, wherein the first, second, and third impedance transformers each comprises a first shunt capacitor, a series inductor, and a second shunt capacitor, wherein the first and second shunt capacitors are coupled to both ends of the series inductor, respectively.

24. The method of claim 21, further comprising:

propagating the first signal from the first signal port to a second intermediate node via a fourth impedance transformer, wherein the first impedance transformer is coupled between the first and second intermediate nodes;

propagating the second signal from the second signal port to a third intermediate node via a fifth impedance transformer, wherein the second impedance transformer is coupled between the first and third intermediate nodes; and

electrically coupling the second intermediate node to the third intermediate node via a third resistor.

25. The method of claim 21, further comprising combining the third signal with a fourth signal to generate a fifth signal.

26. The method of claim 21, further comprising combining fourth and fifth signals to generate the first signal.

27. A wireless communication device, comprising:

at least one antenna;

a set of transceiver chains coupled to the at least one antenna; and

a signal power splitter or combiner coupled to the set of transceiver chains, wherein the signal power splitter or combiner comprises:

- a first signal port;
- a first resistor;
- a first impedance transformer coupled in series with the first resistor between the first signal port and a first intermediate node;
- a second impedance transformer coupled between the first intermediate node and a second signal port;
- a third impedance transformer coupled between the first intermediate node and a third signal port; and
- a second resistor coupled between the second and third signal ports.

28. The wireless communication device of claim 27, wherein the first signal port is coupled to an input of a signal processing circuit, and wherein the second and third ports are coupled to inputs of the set of transceiver chains, respectively.

29. The wireless communication device of claim 27, wherein the second and third signal ports are coupled to outputs of the set of transceiver chains, respectively, and wherein the first signal port is coupled to an input of a signal processing circuit.

30. The wireless communication device of claim 27, wherein the signal power splitter or combiner further comprises:

- a fourth impedance transformer coupled between a second intermediate node and the second signal port, wherein the second impedance transformer is coupled between the first intermediate node and the second intermediate node;
- a fifth impedance transformer coupled between a third intermediate node and the third signal port, wherein the third impedance transformer is coupled between the first intermediate node and the third intermediate node; and
- a third resistor coupled between the second and third intermediate nodes.

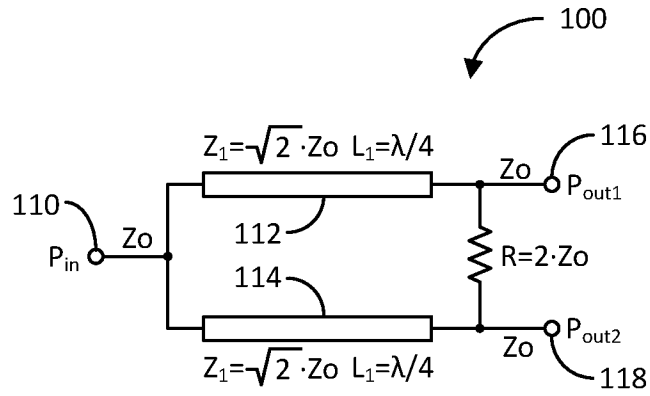


FIG. 1A

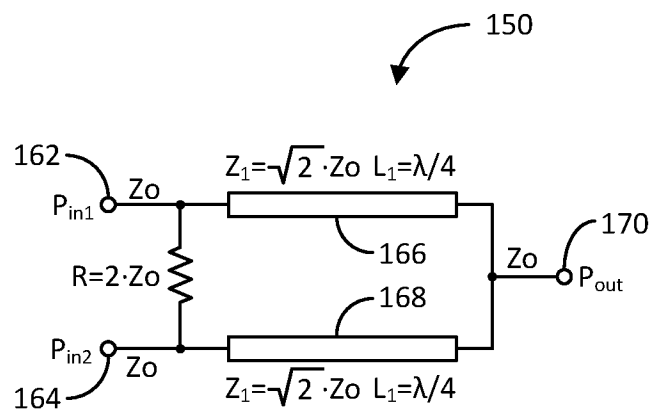


FIG. 1B

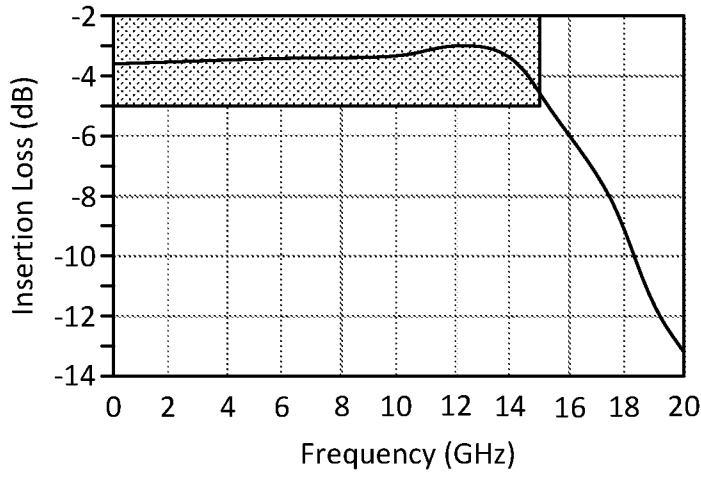


FIG. 2A

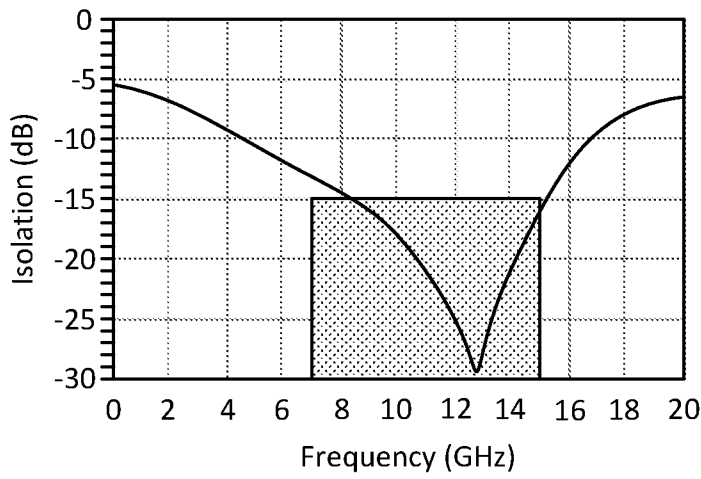


FIG. 2B

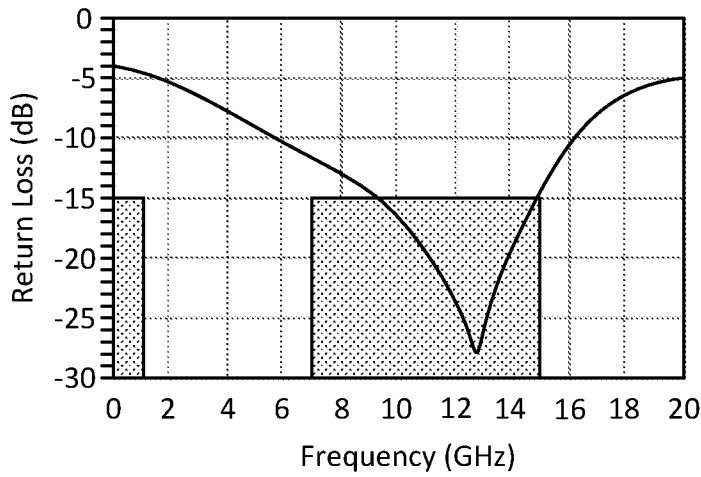


FIG. 2C

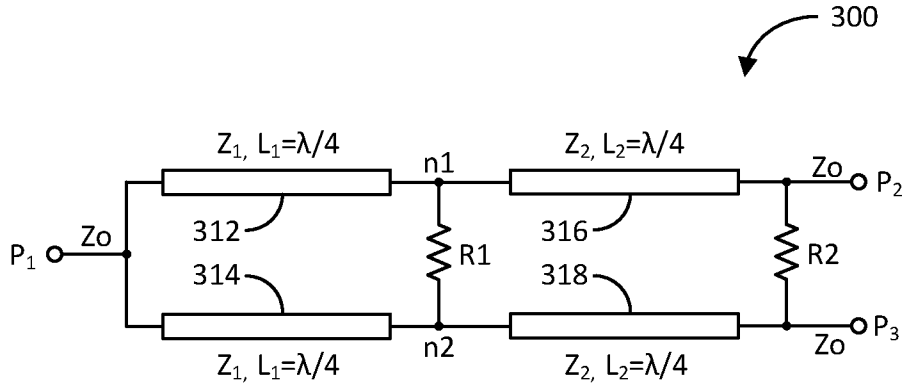


FIG. 3

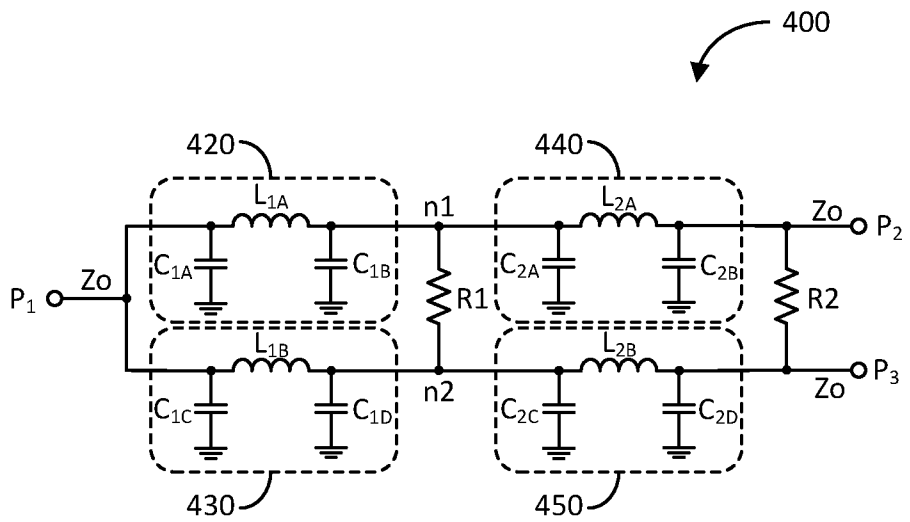


FIG. 4

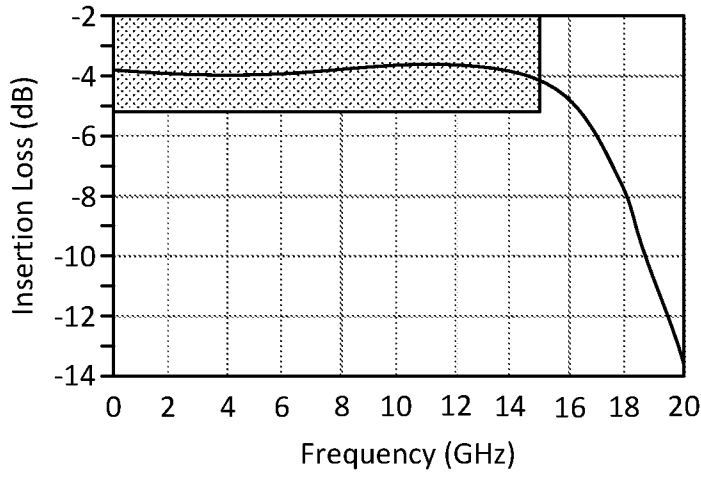


FIG. 5A

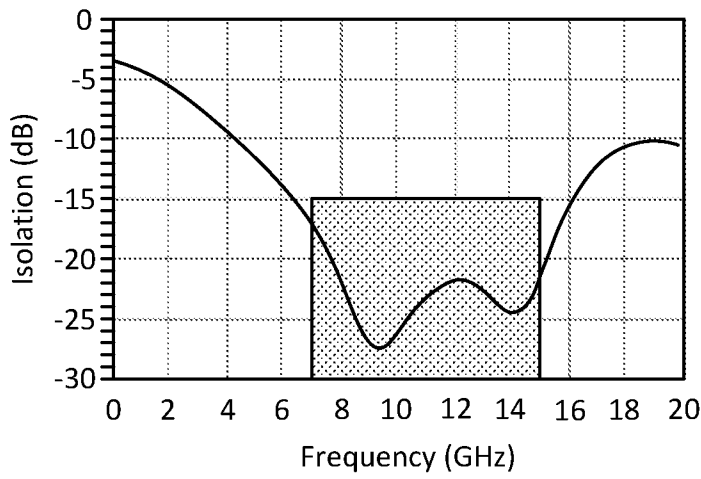


FIG. 5B

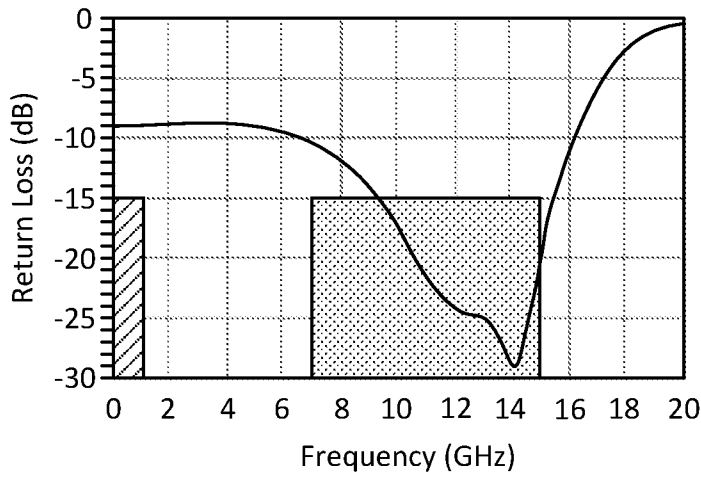


FIG. 5C

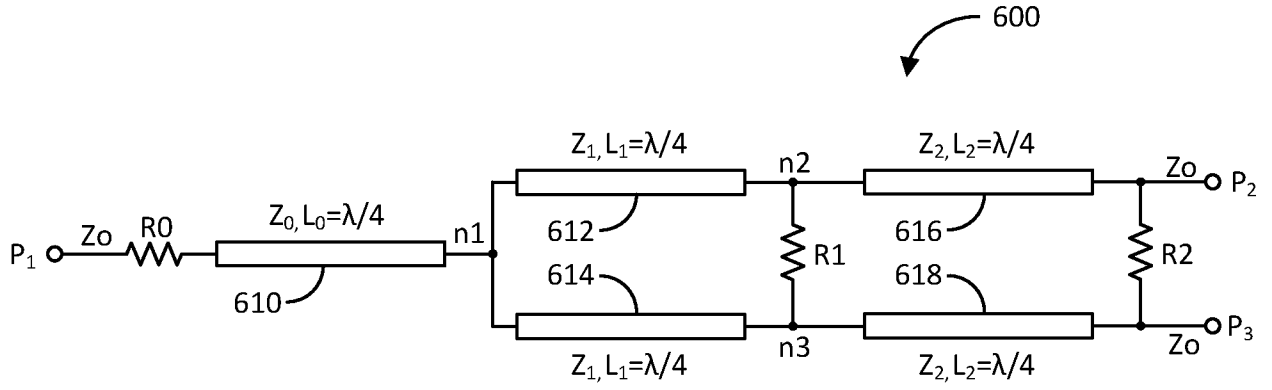


FIG. 6

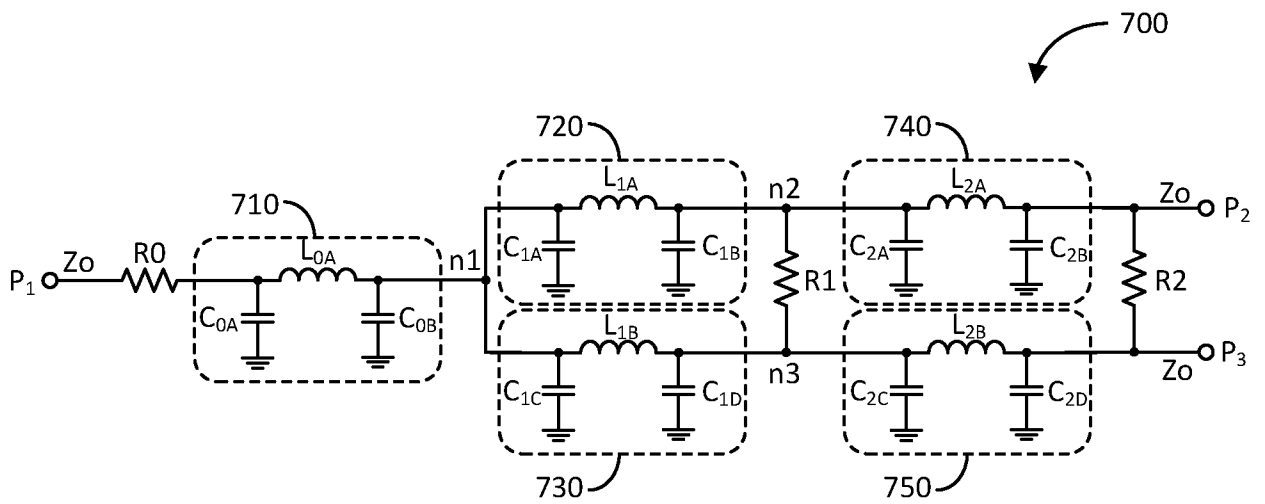


FIG. 7

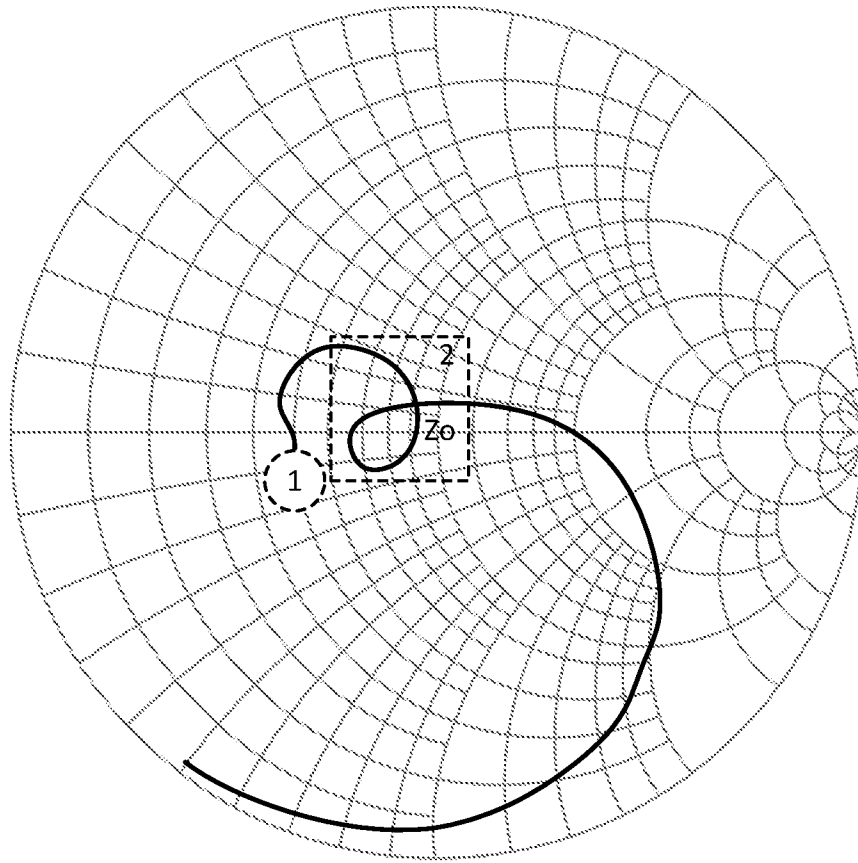


FIG. 8

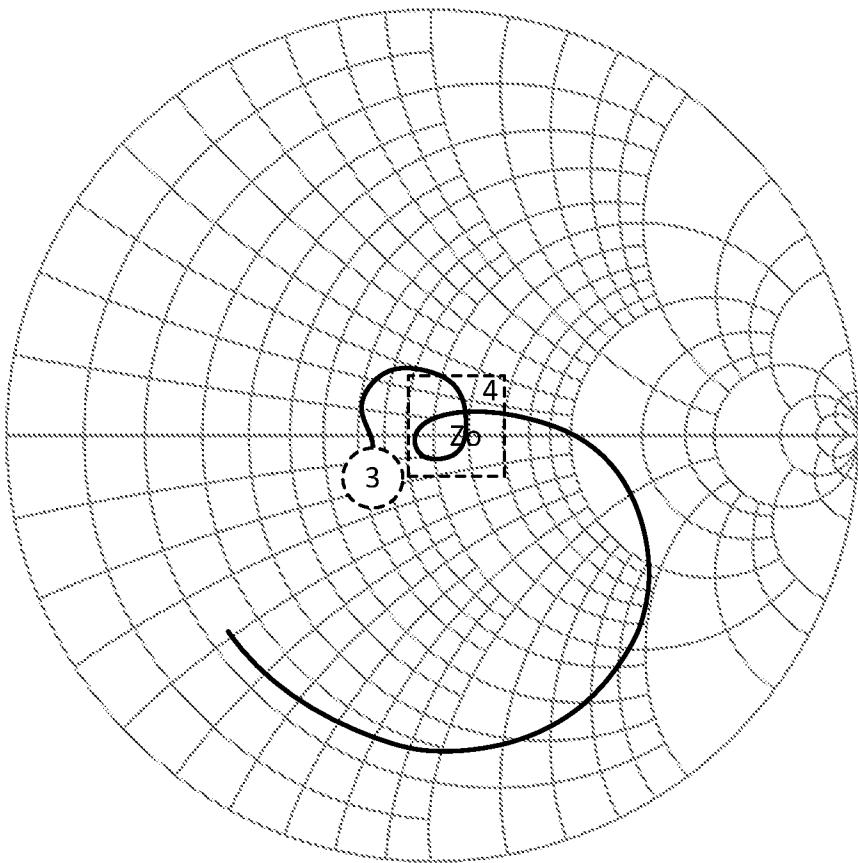


FIG. 9

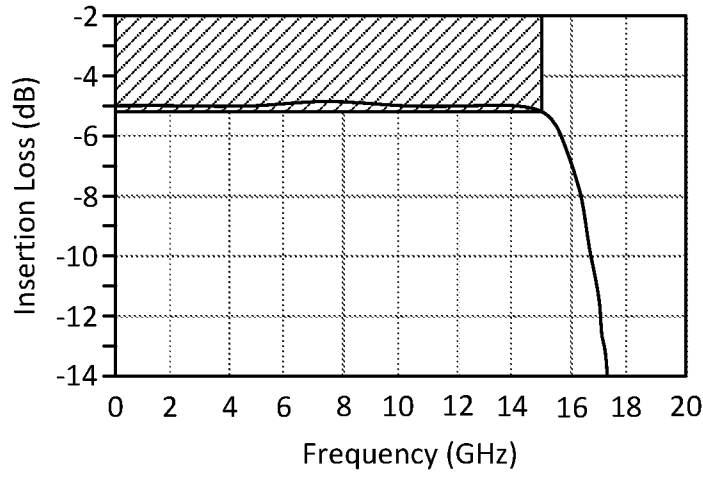


FIG. 10A

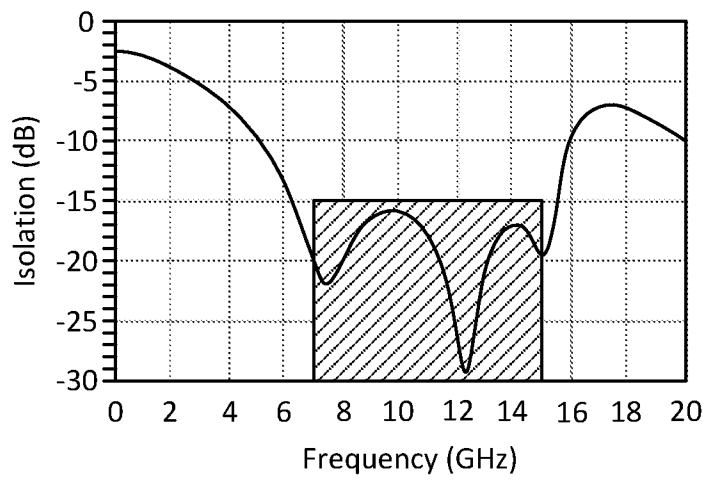


FIG. 10B

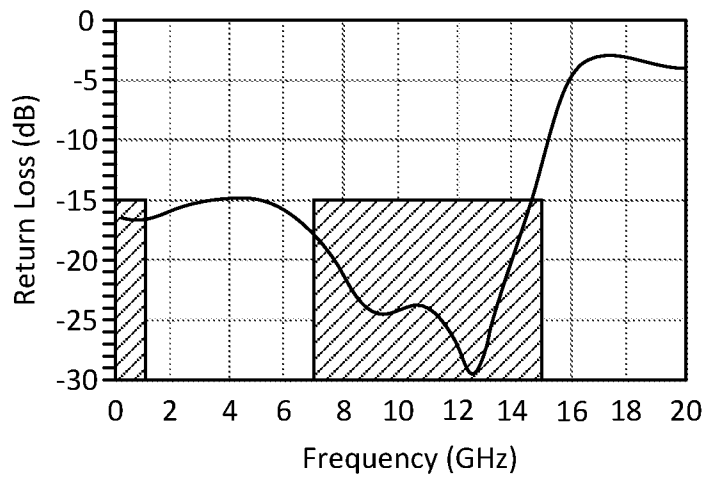


FIG. 10C

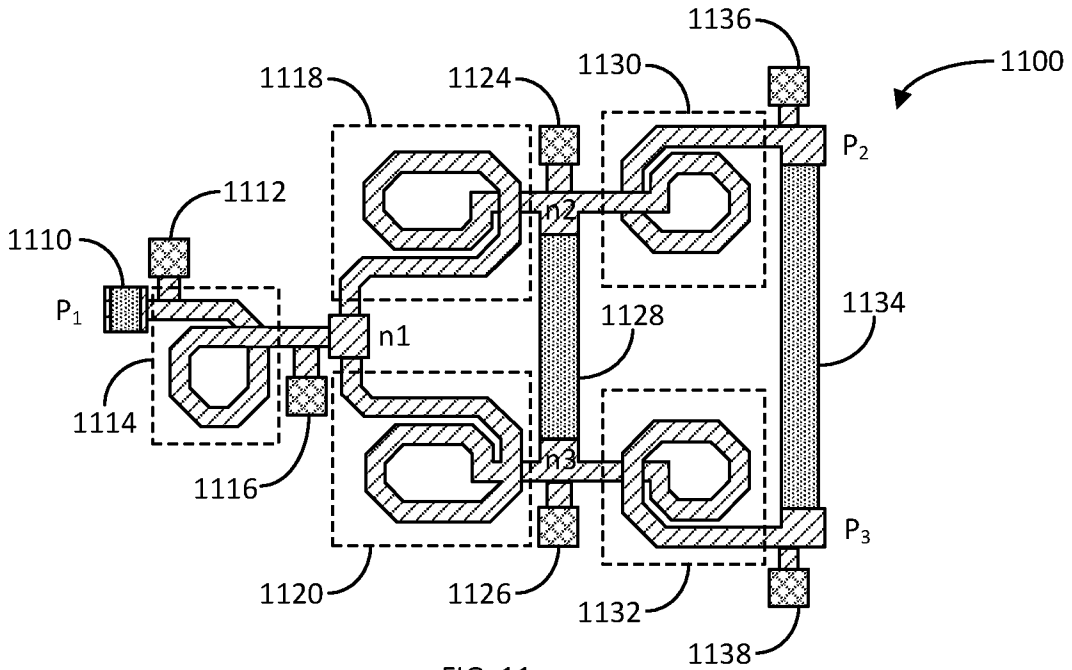


FIG. 11

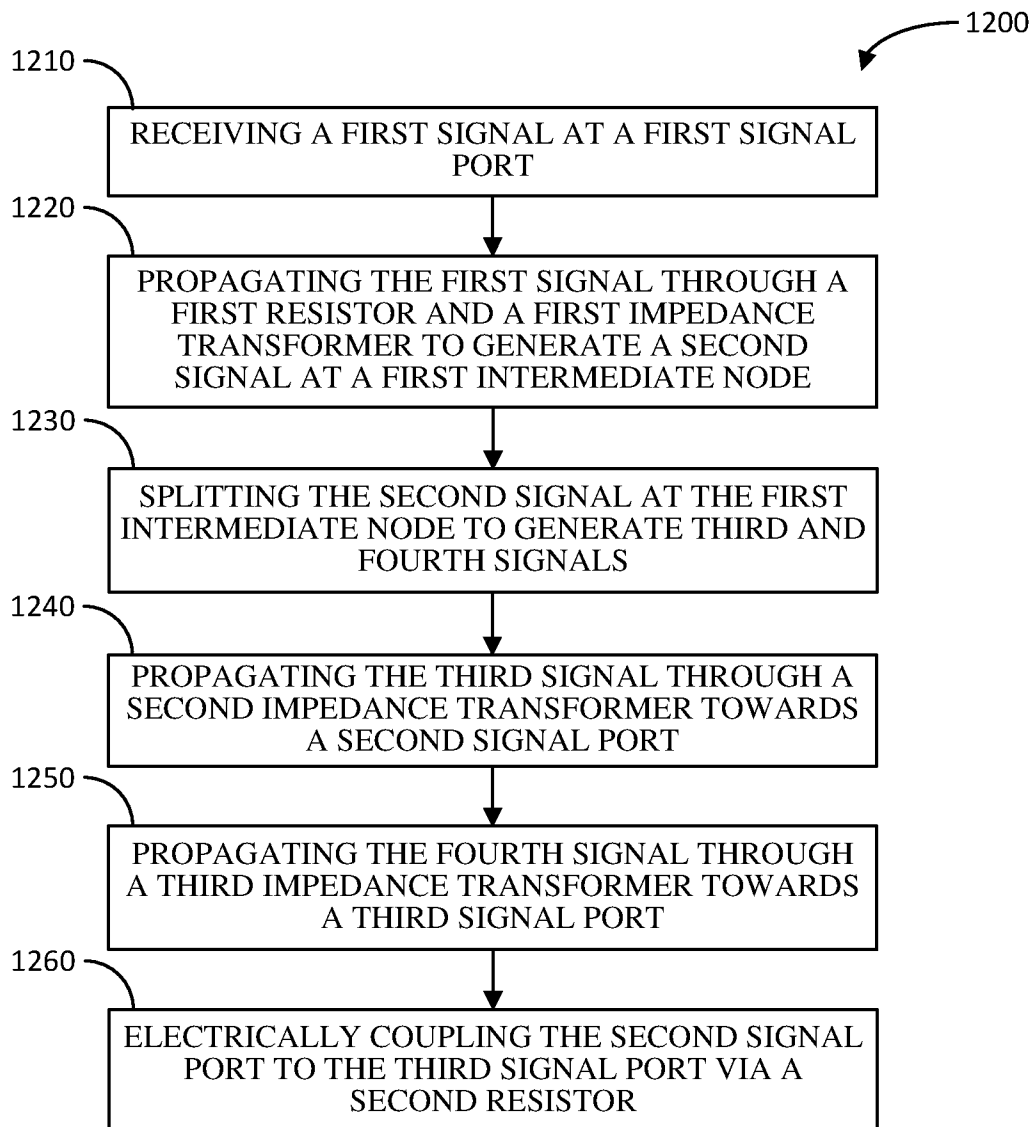


FIG. 12

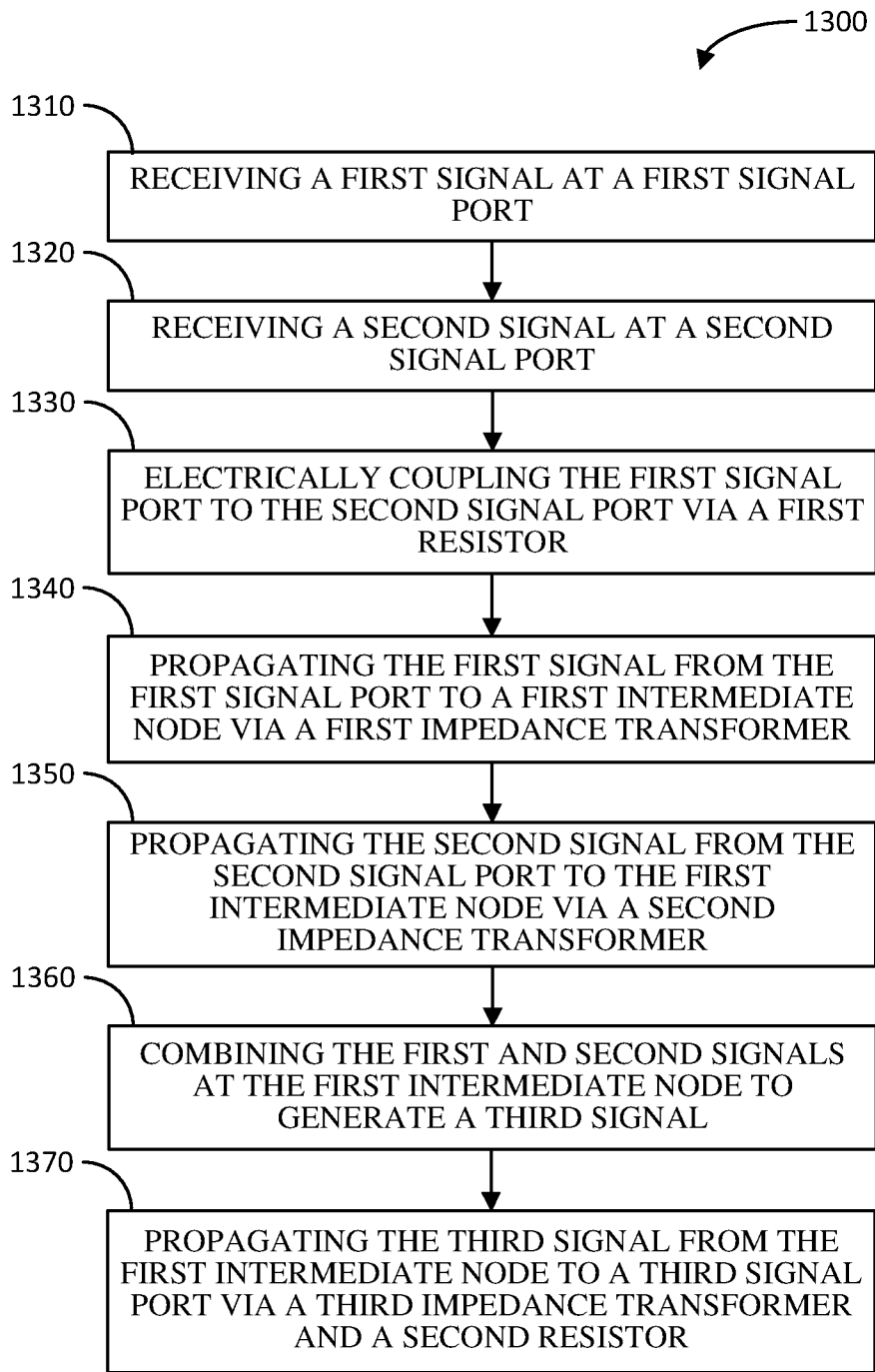


FIG. 13

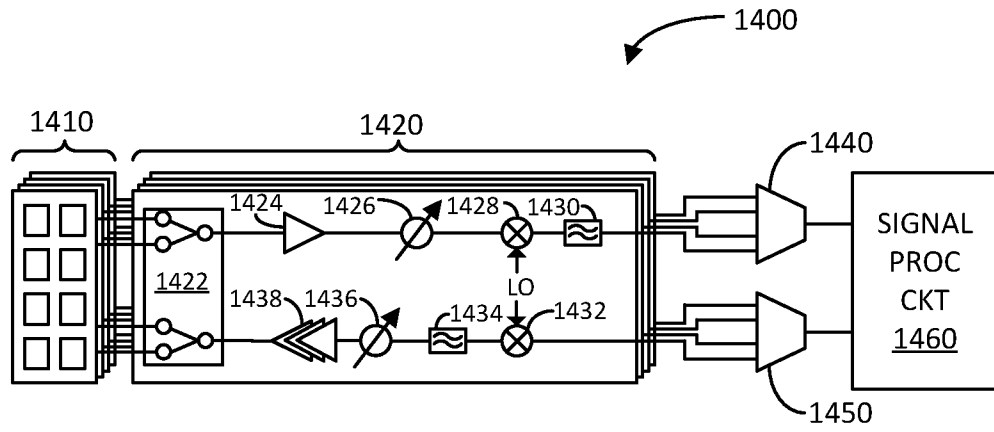


FIG. 14

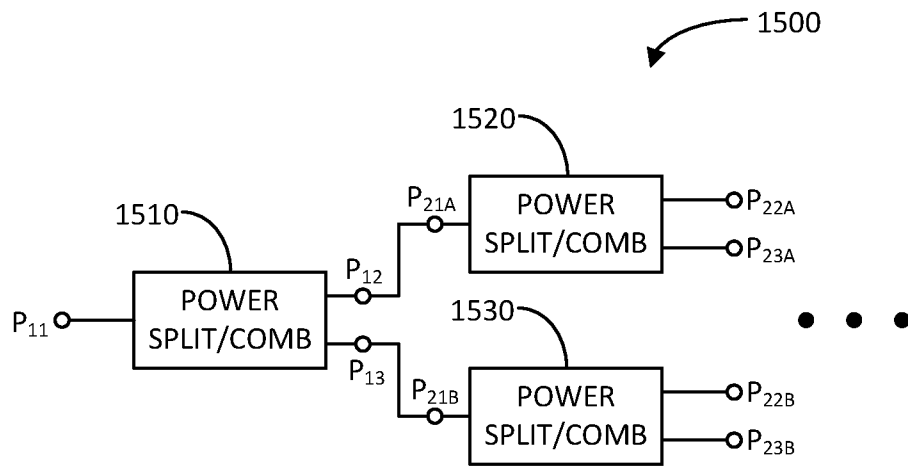


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2022/037358

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H7/48 H01P5/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
 Minimum documentation searched (classification system followed by classification symbols)
H03H H01P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2003 163514 A (AGILENT TECHNOLOGIES JAPAN LTD) 6 June 2003 (2003-06-06) paragraphs [0001], [0011], [0016]; figures 4, 7, 12	1-30
A	BAHL I J: "Ultrabroadband and compact power dividers/combiners on gallium arsenide substrate", IEEE MICROWAVE MAGAZINE, vol. 9, no. 2, April 2008 (2008-04), pages 96-104, XP011225693, section "The Wilkinson Power Divider" bridging pages 98, 99; figures 3-5	1-30

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search 25 October 2022	Date of mailing of the international search report 08/11/2022
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Maget, Judith
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INTERNATIONAL SEARCH REPORT

International application No

PCT/US2022/037358

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>Torgersen Tron: "Wilkinson Power Divider - A Miniaturized MMIC Lumped Component Equivalent", , June 2009 (2009-06), pages 1-146, XP055974394, Retrieved from the Internet: URL:https://ntnuopen.ntnu.no/ntnu-xmlui/bitstream/handle/11250/2369418/348781_FULLTEXT01.pdf?sequence=2 [retrieved on 2022-10-25] pages 5-8; figures 2,4,5</p> <p>-----</p>	1-30
A	<p>JOHWA KIM ET AL: "A Switchless, μm SiGe BiCMOS Technology", -Band Bidirectional Transceiver in 0.12- IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 47, no. 2, February 2012 (2012-02), pages 368-380, XP011393182, figure 1</p> <p>-----</p>	1-30
X	<p>JP H10 233637 A (FUJITSU LTD) 2 September 1998 (1998-09-02) paragraphs [0009], [0010]; figures 1,3</p> <p>-----</p>	1-5,15, 16,21,22
A	<p>EP 0 210 606 A2 (ROHDE & SCHWARZ [DE]) 4 February 1987 (1987-02-04)</p> <p>figures 1,2</p> <p>-----</p>	1,6-12, 14,15, 17,21,23
A	<p>US 5 469 129 A (DYDYK MICHAEL [US]) 21 November 1995 (1995-11-21)</p> <p>figure 6</p> <p>-----</p>	1,6-12, 14,15, 17,21,23
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