(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 September 2002 (06.09.2002)

PCT

(10) International Publication Number
WO 02/069026 A2

(51) International Patent Classification[7]: G02F 1/025

(21) International Application Number: PCT/GB02/00779

(22) International Filing Date: 22 February 2002 (22.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

0104384.3	22 February 2001 (22.02.2001)	GB
0106092.0	13 March 2001 (13.03.2001)	GB
0106338.7	14 March 2001 (14.03.2001)	GB
0107613.2	27 March 2001 (27.03.2001)	GB
0123245.3	27 September 2001 (27.09.2001)	GB

(71) Applicant *(for all designated States except US)*: **BOOKHAM TECHNOLOGY PLC** [GB/GB]; 90 Milton Park, Abingdon, Oxfordshire OX14 4RY (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **VONSOVICI, Adrian, Petru** [RO/GB]; 59 Runnymede, London SW19 2PG (GB).

(74) Agents: **CLAYTON-HATHWAY, Anthony, Nicholas** et al.; Fry Heath & Spence, The Old College, 53 High Street, Horley, Surrey RH6 7BN (GB).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

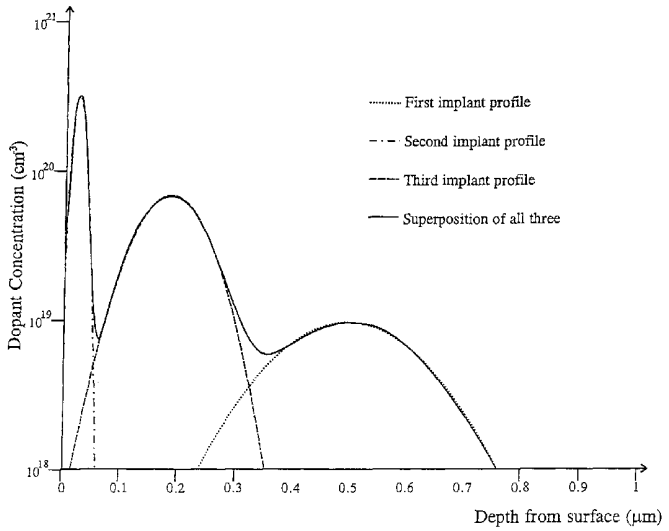
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: ELECTRO-OPTIC DEVICES



(57) Abstract: A method of manufacturing an electro-optic device is described, comprising the steps of applying to a semiconductor a first dose of a dopant impurity to a first depth, and further applying, by implantation, a second dose of dopant impurity at an energy sufficient to implant the dopant to a second depth, the second depth being greater than the first depth. Both doses can be applied by implantation. The second dose can thus extend to the insulating layer of an SOI structure whilst the first offers a good ohmic contact and increased lateral injection efficiency. A third dose of dopant impurity can by applied between the first and second. The application also relates to an electro-optic device comprising a doped region in which the concentration profile of dopant with depth comprises at least one point of inflexion, a minima, and/or a maxima between a pair of minima.

WO 02/069026 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ELECTRO-OPTIC DEVICES

The present invention relates to electro-optic devices, and in particular electro-optic modulators, and methods by which they may be constructed.

Electro-optic modulators are used to affect the complex refractive index of a semiconductor waveguide and thereby affect the phase and amplitude of an optic mode propagating therein. Commonly, in injection-type modulators, a p-i-n diode is formed across the waveguide such that charge carriers are injected into the region in which the mode is propagating. The presence of significant numbers of charge carriers affects the local refractive index and thus the speed of light transmission. This effect can be used in switches, interferometers, attenuators etc.

In silicon-on-insulator (SOI) devices, a buried oxide layer acts as an insulating layer which provides confinement of the charge carriers in the vertical direction. However, it has been found that significant numbers of charge carriers still escape laterally, and this adversely affects both the performance of the device and its reproducibility. We have proposed to deal with this by arranging for the doped regions to extend from the base of a recess formed in the semiconducting layer. Another issue is the thermal and stress loads on the integrated device as a whole involved in the doping process, and the present invention seeks to minimise these.

The present invention therefore provides a method of manufacturing an electro-optic device comprising the steps of applying to a semiconductor a first dose of a dopant impurity to a first depth, and further applying, by implantation, a second dose of dopant impurity at an energy sufficient to implant the dopant to a second depth, the second depth being greater than the first depth.

The semiconductor preferably comprises silicon, but other semiconductors may be used. The dopant preferably is applied above an optical confinement and/or electrically insulating layer situated below a surface of the semiconductor from which the dopant is applied.

Thus, a first dose creates a high dopant concentration near the surface of the semiconductor and allows a good ohmic contact. The second dose creates a deep dopant profile that, where necessary, extends to the insulating layer of an SOI structure for example. This provides the profile needed for the structures described above. To create such a structure by other means would require the dopant to be driven deeply into the semiconductor in a manner that would impose a high thermal load on the device. Thus, to additionally ensure an ohmic contact despite the strong drive-in, the total dopant dose would also need to be high.

It is preferred that both doses are applied by implantation as this will be more straightforward in practice. Likewise, it will usually be more straightforward to apply the first dose prior to the second dose. However, the second dose can be applied first.

It will usually be appropriate for the second dose to be greater than the first, per unit area, typically at least 150% of the first. This is to allow an adequate dopant concentration despite the greater depth over which the second dose is to be spread.

As mentioned above, the invention is particularly appropriate for use with semiconductors comprising a substrate on which there is an insulating layer, over which there is a semiconducting layer in which the dopants are placed, e.g. an SOI device (silicon-on-insulator). More generally, the semiconductor preferably comprises a substrate on which there is an optical confinement layer, over which there is a semiconducting layer in which the dopants are placed. The optical confinement layer preferably comprises such an insulating layer (e.g. silica in the case of the semiconductor being silicon). This is because in such devices we have identified a need to extend the dopant dose to the insulating layer. Thus, it is preferred that the second depth is at least 80% of the thickness of the semiconducting layer, more preferable at least the thickness of the semiconducting layer.

According to the invention, a third or further dose of dopant impurity can also be applied. Typically, which the third dose is greater than the first dose and less than the second dose per unit area and is also applied by ion implantation. Ideally, it is implanted with sufficient energy to reach a third depth which is greater than the first depth and less than the second depth.

It will clearly be simplest for the first, second and third (where applied) dopants to be identical in nature.

The present invention also relates to an electro-optic device comprising a doped region in which the concentration profile of dopant with depth comprises at least one point of inflexion.

It is preferred that the doped region is adjacent an optical waveguide such as a rib waveguide. In such an arrangement, the device can include a further doped region, located such that the waveguide passes between the two doped regions,

the doped regions defining a modulator structure for optical modes conveyed by the waveguide.

Embodiments of the present invention will now be described by way of example, with reference to the accompanying figures, in which;

Figure 1 is a cross-sectional view of a p-i-n diode employing recessed junctions;

Figure 2 is a graph showing the dopant concentration with depth for a two step doping procedure;

Figure 3 is a graph showing the dopant concentration with depth for a three step doping procedure; and

Figures 4 and 5 are graphs showing carrier concentration with position resulting from two-stage implantation.

Figure 1 shows a p-i-n diode of the type to which this invention is directed. It should be understood, however, that the invention is concerned with providing a deep dopant profile in combination with a significant dopant concentration at shallow levels, whilst minimising thermal and other loads on the device. Accordingly, the invention is not limited to devices of the type shown in figure 1.

An SOI structure comprises a substrate 16 over which is formed an insulating layer 14, on which a silicon layer 12 is formed. A ridge 10 in the silicon epi layer 12 defines a waveguide for an optical mode. A cover of silicon dioxide 26 provides electrical and optical isolation and confinement.

A pair of trenches 36, 38 are formed either side of the waveguide 10,

extending generally alongside. Doped regions 18,20 are formed by diffusion and/or implantation from the trenches 36, 38 and in this case extend from the bases of the trenches 36, 38 to the insulating layer 14, providing good electrical confinement in the two lateral directions.

Further integration of lateral p-i-n optical modulators with other integrated optics devices (multiplexers, interferometers, couplers etc.) demands a reduction of the thermal budget and the stress. The standard method of fabrication using predeposition by diffusion demands usage of a silicon nitride mask and high temperature drive-ins which induces great stress and modification of the optical properties of other integrated optics devices. Improvements can be obtained by employing ion-implantation as a predeposition method. This eliminates some of the stress issues associated with silicon nitride layers used as masks, but maintains a high thermal budget for the drive-in process step following the initial deposition. Also, to obtain good efficiency from the injectors, relatively high doses of the implanted dopant elements are necessary. Even in this case the efficiency of the injectors is far from optimum due to the large gradual junction formed by this method.

The present invention addresses the following issues:

- Reduction of the total implantation dose (related to the time of implantation) which is important in order to improve the quality of the junctions.

- Optimisation of the doping profile by using multi-step implantation in order to reduce or eliminate the need for drive-in thermal processing.

- Increasing the injection performance of the p-i-n diodes by using a multi-section doped structure. Each sections plays a role in the

injection, electrical performance of the contacts and carrier leakage blockage.

Therefore the device can approach an optimum design more closely, and can be integrated monolithically with other type of integrated optics devices (such as multiplexers and demultiplexers, interferometric devices, couplers) that could not stand doping processes with high thermal loads and deposition of high stress layers.

The current invention deals with a class of optical modulators realised using a 2D waveguiding structure (typically a rib or strip loaded waveguide) and a lateral injection structure (typically a p-i-n diode). The waveguides often have a buried insulator layer (typically buried oxide in silicon-on-insulator structures). Such a structure using rib waveguide made on SOI and recessed junctions (the junctions are "pushed" to the bottom interface by using an etched trench) is, as metioned, depicted in figure 1.

To achieve the three objectives set out above, an ideal doping profile should address the following issues;

- Good contact resistance, dependent on the concentration of the dopant at the surface

- Good injection level, dependent on the overall doping level of the junctions

- Good blocking of escaping carriers underneath the junctions, dependent mainly on the level of doping at the interface with the buried layer (buried oxide).

Another constraint is the possibility of fabrication using ion-implantation techniques and Rapid Thermal Processing (RTP) with practically no thermal load to the remainder of the wafer. Also, an ideal solution should not rely on the use of high stress dielectric films in the processing (such as silicon nitride) which can perturb other sensitive integrated optics devices.

In a first embodiment (Figure 2), the doping is carried out by a superposition of two profiles. A first implant localised next to the surface will insure a high level of dopant necessary to have a good ohmic contact. The second implant is provided to a greater depth and ensures good injection and carrier blocking. In the embodiment of figure 2 a short drive-in step of 10 minutes at 1050°C using RTP is provided in order to extend the original profile to a somewhat greater depth and also achieve a significantly high level of doping at the interface with the buried oxide. This solution introduces a negligibly small thermal load and is therefore acceptable in practice.

In a second embodiment (Figure 3), the doping profile is obtained by superposition of three implants and does not require any drive-in thermal process. A Rapid Thermal Processing (RTP) step is sufficient to activate the impurities. Therefore, this embodiment is very well adapted for further integration with other integrated optics devices (such as Arrayed Waveguide Gratings, Mach-Zehnder interferometers etc.) which have a high sensitivity to thermal induced stress during processing.

According to this embodiment, a third implant is arranged to inject dopant to a depth intermediate the first and second. This therefore provides a step between the two and allows the second implant to be driven deeper than otherwise.

Simulated carrier concentrations for a two-step profile as per the first embodiment are shown in figures 4 and 5. The concentration of holes is shown at a high injection regime is considered in which p≅n. These allow an evaluation of the injection efficiency in the case of a rib waveguide on an SOI substrate. Each proposed solution is compared against a standard device having a gradual junction made by predeposition of the dopant and a drive-in step.

Experimental data are available for doping profiles obtained for standard structures made by ion implantation dopant predeposition (doses $8x10^{15}cm^{-2}$ for boron and $10^{16}cm^{-2}$ for phosphourus) followed by a drive-in step during thermal oxide growth (40min at 1050°C) and they were used in this calculation.

Figure 4 shows the carrier distribution for the two stage profile of figure 2, at different doses of the second implant, maintaining the first implant dose constant at $2x10^{15}cm^{-2}$ for both dopants. The standard case is depicted as a solid line labelled P. Three cases are shown, in which the second implant dose is $4x10^{15}cm^{-2}$ (line Q), $2.3x10^{15}cm^{-2}$ (line R) and $2.9x10^{15}cm^{-2}$ (line S). It is possible to increase the efficiency of the injection (equivalently the level of injected carrier concentration) by 10% in the case of the second implant having a dose of $2x10^{15}cm^{-2}$.

It is worth noting that, compared to the standard case, the overall dose was 2.5 times smaller whereas the carrier concentrations are comparable. The improvement in injection efficiency for the case of the two-section dopant profile is significant.

Figure 5 shows the results obtained for a three stage profile (figure 3). Again, line P shows the standard case whereas lines T and U refer to second doses of $4x10^{15}cm^{-2}$ and $3.3x10^{15}cm^{-2}$ respectively. For doses about 20% lower than in

the case of two stage profiles, a significant improvement in the injection efficiency of about 60% higher than the standard diode is obtained, together with a reduction in the lateral leakage with respect to the two stage device. This device also has the advantage of being fabricatable using only ion-implantation steps and Rapid Thermal Processing steps, which implies very low thermal budget for the process and therefore compatibility with very sensitive interferometric devices.

It will be understood that many variations may be made to the above-described embodiments without departing from the scope of the present invention.

CLAIMS

1. A method of manufacturing an electro-optic device comprising the steps of applying to a semiconductor a first dose of a dopant impurity to a first depth, and further applying, by implantation, a second dose of dopant impurity at an energy sufficient to implant the dopant to a second depth, the second depth being greater than the first depth.

2. A method according to claim 1, in which the doses of dopant are applied above an optical confinement and/or electrically insulating layer situated below a surface of the semiconductor from which the dopant doses are applied.

3. A method according to claim 1 or claim 2 in which both doses are applied by implantation.

4. A method according to any one of the preceding claims in which the first dose is applied prior to the second dose.

5. A method according to any one of the preceding claims in which the second dose is greater than the first per unit area.

6. A method according to claim 5 wherein the second dose is at least 150% of the first.

7. A method according to any one of the preceding claims in which the semiconductor comprises a substrate on which there is a said insulating and/or optical confinement layer, over which there is a semiconducting layer in which the dopants are placed.

8. A method according to claim 7 in which the second depth is at least 80% of the thickness of the semiconducting layer.

9. A method according to claim 7 in which the second depth is at least the thickness of the semiconducting layer.

10. A method according to any one of the preceding claims in which a third dose of dopant impurity is applied.

11. A method according to claim 10 in which the third dose is greater than the first dose per unit area.

12. A method according to claim 10 or claim 11 in which the third dose is less than the second dose per unit area.

13. A method according to any one of claims 10 to 12 in which the third dopant dose is applied by ion implantation.

14. A method according to claim 13 in which the third dopant dose is implanted with sufficient energy to reach a third depth which is greater than the first depth.

15. A method according to claim 13 or claim 14 in which the third dopant dose is implanted with sufficient energy to reach a third depth which is less than the second depth.

16. A method according to any one of the preceding claims in which the dopant of the first and second doses is identical in nature.

17. An electro-optic device comprising a doped region prepared according to any one of the preceding claims.

18. An electro-optic device comprising a doped region in which the concentration profile of dopant with depth comprises at least one point of inflexion.

19. A device according to claim 18 in which the profile includes a maxima between a pair of minima.

20. A device according to any one of claims 17 to 19 in which the doped region is adjacent an optical waveguide.

21. A device according to claim 20 in which the waveguide is a rib waveguide.

22. A device according to claim 20 or claim 21 which includes a further doped region, the waveguide passing between the two doped regions, the doped regions defining a modulator structure for optical modes conveyed by the waveguide.

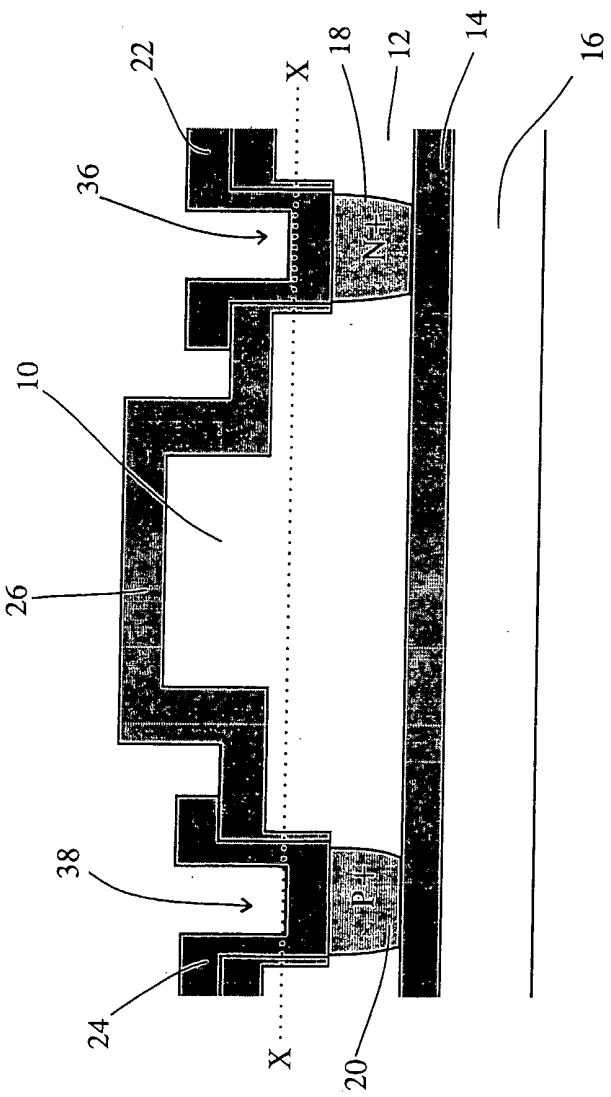


Figure 1

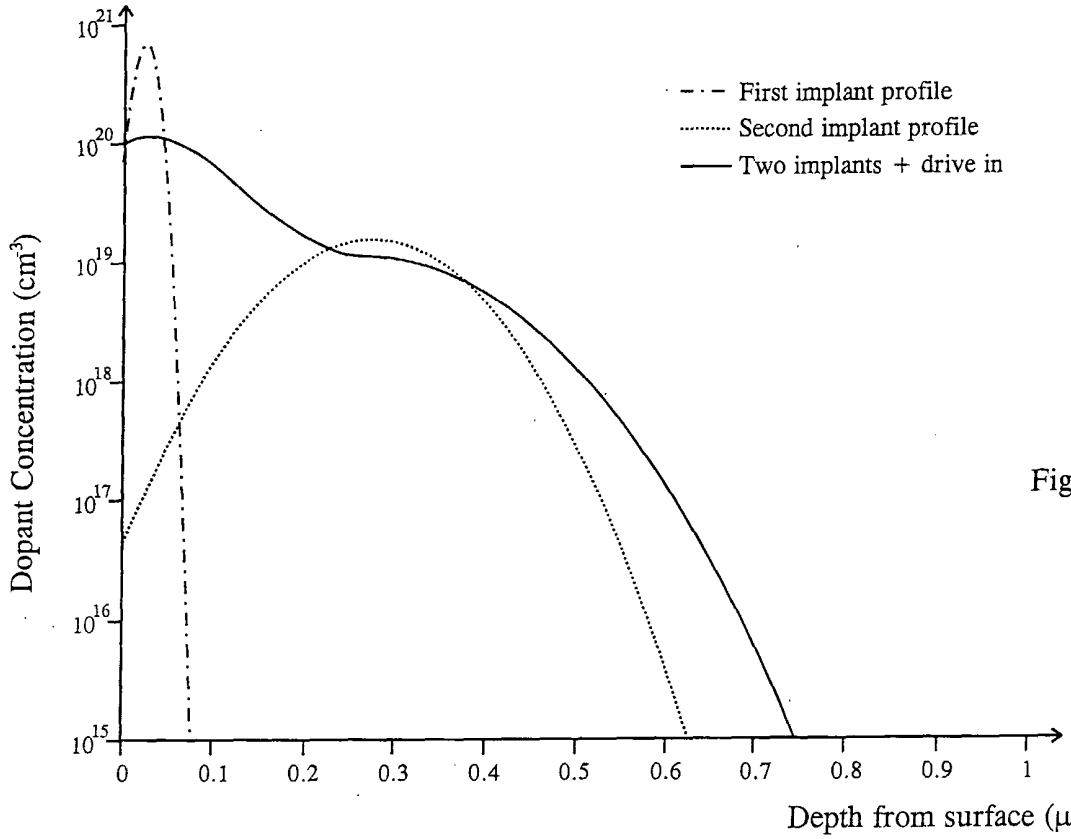

First implant profile
Second implant profile
Two implants + drive in
Dopant Concentration (cm3)
10^21
10^20
10^19
10^18
10^17
10^16
10^15
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Depth from surface (μm)

Fig 2

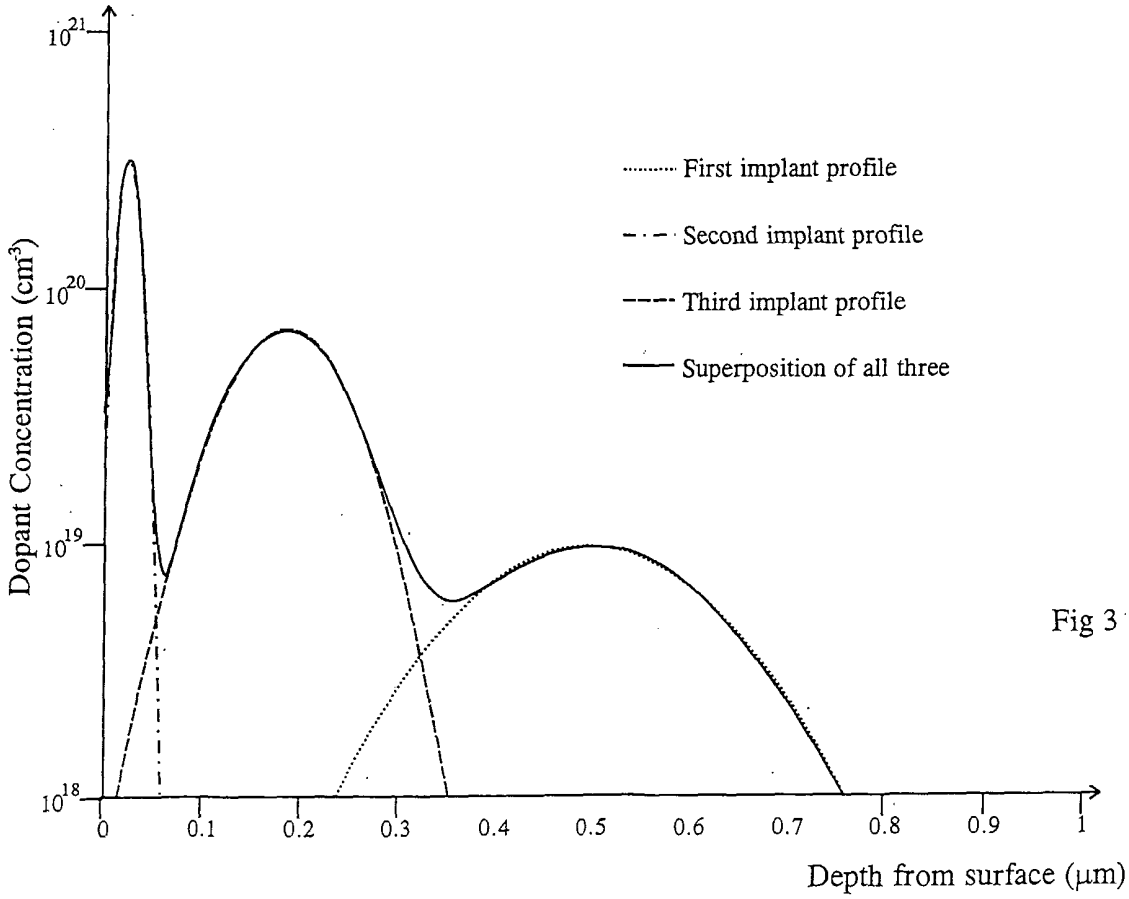

First implant profile
Second implant profile
Third implant profile
Superposition of all three
Dopant Concentration (cm3)
10^21
10^20
10^19
10^18
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Depth from surface (μm)

Fig 3

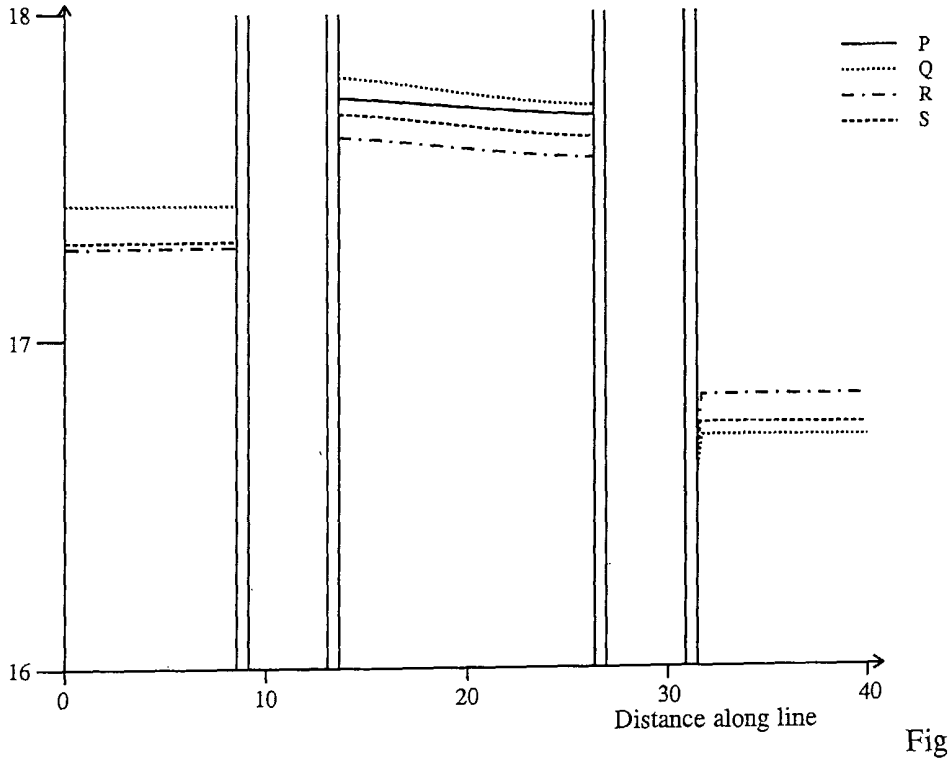

18
17
16
0
10
20
30
40
Distance along line
P
Q
R
S

Fig 4

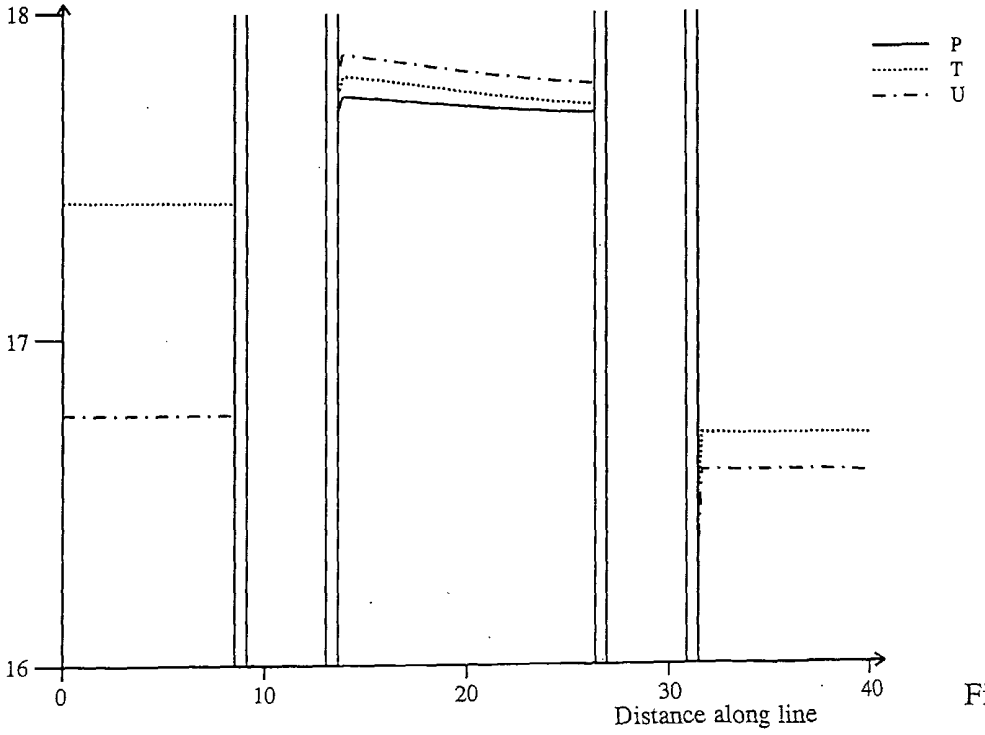

18
17
16
0
10
20
30
40
Distance along line
P
T
U

Fig 5