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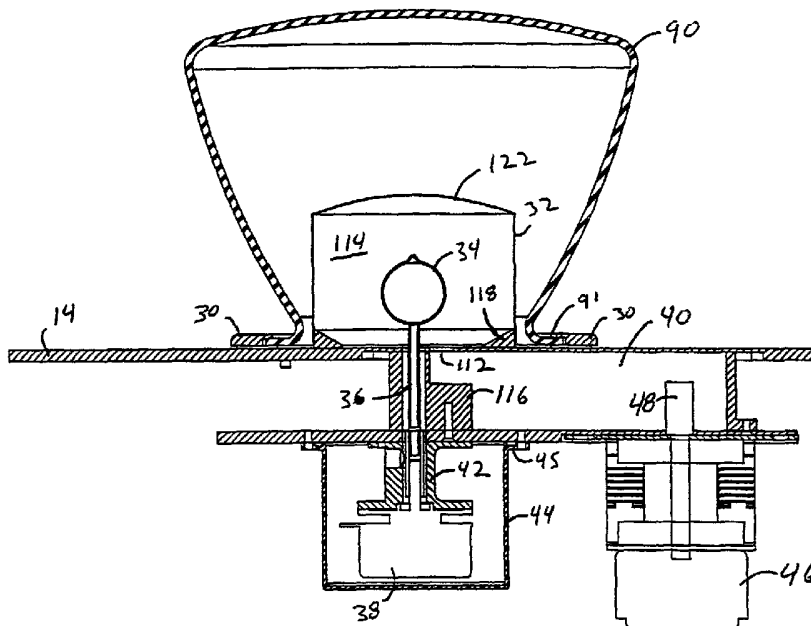
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(54) Title: MICROWAVE ELECTRODELESS LAMP



(57) Abstract: A microwave electrodeless lamp includes an electrodeless bulb (34) enclosing a light generating fill, a mesh screen (32) surrounding the bulb with at least half the bulb volume completely within the mesh; the mesh together with other conductive surface defining a microwave cavity (114), a magnetron (46) for providing microwave energy, and a waveguide (40) for transmitting the microwave energy from the magnetron to the microwave cavity, wherein the minimum distance between the outer bulb surface and the closest portion of the mesh is selected in accordance with the temperature of the bulb during operation and the temperature at which the screen material degrades. Other embodiments and aspects are also disclosed.



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MICROWAVE ELECTRODELESS LAMP

5 [0001] Certain inventions described herein were made with Government support under Contract No. DE-FC26-00NT40988 awarded by the Department of Energy. The Government has certain rights in those inventions.

BACKGROUND

Field of the Invention

0 [0002] The invention relates generally to microwave electrodeless lamps. The invention relates more specifically to a novel microwave cavity configurations for a lamp and improved mesh screen configurations and materials. Another aspect of the invention relates generally to power supplies. This aspect relates more specifically to a novel power factor correction (PFC) circuit and technique.

Related Art

5 [0003] Microwave lamps utilizing cylindrical mesh screens are well known in the art. Most such lamps utilize a relatively narrow screen such that the ratio of the length of the cylindrical cavity to the diameter of the cylindrical cavity is greater than one. In the prior art, a narrow cavity is preferred because it allows the placement of an external reflector closer to the bulb. Using a cylindrical cavity with a small
0 diameter also simplifies the microwave circuit because the lowest frequency resonant mode is utilized with large frequency separation from other resonant modes. The smaller diameter cavity is also less sensitive to changes in the length of the cavity. However, a problem with the narrow cavity is that the proximity of the electrodeless bulb to the screen wall causes overheating of the screen material.
5 Over time the overheating causes degradation of the screen. Once degraded the problem is exacerbated and even greater overheating can lead to thermal runaway, eventually causes failure of the screen and consequently the reliability of the lamp is reduced.

SUMMARY

0 [0004] One object of the invention is to provide an improved microwave electrodeless lamp.

[0005] One aspect of the present invention is achieved by a mesh screen having a lower aspect ratio of length to diameter that reduces the thermal stress on the screen.

[0006] Another object of the invention is to provide an interleaved PFC boost converter circuit that operates over a range of input voltages and frequencies.

[0007] One aspect of the present invention is achieved by sharing of timing information between two sides of an interleaved PFC boost converter. For example, a timing control circuit may provide substantially simultaneous go and stop signals to respective sides of the interleaved PFC boost converter.

[0008] The foregoing and other objects, aspects, advantages, and / or features of the invention described herein are achieved individually and in combination. The invention should not be construed as requiring two or more of such features unless expressly recited in a particular claim.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular description of preferred embodiments as illustrated in the accompanying drawings, in which reference characters generally refer to the same parts throughout the various views. The drawings are not necessarily to scale, the emphasis instead being placed upon illustrating the principles of the invention.

[0010] Fig. 1 is a block diagram of a microwave electrodeless lamp in accordance with the present invention.

[0011] Fig. 2 is a perspective view of an example of a microwave electrodeless lamp in accordance with the present invention.

[0012] Fig. 3 is another perspective view of the microwave electrodeless lamp.

[0013] Fig. 4 is a more detailed perspective view of the lamp with an external cover removed.

[0014] Fig. 5 is another more detailed perspective view of the lamp.

[0015] Fig. 6 is an exploded perspective view showing various components and assemblies of the lamp of the present invention.

[0016] Fig. 7 is a schematic view of an example of a secondary envelope in accordance with the present invention.

- [0017]** Fig. 8 is a cross sectional view of the secondary envelope taken along line 8-8 in Fig. 7.
- [0018]** Fig. 9 is a schematic view of another example of a secondary envelope in accordance with the present invention.
- 5 **[0019]** Fig. 10 is a perspective view of the secondary envelope from Fig. 9.
- [0020]** Fig. 11 is a cross sectional view of selected components of the lamp of the present invention.
- [0021]** Fig. 12 is a perspective view of an example of a mesh screen in accordance with the present invention.
- 0 **[0022]** Fig. 13 is a perspective, cut-away view of the lamp system showing cooling channels.
- [0023]** Fig. 14 is another perspective, cut-away view of the lamp system showing cooling channels.
- [0024]** Fig. 15 is a best fit line graph of light output versus wall plug input for
5 exemplary lamp systems of the present invention.
- [0025]** Fig. 16 is a best fit line graph of lumens per watt versus wall plug input power for the exemplary lamp systems of the present invention.
- [0026]** Fig. 17 is a graph of relative light intensity versus wavelength for a lamp of the present invention.
- 0 **[0027]** Fig. 18 is a comparison graph of light intensity versus angle for a lamp of the present invention.
- [0028]** Fig. 1A is a block diagram of a conventional interleaved PFC circuit.
- [0029]** Fig. 2A is a block diagram of an interleaved PFC circuit in accordance with the present invention.
- 5 **[0030]** Fig. 3A is a more detailed block diagram of an interleaved PFC circuit in accordance with the present invention.
- [0031]** Fig. 4A is a schematic diagram of a first interleaved PFC circuit in accordance with the present invention.
- [0032]** Fig. 5A is a timing diagram of various signals for the circuit from Fig. 4.
- 0 **[0033]** Fig. 6A is a schematic diagram of a second PFC circuit in accordance with the present invention.
- [0034]** Fig. 7A is a schematic diagram of a third PFC circuit in accordance with the present invention.

[0035] Fig. 8A is a graph of PFC voltage versus Input voltage for one example of the present invention.

[0036] Fig. 9A is a graph of the PFC coefficient versus input voltage for one example of the present invention.

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DESCRIPTION

[0037] In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular structures, interfaces, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art having the benefit of the present specification that the invention may be practiced in other embodiments that depart from these specific details. In certain instances, descriptions of well known devices, circuits, and methods are omitted so as not to obscure the description of the present invention with unnecessary detail.

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[0038] With reference to Fig. 1, an example block diagram of a preferred microwave lamp system of the present invention includes an RF assembly providing RF or microwave power. The RF assembly includes a magnetron which generates microwave energy. The microwave energy is transmitted via a waveguide to a microwave cavity, generally comprised of a mesh screen. The microwave cavity is part of the optical cavity assembly which includes the mesh screen and the electrodeless bulb disposed within the screen. The optical cavity further includes an optional reflector for controlling the light output from the bulb. Power is provided to the RF assembly and various other components from a power and control assembly. The power and control assembly receives power from a suitable external source via a power terminal and includes a power supply module for converting the external power to a type of power appropriate for the RF assembly and other electronic components of the lamp. For example, the power supply module may include the novel power factor correction circuit described below in connection with Figs. 1A-9A.

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[0039] The power supply module contains control software for controlling the operation of the power supply. For example, the power supply and control assembly includes a microprocessor for running the control software. An optical sensor provides information to the control assembly which may be used, for example, as a safety interlock. The power and control assembly may include an optional communication module for interfacing with other external devices. The lamp

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components are disposed in a housing assembly which further includes a fan and cooling system.

[0040] Various aspects of the invention described herein relate specifically to one or more of the various assemblies described above and may be practiced independently of the other assemblies. The block diagram in Fig. 1 is only an example of a preferred lamp system and the invention does not require all of the assemblies or the particular structure illustrated in Fig. 1.

[0041] With reference to Figs. 2-6, a lamp 10 includes a housing 12 comprised of a plate 14 and a cover 16. A set of brackets are provided to secure the plate 14 and cover 16 together. The cover 16 provides openings for a cooling air inlet 18 and exhaust air outlets 20. The cover 16 also provides a power receptacle 22 and a covered wiring area 24 for access to an internal power wiring terminal 26. Optional access to a communication port may also be provided through the cover 16.

[0042] A secondary envelope 28 in the shape of a globe is secured to the plate 14 by a pair of retaining brackets 30. The globe 28 protects the microwave cavity and bulb from environmental hazards and may include a gasket, caulking, epoxy, or other suitable material disposed between the lip 31 of the globe 28 and the plate 14 to provide an environmental seal against contaminants. For example, the globe 28 is made from glass and may be transparent or translucent (e.g. frosted).

[0043] The plate 16 provides one end wall of a cylindrical microwave cavity with the remainder of the cavity being defined by a mesh screen 32. The globe 28 protects the screen 32 from mishandling (e.g. accidental deformation). An electrodeless bulb 34 is disposed inside the microwave cavity and includes a stem 36 which is coupled to a motor 38 for rotation of the bulb 34 during lamp operation.

[0044] The plate 16 also provides one wall of a waveguide 40. The stem 36 of the bulb 34 extends past the waveguide 40 (outside of the waveguide 40, see Fig. 11) and through a motor mount 42. The mount 42 further functions to thermally isolate the motor 38 from the RF assembly. A motor cover 44 covers the motor and protects the motor from environmental hazards and may include a gasket, caulking, epoxy, or other suitable material disposed between the lip 45 of the cover 44 and the waveguide 40 to provide an environmental seal against contaminants. For example, the cover 44 is made from plastic or other suitable material. With the globe 28 and

the cover 44, the lamp is well sealed against environmental hazards such as dust or fumes and the lamp reliability is improved.

[0045] The lamp 10 further includes a magnetron 46 positioned against the waveguide 40. The waveguide 40 provides an opening therethrough to receive the antenna 48 of the magnetron 46. Power is provided to the magnetron 46 and other lamp components by a power supply module 50. The power supply module 50 is supported by brackets 52 which further function to thermally isolate the module 50 from the RF assembly. The lamp 10 provides external access to the power terminal assembly 26 through the cover 16.

[0046] The lamp 10 includes an active cooling system for the magnetron 46 and the power supply module 50. Other than rotation of the bulb, no active cooling is provided inside the sealed environment of the globe 28, the waveguide 40, and the motor cover 44. The cooling system includes a fan 54 and a set of ductwork 56, 58, and 60 positioned between the plate 14 / waveguide 40 and the power supply module 50.

[0047] As shown in detail in Figs. 7-8, the globe 28 has a generally spherical shape, truncated on one side providing an opening in the globe 28 and defining a lip 31. Preferably the globe is large enough to not overheat the screen and / or bulb. A glass globe will tend to absorb or shed infrared (IR) light and not reflect the IR back at the screen or bulb.

[0048] An alternative shape for the secondary envelope is shown in Figs. 9-10. A second envelope 90 has the general shape of a hollow truncated cone which is open on its smaller end and closed on its larger end. The envelope 90 further defines a lip 91 around its open end for mounting the envelope 90 to the lamp 10 and sealing the interior of the envelope 90 against environmental hazards.

Advantageously, the secondary envelope 90 can be adapted to function as a reflector for directing light output from the lamp. For example, either the interior or exterior surface of the envelope 90 can be coated or metalized with reflective material. Depending on the application and the material, either the interior or exterior surface may be preferred. For metal materials, it is generally preferred that the coating is thin so that the coating is transparent to RF energy. However, there may be some applications where it is desired that the metal coating be thick enough to provide secondary RF shielding. Another alternative is a thin metal layer to reflect

light which is substantially transparent to RF and a subsequent outer layer which absorbs RF (e.g. thicker resistive material).

[0049] An alternative secondary envelope includes a metal reflector with a light transmissive cover plate and appropriate environmental seals.

5 **[0050]** With reference to Fig. 11, the RF assembly is shown in cross section. The plate 14 defines an opening therethrough which is the coupling slot 112 where microwave energy is transmitted from the waveguide 40 to the microwave cavity 114. The waveguide 40 defines a shoulder 116 near the slot 112 which improves the matching between the magnetron 46 and the cavity 114 and increases the bandwidth. A capacitive tuning element 142 (see Fig. 14) may further improve the match. The element 142 may be adjustable or may have a fixed location.

[0051] The microwave cavity 114 is defined by the mesh screen 32. According to a present aspect of the invention, the dimensions of the cavity 114 are selected in accordance with material characteristics of the screen to improve the lifetime of the screen, and consequently the reliability of the lamp. For most cost effective, practical materials, the resulting screen has a novel aspect ratio (length of the cylindrical cavity : diameter of the cylindrical cavity) as compared to prior mesh screens used to define the microwave cavity of an electrodeless lamp.

0 **[0052]** In general, the material selected for the mesh screen is a metal or metal alloy. Such materials have quantifiable material qualities including the temperature at which the material degrades. Based on a desired operating temperature of the electrodeless bulb, a minimum distance between the bulb and the screen may be determined to keep the screen at a temperature which is well below the temperature at which the screen material degrades.

5 **[0053]** With reference to Figs. 11-12, a preferred mesh screen 32 has a generally right cylindrical shape with a domed end cap 122. A slight tensioning on the domed portion during assembly helps the screen retain its shape with sagging. A preferred material for the mesh screen is aluminum plated stainless steel. Advantageously, both materials are inexpensive, readily available, and well characterized. For example, the aluminum coating is known to undergo a phase change at 495 °C. The aluminum may be applied to the stainless steel as a flashing, for example by an ion beam vapor deposition (IVD) process. Advantageously, the aluminum plated stainless steel has lower resistance and

higher reflectivity as compared to a stainless steel screen. The aluminum protects the stainless steel from oxidation with a self-healing skin of aluminum oxide.

[0054] For a target bulb temperature of about T °C operating in air, the minimum distance between the bulb the material may be determined (e.g. empirically or mathematically) to be about X mm. Accordingly, for a bulb diameter of $D1$ mm, the diameter of the mesh screen is a minimum of $D = D1 + (2 \times X)$.

[0055] A problem with a larger diameter screen is that the cylindrical cavity will support more than one mode of microwave propagation. In accordance with a present aspect of the invention, a diameter of the cavity is selected in accordance with a minimum distance to reduce thermal stress and a length of the cavity is selected to provide frequency separation from undesired microwave modes. For a 110 mm diameter cylindrical cavity, a preferred length of the cavity is about 81 mm. For these cavity dimensions, a TE₁₁₁ mode is supported at 2450 MHz, while the TM₀₁₀ mode has a resonant frequency of 2090 MHz and the TM₀₁₁ mode has a resonant frequency of 2790 MHz. Advantageously, both of these closest modes are several hundred megahertz separated from the desired mode and the desired mode is roughly centered between the frequencies of the other modes.

[0056] The dimensions are also advantageously greater than the above mentioned minimum distance for thermal stress. Operation of the lamp at 1300 W wall plug power (about 950 W RF power) results in a screen temperature of between about 400 °C and 425 °C, which is well below the maximum stable temperature of the screen material.

[0057] A problem with an instability in the RF assembly has been observed with the preferred microwave cavity of the present invention. Namely, the dynamically varying nature of the electrodeless lamp during startup causes dramatic swings in the magnetron current. In accordance with a present aspect of the invention, this problem is solved by reducing the magnetron filament current immediately after the anode startup.

[0058] With reference to Figs. 13-14, respective cut-away perspective views show the paths of cooling air (represented with arrows) for the example lamp of the present invention. The duct 58 divides the airflow into to channels, one past the magnetron 46 and the other past the power supply module 50. The module 50 includes a finned heatsink 144 and the duct 58 provides a shroud 146 over the

finned heatsink to define the air flow channel. As can be seen in Fig. 14, the cover 44 keeps contaminants in the cooling air out of the motor assembly.

[0059] With reference to Figs. 15-17, representative performance graphs for the lamp of the present invention. At about 1300 W of wall plug power, the lamp produces about 120,000 lumens light output, corresponding to an efficiency of about 94 lumens per watt of wall plug power. With respect to RF power (i.e. not counting power supply or magnetron losses), the efficiency rating is of course much higher. A representative light output spectrum is shown in Fig. 17.

[0060] With reference to Fig. 18, another aspect of the present invention relates to provide relatively more directional light output without a dielectric mirror inside the microwave cavity. As can be seen in Figs. 11 and 14, the lamp 10 includes an angled reflector 118 at the base of the microwave cavity. The reflector 118 does not interfere with the microwave mode and is made from metal. The outer wall of the reflector conveniently provides a surface for clamping the fingers of the mesh screen to hold the screen in place. The inside surface of the reflector 118 may be polished, anodized, or otherwise treated to increase the reflectivity of the reflector 118. The inside surface of the plate 14 may likewise be polished or otherwise treated to improve its reflectivity. As shown in Fig. 11, the reflector 118 may cooperate with an external reflector to further control the light output. The graph in Fig. 18 shows a comparison of the relative directivity of the reflector 118 of the present invention versus a cylindrical mesh cavity utilizing a flat dichroic mirror.

[0061] If desirable, a dielectric mirror may be positioned in or over the coupling slot to avoid light loss in the slot. According to a present aspect of the invention, a dielectric mirror is positioned over the inside surface of the plate 14 (including the slot) to reflect light and also to absorb IR to reduce the thermal load on the screen. This configuration may be particularly useful in a down light application because the bulb tends to runs hotter at the highest point of the bulb (with respect to the floor or ground).

Interleaved Power Factor Correction Circuit

[0062] A PFC circuit is utilized to condition an input power signal and provide a more desirably shaped (e.g. less distorted) input power signal by reducing current peaks on the input conductors. Universal line input refers to the ability to operate on

more than one and preferably many of the different power line voltages available around the world.

[0063] One known electrical operating technique for PFC converters is discontinuous-current-mode (DCM) operation. Another technique is referred to as continuous-current-mode (CCM) operation. Critical mode operation is a technique (with respect to the PFC inductors) where the converter is operating with a triangular input current in the region between discontinuous and continuous mode. The benefit of the critical mode technique is that zero-current switching of the PFC-transistor is obtained with high efficiency and reliability. Zero current switching is obtained because the PFC-transistor does not turn-on until the current in the PFC-inductor and the PFC-diode is zero, thereby preventing the flow of recovery current. Several manufacturers of integrated circuits have commercially available control chips targeted for implementing DCM and / or critical mode operation for PFC circuits.

[0064] One example of an interleaved PFC circuit is described in the technical paper entitled "Evaluation of Input Current in the Critical Mode Boost PFC Converter for Distributed Power Systems", by J. Zhang, J. Shao, P.Xu, F. Lee and M. Jovanovic, Center for Power Electronics Systems, pp.27-34, 2000 CPES Power Electronic Seminar Proceedings, September 17-19, 2000.

[0065] An electronic power conversion system is described in U.S. Patent No. 5,892,352, entitled "Synchronization Of The Switching Action Of Hysteresis Current Controlled Parallel Connected Power Electronics Systems".

[0066] Another example of an interleaved PFC circuit is described in U.S. Patent No. 6,091,233, entitled "Interleaved Zero Current Switching in a Power Factor Correction Boost Converter".

[0067] A typical interleaved PFC circuit configuration is shown in Fig. 1A. An input signal I is provided to a master circuit A and a slave circuit B. Operation of the master circuit A is not dependent on operation of the slave circuit B. Operation of the slave circuit B is at least partially dependent on the operation of the master circuit A. For example, as illustrated, a delay circuit D is connected between the master circuit A and the slave circuit B, with the master circuit A providing a signal to the delay circuit D which in turn provides a signal to the slave circuit B. Outputs from the two circuits A and B are combined to provide a conditioned output signal O. An

error signal E is fed back to the converters A and B to adjust the operation of the circuit.

[0068] As illustrated, the timing control of the PFC circuit is uni-directional from the master circuit A to the slave circuit B. For example, in operation the master circuit A measures the PFC-voltage or current and tries to maintain its output at a constant level. The delay circuit D includes a phase shifter which is synchronized to the gate signal of the master circuit A, and provides a 180-degree delay to a stop signal going to the slave circuit B. If the operation of the two circuits A and B is 180 degrees out-of-phase with respect to each other the overall ripple is reduced on the input and the output because when the circuits switch the ripple does not sum up.

[0069] In general a PFC is utilized to reduce high current peaks in the input line and provide an input power signal to downstream electronics having a shape which is closer to a sinusoid. Most PFC circuits work by sensing the current in an inductor. When the current is determined to be zero, one side of an interleaved PFC circuit is triggered by closing a switch to apply power through the PFC inductor to charge up the PFC capacitor. In general the input signal to a PFC stage is sinusoidal and the output of the PFC stage is a well regulated DC signal (with some ripple). The DC output can be passed to any desirable subsequent power supply stage (e.g. a buck or a boost). The operation of each of the two sides of the interleaved PFC stage operates affects the amount of ripple, the efficiency, and the reliability. The effectiveness of the switching operation primarily determines the efficiency and the reliability. For example, a voltage superimposed on the switch before the switch is closed may cause a current spike which lead to reliability problems.

[0070] For interleaved PFC stages, particularly in order to maintain the benefit of universal line input, the switching of the two sides is ideally 180 degrees out of phase with respect to each other. The two sides are frequency modulated with the particular switching frequency adjusted in accordance with the level of the mains signal. Generally, the two sides operate with longer pulses near peaks of the input signal and shorter pulses near zero crossings of the input signals.

[0071] One problem with many conventional PFC circuits using DCM techniques is that at higher power levels (e.g. 300W - 2kW) the triangular input current requires a large and expensive mains filter. A particular problem with circuits topologies similar to that shown in Fig. 1A is providing a delay circuit which provides

accurate phase shift over all the circuit conditions required. A further problem is that variations in component tolerances, particularly the PFC-inductors, may negatively influence the operation of the circuit.

[0072] With reference to Fig. 1A, practical implementations of the PFC circuit exhibit problems for universal line input applications with higher power loading levels. In order to maintain critical mode operation over a wide input operating voltage range, the phase shifter must be accurate over a wide span of frequencies which in practice is difficult to implement. In addition, manufacturing tolerances in the PFC-inductors may cause the inductor values to differ by ten percent or more, at which point zero voltage switching is not achieved. Switching which occurs when operating in continuous mode may cause current spikes which results in reduced efficiency and poor reliability.

[0073] In other words, when the period of operation of the master is shifted other than 180° with respect to the period of operation of the slave, the slave circuit switches at a sub-optimum time. Under these conditions, it is possible that the switching occurs before the current in the diode is zero, thereby causing spikes and stressing the components. Practical implementations may also require a protection circuit due to the possibility of temporary operation in CCM.

[0074] In contrast to the prior art, one aspect of the present invention relates to a PFC stage in which tolerance variations in the PFC inductors may lead to slightly more ripple, but the timing of the switching remains correct. For example, the present invention solves the timing problem by using a shared timing control circuit which inhibits phase shift error and provides no open loop for either portion of the interleaved circuit. Advantageously, even if the amplitude of the inductor currents are slightly different due to tolerance variations the PFC stage operates in critical mode or DCM mode. Accordingly, efficiency and reliability are maintained over a wider range of operating conditions.

[0075] At higher loads, the applicants have also observed in master/slave-type PFC circuits that the slave converter exhibits a sub-frequency oscillation, because there is usually no feedback control signal of the current (sense). The circuit may, with an increased load, lock to a situation with alternating higher and lower current peaks. This is a stable but non-desirable situation where the timing is correct but the current is not. One possible solution to this problem is to add current control to the slave. However, that solution adds components and complexity to the

circuit. Even with current control of the slave, problems remain with respect to manufacturing tolerances and providing an accurate 180° phase shift for universal line input.

[0076] According to a present aspect of the invention, an interleaved PFC circuit utilizes a topology in which neither converter is master or slave. With reference to Fig. 2A, an interleaved PFC circuit 20 includes a first converter A and a second converted B which receive a common input signal I. A timing circuit X is shared between the two converters A and B. The first converter A provides a signal to the timing circuit X and receives a signal from the timing circuit X. Operation of the first converter A is at least partially dependent on the signal it receives from the timing circuit X. The second converter B also provides a signal to the timing circuit X and receives a signal from the timing circuit X. Operation of the second converter B is at least partially dependent on the signal it receives from the timing circuit X. Both converters A and B receive an error signal E. The output from both converters A and B is combined to provide a conditioned output signal O.

[0077] Because the timing circuit X is shared between the two converters A and B, the period of operation of both converters is the same. The PFC circuit is tolerant of manufacturing variations affecting the timing circuit X because such variations are applied equally to both converters A and B. More importantly, the phase shift is accurate under a wide range of operating conditions because the timing circuit X turns off the converter A at the same time it turns on the converter B (and vice versa). Accordingly, there can be no overlap in operation of the two converter stages.

[0078] The converters A and B are configured as two co-equal circuits with a bi-directional timing circuit X controlling the operation of both sides. The novel topology is applicable for all power levels, although it may find particularly beneficial application in the medium power range of 300 W - 2kW. The novel topology is applicable to various regulation control modes including but not limited to voltage, current, and hysteresis.

[0079] With reference to Fig. 3A, a novel timing circuit includes a memory circuit X1, an integrator X2, and a sign detect circuit X3. The memory circuit X1 receives respective signals from both converters A and B and provides an output signal to the integrator X2. The integrator X2 provides a signal to the sign detect

circuit X3 which provides respective signals to both converters A and B. The other circuit connections are as described above with respect to Fig. 2A.

[0080] Operation of the circuit is generally as follows. The two converters A and B work in a desired control mode of, for example, current control or time control.

5 The memory circuit X1 holds a value corresponding to which converter (A or B) operated during the preceding period. The integrator X2 is configured with a suitable time range corresponding to the working frequency of the converter and produces either an increasing or decreasing output in accordance with the signal from the memory circuit X1. The sign detect circuit X3 senses the polarity of the
0 output of the integrator X2 and provides respective signals (e.g. complementary signals) to the converters A and B indicating which of the two converters should operate.

[0081] The memory circuit X1 has an initial value. For example the value is a logical 0 or a logical 1 corresponding to an appropriate output voltage (e.g. zero volts
5 or five volts). The value of the memory circuit X1 is provided to the integrator X2.

The integrator generates a ramp signal which has either a positive slope or a negative slope in accordance with the value of the memory circuit X1. The ramp signal from the integrator X2 is provided to the sign detect circuit X3. The sign detect circuit X3 compares the ramp signal to a reference value. When the ramp
0 signal crosses the reference value the circuit X3 substantially simultaneously provides a "go" signal to one converter and a "stop" signal to the other converter in accordance with the direction of the ramp signal. The converter which received the "go" signal provides a signal to the memory circuit X1 which causes the value of the memory circuit X1 to toggle.

5 **[0082]** With reference to Fig. 4A, a first example PFC circuit 40 includes a first control chip A1 and a second control chip B2 which receive the input signal I1 (e.g. the current sense or output voltage) through respective conditioning components (e.g. resistor R1 / capacitor C1 and resistor R2 / capacitor C2) to a buffer or inverter.

0 The first control chip A1 provides a gate signal A to a gate of a transistor M1. The source of the transistor M1 is grounded and the drain of the transistor M1 is connected to one terminal of a PFC inductor L1 and also to a cathode of a PFC diode D1. A second control chip B2 provides a gate signal B to a gate of a transistor M2. The source of the transistor M2 is grounded and the drain of the transistor M2 is connected to one terminal of a PFC inductor L2 and also to a cathode of a PFC

diode D2. The respective other ends of the PFC inductors L1 and L2 are tied in common and provide the input voltage of the circuit. The anode ends of the PFC diodes D1 and D2 are tied in common (the output) and connected to one terminal of a PFC capacitor C6. The other terminal of the PFC capacitor C6 is grounded.

5 **[0083]** The PFC circuit 40 further includes a timing control circuit shared between the two stages. The timing control circuit includes a toggle flip flop X1 which receives respective toggle signal from the two gate signal lines via respective capacitors C4 and C5. The output signal C of the flip flop X1 is provided to a negative input terminal of an integrator X2 (e.g. comprising a comparator) via a resistor R3. The positive terminal of the integrator is connected to a reference voltage V_{REF1} and the output of the integrator X2 is fed back to the negative input terminal of the integrator X2 via a capacitor C3. The output signal D of the integrator X2 is provided to a sign detect circuit X3 (e.g. comprising an operational amplifier) at the negative input terminal of the circuit X3. The positive terminal of the circuit X3 is connected to a reference voltage V_{REF2} . The output signal E of the sign detect circuit is provided to the first control chip A1 and through an inverter X5 to the second control chip B2.

[0084] The PFC circuit 40 further includes additional logic elements which determine when the two stages may operate. Specifically, the output of the sign detect circuit X3 is combined with respective zero signals from the two stages to ensure that zero current switching is obtained. The non-inverted output of the circuit X3 is provided to a logical NAND circuit X4 and a zero signal Z1 from the first stage is provided to another input of the NAND circuit X4. The output of the NAND circuit X4 is provided to the control chip A1. The inverted output signal F of the circuit X5 is provided to a logical NAND circuit X6 and a zero signal Z2 from the second stage is provided to another input of the NAND circuit X6. The output signal G of the NAND circuit X6 is provided to the control chip B2.

[0085] The general operation of the PFC circuit 40 is as follows. The two control chips A1 and B2 work with a controlled current limit or controlled ON-time corresponding to a feedback signal sensing the PFC-voltage output. The controllers have zero signal control inputs sensing when the current through the PFC-diodes, for each period, has stopped entirely. The memory circuit is the flip-flop X1 that remembers which half of the circuit that produced the last positive going output gate-pulse signal. The integrator X2 is attached to the flip-flop and generates a suitable

time range for the working frequency of the converter. The sign detect circuit X3 senses the polarity of the output of the integrator X2, and has two complementary outputs (one via the inverter X5). For example, reference voltage for the sign detect circuit is 2.5 V if the memory value is either 0 V or 5 V. The logic circuits (X4 and X6) logically combine the zero current signals (Z1 and Z2) of each converter with respective outputs from the sign detector X3 before permitting the respective PFC-control circuit A1 or B2 to start a new period.

[0086] The integrator X2 output generates a delayed "clear-to-go" gate-signal to the respective PFC-controller after the flip-flop X1 has toggled. A new period can start for a converter side when the "clear to go" is in the appropriate state for that side and the zero signal is indicating zero current. The delay function will automatically force the other side to wait if the first side is delayed due to component difference, passive or active. The present invention facilitates 180-degree phase shift for a wide range of frequencies as this phase information is delayed and passed in both directions the same way.

[0087] Any frequency dependent extra delay will be the same both ways, thus symmetry is maintained. This is important as the working frequency varies over a large span, from a low frequency (for example, 40-100kHz in practice with present technology) when the mains voltage is momentarily high until the point where the mains voltage is momentarily close to zero where the frequency can go very high (for example, > 400kHz). The circuit will, if PFC-controllers A1 and B2 are configured with controlled ON-time, give a final dead-time on one of the channels that depends only on possible tolerance variations in the ON-time between the two circuits. The converter side with the longest ON-time will always have minimum dead time.

Variations in the PFC-inductor values will not adversely affect the function of the circuit.

[0088] With reference to Fig. 5A, represent signal waveforms are illustrated for signals A-G, I/L2 and Z2. The signal A is the gate signal to the transistor M2. Signal A goes high at time T0 (Based on the output signal C of the flip flop X1). The duration of the pulse for the signal A depends on the mains voltage and the power level. However the duration of the pulse is not critical to the timing of the circuit because the flip flop X1 is edge triggered. The waveform I/L2 is representative of current flowing through the inductor L2. The current in the inductor L2 increases when the transistor M2 is conducting.

[0089] The signal C is representative of the actual status of the output of the flip flop X1. The output signal C toggles with the rising edge of the signal A and toggles again with the rising edge of the signal B. The output signal D of the integrator X2 starts to go negative at time T0 as a result of the flip flop changing. The output signal E of the comparator X3 goes high when the integrator output signal D goes under the reference level at time T1. The signal E and its complement are substantially simultaneously provided to the two control chips A1 and B1, via additional control logic circuits X4 and X6.

[0090] In this cycle, at time T1, the comparator output E goes from low to high, thus providing a "clear to go" signal on the inverted output signal F for control circuit B1. The control circuit B1 then awaits the arrival of a low signal Z2. The signal Z2 goes low when the inductor L1 has fully released its energy to capacitor C6 via diode D1. The signal Z2 returns to zero at time T1 thus making the signal G go low and enabling the control circuit B1.

[0091] The signal B goes high at time T2 thus causing the transistor M1 to conduct. The operation of the circuit repeats in a symmetrical manner from this point in time with the B side of the circuit instead of the A side of the circuit. The current through L2 starts to increase, the flip flop toggles back to the state before time T0, and the integrator starts to increase its output voltage. When the integrator crosses the reference voltage, one side of X4 is enabled and the control circuit A1 awaits the signal Z1 becoming low.

[0092] From the foregoing it is apparent that both control circuits A1 and B1 are gated by the integrator X2 output and the zero current signals Z1 and Z2. Both signals must be in the appropriate state before switching control. If one side is late in starting due to a late arriving zero signal, then the other side will automatically be delayed a time corresponding to a 180 degree phase shift due to the symmetry of the integrator.

[0093] In the timing diagram as illustrated, the circuit provides headroom between the transition of the signal E and the corresponding zero signal Z1 and Z2. In practical circuits, however, component tolerances may alter the precise symmetry of operation with respect to the zero signals, and one side may have little or no headroom as compared to the other side. An advantage of the circuit is that, even with component tolerance variations, symmetry in time is maintained because the

zero signal is utilized together with the integrator X2 output to activate the next control side of the converter.

[0094] When one half of the circuit stops due to PFC-voltage reaching an upper limit then the other side will stop automatically. In other words, one side cannot operate on its own.

[0095] It is understood that the current sharing may become unbalanced with the effect that the total ripple will increase. However, the amount of ripple is well within acceptable limits, particularly for the advantages provided relating to improved efficiency and reliability.

[0096] Practical circuits may be configured for operation with mains signals from DC to 80 Hz. DC operation makes the interleaved PFC boost converter of the present invention suitable for backup battery power.

[0097] In conventional PFC stages, the PFC capacitor may be life-limiting. The present invention reduces electrical stress on the PFC capacitor, thereby reducing requirements.

[0098] A preferred PFC circuit in accordance with the invention incorporates the following features:

[0099] 1) Interleaved operation with two PFC-inductors and two PFC control chips for higher power operating levels;

[0100] 2) On-time control of both halves of the PFC circuit;

[0101] 3) A shared timing circuit;

[0102] 4) Critical mode operation of the PFC control chips for reliability;

[0103] 5) Critical mode operation for both PFC inductors; and

[0104] 6) Tolerance of a slight amount of DCM operation of one of the circuits.

[0105] Utilising on-time control of the PFC stages reduces or eliminates the effect that manufacturing variations in the PFC inductor values have on the timing and phase-shift between the two channels. The shared timing circuit provides 180-degree phase shift between the two converter's timing for reduced ripple. As noted above, the timing circuit is shared to provide symmetry of the function. The phase information between the two converters is bi-directional in order to get 180-degree phase shift under a wide range of conditions while inhibiting any phase disturbances.

[0106] One stage is always operated in critical mode. The other stage generally operates in the critical mode, but may operate in DCM. DCM is as efficient as CCM and more reliable as compared to CCM.

[0107] There are many practical ways to implement the operating principles mentioned above. The circuit described in Fig. 6A is one example which is simple and does not require a conventional analog amplifier and comparator. It is built with a flip-flop and four high-speed transistors, Q1-Q4, and one integrator (resistors R5, R6 and capacitor C3). The NAND-ing function is implemented by holding respective zero inputs of the PFC-control chips high via Q3 or Q4, thus stopping a new cycle from starting, until the integrator output allows the respective control circuit to re-trigger. (The zero signal is low when the PFC-inductor current is zero)

[0108] The two PFC-controllers operating in critical-mode can basically work according to two dominating techniques. Namely, controlling the on-time or controlling the current.

[0109] Controlling the on-time is an example of a technique used by the TI/Unitrode chip UC3852. The chip uses a constant ON-time set by an error amplifier with respect to the mains frequency. The chip provides a sine-shaped mains current with a high power factor as $I=V \cdot dt/L$. The chip does not control the peak current normally, except for setting an upper limit. However the circuit senses the current at a low minimum level to determine when to turn on the PFC-transistor each cycle.

[0110] These integrated circuits exhibit excellent part to part tolerance. Therefore the RC-link needed by the chip is the predominating source of error.

[0111] A SG-Thomson integrated circuit having part number L6561 uses an example of a technique which involves controlling the current. In this chip, a multiplier having the input from a divider sensing the input voltage and the error amplifier controls the envelope of the peak current. The result will in the end be more or less the same as in the case outlined above, namely the ON-time will be constant over the mains period.

[0112] An advantage of this circuit is the way the circuit determines when to start the next pulse. A zero detector input senses when the voltage reverses over the PFC-inductor. This can only happen after the current through the PFC-diode has stopped entirely. Accordingly, the circuit prevents any recovery current at all.

[0113] The two methods mentioned above treats variations in component values in a different way. Variations in controlling the ON-time will give a variation in peak current but the period time will always stay constant even if the PFC-inductor changes. Controlling the peak current on the other hand is not possible if the period

time has to be the same with different inductor values. At least not if the current is the same for both PFC-circuits.

[0114] It was, as a remainder, for this reason already above concluded that only controlled ON-time would work well. The only really important thing that matters in a topology with controlled ON-time is the difference in the pulse-width of the two converters.

[0115] With reference to Fig. 7A, another aspect of the present invention is based on the L6561 for following reasons. The temperature range and input tolerance of this circuit is very good. The way the controller is re-triggered has attributes which are suitable for implementation of the present invention. The present design incorporates aspects from both circuits above. The present L6561 circuit works primarily with a multiplier for current control thus giving almost constant ON-time but otherwise uses its normal basic functions. An extra external error amplifier circuit is utilized instead of the internal error amplifier. The internal error amplifier is utilized as a comparator.

[0116] Both controllers (A and B) have 6 - IO:s with following functions:

[0117] 1 - Not shown here is the multiplier input to the both controllers A and B with a resistive divider from the rectified mains.

[0118] 2 - The inverter input is for the internal error amplifier. This amplifier has an internal reference of 2.5 V at the non-inverting input.

[0119] 3 (EA) – The error amplifier output is limited to a desired voltage (e.g. 3-4V) by two diodes.

[0120] 4 (Z) – The zero current detection input. Will activate the circuit whenever a low is sensed after a pulse has been generated.

[0121] 5 (I) – The current sense input. This input is used, but not the nominal way, as it is the length of the pulse that terminates the current.

[0122] 6 - Finally, there is a gate output driving the external FET:s. This output synchronizes the timing capacitors C4 and C5 when the signal respectively goes low.

[0123] The on-time control is made possible by having the PFC-controller output discharging a capacitor (C4 and C5) when the PFC-transistor is off. The same capacitors will start to charge at a rate set by the error amplifier X5 output level when a pulse has once started. This charging will continue until the voltage level on the respective capacitor has reached a level of 2.5 V where, in this case, the built in error amplifier of L6561 acts as a comparator. The EA output of L6561 starts

to go low, and as this output level controls the current, the pulse will be terminated when the set value corresponds to the actual current.

[0124] Both circuits will stop entirely when the PFC-voltage is high enough that the dividers formed by R14-R15 and R17-R18 hold respectively timing capacitor permanently charged to 2.5 V. There might be a slight difference of this level between the two circuits due to normal component tolerances. This does not matter, as the integrator with the following AND-gates will not permit one circuit to operate on its own. This is the process that will take over when the mains voltage reaches a peak operating voltage. Both circuits will stop whenever the peak mains voltage is higher than the PFC-capacitor.

[0125] With reference to Figs. 8A and 9A, representative performance graphs of the interleaved PFC circuit of the present invention show the PFC voltage and the PFC coefficient over a range of input voltages. Based on actual hardware tests, examples of the PFC circuit of the present invention generate excellent PFC voltage regulation over a wide input voltage range (see Fig. 8A). The PFC coefficient is maintained at greater than or equal to 0.99 for most of the input range, trailing off slightly at the upper ranges (see Fig. 9A).

[0126] While the invention has been described in connection with what is presently considered to be the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the inventions.

CLAIMS

What is claimed is:

- 5
1. A microwave electrodeless lamp, comprising:
an electrodeless bulb enclosing a light generating fill;
a mesh screen surrounding the bulb with at least half the bulb volume
completely within the mesh; the mesh together with other conductive surface
0 defining a microwave cavity;
a magnetron for providing microwave energy; and
a waveguide for transmitting the microwave energy from the
magnetron to the microwave cavity,
wherein the minimum distance between the outer bulb surface and the
5 closest portion of the mesh is selected in accordance with the temperature of the
bulb during operation and the temperature at which the screen material degrades.
 2. The lamp as recited in claim 1, wherein the length of the microwave
cavity is selected in accordance with a length which provides a desired microwave
0 mode in the cavity for the selected minimum distance and also provides significant
frequency separation from undesired modes.
 3. The lamp as recited in claim 1, wherein the mesh is a cylindrical mesh
made from aluminum plated stainless steel.
5
 4. The lamp as recited in claim 1, further comprising:
a reflector made from conductive material forming one wall of the
microwave cavity.
 - 0 5. A microwave electrodeless lamp, comprising:
an electrodeless bulb enclosing a light generating fill;
a conductive structure defining a microwave cavity;
a magnetron for providing microwave energy; and

a waveguide for transmitting the microwave energy from the magnetron to the microwave cavity,
wherein the magnetron filament current is temporarily reduced after the anode starts.

6. An interleaved power factor correction boost converter, comprising:
a first converter;
a second converter configured to operate in conjunction with the first converter; and

a timing circuit connected to both the first converter and the second converter, wherein timing information is shared between the first converter and the second converter.

7. The circuit as recited in claim 6, wherein the timing circuit provides substantially simultaneous go and stop signals respectively to the first and second converters.

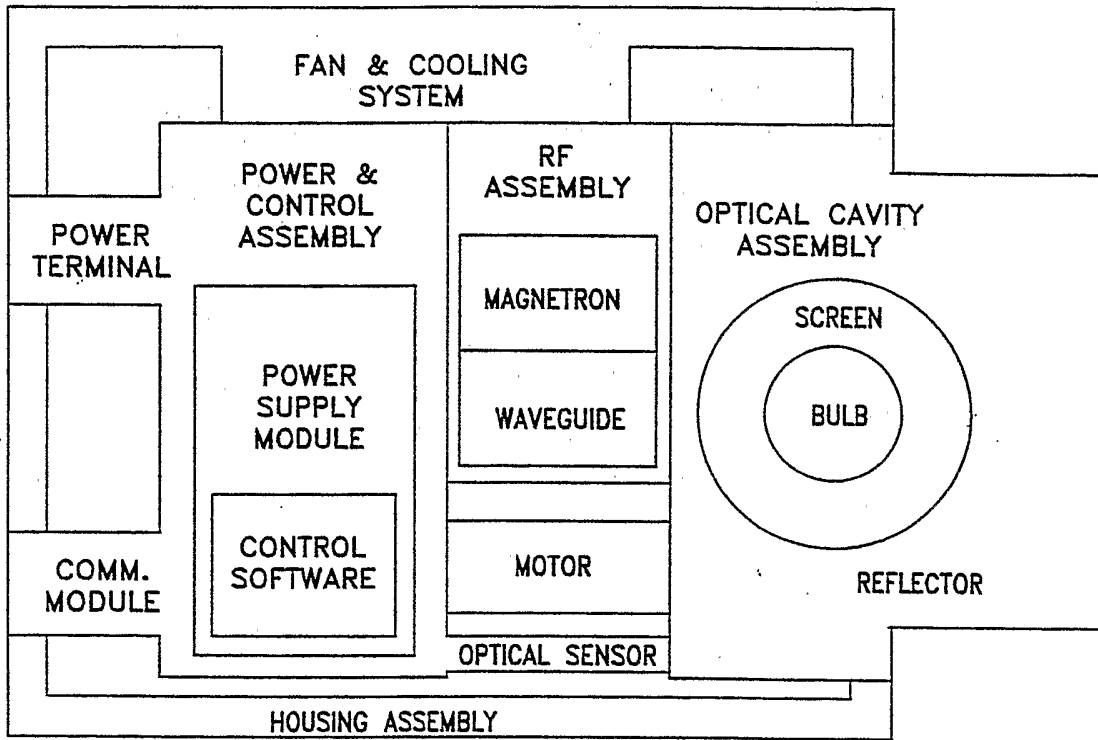


Fig. 1

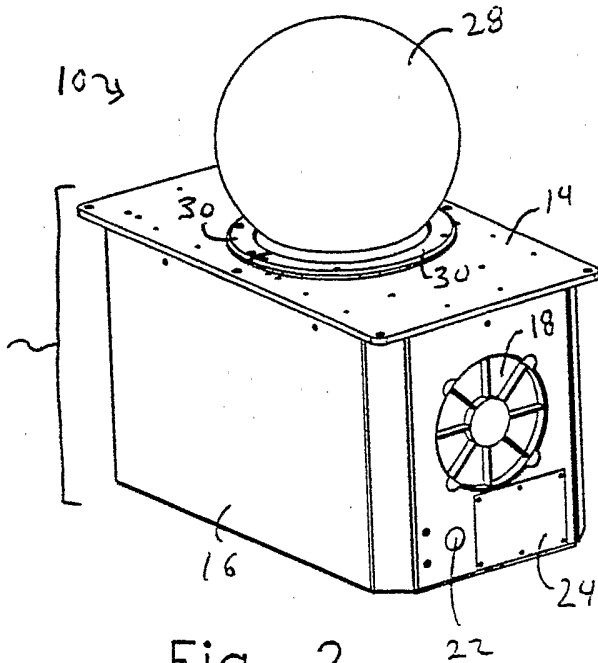


Fig. 2

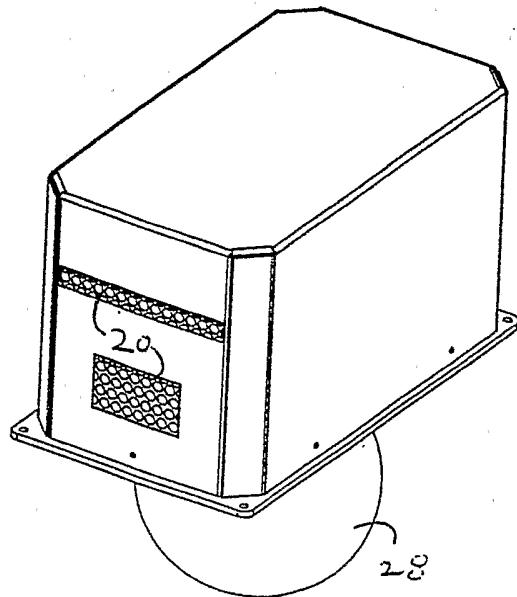


Fig. 3

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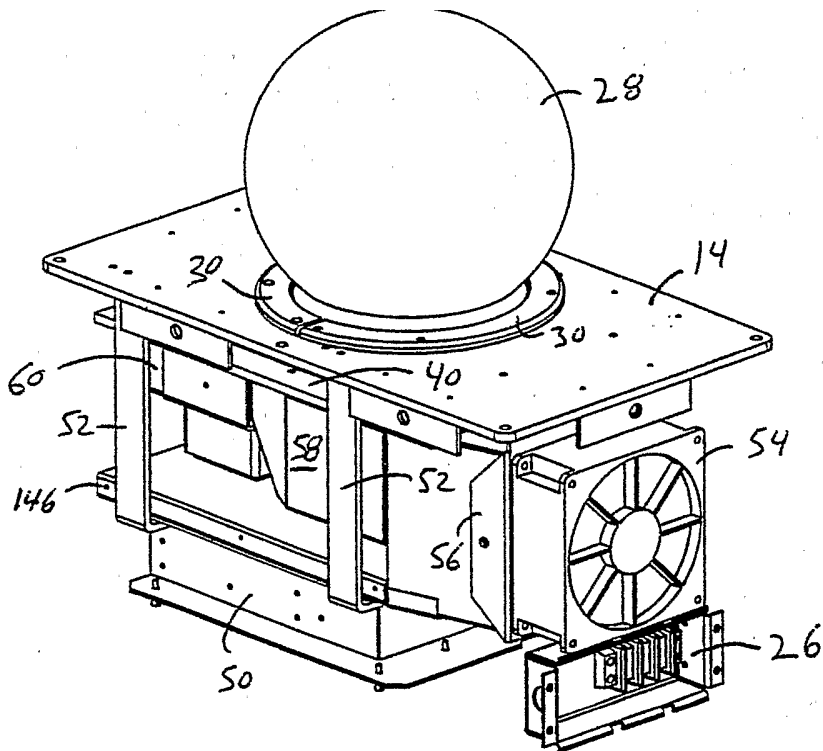


Fig. 4

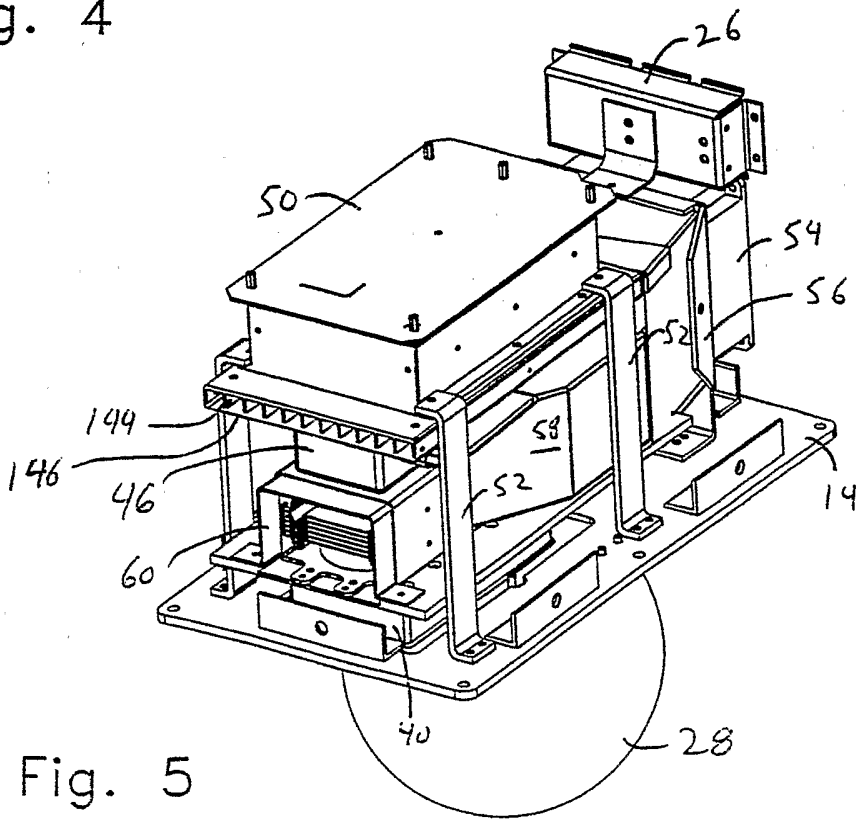


Fig. 5

3/17

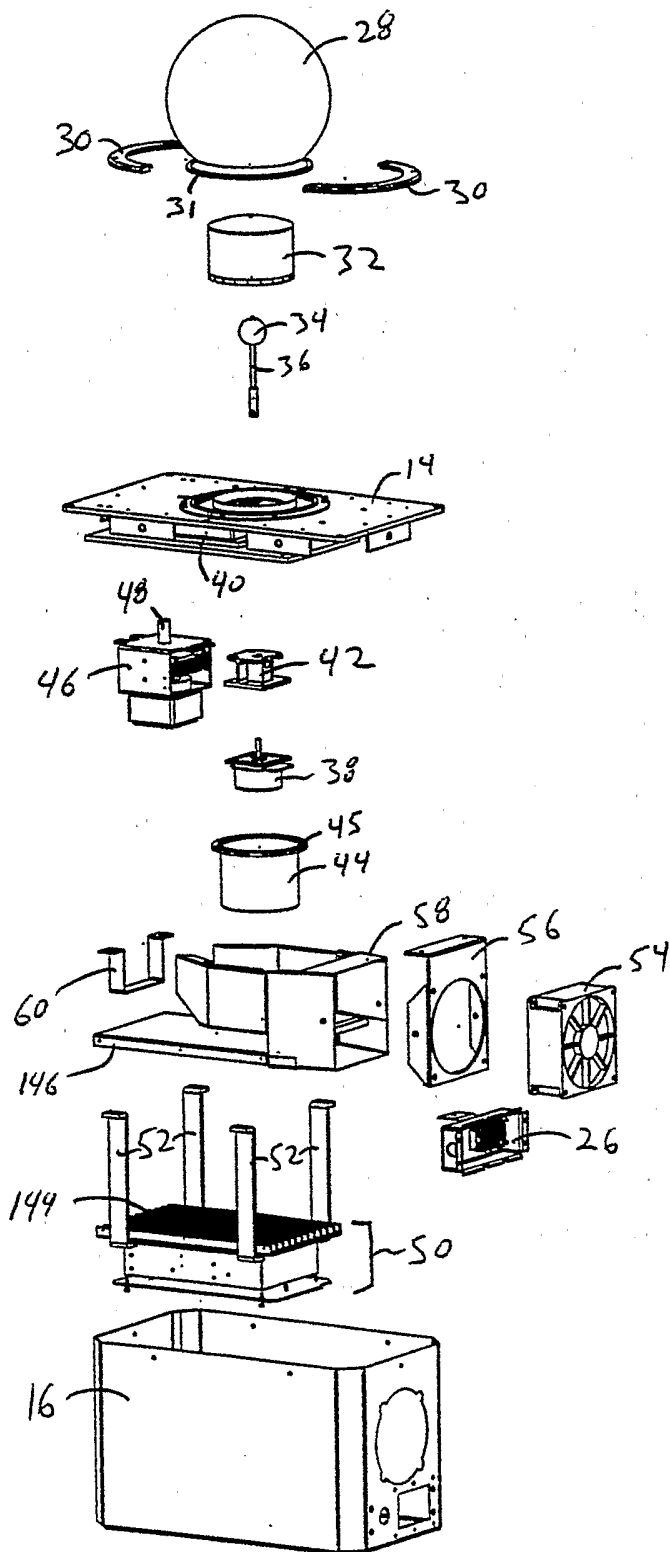


Fig. 6

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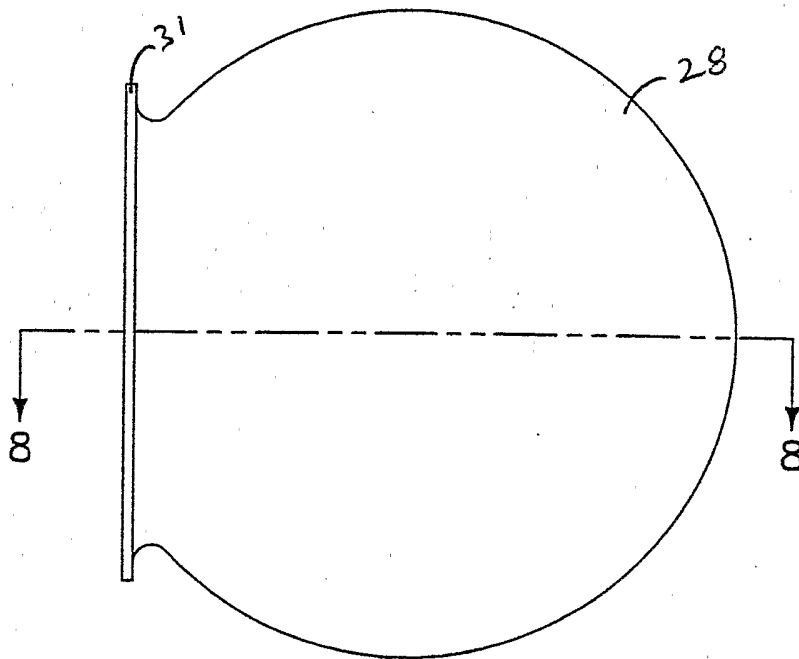


Fig. 7

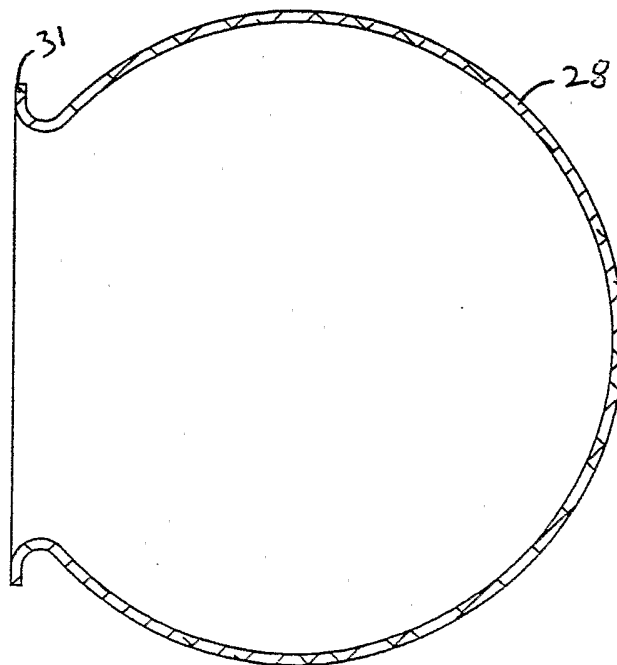


Fig. 8

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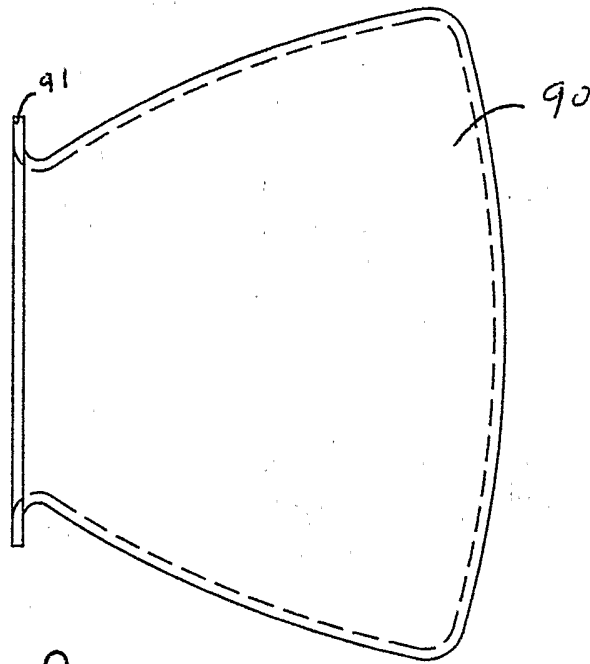


Fig. 9

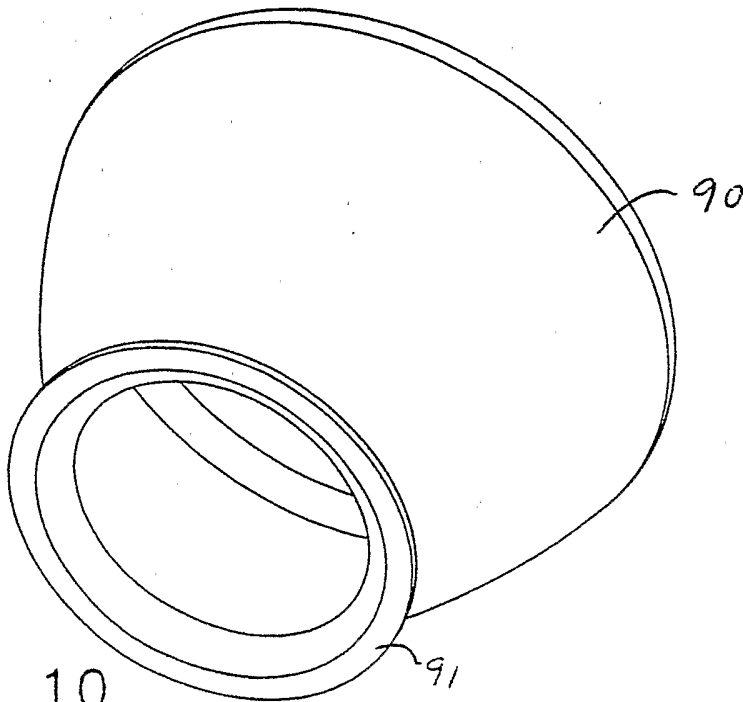


Fig. 10

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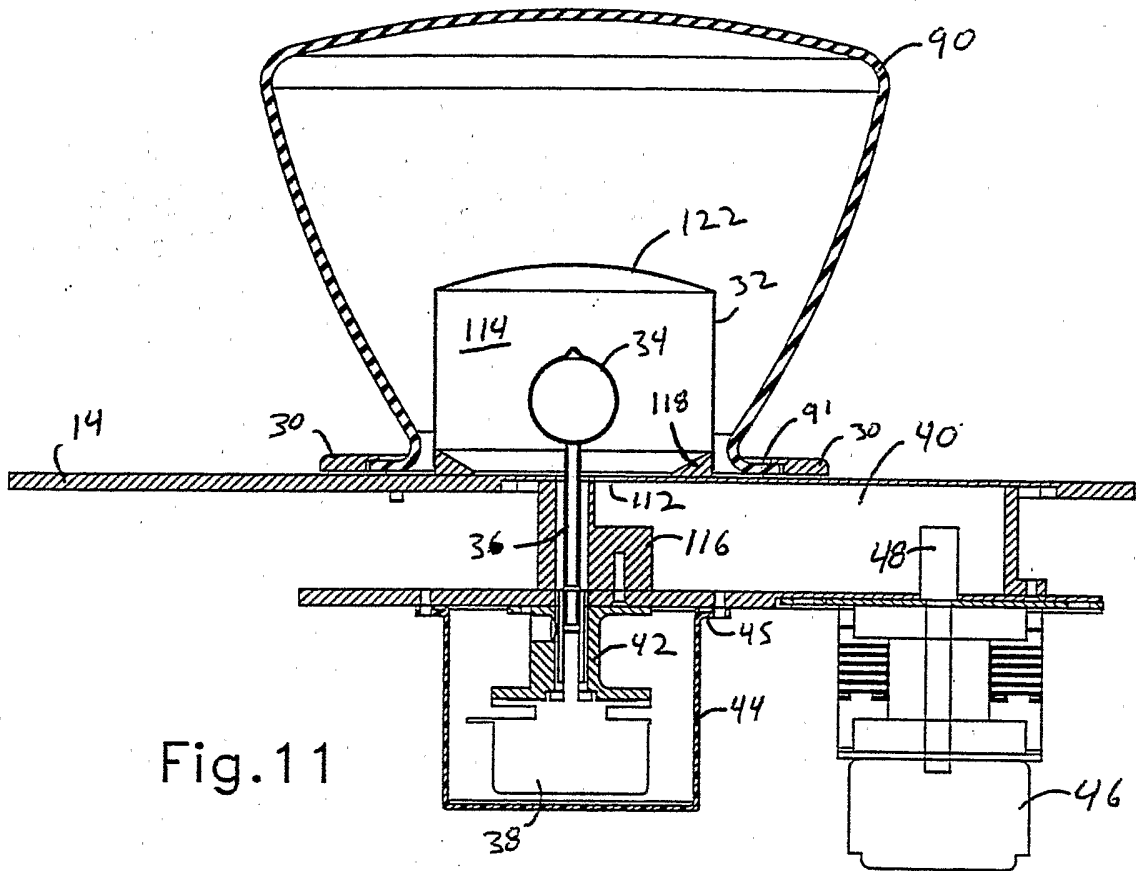


Fig. 11

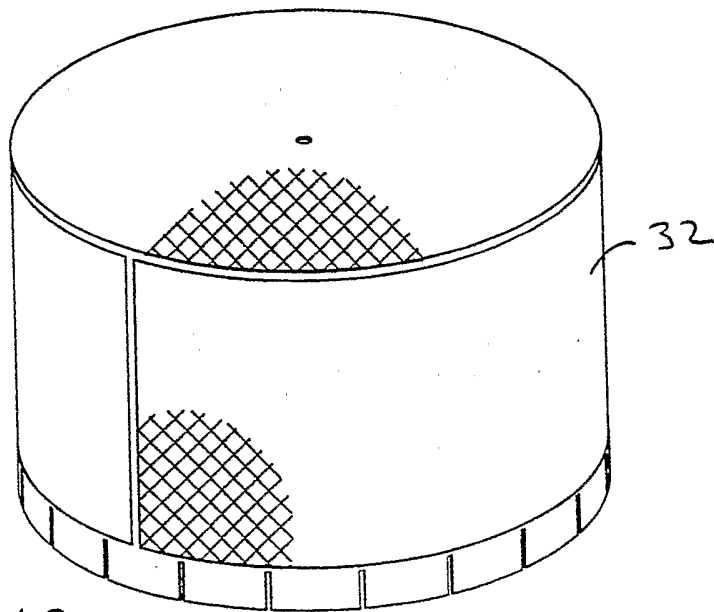


Fig. 12

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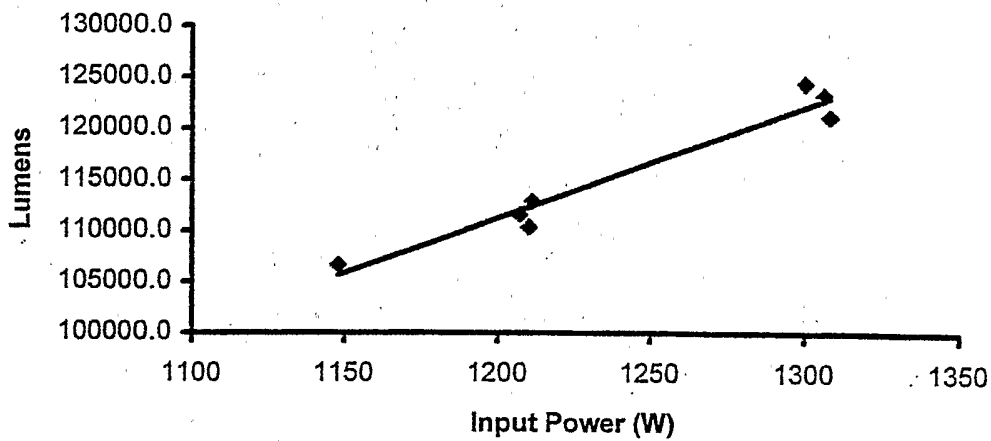


Fig. 15

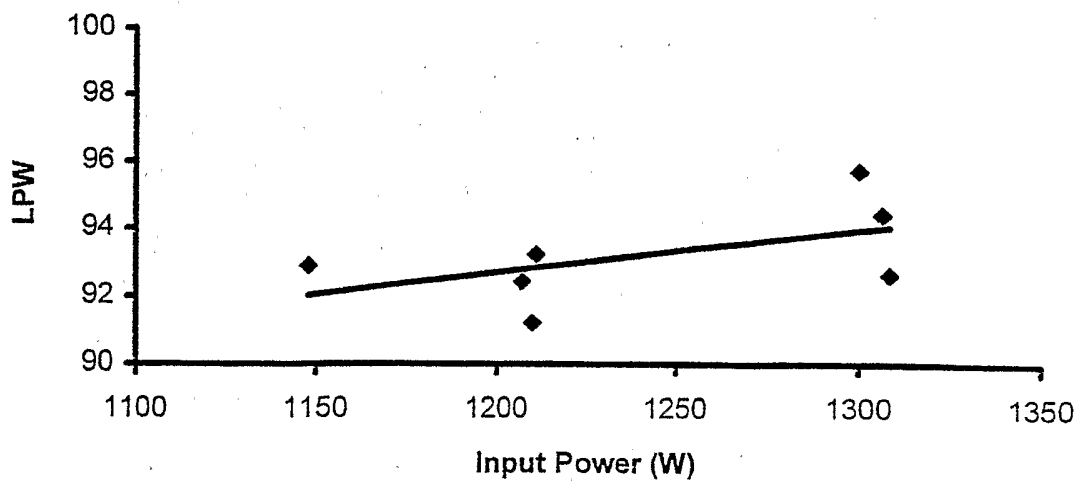


Fig. 16

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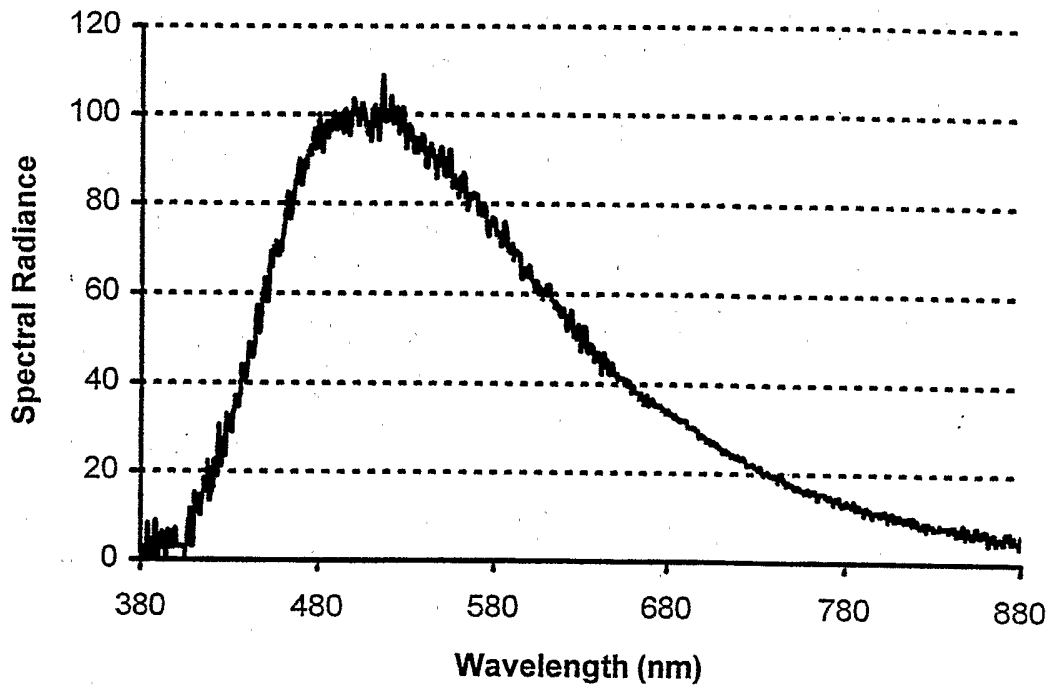


Fig. 17

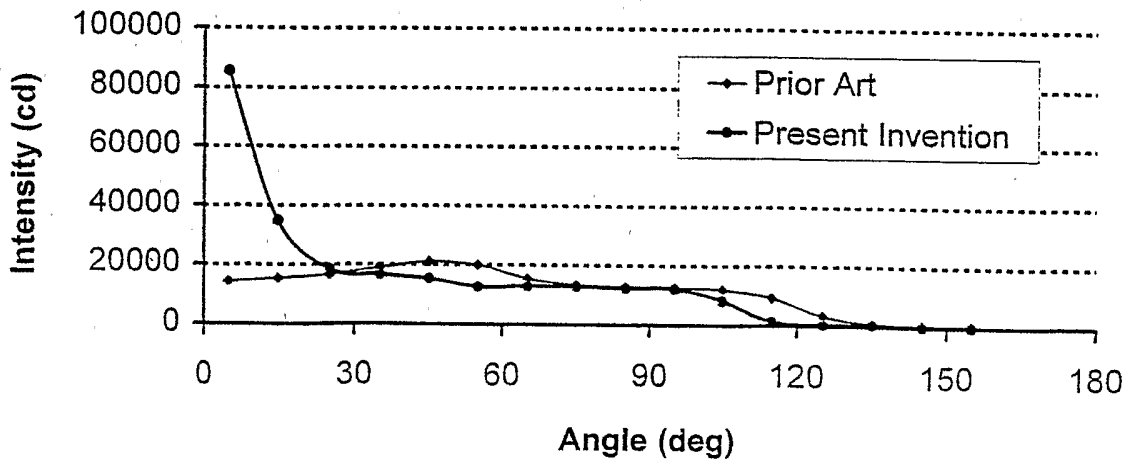


Fig. 18

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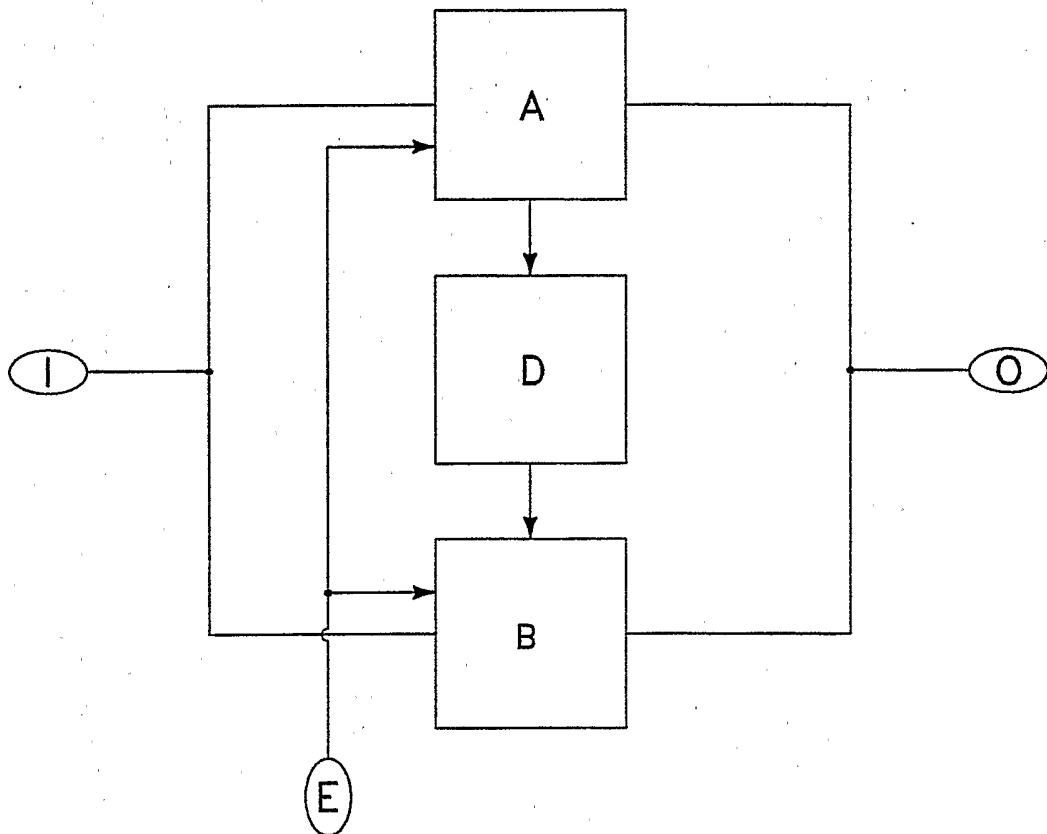


Fig. 1A

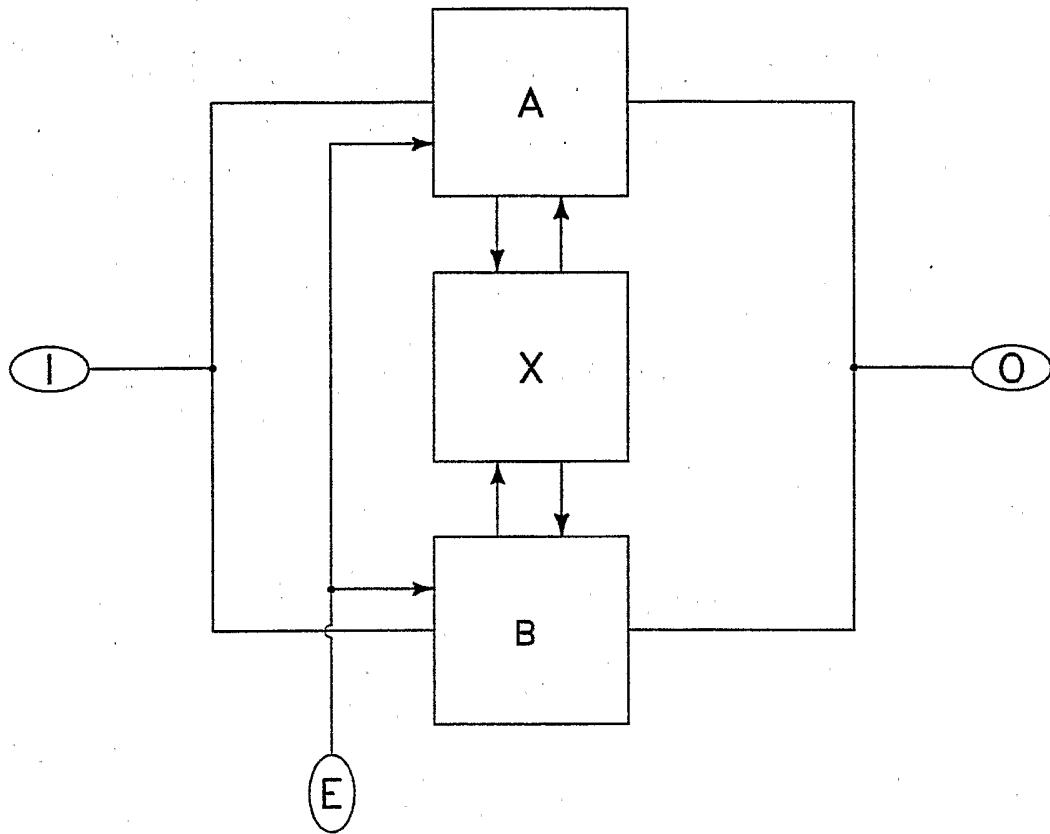


Fig. 2A

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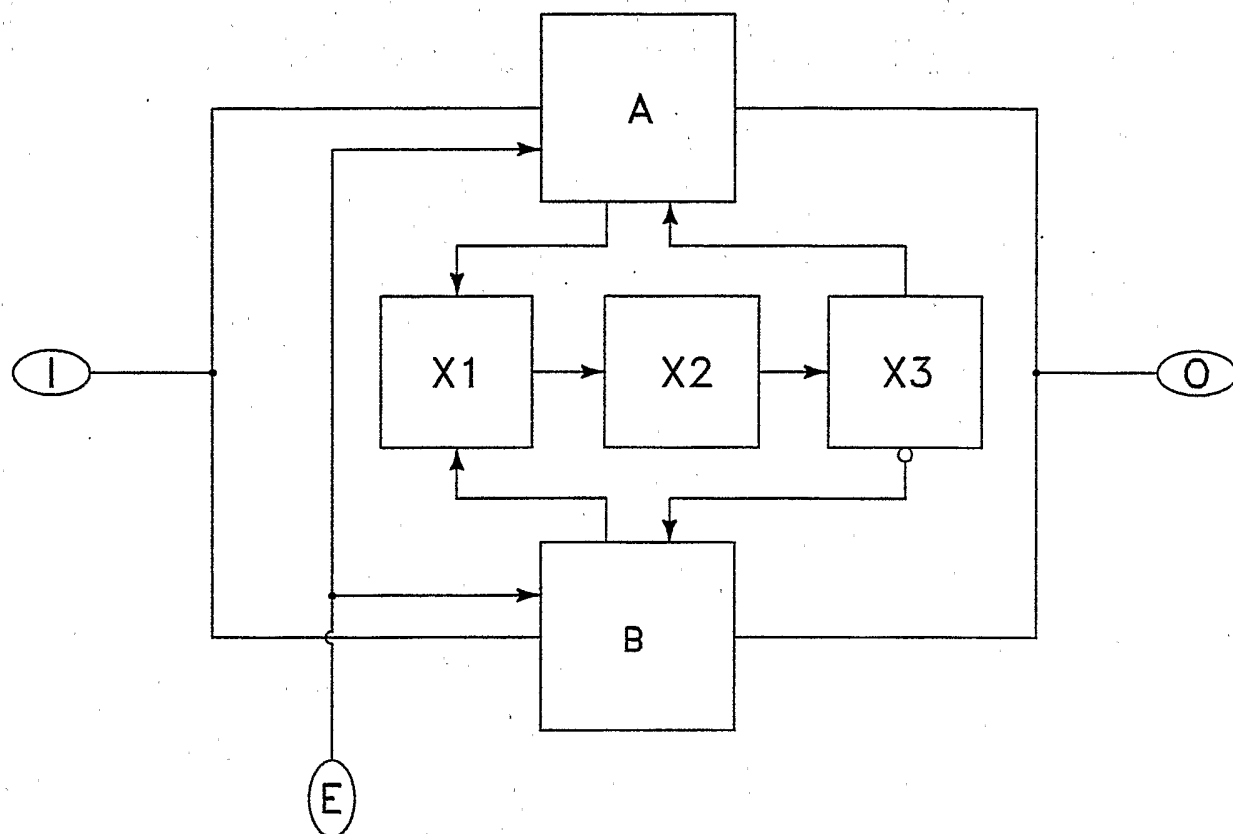


Fig. 3A

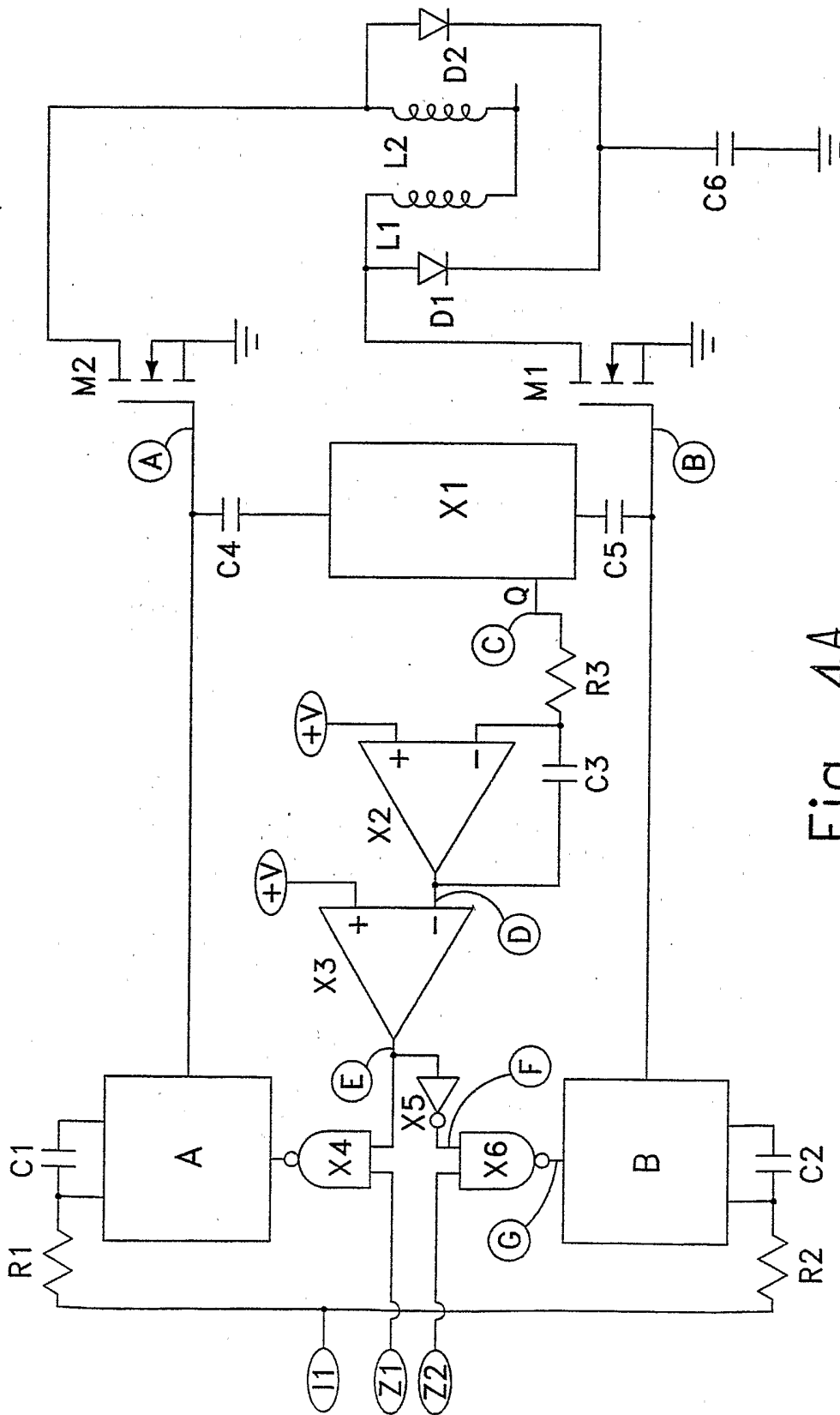


Fig. 4A

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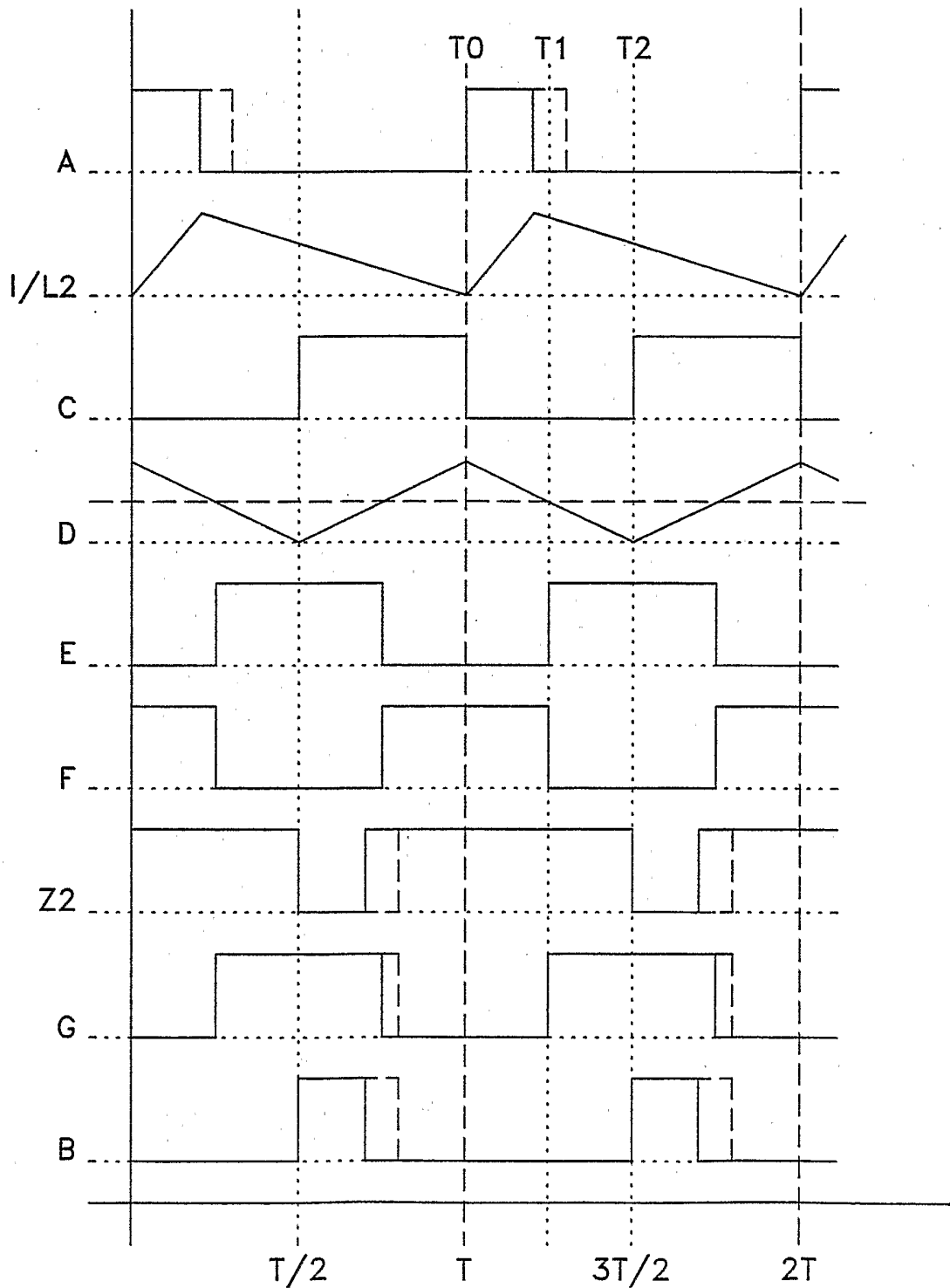


Fig. 5A

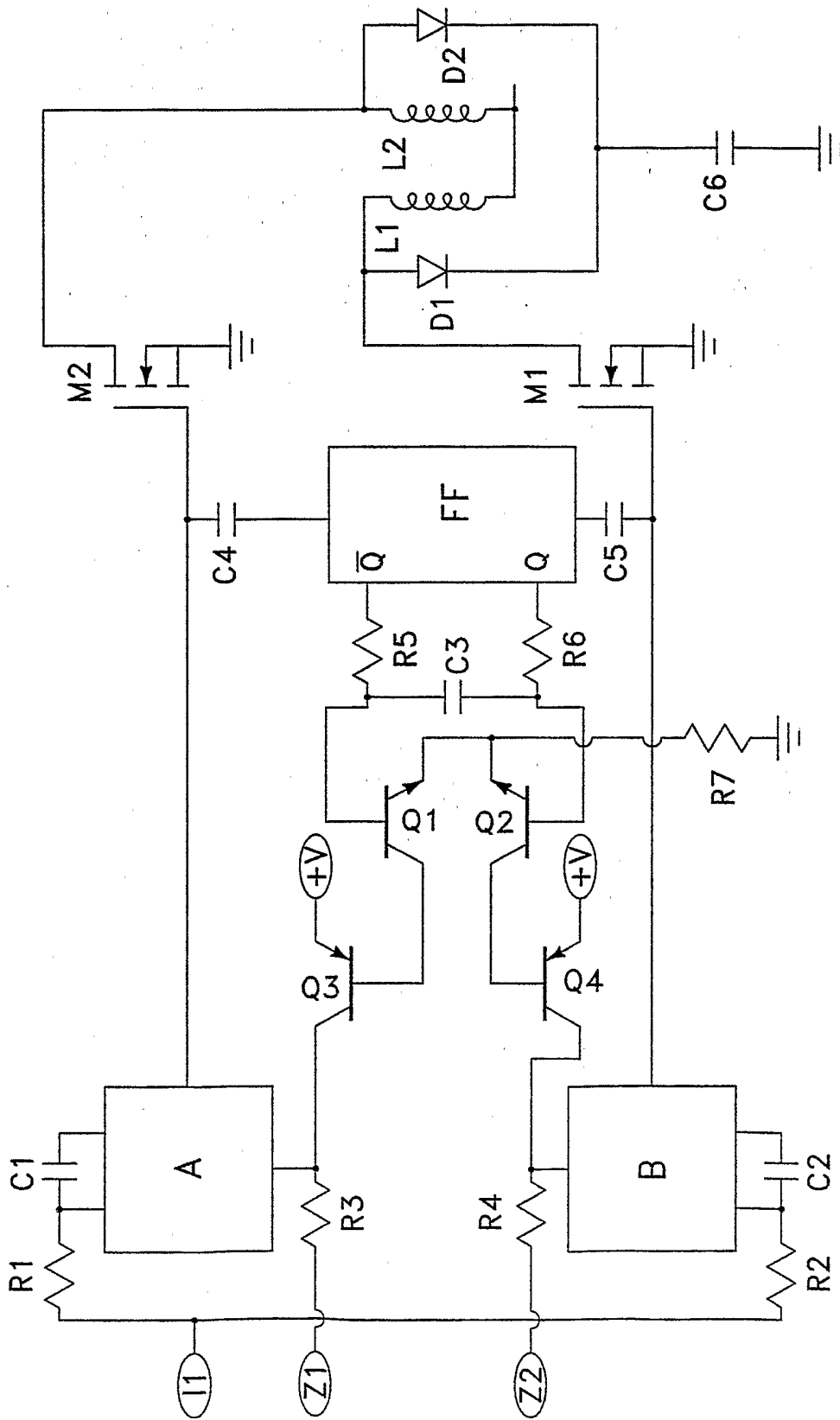


Fig. 6A

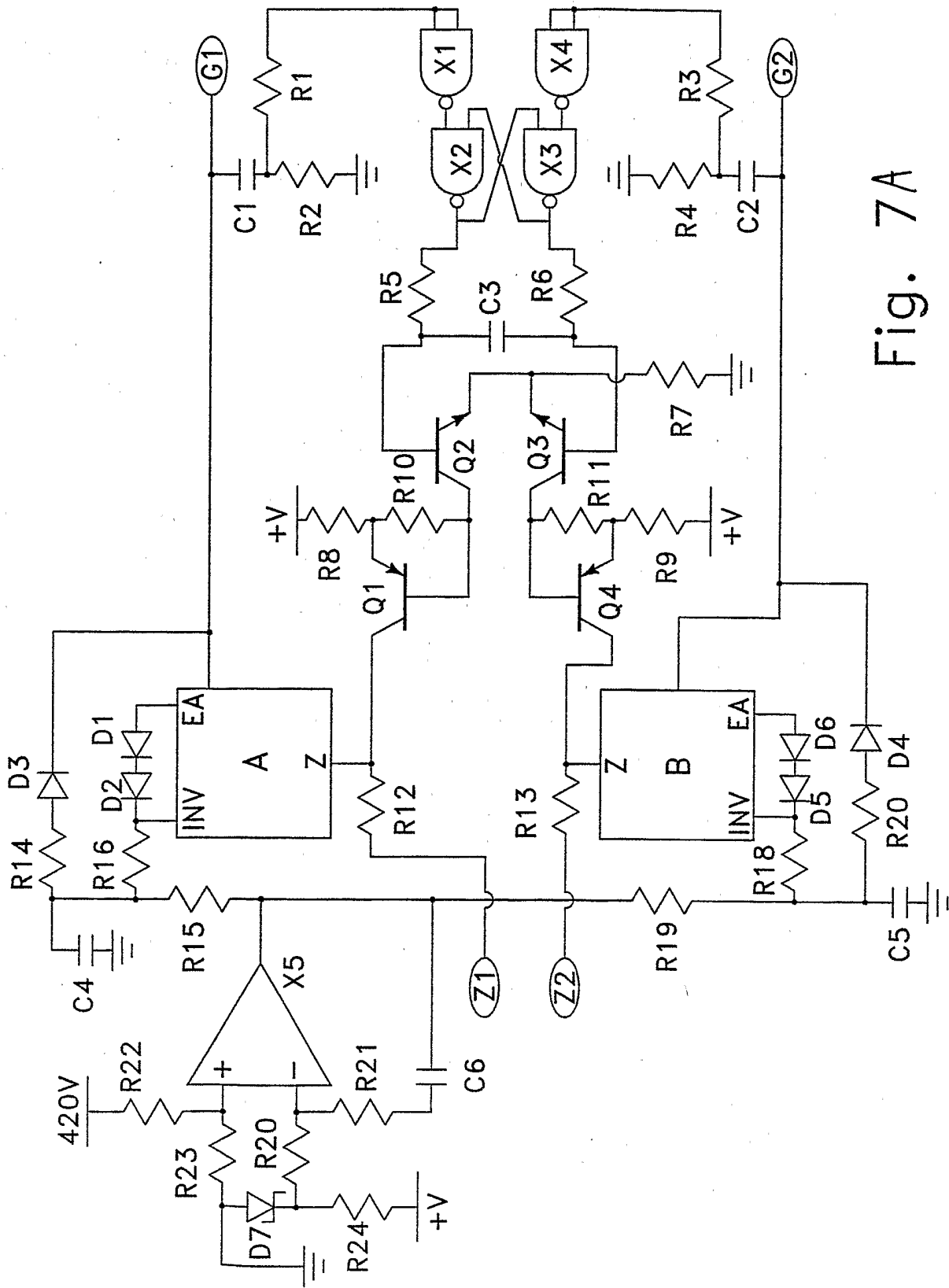


Fig. 7A

17/17

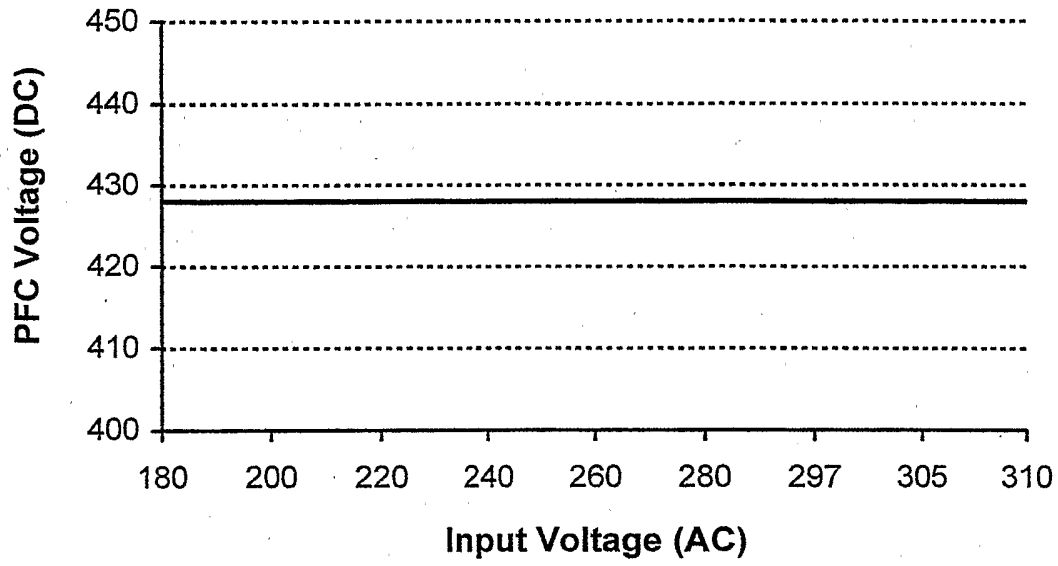


Fig. 8A

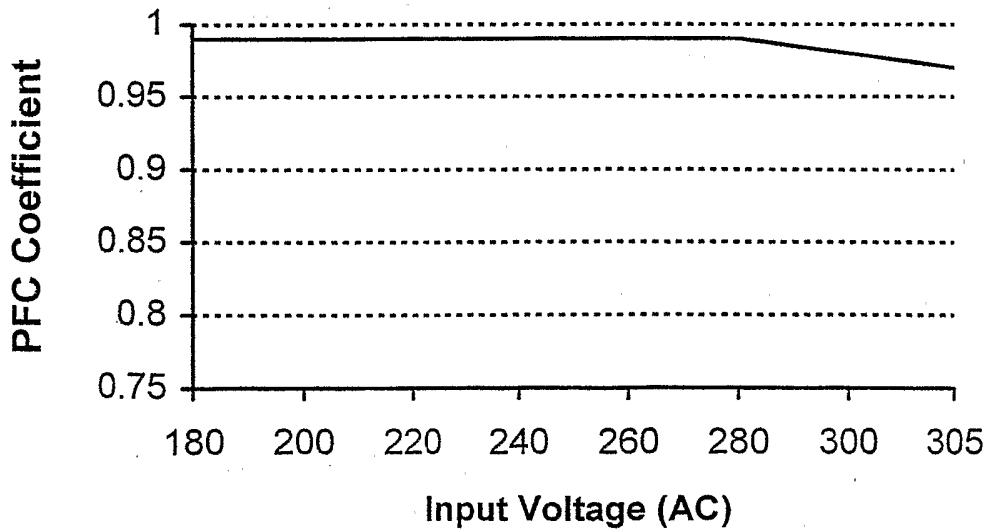


Fig. 9A

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/16212

A. CLASSIFICATION OF SUBJECT MATTER		
IPC(7) : H05B 41/16; H01J 65/04 US CL : 315/248, 39, 267, 344; 313/113, 483; 333/208		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) U.S. : 315/248, 39, 267, 344; 313/113, 483; 333/208		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched none		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EAST Text search, Key Terms: electrodeless, bulb, fill, mesh, cavity, magnetron, waveguide, temperature, distance.		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/0030453 A1 (KIRKPATRICK et al.) 14 March 2002 (14.03.2002); see entire document	1-5
A	US 4,933,602 A (ONO et al.) 12 June 1990 (12.06.1990); see entire document	1-5
A	US 5,841,233 A (URY et al.) 24 November 1998 (24.11.1998); see entire document	1-5
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:		
"A"	document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed	
Date of the actual completion of the international search	Date of mailing of the international search report	
15 September 2003 (15.09.2003)	03 NOV 2003	
Name and mailing address of the ISA/US	Authorized officer	
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	THUY VINH TRAN <i>Diana Amute</i> Telephone No. (703) 305-0012	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US03/16212

Box I Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claim Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claim Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claim Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of Item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Please See Continuation Sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-5

Remark on Protest The additional search fees were accompanied by the applicant's protest.
 No protest accompanied the payment of additional search fees.

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claim(s) 1-5, drawn to a structure of an electrodeless lamp powered by microwave energy.

Group II, claim(s) 6-7, drawn to an arrangement of converters for power factor correction.

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

(i) The structure of an electrodeless lamp powered by microwave energy disclosed in the invention Group I is not capable of using together with the converters arranged for power factor correction disclosed in the invention Group II. In addition, these two inventions have different modes of operation, different functions, or different effect; and

(ii) In this instant case, the invention Group I needs not be configured with a group of converters of the invention Group II to be normally operated; the electrodeless lamp of the invention Group I can be operated by its microwave energy to provide light while the group of converters of the invention Group II can be used to convert signals.