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Schreiner et al.

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[45] **July 22, 1975**

[54] **SOLID STATE FLUORESCENT LAMP BALLAST SYSTEM**

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[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[22] Filed: **Dec. 20, 1973**

[21] Appl. No.: **426,784**

[52] **U.S. Cl.** **315/226**; 315/DIG. 7

[51] **Int. Cl.** **H05b 37/02**

[58] **Field of Search** ..... 315/DIG. 7, DIG. 5, DIG. 4, 315/320, 216, 221, 226, 210

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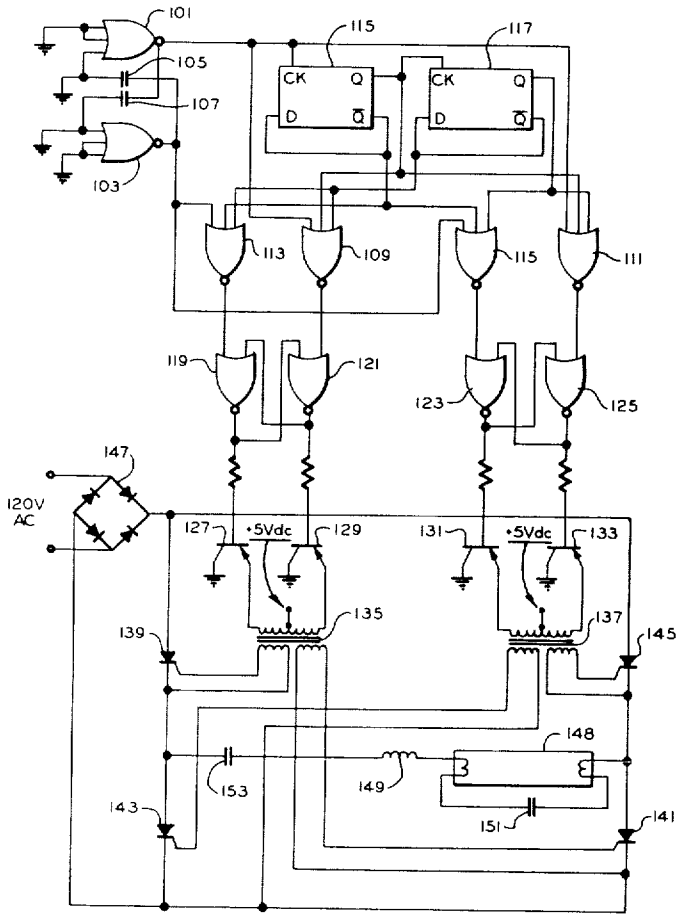
Primary Examiner—Nathan Kaufman

Attorney, Agent, or Firm—Harold Levine; James T. Comfort; Gary C. Honeycutt

[57] **ABSTRACT**

An improved solid-state fluorescent lamp ballast in which line voltage or directly rectified line voltage is chopped to provide a high frequency input to the lamp permitting smaller reactive ballast components to be used. Also shown are various means of switching, means for isolating the high voltage switches for the logic circuits, driving them and various load circuits.

14 Claims, 13 Drawing Figures



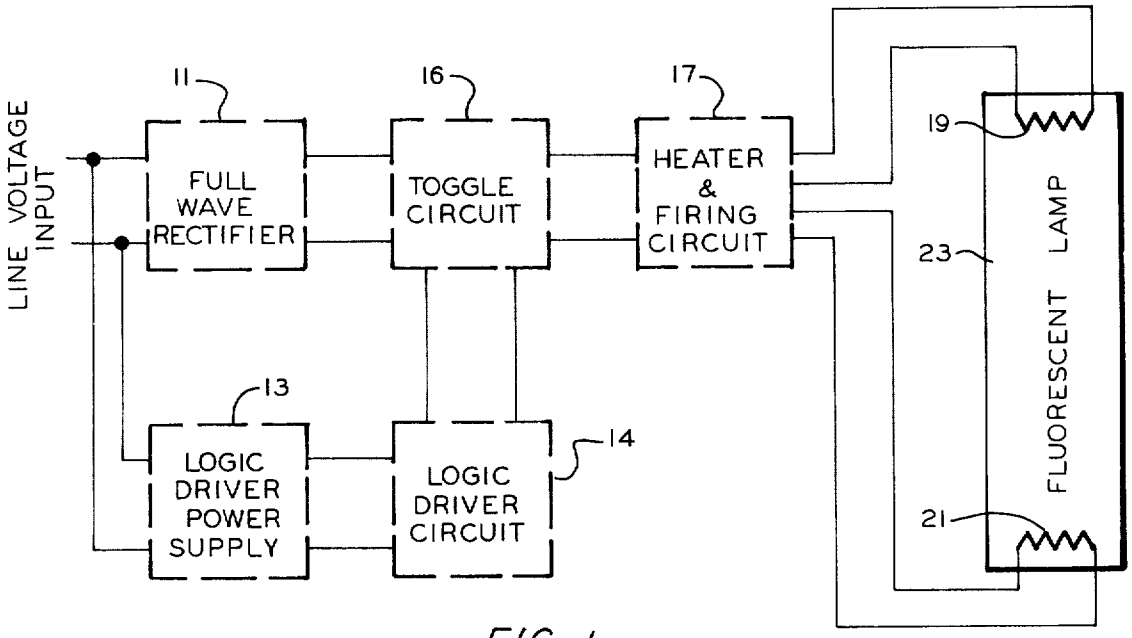

LINE VOLTAGE INPUT
11
FULL WAVE RECTIFIER
16
TOGGLE CIRCUIT
17
HEATER & FIRING CIRCUIT
19
23
21
FLUORESCENT LAMP
13
LOGIC DRIVER POWER SUPPLY
LOGIC DRIVER CIRCUIT
14

FIG. 1

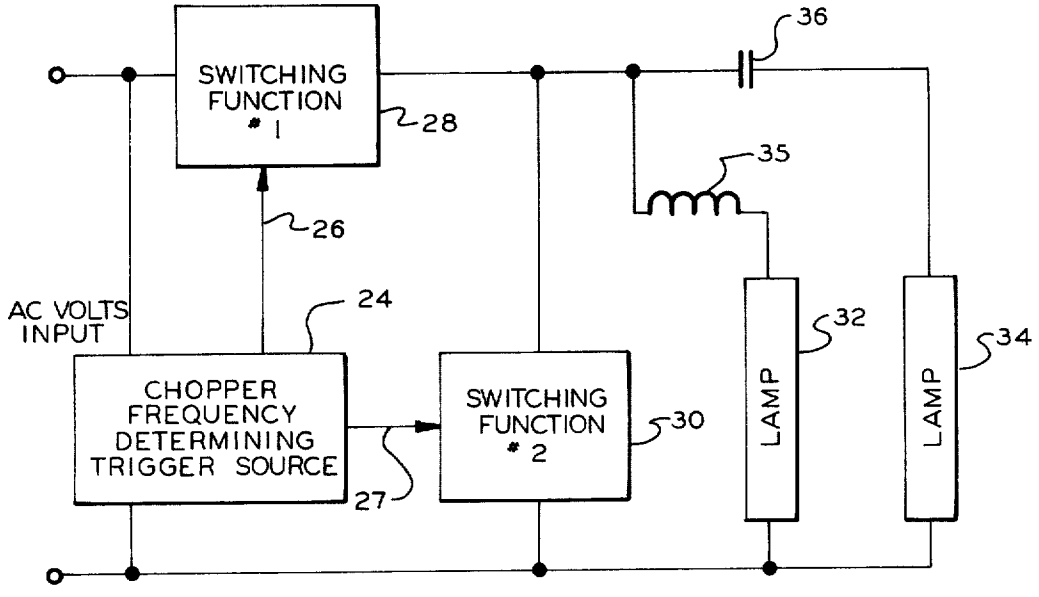

SWITCHING FUNCTION # 1
28
36
35
26
AC VOLTS INPUT
24
CHOPPER FREQUENCY DETERMINING TRIGGER SOURCE
27
SWITCHING FUNCTION # 2
30
LAMP
32
LAMP
34

FIG. 2

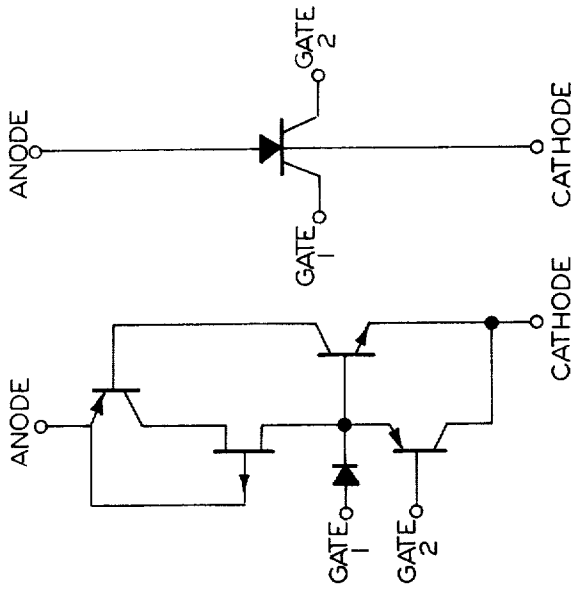

ANODE
GATE 2
CATHODE
GATE 1
CATHODE
ANODE
GATE 1
GATE 2

FIG. 5

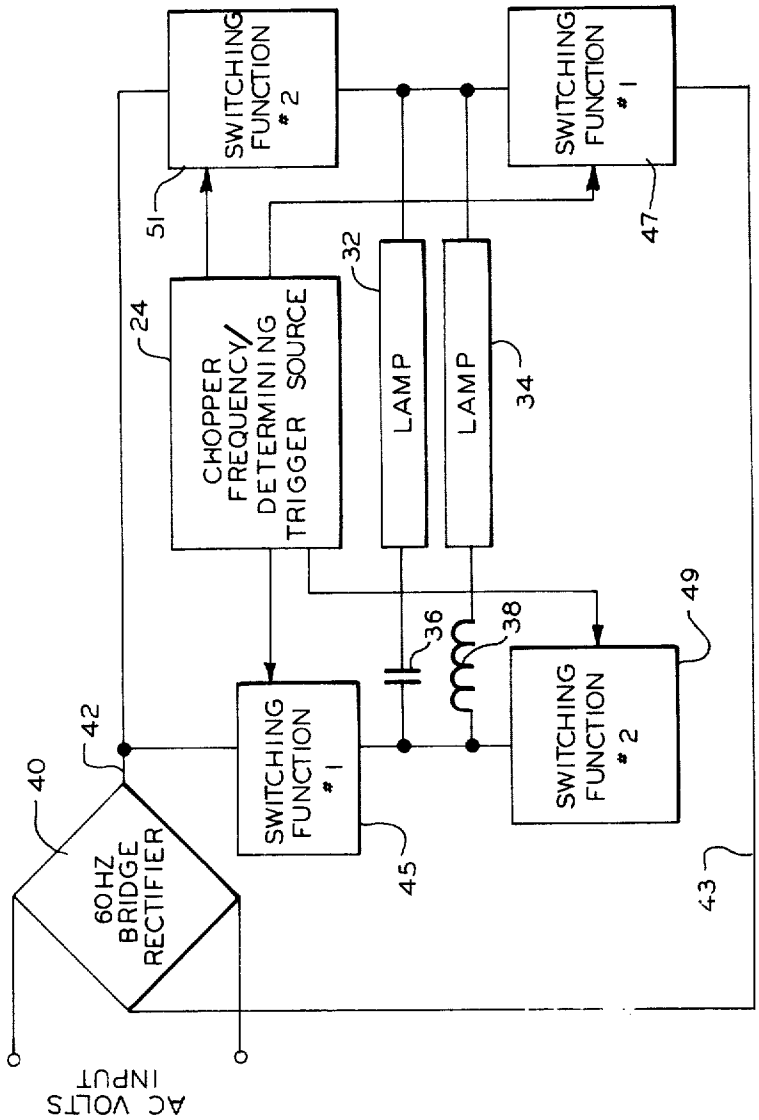

AC VOLTS INPUT
60HZ BRIDGE RECTIFIER
40
42
SWITCHING FUNCTION #1
45
SWITCHING FUNCTION #2
49
43
36
38
CHOPPER FREQUENCY/ DETERMINING TRIGGER SOURCE
24
LAMP
32
LAMP
34
SWITCHING FUNCTION #2
51
SWITCHING FUNCTION #1
47

FIG. 3

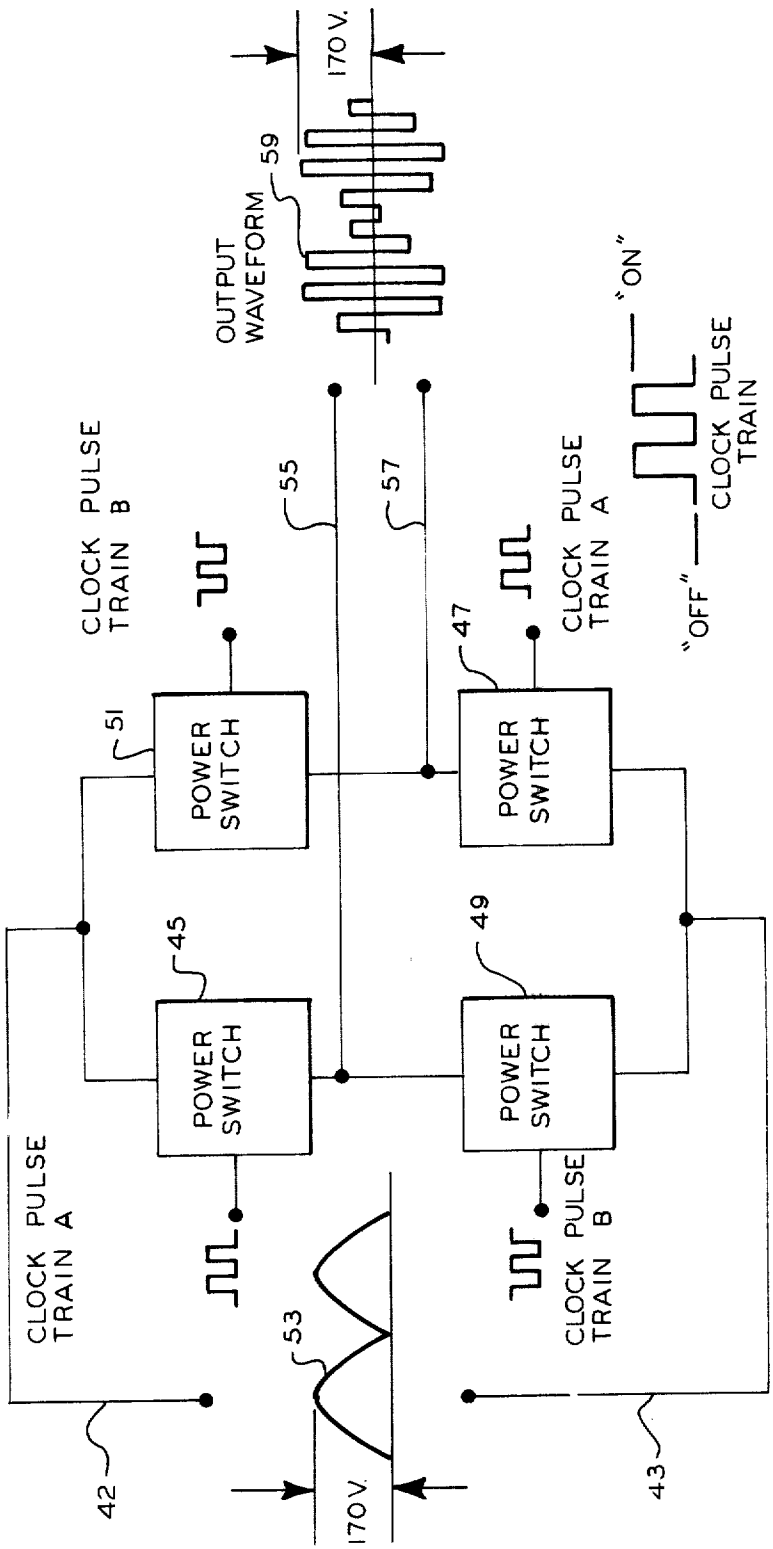

170 V.
OUTPUT WAVEFORM
59
55
57
CLOCK PULSE TRAIN B
CLOCK PULSE TRAIN A
"ON"
"OFF"
CLOCK PULSE TRAIN
51
47
POWER SWITCH
POWER SWITCH
45
49
POWER SWITCH
POWER SWITCH
CLOCK PULSE TRAIN A
CLOCK PULSE TRAIN B
53
170 V
42
43

FIG. 4

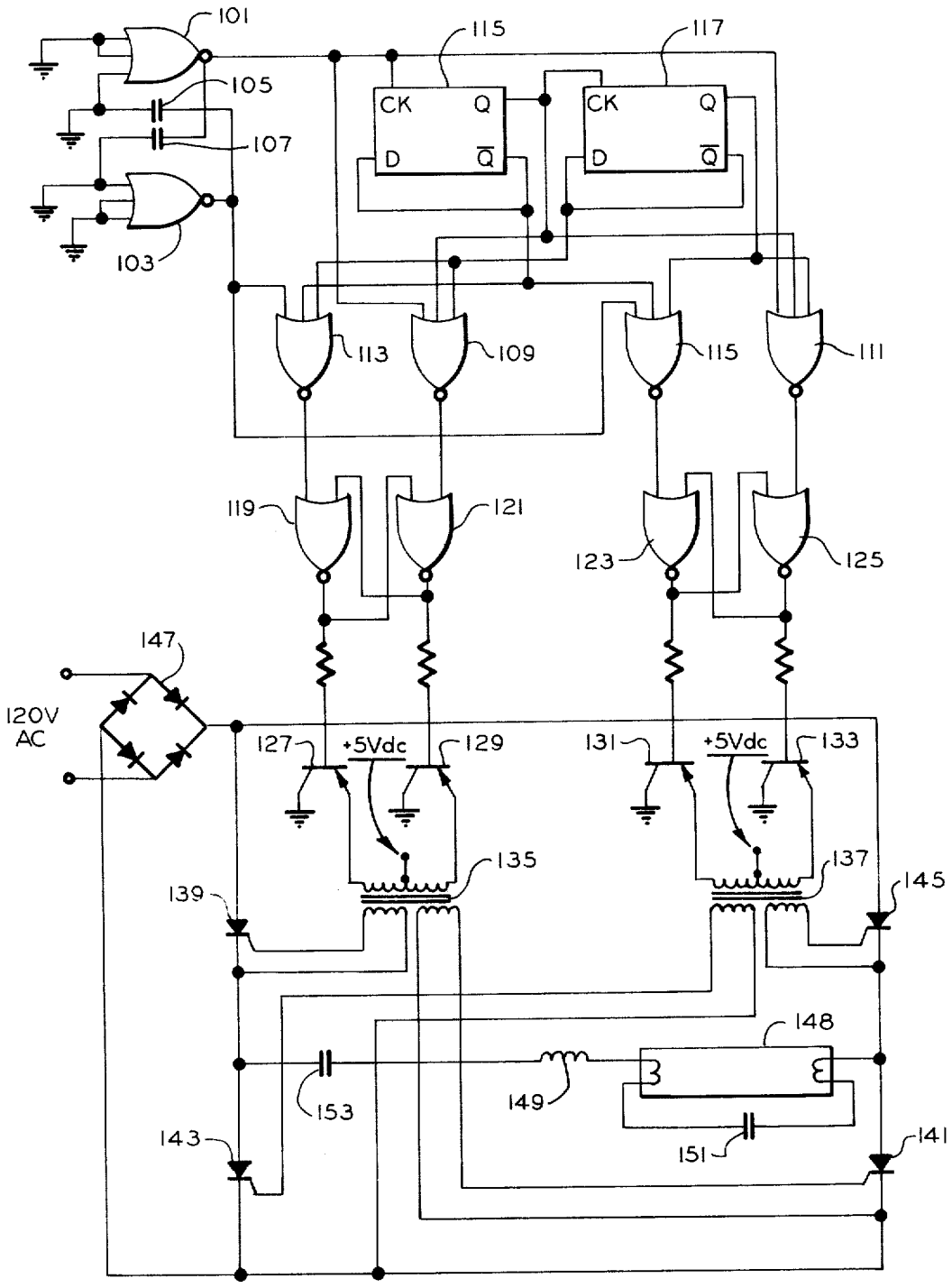

101
105
107
103
115
117
CK
Q
D
Q
113
109
115
111
119
121
123
125
147
120V
AC
127
+5Vdc
129
131
+5Vdc
133
135
137
139
145
148
149
153
143
151
141

FIG. 6

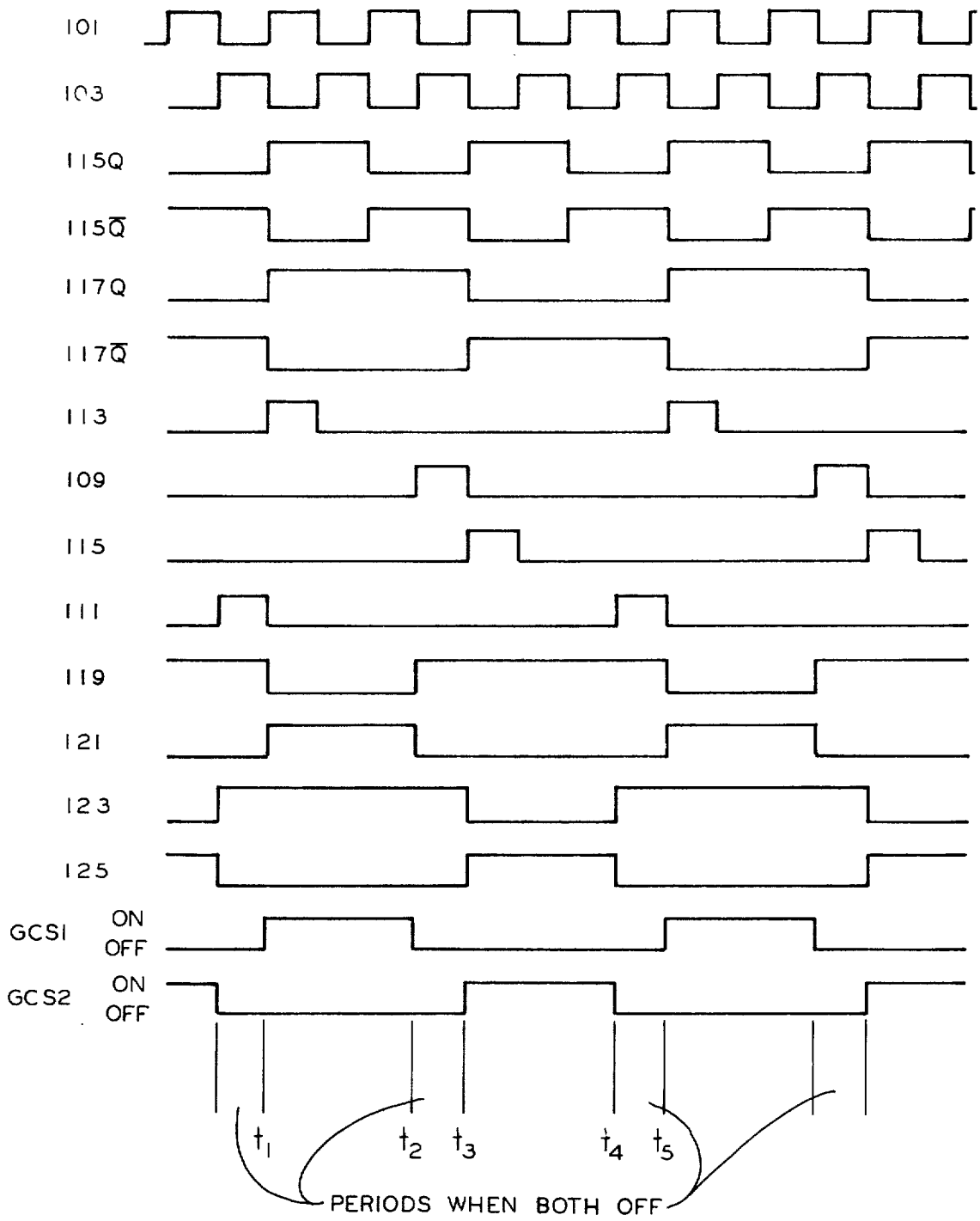

101
103
115Q
115$\overline{Q}$
117Q
117$\overline{Q}$
113
109
115
111
119
121
123
125
GCS1 ON OFF
GCS2 ON OFF
t_1
t_2
t_3
t_4
t_5
PERIODS WHEN BOTH OFF

FIG. 7

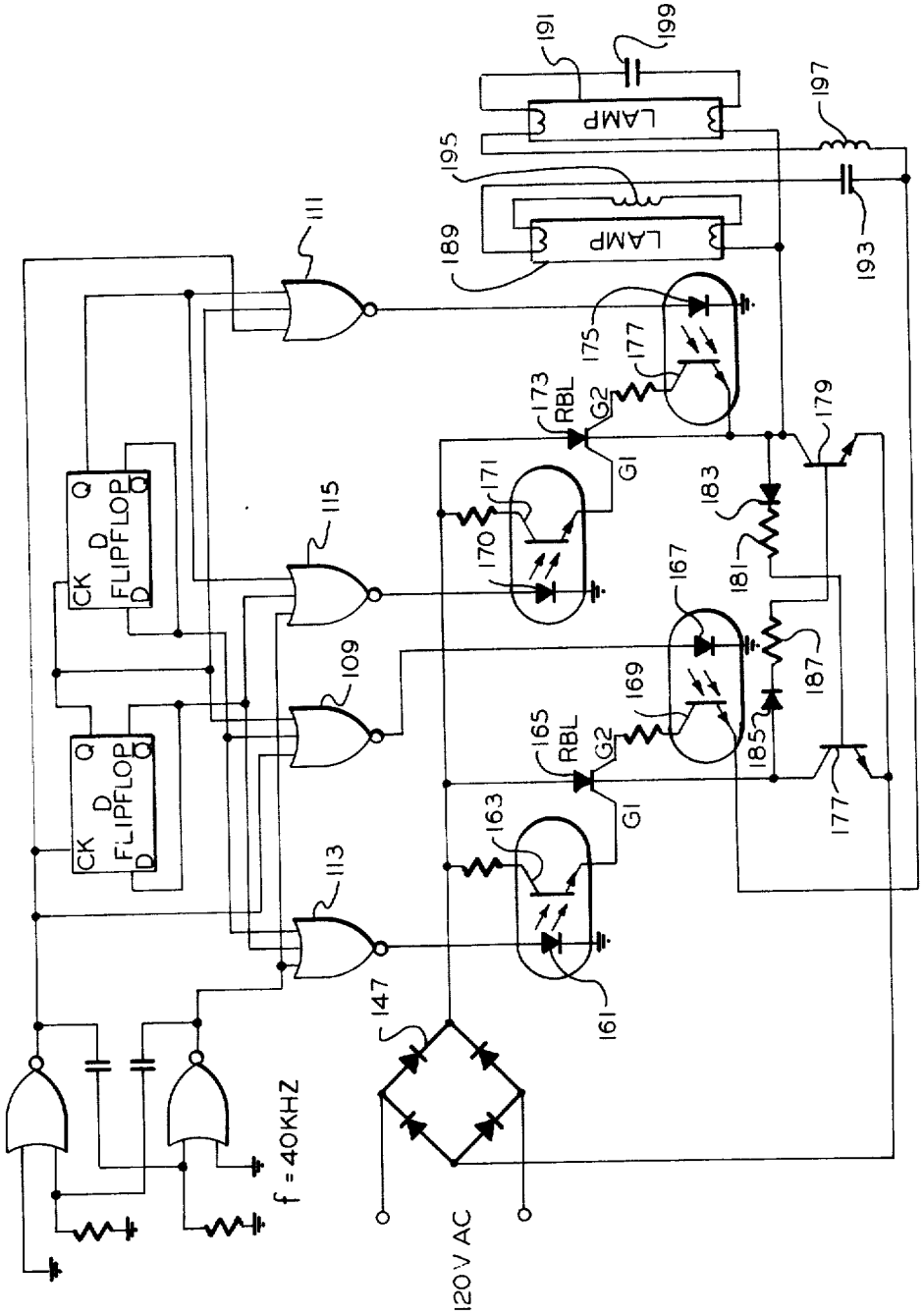

LAMP
LAMP
191
199
197
195
189
193
111
175
177
173
RBL
G2
G1
179
115
171
170
183
167
181
109
169
187
165
RBL
G2
185
G1
177
163
113
147
161
f = 40KHZ
120 V AC
CK
D
FLIPFLOP
Q
CK
D
FLIPFLOP
Q

FIG. 8

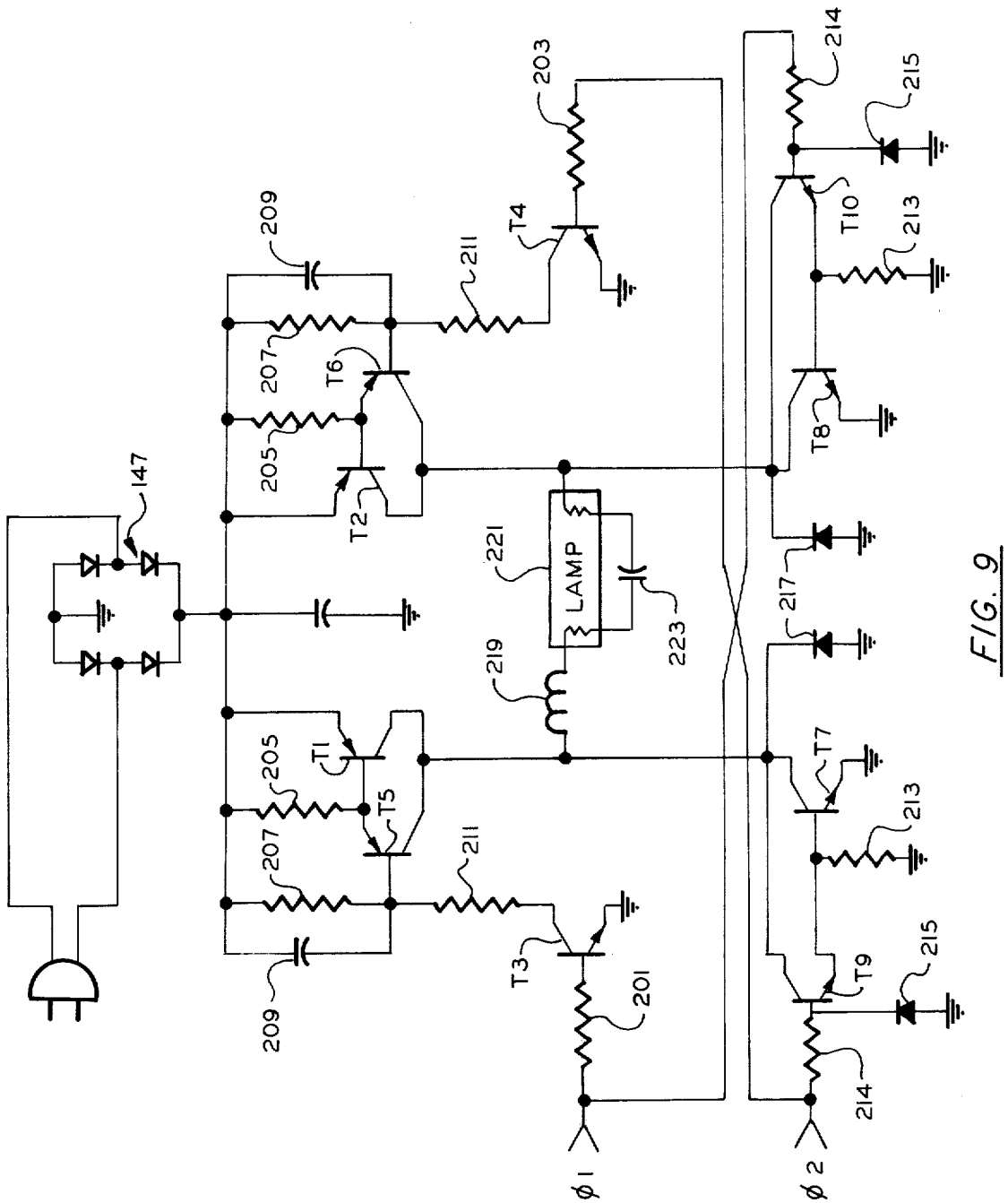

147
209
207
205
T6
T2
211
T4
203
221
LAMP
223
219
T1
T5
T3
201
φ1
φ2
214
215
T10
213
T8
217
T7
T9

FIG. 9

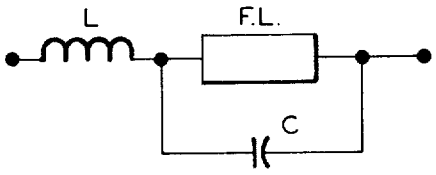


FIG. 10a

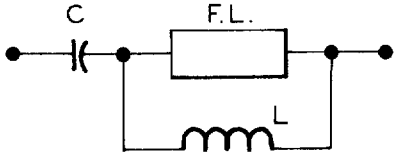


FIG. 10b

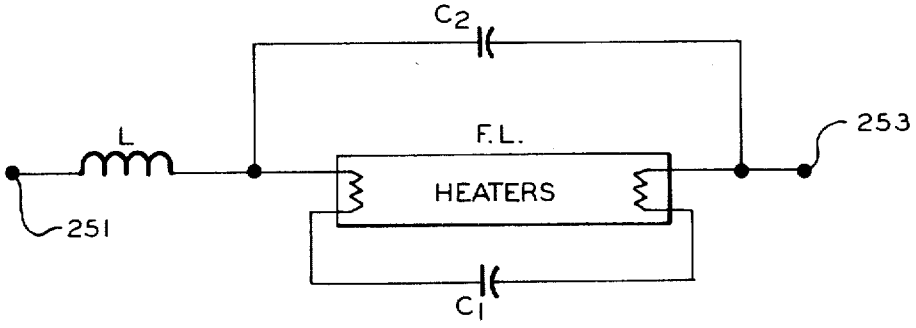


FIG. 10c

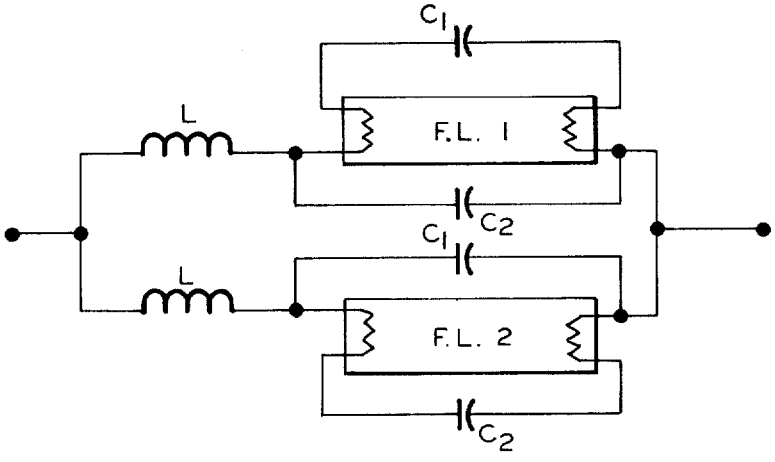


FIG. 10d

SOLID STATE FLUORESCENT LAMP BALLAST SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to fluorescent lamps in general and more particularly to an improved solid-state fluorescent lamp ballast circuit.

A fluorescent lamp is a gaseous discharge device, and it exhibits a negative resistance characteristic when ionization occurs. The ionization is due to the collision of electrons with the gas molecules. The more current in the arc the lower the effective resistance becomes. Therefore, a current-limiting element must be introduced to prevent the lamp from ultimately destroying itself. The source of the electrons for ionization is usually supplied by a cathode in each end of the tube. Fluorescent lamps can be started without cathode pre-heat by increasing the applied lamp voltage until the free electrons are accelerated sufficiently so as to produce the energy necessary for ionization of the gas. This voltage requirement is fairly high, depending upon the tube type and the operating frequency of the system. Moreover, it could be supplied from a reasonably low energy source such as a high-voltage pulse amplifier. Existing current-limiting and starting-ballast functions are usually performed by an inductive ballast designed for a particular gaseous discharge tube.

Most inductive ballasts utilize some type of auto transformer configuration to provide the current-limiting reactance and the high voltage necessary to ionize the tube. The light output, life, and starting reliability of the fluorescent lamp depend greatly upon the design of this ballast. Therefore, the size, weight and reliability of fluorescent lamp ballasts become very important factors in optimizing the total-system efficiency and reliability.

Other types of reactive elements, such as capacitors, can also be used as ballast. However, at 60-Hz line frequency there is a differentiating characteristic in the output of the capacitor ballast which is phase delayed with respect to the input frequency. This characteristic causes very short lamp conduction times and high crest factors. The result is low lamp-illumination efficiency and a pronounced stroboscopic effect.

Resistance ballasting is usually used for dc operation but is not normally used for ac operation because of the poor efficiency as an ac ballast component.

It has been proposed to employ solid-state components for gaseous discharge tube ballasts because of the possibility of achieving increased reliability with an attendant decrease in the size and weight of such ballasts; however, total system economy must be considered as an underlying goal in any such approach. Heretofore, most solid-state ballast approaches have utilized some type of semiconductor inverter circuitry to provide a separate frequency source independent from the 60-Hz line for driving a gaseous discharge tube. Various types of semiconductor inverter circuits have been proposed, most of which utilize two power-switching devices, normally power transistors, and one or more transformers to complete the dc-to-ac conversion function. The advantages of high-frequency operation can be exploited in this approach. However, the inverter circuit must be driven from a 60-cycle ac line and therefore, an additional conversion step from ac to the low-voltage dc is necessary. The high-value passive components, together with the transformer coupling requirements, limit this approach when trying to achieve a high level of monolithic integration.

SUMMARY OF THE INVENTION

The present invention provides a solid-state ballast control for fluorescent gaseous discharge tubes of improved character which does not require an additional conversion step from ac to low-voltage dc.

In all of the embodiments described below, systems are designed to take advantage of the high frequency operating characteristics of the gaseous discharge tubes. Each system operates directly from the 60-Hz line frequency without benefit of an ac to low-voltage dc conversion step. The line voltage or directly rectified line voltage is chopped at high frequency rate and fed to the fluorescent tube through an inductive or capacitive ballast component. This permits making optimum use of the high frequency operating characteristics of the fluorescent lamp to achieve increased illumination efficiency without the associated power loss in external transformers common in typical ac to dc converters. In addition, the high frequency operation allows smaller and lower cost external reactive components necessary for ballasting the fluorescent tube.

In one embodiment shown, designated a half-wave system, line voltage is used directly and chopper switches provided with one in series and one shunted across the line to provide half-wave voltage cycles to the lamp. A system such as this requires a higher input voltage and needs transistors capable of bi-lateral voltage operation. The preferred embodiment in general terms comprises a full-wave rectifier such as a bridge rectifier with two sets of switches in series across the rectified output. The load is connected between the junctions of each pair of switches. Thus, on each side of the load there is an upper and lower switch with the upper switch connected to the high voltage of the bridge and the lower switch to the low or ground side of the bridge. A trigger source is provided for controlling the four switches and acts to alternately turn on an upper and a lower switch of opposite pairs. Thus, during one-half of the high frequency cycle the current flows through the first upper switch to the load and through the second lower switch back to the rectifier. When the next cycle, the other upper switch is turned on to provide voltage to the other side of the load, through the load and through the first lower switch back to the rectifier.

Various types of switching devices are disclosed including transistors, gate control switches, and regenerative bi-stabled latches.

Because the upper switching devices of the pairs can have a high voltage on their control terminal, isolation between the trigger source which comprises logic circuits and the switching device is required. Thus, various means of obtaining this isolation such as through transformer coupling, opto-electronic coupling and transistor level shifter coupling are also disclosed.

Also shown are various types of load circuits for use with the fluorescent lamps, which circuits provide the necessary current limiting and high voltage on startup.

BRIEF DESCRIPTIONS OF THE DRAWINGS

FIG. 1 is a basic block diagram of the solid-state ballast system of the present invention.

FIG. 2 is a block diagram illustrating a half-wave system.

FIG. 3 is a block diagram illustrating a full-wave system.

FIG. 4 is a block diagram helpful in understanding the operation of the system of FIG. 3.

FIG. 5 is a circuit diagram of the equivalent circuit of a regenerative bi-stable latch.

FIG. 6 is a circuit diagram of an embodiment of the present invention using gate controlled switches and transformer isolation.

FIG. 7 is a timing diagram associated with FIG. 6.

FIG. 8 illustrates a similar embodiment in which regenerative bi-stable latches and transistors are used as switches and which has opto-electronic isolation.

FIG. 9 is a circuit diagram of an embodiment in which all switches are transistors and isolation obtained using level shifting transistors.

FIGS. 10 *a–d* illustrates various load circuits which may be used in the system of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The basic functional block diagram of the system is shown in FIG. 1. The line voltage is provided to a full-wave rectifier 11 shown in dotted lines because in one embodiment of the invention such a rectifier is not used. Power is also provided to a logic driver power supply 13. This may be a power supply of well known type in which rectifiers and zener diodes are used to develop the necessary voltages needed for operating logic circuits. This power output, for example, at 5 volts dc, is provided to a logic driver circuit 14. The output of the full-wave rectifier, or in the case where the rectifier is not used the ac voltage directly, is provided to a toggle circuit 16. This will comprise a plurality of switches being driven by the logic driver circuit. The logic driver circuit will include an oscillator which operates at a high frequency such as 10,000 KHz. The toggle circuit chops the input voltage at this frequency and provides the high frequency output to a heater and firing circuit 17 from which an output is applied to the two heater ends 19 and 21 of the fluorescent lamp 23.

An embodiment in which the ac voltage is applied without the use of a rectifier is shown in FIG. 2. Therein, there is shown a chopper frequency determining source 24 which will have the components equivalent to blocks 13 and 14 of FIG. 1 to develop high frequency output pulses. Two separate pulse trains are provided. One on line 26 and the other on line 27. These are provided as inputs to blocks 28 and 30 indicated respectively as switching function 1 and switching function 2. Each of switching blocks 28 and 30 is connected for a time equal to half the period of the high frequency source and is then turned on. Switching blocks 28 and 30 are thus alternately turned on and off thereby providing a half-wave high frequency 60 cycle modulated signal to fluorescent lamps 32 and 34. A capacitive ballast element 36 is shown at the input to lamp 34 and an inductive ballast element 28 at the input to lamp 32. The half-wave configuration of FIG. 2 requires a higher ac input voltage, e.g. 220 volts, ac in order to develop sufficient voltage to start a 120 volt lamp. Despite this fact however, the number of components in this system are minimized to effect off-setting economics. Since the 60 cycle voltage goes both positive and negative, the switching elements in the switching blocks 24 and 28 and 30 must be capable of bilateral voltage control.

FIG. 3 illustrates in block diagram form a full-wave system. In this system, the ac input voltage is first rectified in a full-wave rectifier bridge 40. Full-wave rectified voltage is then provided as outputs on lines 42 and 43. In this embodiment, four switching blocks, two of which are designated switching function 1 and numbered 45 and 47 respectively and two of which are designated switching function 2 and numbered 49 and 51 must be provided. Thus, the chopper frequency trigger source 24 is required to provide four separate outputs in this case. Since the output of the bridge 40 is at a single polarity, the switching devices used in switching function blocks need only be capable of handling unilateral voltages. In addition, the peak to peak high frequency ac voltage excursion supplied to the load is double the ac voltage available from the previous half-wave configuration of FIG. 1 resulting in sufficient starting voltage from a 120 voltage ac line input to effect operation of 120 volt lamps.

Basic operation of the circuit can be seen from FIG. 4 which illustrates the various wave forms which are applied and developed in the system. The rectified ac voltage is shown as wave form 53 and is provided on the lines 42 and 43 to the switches 45, 47, 49 and 51. On FIG. 3 the switching function is designated as power switches indicating a single switch in each block. The trigger source 24 of FIG. 3 develops two pulse trains designated on FIG. 4 as clock pulse train A and clock pulse train B. Clock pulse train A is provided to the power switches 45 and 47 and clock pulse train B to the power switches 49 and 51. As shown the two clock pulse trains are complementary so that during one-half cycle, power switches 45 and 47 will be turned on permitting the voltage on line 42 to be switched through power switch 45 to the load on line 55, return from the load on line 57 through power switch 47 and back on line 43 to the rectifier bridge. During the next half cycle power switches 45 and 47 will be turned off and power switches 49 and 51 turned on allowing the voltage on line 43 to be provided through power switch 49 over line 55 to the load and return over line 57 through power switch 51 and line 42 back to the rectifier. The resulting output wave form is indicated as wave form 59. As illustrated, it will be at a high frequency modulated by the 60-Hz input frequency. Although shown as directly complementary, i.e., a two phase timing sequence for clock pulse trains A and B, it is preferable that delay periods be inserted between the turn-off of one pair of power switches and the turn-on of the next. Thus, a four phase trigger source enables one switching function to completely turn-off prior to the turn on of the other.

In each of these systems, means must be provided for starting. Existing lamps require a cathode type heater to generate the electron source for starting. When operating at 60-Hz the physical dimensions of this transformer are quite large. However, at an operating frequency of 10-KHz or above, the size, weight and cost of a transformer to perform this function is drastically reduced. Thus, a 10-KHz transformer may be used to provide this function, but other alternatives which avoid the use of a transformer are possible as will be subsequently described.

Various devices may be used as the power switches 45, 47, 49 and 51 of FIG. 4. For example, high voltage transistor structures may be used in all four positions. Such an arrangement requires that the four phase trig-

ger source be increased in complexity so that it can develop a two phase half cycle pulse. This is required because a transistor is not a latch-type device. The drive power required to turn-on a transistor in this application is relatively high due to the application of drive power during the entire on period i.e., at approximately 50% duty cycle. The lower current gain characteristic typical of high voltage transistor structures also results in higher average drive power requirements. Turn-off requirements partially offset the higher turn-on requirement since the device will switch off simply by removing the turn-on pulse. A transistor device for this application should have a relatively low collector current density in order to maintain a reasonable compromise between current gain and current carrying capabilities.

A second type of device which can be used as the power switches of FIG. 4 is a semiconductor latching device such as an SCR or a triac. These devices are switched on by applying a signal to the gate of the device but they cannot be switched off by using a gate signal. There is a special type of latch device that is essentially an SCR structure which has been designed to be switched off by a negative applied gate signal. This device is known as a gate controlled switch [GCS]. Thus, four high voltage GCSs may be used as the power switches **45, 47, 49** and **51** of FIG. **4.** These are turned on and off with the application of positive and negative pulses respectively to the gate of the device. Since device latches on until turned off, the power drive requirements for turn-on are extremely low [typically a ten micro-second, 25 milli watt pulse]. The turn-off is not regenerative and therefore the turn-off power drive is dependent on the current level being switched and is considerably higher than the turn-on requirement, [typically a ten micro-second 700 milli watt pulse for 2.0 amp conduction current]. However, the average trigger power is still lower than when using transistors, since the turn-off also needs only a low duty cycle pulse. A further possibility is the use of a combination of transistors and GCSs. In such an arrangement the turn-on and turn-off control is derived from the GCS and therefore the low duty cycle drive power requirements are obtained. The high voltage transistor is slave driven with its phase current derived from the turn-on of the appropriate GCS and therefore very low current gains are useable relaxing the design restrictions considerably to result in higher potential yields. The chip sizes are compromised since the area would be larger than the GCS approach but smaller than the all transistor approach. Such a system will be described below.

A further possibility is a regenerative bi-stable latch whose equivalent structure is illustrated by FIG. **5.** Its terminals include an anode, a cathode and two gates, one for turning on and the other for turning off. It has turn-on characteristics which are regenerative similar to a GCS therefore allowing large load currents to be switched on with very low gate trigger. It also has regenerative turn-off characteristics which result in an order of magnitude improvement in the turn-off drive required for the GCS. This gives it an advantage over the GCS or the transistor as a high gain power switching element. Since the basic structure is a latch type device, very high active area densities are possible with associated reduction in chip size and cost. Switching speed is comparable to GCS type devices. Tests on preliminary discrete configuration of a 20 amp device show a turn-on current level of **5** micro amps and turn-off levels in the range of 100 microamps.

An embodiment using four GCS devices for switching is illustrated in FIG. **6.** Two NOR gates **101** and **103** are capacitively cross coupled using capacitors **105** and **107** to provide an oscillator in the form of an a stable multi-vibrator with complementary outputs. The output of gate **101** is provided as an input to NOR gates **109** and **111.** The output of gate **103** is provided as an input to NOR gates **113** and **115.** The output of gate **101** is also provided as the clock input to a first D type flip-flop **115.** Flip-Flop **115** has its Q output coupled to the clock input of a second D type flip-flop **117** and also as a second input to gates **109** and **111.** The $\overline{Q}$ output of flip-flop **115** is coupled as a second input to gates **113** and **115** and to the D input of flip-flop **115.** The Q output of flip-flop **117** is the third input to gates **111** and **115** and its $\overline{Q}$ output the third input to gates **109** and **113.** The output of gate **113** is an input to gate **119,** the output of gate **109** an input to gate **121,** the output of gate **115** an input to gate **123** and the output of gate **111** an input gate **125.** NOR gates **119** and **121** are cross-coupled to form a set-reset flip-flop. Similarly NOR gates **123** and **125** are cross-coupled. The output of gate **119** is the input to the base of a transistor **127,** the output of gate **121** is the input to the base of transistor **129,** the output of gate **123** is the input to the base of a transistor **131,** and the output of gate **125** is the input to the base of transistor **133.** Each of the transistors has its collector at ground. Transistor **127** has its emitter coupled to one end of the primary winding of a transformer **135.** The other end of the primary winding of transformer **135** is coupled to the emitter of transistor **129.** Similarly, the emitter of transistor **131** is coupled to one end of the primary of a transformer **137** and the emitter of transistor **133** coupled to the other end of that transformer. Each of the transformer primaries has a center tap which is at a positive voltage, for example, **5** volts dc. Each of the transformers also has two secondaries. The two secondaries of transformer **135** are coupled respectively to the gate control switches **139** and **141.** The two secondaries of the transformer **137** are coupled to the gate control switches **143** and **145.**

Operation of this portion of the circuit, which is the trigger source **24** shown on FIG. **3,** can best be understood by reference to the timing diagram of FIG. **7.** The gates **101** and **103** provide complementary output pulses as indicated. The pulses are provided to the D type flip-flop **115** and to the gate as described above. The flip-flop **115** effects a division by two and the flip-flop **117** a second division by two as indicated by their respective wave forms. The result at the output of gates **109, 111, 113** and **115** is as shown. Similarly, the outputs of the gates **119, 121, 123** and **125** in response to these outputs are also shown. When gate **119** goes low, transistor **127** will be turned on and the secondaries of transformer **135** will provide positive output pulses to turn-on the gate control switches **139** and **141.** This occurs at the time indicated as T1 on FIG. **7.** At time T2, gate **121** goes low and gate **119** goes high turning off the transistor **127** and turning on transistor **129.** This results in a negative output pulse turning off the gate control switches **139** and **141.** At time T3 the output of gate **123** goes low, turning on transistor **131** and resulting in a positive output pulse to the gate control switches **143** and **145** to turn them on. At time T4 the

output of gate 125 goes low and the output of gate 123 goes high turning off transistor 131 and turning on transistor 133 to result in a negative pulse out of the secondary of transformer 137 to turn-off the gate control switches 143 and 145. At time T5 the complete process is started again. Note that between the time T2 and T3 and the times T4 and T5 all gate control switches are turned off. This insures that both sets of gate control switches cannot be on at the same time which, as noted above, could result in a catastrophic failure of the system. Also as described above, this switching of the gate control switches results in the dc output of the bridge 147 being provided to the fluorescent lamp 149 at a high alternating frequency.

To provide the desired current source for starting, the circuit of FIG. 6 utilizes the Boucherot effect in which the LC circuit comprising the ballast inductor 149 and capacitor 151 are selected to resonate near the input frequency. This results in a sufficient voltage to initiate the arc in the lamp. Also shown is a ballast capacitor 153 in series with conductor 149. Particular arrangements for obtaining the required current for starting will be described in more detail below.

A further embodiment of the invention is illustrated in FIG. 8. The primary difference between this embodiment and that of FIG. 6 is in the elimination of the transformers and in the use of a combination of RBL's and transistors as the switching devices rather than the use of gate controlled switches. This construction allows the whole circuit with the exception of the external ballast components to be manufactured on a single integrated circuit chip. In this embodiment, the trigger circuit is similar to that in FIG. 6 except that the flip-flops comprising the gates 119, 121, 123 and 125 are not present. The outputs are taken directly from the gates 113, 109, 115 and 111. The output of gate 113 is provided to an optical coupling device which comprises a light emitting diode 161 which images its beam on a photo-transistor 163. Thus a pulse output from gate 113 will result in a light output from the light emitting diode 163 to turn-on the photo-transistor 163. The output of the photo-transistor 163 is coupled to the first gate of an RBL 165 to turn that device on. The output of gate 109 is similarly coupled to a light emitting diode 167 which images its light on a photo-transistor 169 coupled to a second gate of the RBL 165. An output from gate 109 will thus cause light emitting diode 167 to have an output turning on transistor 169 to turn-off the RBL 165. Gate 115 is coupled to a similar optical coupling device comprising light emitting diode 169 and photo-transistor 171. As in the manner described above, an output from gate 115 will turn on an RBL 173. Similarly, the output of gate 111 which is coupled through light emitting diode 175 and photo-transistor 177 to the G2 gate of RBL 173 will turn-off that device. The second switching elements comprise transistors 177 and 179. The base of transistor 177 is coupled through a resistor 181 and diode 183 to the cathode of RBL 173. Similarly, the base of transistor 179 is coupled through diode 185 and resistor 187 to the cathode of RBL 165. This will result in the transistors being slaved to their respective RBLs. Thus, when RBL 173 is turned on by a signal at its gate G1, the positive voltage output will be applied to the base of transistor 177 turning that transistor on and providing a return path for the current through the lamp. Similarly, when RBL 165 is turned on, the voltage at its cathode will turn-on transistor 179. Lamps 189 and 191 are coupled across the output of the switching circuit in the manner described above. Lamp 189 is shown with a series capacitive ballast element 193 and a parallel inductive element 195. Lamp 191 has an inductive ballast element 197 with a capacitor 199 M parallel. These will be resonant circuits to provide the required starting current as will be described in more detail below.

The optical coupling devices in the case of FIG. 8 and the transformers in the case of FIG. 6 provide the necessary isolation between the logic circuit in the power switches. This isolation is required since on either side of the circuit, when the lower switch is in the off state the upper switch of the pair is on. This results in its negative terminal being near the input potential from the full-wave rectifier. Since its control terminal i.e., base or gate potential must always be close to that of its negative terminal which may be as high as 170 volts, the drive to the control terminal from the logic circuits cannot be supplied directly by logic elements which only have a low voltage handling capability. Thus, the transformer or optical coupling is used as illustrated.

FIG. 9 illustrates an embodiment in which all elements are transistors. This arrangement avoids the use of either transformer or optical coupling between the logic circuits and the power switching circuits through use of a novel level switching circuit further simplifying the integration of the circuit. The trigger logic circuits are not shown with FIG. 9 but can be similar to those shown in connection with FIG. 6 with the outputs of gate 121 and 125 as shown on FIG. 7 provided as the respective inputs. As noted above, this insures that one pair of switches is completely turned off before the other is turned on. These outputs are present for the whole on period and thus will hold their respective transistors on as required. The phase one input is provided through a resistor 201 to the base of a transistor designated T3. The phase 2 input is provided through resistor 203 to a transistor T4. These transistors are used as level shifters to enable the switches to be switched on and off by low logic voltages. Each of the switches at the top of the Figure comprises a Darlington pair. The one switch comprises the pair made up of transistors T1 and T5. The second pair is made up of the transistors T2 and T6. Load resistors 205, biasing resistors 207 and capacitors 209 are suitably provided for each Darlington pair. The outputs of the respective transistors T3 and T4 are coupled to the bases of T5 and T6 through resistors 211. The second set of switches are formed by Darlington pair T7 and T9 and T8 and T10 respectively. Resistors 213 and diodes 215 and 217 are provided in each of the circuits in conventional fashion. The bases of transistors T10 and T9 are coupled respectively to the phase 1 and phase 2 inputs. Since these transistors will never have a very high voltage on their bases, direct coupling to the logic signals is possible. Operation is similar to that described above with the phase 1 signal turning on the Darlington pair comprising T1 and T5 to provide current through the ballast inductance 219 to the lamp 221 and to turn on the pair comprising transistor T8 and T10 to provide a return path to ground. During the next high frequency cycle, the phase 2 signal will turn-on the pair comprising T2 and T6 and the pair comprising T9 and T7.

The level shifter is implemented by using a PNP transistor for the upper power switch i.e., transistors T5 and T6, and using a high voltage NPN level shifter transis-

tor to drive the PNP transistor. The level shifting transistor must have the same voltage handling capabilities as the power switches. However, its current handling capability is much smaller. In order to minimize this, rather than using single PNP transistors as the upper switches, Darlington pairs are used.

A capacitor **223** is provided in parallel with the lamp to provide the resonant circuit required for start-up. The resonant circuit comprising inductor **219** and capacitor **223** should be selected to have a resonant frequency which is near but not at the frequency of the high frequency switching signal. This is disclosed in more detail in application serial no. (Case No. TI-5261) filed on even date herewith. Operation of this series resonance circuit briefly is as follows: The resonance circuit provides sufficient voltage boost to provide a high enough voltage across the lamp for start-up. That is, the voltage from one filament to the other. However, in addition, heater current must be provided to the filaments. This can be done with small transformers. However, it has been found that by placing the capacitor in series with the filaments the roughly correct average heater current is provided. The inductor **219** then acts during the operation to limit the load current to the desired value. Thus, all the various requirements for the lamp circuit are met.

In the embodiment of FIG. **9**, typical values are as follows:

Resistor **205** - **62** Ω
Resistor **207** - **510** Ω
Capacitor **209** - **0.01** uf
Resistors **211** - **2K** Ω
Resistors **201** - **430** Ω
Resistor **214** - **20** Ω
Resistor **213** - **150** Ω
Inductor **219** - **3.75** mh and
Capacitor **223** - **0.0401**

The figures of inductance and capacitance are for a high frequency input at the phase **1** and phase **2** inputs having a repetition rate of 10,000 pulses per second. These values result in a load circuit which is resonant at a frequency above the frequency of the load exitation. This class of operation secures the necessary voltage boost from operation near resonance without excessive voltage boost and excessive load current at initial start-up which results from operation at resonance. The load circuit in general must be designed so as to provide sufficient voltage boost to fire the lamp at initial start-up and at each succeeding cycle of the voltage input. It must also operate so as to provide the necessary current limiting reactance and must not provide excessive voltage boost or load current at initial turn-on. Although in this preferred embodiment, the resonant frequency of the circuit is above the frequency of the input signal, it is also possible to operate below that frequency.

Various load circuits are possible as illustrated on FIG. **10**. FIG. **10***a* illustrates the load circuit discussed above. A load circuit such as that shown on FIG. **10***b* with a series capacitor and a shunt inductance is also possible. FIG. **10***c* illustrates a circuit which permits adjusting the load circuit resonant frequency and the internally supplied heater current independently. When a high frequency driving voltage is provided to the nodes **251** and **253** of the circuit of FIG. **10**, values for L and C_1 and C_2 can be selected to satisfy the load circuit requirements for voltage boost and the current limiting reactance and at the same time provide desired or required ac lamp heater current. This is true since the current is split between the capacitors C_1 and C_2. Thus, the overall capacitance can be selected as required heater current flows. This allows more independence in the selection of the inductor L in regard to its current limiting capabilities. FIG. **10***d* illustrates a load circuit for 2 lamps. Essentially, this comprises two separate load circuits according to the embodiment of FIG. **10***c*, both driven by a common toggle circuit such as that described above.

Thus an improved solid-state fluorescent lamp ballast circuit has been shown. Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from the spirit of the invention which is intended to be limited solely by the appended claims.

What is claimed is:

1. A solid-state fluorescent lamp ballast circuit system comprising:
a gaseous discharge lamp;
full-wave rectifying means for supplying a pulsating voltage;
a first switch coupling one side of the output of said rectifying means to one side of said lamp;
a second switch coupling said one rectifying means side to the other side of said lamp;
a third switch coupling the other side of said rectifying means to said one side of said lamp;
a fourth switch coupling said other side of said rectifying means to said other side of said lamp;
trigger means for providing first and second complementary pulse trains, said first pulse train being coupled to said first and fourth switches, said second pulse trains being coupled to said second and third switches; and
reactive means coupling said switching means to said lamp.

2. The invention according to claim **1** wherein said first, second, third and fourth switches comprise gate controlled switches.

3. The invention according to claim **1** wherein said first, second, third and fourth switches comprise regenerative bistable latch type devices.

4. The invention according to claim **1** wherein said first and second switches comprise gate controlled switches and said third and fourth switches comprise transistors.

5. The invention according to claim **1** wherein said first and second switches comprise regernative bistable latch type devices and said third and fourth switches comprise transistors.

6. The invention according to claim **1** wherein said first, second, third and fourth switches comprise transistors.

7. The invention according to claim **6** wherein each of said first, second, third and fourth switches comprises a Darlington pair of transistors.

8. The invention according to claim **1** and further including high voltage isolation means between at least said first and second switches and said first and second output pulse trains from said trigger means.

9. The invention according to claim **8** wherein said isolation means comprise transformers.

10. The invention according to claim **9** wherein said isolation means comprise optical isolation means.

11. The invention according to claim 10 wherein said optical isolation means comprise:

a. A light emitting diode coupled to one of said pulse trains; and

b. a photo transistor adjacent to said diode and coupled to one of said switches.

12. The invention according to claim 8 wherein said isolation means comprises a level shifter transistor.

13. The invention according to claim 1 wherein said ballast reactance comprises an inductor selected to limit the current to said lamp and further including a capacitor shunted across said lamp said capacitor selected to form a tuned circuit with said inductor which has a resonance near the frequency of the output of said trigger means.

14. The invention according to claim 1 wherein said first and second pulse trains have alternating on periods which are separated by a period when both pulse trains are in an off period.

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