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*[Continued on next page]*

(54) Title: SPUTTERING TARGET AND METHOD FOR MANUFACTURING THE SAME, AND TRANSISTOR

FIG. 1A

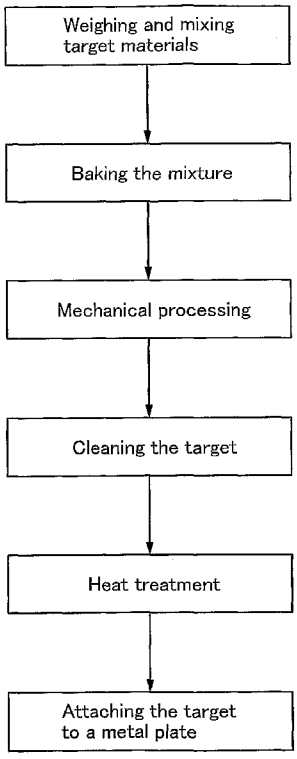


FIG. 1B

FIG. 1C

FIG. 1D

FIG. 1E

FIG. 1F

(57) Abstract: To provide a deposition technique for forming an oxide semiconductor film. An oxide semiconductor film is formed using a sputtering target which contains a sintered body of metal oxide and in which the concentration of hydrogen contained in the sintered body of metal oxide is, for example, as low as 1 $x10^{16}$ atoms/$cm^3$ or lower, so that the oxide semiconductor film contains a small amount of impurities such as a hydrogen atom and a compound containing a hydrogen atom typified by $H_2O$. Further, this oxide semiconductor film is used as an active layer of a transistor.

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DESCRIPTION

# SPUTTERING TARGET AND METHOD FOR MANUFACTURING THE SAME, AND TRANSISTOR

## TECHNICAL FIELD

[0001]

The present invention relates to a sputtering target and a method for manufacturing the sputtering target. In addition, the present invention relates to a transistor manufactured using the sputtering target.

## BACKGROUND ART

[0002]

A transistor formed over a flat plate such as a glass substrate, which is typically used in a liquid crystal display device, is generally formed using a semiconductor material such as amorphous silicon or polycrystalline silicon. A transistor manufactured using amorphous silicon has low field effect mobility, but can be formed over a larger glass substrate. In contrast, a transistor manufactured using polycrystalline silicon has high field effect mobility, but needs a crystallization step such as laser annealing and is not always suitable for being formed over a large glass substrate.

[0003]

In view of the foregoing, a technique in which a transistor is manufactured using an oxide semiconductor as a semiconductor material and applied to an electronic device or an optical device has attracted attention. For example, Patent Document 1 and Patent Document 2 disclose a technique by which a transistor is manufactured using zinc oxide or an In-Ga-Zn-O-based oxide semiconductor as a semiconductor material and such a transistor is used as a switching element or the like of an image display device.

[0004]

A transistor in which a channel formation region (also referred to as a channel region) is provided in an oxide semiconductor can have higher field effect mobility than

a transistor in which amorphous silicon is used. An oxide semiconductor film can be formed by a sputtering method or the like at a relatively low temperature. Its manufacturing process is easier than that of a transistor manufactured using polycrystalline silicon.

[0005]

Transistors which are manufactured using such an oxide semiconductor over a glass substrate, a plastic substrate, or the like are expected to be applied to display devices such as a liquid crystal display, an electroluminescent display (also referred to as an EL display), and electronic paper.

[Reference]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

## DISCLOSURE OF INVENTION

[0007]

However, characteristics of a semiconductor element manufactured using an oxide semiconductor are not yet sufficient. For example, controlled threshold voltage, high operation speed, a relatively easy manufacturing process, and sufficient reliability are required for a transistor manufactured using an oxide semiconductor film.

[0008]

It is an object of one embodiment of the present invention to provide a deposition technique for forming an oxide semiconductor film. In addition, it is an object of one embodiment of the present invention to provide a method for manufacturing a highly reliable semiconductor element in which the oxide semiconductor film is used.

[0009]

The threshold voltage of a transistor in which an oxide semiconductor is used is affected by the density of carriers in the oxide semiconductor film. The carriers in the oxide semiconductor film are generated due to impurities contained in the oxide semiconductor film. For example, impurities such as a compound containing a hydrogen atom typified by water ($H_2O$); a compound containing a carbon atom; a

hydrogen atom; or a hydrogen atom which are contained in the oxide semiconductor film formed causes an increase in the density of the carriers in the oxide semiconductor film.

[0010]

It is difficult to control deterioration over time, such as a shift in the threshold voltage, of a transistor manufactured using the oxide semiconductor film containing impurities such as a hydrogen atom or a compound containing a hydrogen atom typified by water ($H_2O$).

[0011]

The inventors thought that in order to achieve the above-described objects, a conductive film, which contains a small amount of impurities such as a compound containing a hydrogen atom typified by water ($H_2O$) or a hydrogen atom, is used as a conductive film for a source electrode and a drain electrode and is formed over or below an oxide semiconductor film, so that impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film and the purity of the oxide semiconductor film is increased; consequently, deterioration of a transistor over time due to the impurities such as hydrogen or water might be suppressed. The conductive film is processed into a desired shape by etching or the like, so that the source electrode and the drain electrode can be formed.

[0012]

In view of the above, one embodiment of the present invention is to form a conductive film which contains a small amount of impurities by eliminating impurities which affect the density of carriers in a sputtering target used for deposition, for example, impurities such as a hydrogen atom or a compound containing a hydrogen atom typified by water ($H_2O$).

[0013]

A sputtering target according to one embodiment of the present invention is a sputtering target for forming a conductive film. The sputtering target contains a sintered body of a metal material whose electronegativity is lower than that of hydrogen of 2.1. The sintered body contains hydrogen at a concentration of lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

[0014]

Further, a sputtering target according to one embodiment of the present invention is a sputtering target for forming a conductive film. The sputtering target contains a sintered body of a metal material of at least any one of aluminum, copper, chromium, tantalum, titanium, molybdenum, and tungsten. The sintered body contains hydrogen at a concentration lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

[0015]

Further, a sputtering target according to one embodiment of the present invention is a sputtering target for forming a conductive film. The sputtering target contains a sintered body of a metal material in which silicon, titanium, tantalum, tungsten, molybdenum, chromium, neodymium, scandium, or yttrium is mixed with aluminum at 0.1 at.% to 3 at.%. The sintered body contains hydrogen at a concentration lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

[0016]

A transistor according to one embodiment of the present invention includes a conductive film formed using any of the above sputtering targets, in contact with an active layer.

[0017]

A method for manufacturing a sputtering target according to one embodiment of the present invention includes the steps of forming a sintered body of a metal material by baking the metal material, forming a target with a desired shape by machining the sintered body of the metal material, cleaning the target, and performing heat treatment on the target which has been cleaned.

[0018]

A method for manufacturing a sputtering target according to one embodiment of the present invention includes the steps of forming a sintered body of a metal material by baking the metal material, forming a target with a desired shape by machining the sintered body of the metal material, cleaning the target, performing heat treatment on the target which has been cleaned, and attaching the target to a backing plate.

[0019]

Note that in this specification, a sintered body of a metal material which has a

desired shape after being machined is referred to as a "target" in some cases. Further, in some cases, a combination of the target and a backing plate is particularly referred to as a "sputtering target".

[0020]

The ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps and the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0021]

In this specification, "oxynitride" refers to a substance that contains more oxygen atoms than nitrogen atoms and nitride oxide refers to a substance that contains more nitrogen atoms than oxygen atoms. For example, a "silicon oxynitride film" means a film that contains oxygen atoms and nitrogen atoms so that the number of the oxygen atoms is larger than that of the nitrogen atoms and, in the case where measurements are performed using Rutherford backscattering spectrometry (RBS) and hydrogen forward scattering (HFS), contains oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 50 at.% to 70 at.% inclusive, 0.5 at.% to 15 at.% inclusive, 25 at.% to 35 at.% inclusive, and 0.1 at.% to 10 at.% inclusive, respectively. Further, a "silicon nitride oxide film" means a film that contains nitrogen atoms and oxygen atoms so that the number of the nitrogen atoms is larger than that of the oxygen atoms and, in the case where measurements are performed using RBS and HFS, contains oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 5 at.% to 30 at.% inclusive, 20 at.% to 55 at.% inclusive, 25 at.% to 35 at.% inclusive, and 10 at.% to 30 at.% inclusive, respectively. Note that percentages of nitrogen, oxygen, silicon, and hydrogen fall within the ranges given above, where the total number of atoms contained in the silicon oxynitride film or the silicon nitride oxide film is defined as 100 at.%.

[0022]

In this specification and the like, the terms "over" and "below" do not necessarily mean "directly on" and "directly below", respectively, in the description of a physical relationship between components. For example, the expression of "a first gate electrode over a gate insulating layer" does not exclude the case where another

component is interposed between the gate insulating layer and the gate electrode. In addition, the terms "over" and "below" are used only for convenience of the description. Unless otherwise specified, the case where the positions thereof are interchanged is included.

[0023]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" are formed in an integrated manner.

[0024]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification.

[0025]

Note that in this specification, the concentration of hydrogen in a target, an oxide semiconductor film, or a conductive film is measured by secondary ion mass spectrometry (SIMS). Note that it is known that it is difficult, in principle, to obtain correct data in the proximity of a surface of a sample or in the proximity of an interface between stacked films formed using different materials by the SIMS analysis. Thus, in the case where distributions of the hydrogen concentrations of the films in thickness directions are analyzed by SIMS, an average value in a region where the films are provided, the value is not greatly changed, and substantially the same strength can be obtained is employed as the hydrogen concentration. Further, in the case where the thickness of the film is small, a region where substantially the same strength can be obtained cannot be found in some cases due to the influence of the concentration of hydrogen in the films adjacent to each other. In that case, the maximum value or the minimum value of the hydrogen concentration of a region where the films are provided is employed as the hydrogen concentration of the film. Furthermore, in the case where a mountain-shaped peak having the maximum value and a valley-shaped peak having the minimum value do not exist in the region where the films are provided, the value of

the inflection point is employed as the hydrogen concentration.

[0026]

According to one embodiment of the present invention, a sputtering target which contains a small amount of impurities such as a hydrogen atom or a compound containing a hydrogen atom typified by water ($H_2O$) can be provided. Further, a conductive film in which the amount of impurities is reduced can be formed using the sputtering target. Further, a method for manufacturing a highly reliable semiconductor element in which an oxide semiconductor film formed in contact with the conductive film is used as an active layer can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0027]

In the accompanying drawings:

FIGS. 1A to 1F are a flowchart of a method for manufacturing a sputtering target;

FIG. 2A is a plan view of a transistor according to Embodiment and FIG. 2B is a cross-sectional view thereof;

FIGS. 3A to 3E illustrate a manufacturing process of a transistor according to Embodiment;

FIG. 4A is a plan view of a transistor according to Embodiment and FIG. 4B is a cross-sectional view thereof;

FIGS. 5A to 5E illustrate a manufacturing process of a transistor according to Embodiment;

FIGS. 6A and 6B are cross-sectional views of transistors according to Embodiment;

FIGS. 7A to 7E illustrate a manufacturing process of a transistor according to Embodiment;

FIGS. 8A to 8E illustrate a manufacturing process of a transistor according to Embodiment;

FIGS. 9A to 9D illustrate a manufacturing process of a transistor according to Embodiment;

FIGS. 10A to 10D illustrate a manufacturing process of a transistor according

to Embodiment;

FIG. 11 is a cross-sectional view of a transistor according to Embodiment;

FIG. 12 is a cross-sectional view of a transistor including an oxide semiconductor;

FIGS. 13 is an energy band diagrams (schematic diagrams) along an A-A' section in FIG. 12;

FIG. 14A shows a diagram illustrating a state where a positive potential ($V_G>0$) is applied to a gate electrode (GE1) and FIG. 14B is a diagram illustrating a state where a negative potential ($V_G<0$) is applied to the gate electrode (GE1);

FIG. 15 shows a diagram illustrating the relation between the vacuum level and the work function of a metal ($\phi_M$) and between the vacuum level and the electron affinity ($\chi$) of an oxide semiconductor; and

FIGS. 16A to 16F illustrate electronic devices.

## BEST MODE FOR CARRYING OUT THE INVENTION

[0028]

Hereinafter, Embodiments of the present invention will be described in detail below with reference to the accompanying drawings. The present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways without departing from the spirit and scope of the present invention. Note that in the drawings of this specification, the identical portions or portions having a similar function are denoted by the identical reference numerals, and description thereon may be omitted.

[0029]

(Embodiment 1)

In this embodiment, a method for manufacturing a sputtering target (hereinafter, also referred to as a target) that is one embodiment of the present invention will be described with reference to FIGS. 1A to 1F. FIGS. 1A to 1F are a flow chart illustrating an example of a method for manufacturing a sputtering target according to this embodiment.

[0030]

First, target materials are weighed as appropriate, and the weighed target materials are mixed while they are crushed in a ball mill or the like (FIG. 1A). As a material for a target for forming a conductive film, which is described in this embodiment, for example, a material can be used, in which an element which prevents hillocks or whiskers from being generated on an aluminum film, such as silicon (Si), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), scandium (Sc), yttrium (Y), or a lanthanum material is mixed with aluminum (Al) powder at 0.1 at.% to 3 at.%.

[0031]

Note that the material that can be used for the target is not limited to the above materials, and a metal material such as aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), molybdenum (Mo), or tungsten (W) can be used alone or in combination as appropriate. Note that a metal material having a low electronegativity, specifically a metal material having a lower electronegativity than hydrogen, such as aluminum, titanium, chromium, copper, or tantalum, is preferably used, in which case, when a conductive film is formed in contact with an oxide semiconductor film, impurities such as moisture or hydrogen are easily extracted from the oxide semiconductor film. Among the metal materials having a low electronegativity given above, titanium is particularly preferable because of its low contact resistance with an oxide semiconductor film.

[0032]

Alternatively, conductive metal oxide may be used as the target material. As the conductive metal oxide, indium oxide ($In_2O_3$), tin oxide ($SnO_2$), zinc oxide (ZnO), an indium oxide-tin oxide ($In_2O_3$-$SnO_2$, abbreviated to ITO) alloy, an indium oxide-zinc oxide ($In_2O_3$-ZnO) alloy, or the like can be used. Further alternatively, as the target material, silicon or silicon oxide may be added to a metal oxide material.

[0033]

Next, the mixture is formed into a predetermined shape and baked, so that a sintered body of the metal material is obtained (FIG. 1B). When the target material is baked, hydrogen, moisture, hydrocarbon, or the like can be prevented from being mixed into the target. The baking can be performed in an inert gas atmosphere (e.g., a nitrogen atmosphere or a rare gas atmosphere), in vacuum, or in a high-pressure

atmosphere, and may be performed while mechanical pressure is applied. As a baking method, an atmospheric sintering method, a pressure sintering method, or the like can be used as appropriate. A hot pressing method, a hot isostatic pressing (HIP) method, a discharge plasma sintering method, or an impact method is preferably used as a pressure sintering method. Although the maximum temperature of the baking is selected in accordance with the sintering temperature of the target material, it is preferably approximately 1000 °C to 2000 °C, more preferably 1200 °C to 1500 °C. In addition, although the period in which the maximum temperature is held is selected in accordance with the target material, it is preferably 0.5 hours to 3 hours.

[0034]

Note that the filling rate of a metal target of this embodiment is preferably greater than or equal to 90 % and less than or equal to 100 %, more preferably greater than or equal to 95 % and less than or equal to 99.9 %. A metal target with high filling rate makes it possible to remove cavities that allow impurities such as moisture to be adsorbed on the target at the time of sputtering deposition. In addition, during sputtering deposition, generation of nodules can be prevented, uniform discharge can be performed, and generation of particles can be suppressed. Furthermore, the smoothness of a surface of a formed conductive film is favorable.

[0035]

Next, mechanical processing is performed in order to obtain a target having desired dimensions, shape, and surface roughness (FIG. 1C). As a processing means, for example, mechanical polishing, chemical mechanical polishing (CMP), or a combination of these can be used.

[0036]

After that, in order to remove minute dust and components of a grinding solution generated by the mechanical processing, the target is cleaned by ultrasonic cleaning in which the target is soaked in water or an organic solvent, cleaning with running water, or the like (FIG. 1D). By performing cleaning after the mechanical processing, a target from which dust and impurities have been removed can be obtained, and a film with high purity and high quality can be formed using the target.

[0037]

Next, heat treatment is performed on the target after being cleaned (FIG. 1E). The heat treatment is preferably performed in an inert gas atmosphere (e.g., a nitrogen atmosphere or a rare gas atmosphere). The temperature of the heat treatment differs depending on the target material, the temperature at which the target material does not get denatured and hydrogen or moisture on a surface of the target or in the target is sufficiently eliminated is employed. Specifically, the temperature is higher than or equal to 150 °C and lower than or equal to 750 °C, preferably higher than or equal to 425 °C and lower than or equal to 750 °C. The heating period is set so that the concentration of hydrogen in the target can be sufficiently reduced, and specifically is 0.5 hours or more, preferably 1 hour or more. The heat treatment after the cleaning makes it possible to eliminate hydrogen, moisture, or the like mixed into the target due to the cleaning can be eliminated from the target. Note that the heat treatment may be performed in vacuum or in a high-pressure atmosphere.

[0038]

For example, the target is introduced into an electric furnace that is a kind of heat treatment apparatus, heat treatment is performed in a nitrogen atmosphere, and then the target is prevented from being exposed to air so that entry of water or hydrogen into the target is prevented, whereby a target in which the nitrogen concentration is reduced is obtained. Slow cooling is performed in one furnace in a nitrogen atmosphere from heating temperature $T$ to a temperature low enough to prevent entry of water; specifically, the slow cooling is performed in a nitrogen atmosphere until the temperature drops by 100 °C or more from heating temperature $T$. The heat treatment is performed in a helium atmosphere, a neon atmosphere, an argon atmosphere, or the like without limitation to a nitrogen atmosphere.

[0039]

Note that the heat treatment apparatus is not limited to the electric furnace and may be, for example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp,

or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heating an object to be processed by thermal radiation using light emitted from the above-described lamp and by conduction of heat from a gas heated by light emitted from a lamp. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used. In addition, the LRTA apparatus and the GRTA apparatus may be provided with a device that heats the product by heat conduction or heat radiation from not only a lamp but also a heater such as a resistance heater.

[0040]

Note that in the heat treatment, it is preferable that moisture, hydrogen, and the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus be set to be 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0041]

The hydrogen concentration of the metal target described in this embodiment, which is measured by secondary ion mass spectrometry (SIMS), can be $5 \times 10^{19}$ atoms/cm$^3$ or lower, preferably $5 \times 10^{18}$ atoms/cm$^3$ or lower, more preferably $5 \times 10^{17}$ atoms/cm$^3$ or lower or $1 \times 10^{16}$ atoms/cm$^3$ or lower by the heat treatment performed after the cleaning. Thus, the concentration of hydrogen in the conductive film formed using the target can be reduced.

[0042]

After that, the target is attached to a metal plate called a backing plate (FIG. 1F). A backing plate has functions of cooling a target material and being a sputtering electrode, and thus is preferably formed using copper, which is excellent in thermal conductivity and electric conductivity. Alternatively, titanium, a copper alloy, a stainless steel alloy, or the like can be used instead of copper. A cooling path is formed inside or on the back surface of the backing plate, and water, oil, or the like circulates through the cooling path as a coolant; thus, the cooling efficiency of a target at the time of sputtering deposition can be increased. Note that water vaporizes at 100 °C;

therefore, in the case where the temperature of the target needs to be kept at 100 °C or higher, oil or the like is preferable to water.

[0043]

The target can be attached to the backing plate by, for example, electron beam welding. The electron beam welding refers to a method in which electrons generated in a vacuum atmosphere are accelerated, focused, and then delivered to an object, whereby welding can be performed only on a portion which is desired to be welded without damage on the material property of portions of the object except for the welded portion. In the electron beam welding, the shape of the welded portion and the depth of welding can be controlled. Since the welding is performed in vacuum, hydrogen, moisture, hydrocarbon, and the like can be prevented from attaching to the target.

[0044]

As a brazing material for attaching the target to the backing plate, metal (Au), bismuth (Bi), tin (Sn), zinc (Zn), or indium (In), an alloy thereof, a low-melting-point alloy solder, or the like can be preferably used. Note that a metal (or alloy) material with high conductivity is preferably used as a brazing material. Further, a back coat layer may be formed between the brazing material and the target. The formation of the back coat layer makes it possible to improve the adhesion between the target and the backing plate.

[0045]

In this embodiment, an example in which heat treatment after cleaning is performed before the attachment of the target to the backing plate is described; however, the embodiments of the present invention are not limited thereto, and heat treatment may be performed after the attachment of the target and the backing plate or may be performed plural times before and after the attachment. Note that it is preferable that heat treatment after the attachment of the target and the backing plate be performed at higher than or equal to 150 °C and lower than or equal to 350 °C, in consideration of the heat resistance of the brazing material or the backing plate. Heat treatment is preferably performed in an inert gas atmosphere (a nitrogen atmosphere or a rare gas atmosphere).

[0046]

It is preferable that the target which has been subjected to heat treatment be transferred, stored, and the like in a high-purity oxygen gas atmosphere, a high-purity nitrous oxide ($N_2O$) gas atmosphere, or an ultra dry air (having a dew point of −40 °C or lower, preferably −60 °C or lower) atmosphere, in order to prevent entry of moisture or hydrogen. The target may be covered with a protective material formed of a material with low water permeability such as a stainless steel alloy, and the above gas may be introduced into a gap between the protective material and the target. It is preferable that the oxygen gas and the nitrous oxide ($N_2O$) gas do not contain water, hydrogen, and the like. Alternatively, the purity of an oxygen gas or a nitrous oxide ($N_2O$) gas is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (that is, the impurity concentration of the oxygen gas or the nitrous oxide ($N_2O$) gas is 1 ppm or lower, preferably 0.1 ppm or lower).

[0047]

Through the above-described steps, the sputtering target in this embodiment can be manufactured. In the manufacturing process, heat treatment is performed on the sputtering target described in this embodiment after the cleaning, whereby impurities such as a hydrogen atom or a compound containing a hydrogen atom are eliminated, which results in a reduction in impurities. Therefore, the impurities contained in a conductive film formed using the target can also be reduced.

[0048]

The conductive film is used as a conductive film for forming source and drain electrodes of a transistor and is formed over or below an oxide semiconductor film used as an active layer, so that impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film, which allows the purity of the oxide semiconductor film to be increased. As a result, a transistor whose deterioration over time due to impurities such as hydrogen or moisture is suppressed can be manufactured. Further, a metal having a lower electronegativity than hydrogen is used as a material used for the conductive film, so that a larger amount of impurities can be extracted.

[0049]

Note that impurities such as a hydrogen atom may be eliminated by irradiation

using a UV lamp in vacuum instead of heat treatment, or irradiation using a UV lamp and heat treatment may be used in combination.

[0050]

Similarly, the target is set in a sputtering apparatus in an inert gas atmosphere (a nitrogen atmosphere or a rare gas atmosphere) without being exposed to air, so that hydrogen, moisture, hydrocarbon, or the like can be prevented from attaching to the target.

[0051]

After the target is set in the sputtering apparatus, dehydrogenation treatment is preferably performed to remove hydrogen which remains on a surface of or inside the target material. As the dehydrogenation treatment, a method in which the inside of a film formation chamber is heated to 200 °C to 600 °C under reduced pressure, a method in which introduction and removal of nitrogen or an inert gas are repeated while heating is performed, and the like can be given. In this case, not water but oil or the like is preferably used as a coolant for the target. Although a certain level of effect can be obtained when introduction and removal of nitrogen are repeated without heating, it is preferable to perform the treatment while heating is performed. Alternatively, oxygen, an inert gas, or both oxygen and an inert gas may be introduced into the film formation chamber, and plasma of an inert gas and/or oxygen may be generated using high-frequency waves or microwaves. Although a certain level of effect can be obtained when the treatment is performed without heating, it is preferable to perform the treatment while heating is performed.

[0052]

Note that this embodiment can be combined with any of the other Embodiments as appropriate.

[0053]

(Embodiment 2)

In this embodiment, an example of manufacturing a transistor as a semiconductor device manufactured using the target in Embodiment 1 will be described. In a transistor 410 described in this embodiment, a conductive formed using the sputtering target described in Embodiment 1 can be used as a conductive film for forming a source electrode and a drain electrode.

[0054]

One embodiment of a transistor and one embodiment of a method for manufacturing the transistor according to this embodiment will be described with reference to FIGS. 2A and 2B and FIGS. 3A to 3E.

[0055]

Examples of a plan structure and a cross-sectional structure of a transistor are respectively illustrated in FIGS. 2A and 2B. The transistor 410 illustrated in FIGS. 2A and 2B is one of top-gate transistors.

[0056]

FIG. 2A is a plan view of the top-gate transistor 410 and FIG. 2B is a cross-sectional view taken along line C1-C2 in FIG. 2A.

[0057]

The transistor 410 includes, over a substrate 400, an insulating layer 407, an oxide semiconductor layer 412, a source or drain electrode layer 415a, a source or drain electrode layer 415b, a gate insulating layer 402, and a gate electrode layer 411. A wiring layer 414a and a wiring layer 414b are provided in contact with and electrically connect to the source or drain electrode layer 415a and the source or drain electrode layer 415b, respectively.

[0058]

Although the transistor 410 is described as a single-gate transistor, a multi-gate transistor including a plurality of channel formation regions can be formed when needed.

[0059]

A process of manufacturing the transistor 410 over a substrate 400 will be described below with reference to FIGS. 3A to 3E.

[0060]

Although there is no particular limitation on a substrate that can be used as the substrate 400 having an insulating surface, it is necessary that the substrate have at least heat resistance high enough to withstand heat treatment performed later. A glass substrate made of barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0061]

In the case where the temperature of the heat treatment performed later is high, a glass substrate whose strain point is higher than or equal to 730 °C is preferably used. As a material for the glass substrate, for example, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used. Note that, in general, in the case where a larger amount of barium oxide (BaO) than boron oxide is contained, a more practical heat-resistant glass substrate can be obtained. Therefore, a glass substrate containing a larger amount of barium oxide (BaO) than boron oxide ($B_2O_3$) is preferably used.

[0062]

Note that a substrate formed of an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate may be used instead of the above glass substrate. Alternatively, a crystallized glass substrate or the like can be used. Further alternatively, a plastic substrate or the like can be used as appropriate.

[0063]

First, the insulating layer 407 serving as a base film is formed over the substrate 400 having an insulating surface. As the insulating layer 407 that in contact with the oxide semiconductor layer, an oxide insulating layer such as a silicon oxide layer, a silicon oxynitride layer, an aluminum oxide layer, or an aluminum oxynitride layer is preferably used. As a method for forming the insulating layer 407, a plasma CVD method, a sputtering method, or the like can be used; however, it is preferable that the insulating layer 407 be formed by a sputtering method so that the insulating layer 407 does not contain a large amount of hydrogen.

[0064]

In this embodiment, a silicon oxide layer is formed as the insulating layer 407 by a sputtering method. A silicon oxide layer is formed as the insulating layer 407 over the substrate 400 in such a manner that the substrate 400 is transferred to a treatment chamber, a sputtering gas which contains high-purity oxygen and from which hydrogen and moisture have been removed is introduced thereinto, and a silicon target is used. The temperature of the substrate 400 may be room temperature, or the substrate 400 may be heated.

[0065]

For example, a silicon oxide layer is formed by an RF sputtering method under

the conditions that quartz (preferably, synthetic quartz) is used, the substrate temperature is 108°C, the distance between the substrate and the target (T-S distance) is 60 mm, the pressure is 0.4 Pa, the high-frequency power is 1.5 kW, and the atmosphere is an atmosphere containing oxygen and argon (the flow ratio of oxygen to argon is 1:1 (each flow rate is 25 sccm)). The thickness of the silicon oxide layer is 100 nm. Note that instead of quartz (preferably, synthetic quartz), a silicon target can be used as a target for forming the silicon oxide layer. As a sputtering gas, oxygen or a mixed gas of oxygen and argon is used.

[0066]

In this case, it is preferable that the insulating layer 407 be formed while moisture remaining in the treatment chamber is removed so that the insulating layer 407 does not contain hydrogen, hydroxyl groups, or moisture.

[0067]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. An evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated using a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like, for example, are removed; thus, the concentration of impurities in the insulating layer 407 formed in the treatment chamber can be reduced.

[0068]

As a sputtering gas used in forming the insulating layer 407, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0069]

Examples of a sputtering method include an RF sputtering method in which a high-frequency power source is used for a sputtering power supply, a DC sputtering method in which a DC power source is used, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is mainly used in the case where an insulating film is formed, and a DC sputtering method is mainly used in the case where a metal film is formed.

[0070]

In addition, there is also a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be formed to be stacked in the same chamber, or a film of plural kinds of materials can be formed by electric discharge at the same time in the same chamber.

[0071]

In addition, there are a sputtering apparatus provided with a magnet system inside the chamber and used for a magnetron sputtering method, and a sputtering apparatus used for an ECR sputtering method in which plasma generated with the use of microwaves is used without using glow discharge.

[0072]

Further, as examples of a deposition method using a sputtering method, there are a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering method in which a voltage is also applied to a substrate during deposition.

[0073]

The insulating layer 407 can also have a stacked-layer structure. For example, a nitride insulating layer such as a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, or an aluminum nitride oxide layer and the above-described oxide insulating layer may be stacked in this order over the substrate 400.

[0074]

For example, a silicon nitride layer is formed using a silicon target by introducing a sputtering gas which contains high-purity nitrogen and from which hydrogen and moisture have been removed, to a space between the silicon oxide layer and the substrate. In this case also, it is preferable that the silicon nitride layer be formed while moisture remaining in the treatment chamber is removed in a manner similar to that of the silicon oxide layer.

[0075]

Also in the case where the silicon nitride layer is formed, the substrate may be heated at the time of deposition.

[0076]

In the case where the silicon nitride layer and the silicon oxide layer are stacked to form the insulating layer 407, the silicon nitride layer and the silicon oxide layer can be formed in one treatment chamber with the use of the same silicon target. First, a sputtering gas containing nitrogen is introduced and a silicon nitride layer is formed using a silicon target placed inside the treatment chamber, and then the sputtering gas is switched to a sputtering gas containing oxygen and a silicon oxide layer is formed using the same silicon target. Since the silicon nitride layer and the silicon oxide layer can be formed in succession without exposure to air, impurities such as hydrogen or moisture can be prevented from being adsorbed on a surface of the silicon nitride layer.

[0077]

Next, an oxide semiconductor film is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the insulating layer 407.

[0078]

In order that hydrogen, hydroxyl, and moisture are contained as little as possible in the oxide semiconductor film, it is preferable that the substrate 400 over which the insulating layer 407 is formed be preheated in a preheating chamber of the sputtering apparatus, so that impurities such as hydrogen or moisture adsorbed on the substrate 400 are eliminated and removed, as pretreatment for deposition. As an evacuation unit provided for the preheating chamber, a cryopump is preferably used. Note that this preheating treatment can be omitted. This preheating may be similarly performed on the substrate 400 over which the gate insulating layer 402 has not formed yet, or on the substrate 400 over which the source or drain electrode layer 415a and the source or drain electrode layer 415b have not formed yet.

[0079]

Note that before the oxide semiconductor film is formed by a sputtering method, dust attached to a surface of the insulating layer 407 is preferably removed by reverse sputtering in which plasma is generated by introduction of an argon gas. The reverse sputtering refers to a method in which, without application of voltage to a target side, a high-frequency power source is used for application of voltage to a substrate side in an argon atmosphere and plasma is generated in the vicinity of the substrate to

modify a surface. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used.

[0080]

As the oxide semiconductor film, a four-component metal oxide film such as an In-Sn-Ga-Zn-O-based film; a three-component metal oxide film such as an In-Ga-Zn-O-based film, an In-Sn-Zn-O-based film, an In-Al-Zn-O-based film, a Sn-Ga-Zn-O-based film, an Al-Ga-Zn-O-based film, or a Sn-Al-Zn-O-based film; or a two-component metal oxide film such as an In-Zn-O-based film, a Sn-Zn-O-based film, an Al-Zn-O-based film, a Zn-Mg-O-based film, a Sn-Mg-O-based film, or an In-Mg-O-based film; or a single-component metal oxide film such as an In-O-based film, a Sn-O-based film, or a Zn-O-based film can be used. In addition, the above oxide semiconductor film may contain $SiO_2$.

[0081]

As the oxide semiconductor film, a thin film represented by $InMO_3(ZnO)_m$ ($m > 0$) can be used. Here, $M$ represents one or more metal elements selected from gallium (Ga), aluminum (Al), manganese (Mn), and cobalt (Co). For example, $M$ can be gallium (Ga), gallium (Ga) and aluminum (Al), gallium (Ga) and manganese (Mn), gallium (Ga) and cobalt (Co), or the like. An oxide semiconductor film whose composition formula is represented by $InMO_3(ZnO)_m$ ($m > 0$) where at least Ga is contained as $M$ is referred to as the In-Ga-Zn-O-based oxide semiconductor described above, and a thin film thereof is also referred to as an In-Ga-Zn-O-based film.

[0082]

As a sputtering gas used in forming the oxide semiconductor film, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0083]

As a target for forming the oxide semiconductor film by a sputtering method, an oxide semiconductor target for film formation including zinc oxide as a main component can be used. As another example of an oxide semiconductor target for film formation, an oxide semiconductor target for film formation including In, Ga, and Zn (composition ratio of $In_2O_3:Ga_2O_3:ZnO = 1:1:1$ (molar ratio)) can be used. As the

oxide semiconductor target for film formation containing In, Ga, and Zn, a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:2 (molar ratio) or a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:4 (molar ratio) can also be used. The filling rate of the oxide semiconductor target for film formation is higher than or equal to 90 % and lower than or equal to 100 %, preferably higher than or equal to 95 % and lower than or equal to 99.9 %. With the use of the oxide semiconductor target for film formation with a high filling rate, a dense oxide semiconductor film is formed.

[0084]

The oxide semiconductor film is formed over the substrate 400 in such a manner that the substrate is held in the treatment chamber maintained at reduced pressure, a sputtering gas from which hydrogen and moisture have been removed is introduced into the treatment chamber while moisture remaining therein is removed, and metal oxide is used as a target. In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$) (preferably also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced. The substrate may be heated when the oxide semiconductor film is formed.

[0085]

As an example of the deposition condition, the following conditions are employed: the substrate temperature is room temperature, the distance between the substrate and the target is 110 mm, the pressure is 0.4 Pa, and the direct-current (DC) power is 0.5 kW, and the atmosphere is an atmosphere containing oxygen and argon (the flow rate of oxygen is 15 sccm and the flow rate of argon is 30 sccm). Note that a pulsed direct-current (DC) power source is preferably used, in which case powder substances (also referred to as particles or dust) that are generated in deposition can be reduced and the thickness can be uniform. The oxide semiconductor film preferably has a thickness greater than or equal to 5 nm and less than or equal to 30 nm. Note

that the appropriate thickness differs depending on the oxide semiconductor material, and the thickness may be set as appropriate depending on the material.

[0086]

Next, the oxide semiconductor film is processed into an island-shaped oxide semiconductor layer 412 in a first photolithography step (see FIG. 3A). A resist mask for forming the island-shaped oxide semiconductor layer 412 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0087]

Note that the etching of the oxide semiconductor film here may be performed by dry etching, wet etching, or both wet etching and dry etching.

[0088]

As an etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine ($Cl_2$), boron chloride ($BCl_3$), silicon chloride ($SiCl_4$), or carbon tetrachloride ($CCl_4$)) is preferably used.

[0089]

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon tetrafluoride ($CF_4$), sulfur hexafluoride ($SF_6$), nitrogen trifluoride ($NF_3$), or trifluoromethane ($CHF_3$)); hydrogen bromide (HBr); oxygen ($O_2$); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0090]

As the dry etching method, a parallel plate RIE (reactive ion etching) method or an ICP (inductively coupled plasma) etching method can be used. In order to etch the films into desired shapes, the etching conditions (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, and the like) are adjusted as appropriate.

[0091]

As an etchant used for wet etching, a mixed solution of phosphoric acid, acetic acid, and nitric acid, or the like can be used. Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0092]

The etchant used in the wet etching is removed together with the etched materials by cleaning. The waste liquid containing the etchant and the material etched off may be purified and the material may be reused. A material such as indium contained in the oxide semiconductor layer is collected from the waste liquid after the etching and is reused, so that the resources can be efficiently used and the cost can be reduced.

[0093]

The etching conditions (such as an etchant, etching time, and temperature) are adjusted as appropriate depending on the material so that the oxide semiconductor film can be etched into a desired shape.

[0094]

In this embodiment, the oxide semiconductor film is processed into the island-shaped oxide semiconductor layer 412 by a wet etching method using a mixed solution of phosphoric acid, acetic acid, and nitric acid as an etchant.

[0095]

Next, first heat treatment is performed on the oxide semiconductor layer 412. The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and heat treatment is performed on the oxide semiconductor layer at 450 °C in a nitrogen atmosphere for one hour, and then water and hydrogen are prevented from entering the oxide semiconductor layer with the oxide semiconductor layer not exposed to air, so that the oxide semiconductor layer is obtained. Through the first heat treatment, the oxide semiconductor layer 412 can be dehydrated or dehydrogenated, so that the oxide semiconductor layer becomes an intrinsic (i-type) semiconductor or a substantially i-type semiconductor. Thus, deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage can be prevented from being promoted, and off-state current can be reduced.

[0096]

Note that the heat treatment apparatus is not limited to an electronic furnace,

and may be provided with a device that heats an object to be processed by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0097]

For example, as the first heat treatment, GRTA may be performed as follows: the substrate is transferred and put in an inert gas which has been heated to a temperature as high as 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables a high-temperature heat treatment in a short time.

[0098]

Note that in the first heat treatment, it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus be set to be 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0099]

Further, the oxide semiconductor layer might be crystallized to become a microcrystalline film or a polycrystalline film depending on the condition of the first heat treatment or the material for the oxide semiconductor layer. For example, the oxide semiconductor layer might be crystallized to become a microcrystalline oxide semiconductor film having a degree of crystallization of 90 % or more, or 80 % or more. Further, depending on the condition of the first heat treatment and the material for the

oxide semiconductor layer, the oxide semiconductor layer might become an amorphous oxide semiconductor film containing no crystalline component. The oxide semiconductor layer may become an oxide semiconductor film in which a microcrystalline portion (with a grain diameter greater than or equal to 1 nm and greater than or less than 20 nm, typically greater than or equal to 2 nm and less than or equal to 4 nm) is mixed into an amorphous oxide semiconductor.

[0100]

The first heat treatment for the oxide semiconductor layer can be performed on the oxide semiconductor film that has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out of the heating apparatus after the first heat treatment, and then a photolithography step is performed.

[0101]

The heat treatment which has an effect of dehydrating or dehydrogenating the oxide semiconductor layer may be performed at any of the following timings: after the oxide semiconductor layer is formed; after a conductive film is stacked over the oxide semiconductor layer; after the conductive film is patterned into a source electrode and a drain electrode; and after a gate insulating layer is formed over the source electrode and the drain electrode.

[0102]

Note that in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 is provided as the conductive film for forming the source electrode layer and the drain electrode layer. The conductive film is a conductive film in which the hydrogen concentration is reduced; thus, heat treatment is performed after the formation of the conductive film, so that the purity of the oxide semiconductor film can be further increased. In the case where heat treatment is performed after the formation of the conductive film, the temperature of the heat treatment is preferably higher than or equal to 100 °C and lower than 300 °C, more preferably 220 °C to 280 °C.

[0103]

Next, a conductive film is formed over the insulating layer 407 and the oxide semiconductor layer 412. The conductive film is formed by a sputtering method with

the use of the sputtering target described in Embodiment 1. As examples of the material for the conductive film, the following can be given: an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W), an alloy containing any of the elements, an alloy film combining the elements, and the like. Alternatively, one or more materials selected from manganese (Mn), magnesium (Mg), zirconium (Zr), beryllium (Be), and thorium (Th) may be used. Note that a metal having a low electronegativity such as aluminum (Al) or magnesium (Mg), a metal compound, or an alloy is preferably used as the material for the conductive film.

[0104]

Further, the conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon; a two-layer structure of an aluminum film and a titanium film stacked thereover; a three-layer structure of a titanium film, an aluminum film stacked thereover, and a titanium film stacked thereover; and the like can be given. Alternatively, a film, an alloy film, or a nitride film which contains aluminum (Al) and one or more elements selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc) may be used. For example, it is preferable that a conductive film be formed using a metal having a low electronegativity, a metal compound, or an alloy over a conductive film formed using a metal material having low contact resistance with an oxide semiconductor film, such as titanium, tungsten, or molybdenum.

[0105]

The conductive film formed using the target described in Embodiment 1 is used as the conductive film in this embodiment; thus, impurities such as moisture or hydrogen in the oxide semiconductor layer, at an interface between the oxide semiconductor layer and the conductive film, and in the vicinity thereof are absorbed or adsorbed by the conductive film. Thus, elimination of impurities such as moisture or hydrogen makes it possible to obtain an i-type (intrinsic) oxide semiconductor layer or an oxide semiconductor layer that is as close to an i-type oxide semiconductor layer as possible, to prevent deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage, from being promoted, and to reduce

off-state current.

[0106]

Note that in addition to the above structure, heat treatment may be performed in an atmosphere of an inert gas such as nitrogen or a rare gas (e.g., argon or helium) with the conductive film exposed so that moisture or hydrogen adsorbed on a surface of the conductive film or in the conductive film is removed. The temperature range of the heat treatment is higher than or equal to 100 °C and lower than 300 °C, preferably 220 °C to 280 °C. The above heat treatment allows impurities such as moisture or hydrogen in the oxide semiconductor layer, at the interface between the oxide semiconductor layer and the conductive film, and in the vicinity thereof to be absorbed and adsorbed more easily by the conductive film.

[0107]

Next, in a second photolithography step, a resist mask is formed over the conductive film and the conductive film is selectively etched, so that the source or drain electrode layer 415a and the source or drain electrode layer 415b are formed, and then the resist mask is removed (see FIG. 3B). Note that end portions of the source electrode layer and the drain electrode layer are preferably in a tapered shape, in which case the coverage with a gate insulating layer that is stacked thereover can be improved.

[0108]

In this embodiment, as the source or drain electrode layer 415a and the source or drain electrode layer 415b, a titanium film is formed to a thickness of 150 nm by a sputtering method.

[0109]

Note that in order to prevent the oxide semiconductor layer 412 from being removed and the insulating layer 407 therebelow from being exposed at the time of the etching of the conductive film, each material and etching conditions are adjusted as appropriate.

[0110]

In this embodiment, a titanium film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used for the oxide semiconductor layer 412, and an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a

hydrogen peroxide solution) is used as an etchant for the titanium film.

[0111]

Note that, in the second photolithography step, only part of the oxide semiconductor layer 412 is etched in some cases, so that an oxide semiconductor layer having a groove (a depressed portion) is formed. In addition, the resist mask for forming the source electrode layer 415a and the drain electrode layer 415b may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0112]

Ultraviolet light, KrF laser light, or ArF laser light is used for light exposure for forming the resist mask in the second photolithography step. Channel length $L$ of a transistor that is completed later is determined by a distance between bottom ends of the source electrode layer and the drain electrode layer, which are adjacent to each other over the oxide semiconductor layer 412. Note that in the case of a pattern having a channel length $L$ of less than 25 nm, light exposure for forming the resist mask in the second photolithography step is performed using extreme ultraviolet light with an extremely short wavelength of several nanometers to several tens of nanometers. Light exposure using extreme ultraviolet light enables high resolution and deep depth of focus. Thus, the channel length $L$ of the transistor that is completed later can be greater than or equal to 10 nm and less than or equal to 1000 nm and the operation speed of a circuit can be increased and furthermore the value of off-state current is extremely small, so that low power consumption can be achieved.

[0113]

Next, the gate insulating layer 402 is formed over the insulating layer 407, the oxide semiconductor layer 412, the source or drain electrode layer 415a, and the source or drain electrode layer 415b (see FIG. 3C).

[0114]

Here, the oxide semiconductor that is made to be an intrinsic oxide semiconductor or a substantially intrinsic oxide semiconductor (the oxide semiconductor that is purified) by removal of impurities is extremely sensitive to the interface state and the interface electric charge; thus, an interface between the oxide semiconductor and the gate insulating film is important. Therefore, the gate insulating

film (GI) that is in contact with the purified oxide semiconductor needs to have higher quality.

[0115]

For example, a high-density plasma CVD method using microwaves (2.45 GHz) is preferably employed, in which case an insulating film which is dense, has high withstand voltage, and has high quality can be formed. The purified oxide semiconductor and the high-quality gate insulating film are in close contact with each other, whereby the interface state can be reduced and favorable interface characteristics can be obtained.

[0116]

Further, since the insulating film formed with the high-density plasma CVD apparatus can have a uniform thickness, the insulating film has excellent step coverage. Further, with the high-density plasma CVD apparatus, the thickness of a thin insulating film can be controlled precisely.

[0117]

Needless to say, another film formation method such as a sputtering method or a plasma CVD method can be employed as long as the method enables formation of a good-quality insulating film as a gate insulating film. Further, an insulating film whose film quality and characteristic of an interface between the insulating film and an oxide semiconductor are improved by heat treatment performed after the formation of the insulating film may be formed as a gate insulating film. In any case, any insulating film may be used as long as the insulating film has characteristics of enabling reduction in interface state density of an interface between the insulating film and an oxide semiconductor and formation of a favorable interface as well as having favorable film quality as a gate insulating film.

[0118]

Further, when an oxide semiconductor containing impurities is subjected to a gate bias-temperature stress test (BT test) at 85 °C, at a voltage applied to the gate of $2 \times 10^6$ V/cm, for 12 hours, a bond between the impurity and a main component of the oxide semiconductor is cleaved by a high electric field (*B*: bias) and a high temperature (*T*: temperature), and a generated dangling bond induces shift in the threshold voltage

($V_{th}$). In contrast, the present invention makes it possible to obtain a transistor which is stable to a BT test by removing impurities in an oxide semiconductor, especially hydrogen, moisture, and the like as much as possible to obtain a favorable characteristic of an interface between the oxide semiconductor and a gate insulating film as described above.

[0119]

The gate insulating layer can be formed to have a single-layer structure or a stacked-layer structure using a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer.

[0120]

The gate insulating layer is formed using a high-density plasma CVD apparatus. Here, a high-density plasma CVD apparatus refers to an apparatus which can realize a plasma density of $1 \times 10^{11}/cm^3$ or higher. For example, plasma is generated by applying a microwave power of 3 kW to 6 kW, so that an insulating film is formed.

[0121]

A monosilane gas ($SiH_4$), nitrous oxide ($N_2O$), and a rare gas are introduced into a chamber as a source gas to generate high-density plasma at a pressure of 10 Pa to 30 Pa, so that an insulating film is formed over a substrate having an insulating surface, such as a glass substrate. After that, supply of a monosilane gas may be stopped, and nitrous oxide ($N_2O$) and a rare gas may be introduced without exposure to the air to perform plasma treatment on a surface of the insulating film. The plasma treatment performed on the surface of the insulating film by introduction of nitrous oxide ($N_2O$) and a rare gas is performed at least after the insulating film is formed. The insulating film formed through the above process procedure has a small thickness and corresponds to an insulating film whose reliability can be ensured even though it has a thickness less than 100 nm, for example.

[0122]

The flow ratio of a monosilane gas ($SiH_4$) to nitrous oxide ($N_2O$) which are introduced into the chamber is in the range of 1:10 to 1:200. In addition, as a rare gas which is introduced into the chamber, helium, argon, krypton, xenon, or the like can be used. In particular, argon, which is inexpensive, is preferably used.

[0123]

Unlike an insulating film formed using a conventional parallel plate plasma CVD apparatus in many points, the insulating film formed through the above process procedure has an etching rate which is lower than that of the insulating film formed using the conventional parallel plate plasma CVD apparatus by greater than or equal to 10 % or greater than or equal to 20 % in the case where the etching rates with the same etchant are compared with each other. Thus, it can be said that the insulating film obtained with a high-density plasma CVD apparatus is a dense film.

[0124]

In this embodiment, a silicon oxynitride film (also referred to as $SiO_xN_y$ ($x > y > 0$)) having a thickness of 100 nm is used as the gate insulating layer 402. The gate insulating layer 402 is formed in such a manner that monosilane ($SiH_4$), nitrous oxide ($N_2O$), and argon (Ar) are used as film formation gases at flow rate of $SiH_4/N_2O/Ar$ = 250/2500/2500 (sccm) in a high-density plasma CVD apparatus, and plasma is generated by applying a microwave power of 5 kW at a deposition pressure of 30 Pa and a deposition temperature of 325 °C.

[0125]

Alternatively, the gate insulating layer 402 may be formed by a sputtering method. In the case where a silicon oxide film is formed by a sputtering method, a silicon target or a quartz target is used as a target, and oxygen or a mixed gas of oxygen and argon is used as a sputtering gas. The use of a sputtering method makes it possible to prevent the gate insulating layer 402 from containing a large amount of hydrogen.

[0126]

The gate insulating layer 402 can have a structure in which a silicon oxide layer and a silicon nitride layer are stacked in this order over the source or drain electrode layer 415a and the source or drain electrode layer 415b. For example, the gate insulating layer 402 having a thickness of 100 nm may be formed in such a manner that a silicon oxide layer ($SiO_x$ ($x > 0$)) having a thickness of 5 nm to 300 nm inclusive (50 nm in this embodiment) is formed as a first gate insulating layer and a silicon nitride layer ($SiN_y$ ($y > 0$)) having a thickness of 50 nm to 200 nm inclusive (50 nm in this embodiment) is stacked over the first gate insulating layer as a second gate insulating layer by a sputtering method. For example, a silicon oxide layer with a thickness of

100 nm can be formed by an RF sputtering method in an atmosphere containing oxygen and argon (the flow ratio of oxygen to argon is 1:1 (each flow rate is 25 sccm)), under conditions where the pressure is 0.4 Pa, and the high-frequency power is 1.5 kW.

[0127]

Next, a resist mask is formed in a third photolithography step, and part of the gate insulating layer 402 is removed by selective etching, so that an opening 421a and an opening 421b that respectively reach the source or drain electrode layer 415a and the source or drain electrode layer 415b are formed (see FIG. 3D).

[0128]

Next, a conductive film is formed over the gate insulating layer 402 and in and on the openings 421a and 421b. After that, in a fourth photolithography step, the gate electrode layer 411 and the wiring layers 414a and 414b are formed. Note that a resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0129]

The gate electrode layer 411, the wiring layers 414a and 414b can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material which contains any of these materials as a main component.

[0130]

For example, as a two-layer structure of each of the gate electrode layer 411, the wiring layer 414a, and the wiring layer 414b, the following structures are preferable: a two-layer structure of an aluminum layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a titanium nitride layer or a tantalum nitride layer stacked thereover, and a two-layer structure of a titanium nitride layer and a molybdenum layer. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable. Note that the gate electrode layer can be formed using a light-transmitting conductive film. As an example of the light-transmitting conductive film, a light-transmitting conductive oxide

or the like can be given.

[0131]

In this embodiment, as the gate electrode layer 411 and the wiring layers 414a and 414b, a titanium film is formed to a thickness of 150 nm by a sputtering method. Note that the target described in Embodiment 1 may be used as a sputtering target.

[0132]

Next, second heat treatment (preferably at higher than or equal to 100 °C and lower than 300 °C, more preferably, at 220 °C to 280 °C) is performed in an inert gas atmosphere or an oxygen gas atmosphere. In this embodiment, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. The second heat treatment may be performed after a protective insulating layer or a planarization insulating layer is formed over the transistor 410.

[0133]

Heat treatment may be further performed at temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating layer. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened.

[0134]

Through the above-described steps, the transistor 410 including the oxide semiconductor layer 412 in which the concentration of hydrogen, moisture, hydride, or hydroxide is reduced can be formed (see FIG. 3E).

[0135]

In addition, a protective insulating layer or a planarization insulating layer for planarization may be formed over the transistor 410. For example, a protective insulating layer can be formed to have a single-layer structure or a stacked-layer

structure of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer.

[0136]

The planarization insulating layer can be formed of a heat-resistant organic material, such as polyimide, acrylic, polyimide amide, benzocyclobutene, polyamide, or epoxy. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. The planarization insulating layer may be formed by stacking a plurality of insulating films formed of these materials.

[0137]

Note that the siloxane resin corresponds to a resin including a Si-O-Si bond formed using a siloxane-based material as a starting material. The siloxane-based resin may include as a substituent an organic group (e.g., an alkyl group or an aryl group) or a fluoro group. In addition, the organic group may include a fluoro group.

[0138]

There is no particular limitation on the method for forming the planarization insulating layer, and the planarization insulating layer can be formed, depending on the material, by a method such as a sputtering method, an SOG method, a spin coating method, a dipping method, a spray coating method, or a droplet discharge method (such as an inkjet method, screen printing, or offset printing), or with a tool such as a doctor knife, a roll coater, a curtain coater, or a knife coater.

[0139]

In the transistor described in this embodiment, the conductive film used for the source electrode layer and the drain electrode layer is formed using the sputtering target described in Embodiment 1. The conductive film is formed in contact with the oxide semiconductor film used as an active layer, so that impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film, which leads to an increase in the purity of the oxide semiconductor film. Further, moisture remaining in the reaction atmosphere is removed at the time of the formation of the oxide semiconductor film, so that the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Accordingly, the oxide semiconductor film can be stabilized.

[0140]

In the transistor according to one embodiment of the present invention, the carrier density of an oxide semiconductor film used as an active layer is lower than or equal to $1 \times 10^{12}/cm^3$, preferably, lower than or equal to $1 \times 10^{11}/cm^3$. In other words, the carrier density of the oxide semiconductor layer is lower than or equal to the measurement limit and made as close to zero as possible.

[0141]

The purified oxide semiconductor layer is used in the transistor as described above, whereby a transistor in which off-state current is reduced to, for example, $1 \times 10^{-13}$ A or lower can be provided.

[0142]

As an example of a semiconductor material to be compared with an oxide semiconductor, silicon carbide (for example, 4H-SiC) is given. An oxide semiconductor and 4H-SiC has some common features. The carrier density is one example thereof. In accordance with Fermi-Dirac distribution, the density of minority carriers in the oxide semiconductor is estimated to be $1 \times 10^{-7}/cm^3$, which is an extremely low value, similarly to $6.7 \times 10^{-11}/cm^3$ in 4H-SiC. In comparison with the intrinsic carrier density (approximately $1.4 \times 10^{10}/cm^3$) of silicon, it is well understood that the degree is extraordinary.

[0143]

In addition, since the energy band gap of an oxide semiconductor is 3.0 eV to 3.5 eV and the energy band gap of 4H-SiC is 3.26 eV, an oxide semiconductor and silicon carbide are in common in that both are wide-gap semiconductors.

[0144]

On the other hand, there is a significant difference between an oxide semiconductor and silicon carbide. That is the process temperature. Since heat treatment at 1500 °C to 2000 °C is needed for silicon carbide in general, a stacked-layer structure of silicon carbide and a semiconductor element formed using another semiconductor material is difficult to be formed. This is because a semiconductor substrate or a semiconductor element is destroyed with such high temperature. In contrast, an oxide semiconductor can be manufactured through heat treatment at 300 °C

to 500 °C (lower than or equal to the glass transition temperature, approximately 700 °C at maximum); therefore, a semiconductor element can be formed using an oxide semiconductor after an integrated circuit is formed using another semiconductor material.

[0145]

In addition, in the case of using an oxide semiconductor, there is an advantage that a substrate with low heat resistance such as a glass substrate can be used, which is different from the case of silicon carbide. Moreover, an oxide semiconductor can be deposited without high-temperature heat treatment, so that energy cost can be reduced sufficiently as compared with of the case of using silicon carbide.

[0146]

An oxide semiconductor is generally considered as an n-type semiconductor; however, according to one embodiment of the invention disclosed herein, an i-type semiconductor is realized by removal of impurities, particularly water or hydrogen. In this respect, it can be said that one embodiment of the invention disclosed herein includes a novel technical idea because the oxide semiconductor according to one embodiment of the invention is made to be i-type in a manner different from that of silicon or the like which is made to be i-type by addition of impurities.

[0147]

<Electrical Conduction Mechanism of Transistor Including Oxide Semiconductor>

An electrical conduction mechanism of a transistor including an oxide semiconductor will be described with reference to FIG. 12, FIG. 13, FIGS. 14A and 14B, and FIG. 15. Note that the following description is based on the assumption of an ideal situation for easy understanding and does not necessarily reflect a real situation. Note also that the following description is just a consideration and does not affect the validity of the invention.

[0148]

FIG. 12 is a cross-sectional view of a transistor (thin film transistor) including an oxide semiconductor. An oxide semiconductor layer (OS) is provided over a gate electrode (GE1) with a gate insulating layer (GI) interposed therebetween, and a source electrode (S) and a drain electrode (D) are provided thereover. An insulating layer is provided so as to cover the source electrode (S) and the drain electrode (D).

[0149]

FIG. 13 is an energy band diagram (schematic diagram) of the A-A' section in FIG. 12. In FIG. 13, a black circle (●) and a white circle (○) represent an electron and a hole and have electric charges (−q, +q), respectively. With a positive voltage ($V_D$ > 0) applied to the drain electrode, the dashed line shows the case where no voltage is applied to the gate electrode ($V_G$ = 0) and the solid line shows the case where a positive voltage is applied to the gate electrode ($V_G$ > 0). In the case where no voltage is applied to the gate electrode, carriers (electrons) are not injected to the oxide semiconductor side from an electrode because of high potential barrier, so that a current does not flow, which means an off state. On the other hand, when a positive voltage is applied to the gate electrode, potential barrier is lowered, and thus a current flows, which means an on state.

[0150]

FIGS. 14A and 14B are energy band diagrams (schematic diagrams) of the B-B' section in FIG. 12. FIG. 14A illustrates an on state in which a positive voltage ($V_G$ > 0) is applied to the gate electrode (GE1) and carriers (electrons) flow between the source electrode and the drain electrode. FIG. 14B illustrates an off state in which a negative voltage ($V_G$ < 0) is applied to the gate electrode (GE1) and minority carriers do not flow.

[0151]

FIG. 15 illustrates the relationships between the vacuum level and the work function of a metal ($\phi_M$) and between the vacuum level and the electron affinity ($\chi$) of an oxide semiconductor.

[0152]

At normal temperature, electrons in the metal are degenerated and the Fermi level is located in the conduction band. On the other hand, a conventional oxide semiconductor is an n-type semiconductor, in which the Fermi level ($E_F$) is away from the intrinsic Fermi level ($E_i$) located in the middle of a band gap and is located closer to the conduction band. Note that it is known that some hydrogen is a donor in an oxide semiconductor and is one factor causing an oxide semiconductor to be an n-type semiconductor.

[0153]

On the other hand, an oxide semiconductor according to one embodiment of the disclosed invention is an intrinsic (i-type) or a substantially intrinsic oxide semiconductor which is obtained by removing hydrogen that is a factor for an n-type semiconductor from an oxide semiconductor and purifying the oxide semiconductor such that an element other than a main component of the oxide semiconductor (i.e., an impurity element) is prevented from being contained therein as much as possible. In other words, a feature is that a purified i-type (intrinsic) semiconductor, or a semiconductor close thereto, is obtained not by adding an impurity element but by removing an impurity such as hydrogen or water as much as possible. Thus, the Fermi level ($E_F$) can be comparable with the intrinsic Fermi level ($E_i$).

[0154]

It is said that the band gap ($E_g$) of an oxide semiconductor is 3.15 eV and the electron affinity ($\chi$) is 4.3 V. The work function of titanium (Ti) included in the source electrode and the drain electrode is substantially equal to the electron affinity ($\chi$) of the oxide semiconductor. In that case, a Schottky barrier for electrons is not formed at an interface between the metal and the oxide semiconductor.

[0155]

At that time, the electron moves in the vicinity of the interface between the gate insulating layer and the purified oxide semiconductor (the lowest portion of the oxide semiconductor which is stable in terms of energy) as illustrated in FIG. 14A.

[0156]

In addition, as illustrated in FIG. 14B, when a negative potential is applied to the gate electrode (GE1), the value of current is extremely close to zero because holes that are minority carriers are substantially zero.

[0157]

In such a manner, an intrinsic (i-type) or substantially intrinsic oxide semiconductor is obtained by being purified such that an element other than its main element (i.e., an impurity element) is contained as little as possible. Thus, characteristics of the interface between the oxide semiconductor and the gate insulating layer become obvious. For that reason, the gate insulating layer needs to be able to

form a favorable interface with the oxide semiconductor. Specifically, it is preferable to use, for example, an insulating layer formed by a CVD method using high-density plasma generated with a power supply frequency in the range of the VHF band to the microwave band, an insulating layer formed by a sputtering method, or the like.

[0158]

When the oxide semiconductor is purified and the interface between the oxide semiconductor and the gate insulating layer is made favorable, in the case where the transistor has a channel width ($W$) of $1 \times 10^4$ μm and a channel length ($L$) of 3 μm, for example, it is possible to realize an off-state current of $10^{-13}$ A or less and a subthreshold swing (S value) of 0.1 V/dec. (with a 100-nm-thick gate insulating layer).

[0159]

The oxide semiconductor is purified as described above so as to contain an element other than its main element (i.e., an impurity element) as little as possible, so that the thin film transistor can operate in a favorable manner.

[0160]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0161]

(Embodiment 3)

In this embodiment, an example of manufacturing a transistor as a semiconductor device which is manufactured using the target in Embodiment 1 will be described. Note that the same portions as in Embodiment 2 or portions having functions similar to those in Embodiment 2, and steps for forming such portions may be similar to those in Embodiment 2, and description thereof will not be repeated. In a transistor 460 described in this embodiment, a conductive film which is formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0162]

One embodiment of a transistor and one embodiment of a method for manufacturing the transistor in this embodiment will be described with reference to FIGS. 4A and 4B and FIGS. 5A to 5E.

[0163]

An example of a plan structure and a cross-sectional structure of a transistor are illustrated in FIGS. 4A and 4B, respectively. The transistor 460 illustrated in FIGS. 4A and 4B is one of top-gate transistors.

[0164]

FIG. 4A is a plan view of the top-gate transistor 460, and FIG. 4B is a cross-sectional view taken along line D1-D2 in FIG. 4A.

[0165]

The transistor 460 includes an insulating layer 457, a source or drain electrode layer 465a (465a1 and 465a2), an oxide semiconductor layer 462, a source or drain electrode layer 465b, a wiring layer 468, a gate insulating layer 452, and a gate electrode layer 461 (461a and 461b) over a substrate 450 having an insulating surface. The source or drain electrode layer 465a (465a1 and 465a2) is electrically connected to a wiring layer 464 through the wiring layer 468. Further, although not illustrated, the source or drain electrode layer 465b is electrically connected to a wiring layer through an opening provided in the gate insulating layer 452.

[0166]

Hereinafter, a process of manufacturing the transistor 460 over the substrate 450 will be described with reference to FIGS. 5A to 5E.

[0167]

First, the insulating layer 457 that serves as a base film is formed over the substrate 450 having an insulating surface.

[0168]

In this embodiment, a silicon oxide layer is formed as the insulating layer 457 by a sputtering method. The silicon oxide layer is formed as the insulating layer 457 over the substrate 450 in such a manner that the substrate 450 is transferred to a treatment chamber, a sputtering gas which contains high-purity oxygen from which hydrogen and moisture have been removed is introduced, and a silicon target or quartz (preferably synthetic quartz) is used. As a sputtering gas, an oxygen gas or a mixed gas of oxygen and argon is used.

[0169]

For example, a silicon oxide layer is formed by an RF sputtering method under

conditions that the purity of a sputtering gas is 6N; quartz (preferably synthetic quartz) is used; the substrate temperature is 108 °C; the distance between the substrate and the target (the T-S distance) is 60 mm; the pressure is 0.4 Pa; the high frequency power is 1.5 kW; and the atmosphere is an atmosphere containing oxygen and argon (the flow ratio of oxygen to argon is 1:1 (each flow rate is 25 sccm)). The thickness of the silicon oxide layer is 100 nm. Note that instead of quartz (preferably, synthetic quartz), a silicon target can be used as a target for forming the silicon oxide layer.

[0170]

In that case, the insulating layer 457 is preferably formed while moisture remaining in the treatment chamber is removed in order to prevent hydrogen, hydroxyl groups, or moisture from being contained in the insulating layer 457. From the treatment chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed, whereby the concentration of impurities in the insulating layer 457 formed in the treatment chamber can be reduced.

[0171]

As a sputtering gas used for forming the insulating layer 457, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0172]

The insulating layer 457 may have a stacked-layer structure and, for example, may have a stacked-layer structure in which a nitride insulating layer such as a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, or an aluminum nitride oxide layer and the above-described oxide insulating layer are stacked in this order over the substrate 450.

[0173]

For example, a silicon nitride layer is formed using a silicon target by introducing a sputtering gas which contains high-purity nitrogen and from which hydrogen and moisture have been removed, to a space between the silicon oxide layer and the substrate. In this case also, it is preferable that the silicon nitride layer be formed while moisture remaining in the treatment chamber is removed in a manner

similar to that of the silicon oxide layer.

[0174]

Next, a conductive film is formed over the insulating layer 457 by a sputtering method with the use of the sputtering target described in Embodiment 1, a resist mask is formed over the conductive film in a first photolithography step, and the conductive film is selectively etched, so that the source or drain electrode layers 465a1 and 465a2 are formed, and then the resist mask is removed (see FIG. 5A). The source or drain electrode layers 465a1 and 465a2 are a continuous film although illustrated as being separated in the cross-sectional view. Note that end portions of the formed source or drain electrode layers 465a1 and 465a2 are preferably in a tapered shape, in which case the coverage with a gate insulating layer that is stacked thereover can be improved.

[0175]

As the material for the source or drain electrode layers 465a1 and 465a2, there are an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W), an alloy containing any of these elements as a component, an alloy in which any of these elements are combined, and the like. Alternatively, one or more materials selected from manganese (Mn), magnesium (Mg), zirconium (Zr), beryllium (Be), and thorium (Th) may be used. Note that a metal material having lower electronegativity than hydrogen is preferably contained, in which case an effect of extracting impurities from the oxide semiconductor film can be more effective. Further, the conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon; a two-layer structure of an aluminum film and a titanium film stacked thereover; a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order; and the like can be given. Alternatively, a film, an alloy film, or a nitride film of a combination of Al and one or more elements selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc) may be used.

[0176]

In this embodiment, as the source or drain electrode layers 465a1 and 465a2, a titanium film is formed to a thickness of 150 nm by a sputtering method using the target

described in Embodiment 1.

[0177]

Then, an oxide semiconductor film is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the insulating layer 457.

[0178]

Next, the oxide semiconductor film is processed into an island-shaped oxide semiconductor layer 462 in a second photolithography step (see FIG. 5B). In this embodiment, the oxide semiconductor film is formed by a sputtering method with the use of an In-Ga-Zn-O-based oxide semiconductor target for film formation.

[0179]

The oxide semiconductor film is formed over the substrate 450 in such a manner that the substrate is held in a treatment chamber maintained at reduced pressure, a sputtering gas from which hydrogen and moisture have been removed is introduced into the treatment chamber while the moisture remaining therein is removed, metal oxide is used as a target. In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$) (preferably also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced. Further, the substrate may be heated to 100 °C to 400 °C at the time of forming the oxide semiconductor film.

[0180]

As a sputtering gas used for forming the oxide semiconductor film, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0181]

As an example of the deposition condition, the following conditions are employed: the distance between the substrate and the target is 110 mm, the pressure is

0.4 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an atmosphere containing oxygen and argon (the flow rate of oxygen is 15 sccm and the flow rate of argon is 30 sccm). Note that a pulsed direct-current (DC) power source is preferably used, in which case powder substances (also referred to as particles or dust) that are generated in deposition can be reduced and the thickness can be uniform. The oxide semiconductor film preferably has a thickness greater than or equal to 5 nm and less than or equal to 30 nm. Note that the appropriate thickness differs depending on the oxide semiconductor material, and the thickness may be set as appropriate depending on the material.

[0182]

In this embodiment, the oxide semiconductor film is processed into the island-shaped oxide semiconductor layer 462 by a wet etching method using a mixed solution of phosphoric acid, acetic acid, and nitric acid as an etchant.

[0183]

In this embodiment, first heat treatment is performed on the oxide semiconductor layer 462. The temperature of the first heat treatment is higher than or equal to 100 °C and lower than or equal to 450 °C. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and heat treatment is performed on the oxide semiconductor layer at 450 °C in a nitrogen atmosphere for one hour, and then water and hydrogen are prevented from entering the oxide semiconductor layer with the oxide semiconductor layer not exposed to air; thus, the oxide semiconductor layer is obtained. Through the first heat treatment, the oxide semiconductor layer 462 can be dehydrated or dehydrogenated.

[0184]

The conductive film formed using the target described in Embodiment 1 is used as the conductive film in this embodiment; thus, impurities such as moisture or hydrogen in the oxide semiconductor layer or the insulating layer, at an interface between the oxide semiconductor layer and the insulating layer, and in the vicinity thereof are absorbed or adsorbed by the conductive film. Thus, elimination of impurities such as moisture or hydrogen makes it possible to obtain an i-type (intrinsic) oxide semiconductor layer or an oxide semiconductor layer that is as close to an i-type

oxide semiconductor layer as possible, and deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage, can be prevented from being promoted and off-state current can be reduced.

[0185]

Note that the heat treatment apparatus is not limited to an electronic furnace, and may be provided with a device that heats an object by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. For example, as the first heat treatment, GRTA may be performed as follows: the substrate is transferred and put in an inert gas which has been heated to a temperature as high as 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables a high-temperature heat treatment in a short time.

[0186]

Note that in the first heat treatment, it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus be set to be 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0187]

Further, the oxide semiconductor layer might be crystallized to become a microcrystalline film or a polycrystalline film depending on the condition of the first heat treatment or the material for the oxide semiconductor layer.

[0188]

The first heat treatment for the oxide semiconductor layer can be performed on the oxide semiconductor film that has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out of the heating apparatus after the first heat treatment, and then a photolithography step is performed.

[0189]

The heat treatment having an effect of dehydration or dehydrogenation of the oxide semiconductor layer may be performed at any of the following timings: after the oxide semiconductor layer is formed; after a source electrode and a drain electrode are further stacked over the oxide semiconductor layer; and after a gate insulating layer is formed over the source electrode and the drain electrode.

[0190]

Next, a conductive film is formed over the insulating layer 457 and the oxide semiconductor layer 462 by a sputtering method with the use of the sputtering target described in Embodiment 1, a resist mask is formed over the conductive film in a third photolithography step, and the conductive film is selectively etched, so that the source or drain electrode layer 465b and the wiring layer 468 are formed, and then the resist mask is removed (see FIG. 5C). The source or drain electrode layer 465b and the wiring layer 468 may be formed using a material and through a step that are similar to those of the source or drain electrode layers 465a1 and 465a2.

[0191]

In this embodiment, a titanium film with a thickness of 150 nm is formed as the source or drain electrode layer 465b and the wiring layer 468 by a sputtering method. In this embodiment, the same titanium films are used for the source and drain electrode layers 465a1 and 465a2 and the source or drain electrode layer 465b; thus, the etching rate of the source or drain electrode layers 465a1 and 465a2 is the same or substantially the same as that of the source or drain electrode layer 465b. For that reason, the wiring layer 468 is provided over a part of the source or drain electrode layer 465a2 which is not covered with the oxide semiconductor layer 462 so that the source and drain electrode layers 465a1 and 465a2 are prevented from being etched at the time of etching of the source or drain electrode layer 465b. In the case of using different materials which provide high selectivity ratio of the source or drain electrode layer 465b to the source or drain electrode layer 465a1 and 465a2 in the etching step, the wiring layer 468 which protects the source or drain electrode layer 465a2 in etching is not necessarily provided.

[0192]

Note that in order to prevent the oxide conductive layer 462 from being removed at the time of etching of the conductive film, materials and etching conditions

of the conductive film and the oxide semiconductor layer 462 are adjusted as appropriate.

[0193]

In this embodiment, a titanium film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used for the oxide semiconductor layer 462, and an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant.

[0194]

Note that, in the third photolithography step, only part of the oxide semiconductor layer 462 is etched in some cases, so that an oxide semiconductor layer having a groove (a depressed portion) is formed. In addition, the resist mask for forming the source or drain electrode layer 465b and the wiring layer 468 may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0195]

Next, a gate insulating layer 452 is formed over the insulating layer 457, the oxide semiconductor layer 462, the source or drain electrode layers 465a1 and 465a2, the source or drain electrode layer 465b, and the wiring layer 468.

[0196]

The gate insulating layer 452 can be formed in a single layer or a stacked layer using a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer by a plasma CVD method, a sputtering method, or the like. In order to prevent the gate insulating layer 452 from containing a large amount of hydrogen, the gate insulating layer 452 is preferably formed by a sputtering method. In the case where a silicon oxide film is formed by a sputtering method, a silicon target or a quartz target is used as a target, and oxygen or a mixed gas of oxygen and argon is used as a sputtering gas.

[0197]

The gate insulating layer 452 can have a structure in which a silicon oxide layer and a silicon nitride layer are stacked in this order over the source or drain electrode layers 465a1 and 465a2 and the source or drain electrode layer 465b. In this embodiment, a silicon oxide layer with a thickness of 100 nm is formed by an RF

sputtering method under the conditions that the pressure is 0.4 Pa, the high-frequency power is 1.5 kW, and the atmosphere is an atmosphere containing oxygen and argon (the flow ratio of oxygen to argon is 1:1 (each flow rate is 25 sccm)).

[0198]

Next, a resist mask is formed in a fourth photolithography step, and part of the gate insulating layer 452 is removed by selective etching, so that an opening 423 that reaches the wiring layer 468 is formed (see FIG. 5D). Although not illustrated, an opening that reaches the source or drain electrode layer 465b may be formed at the time of forming the opening 423. In this embodiment, an example is described in which the opening that reaches the source or drain electrode layer 465b is formed after an interlayer insulating layer is further stacked, and then a wiring layer for electric connection is formed in the opening.

[0199]

Next, a conductive film is formed over the gate insulating layer 452 and in and on the opening 423. After that, in a fifth photolithography step, the gate electrode layer 461 (461a and 461b) and the wiring layer 464 are formed. Note that a resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0200]

The gate electrode layer 461 (461a and 461b) and the wiring layer 464 can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which contains any of these materials as a main component. The target described in Embodiment 1 may be used as a sputtering target for forming the gate electrode layer 461 (461a and 461b) and the wiring layer 464.

[0201]

In this embodiment, as the gate electrode layer 461 (461a and 461b) and the wiring layer 464, a titanium film is formed to a thickness of 150 nm by a sputtering method.

[0202]

Next, second heat treatment (for example, at higher than or equal to 100 °C and

lower than 300 °C, preferably, at 220 °C to 280 °C) is performed in an inert gas atmosphere or an oxygen gas atmosphere. In this embodiment, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. The second heat treatment may be performed after a protective insulating layer or a planarization insulating layer is formed over the transistor 460.

[0203]

Heat treatment may be further performed at temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating layer. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened.

[0204]

Through the above-described steps, the transistor 460 including the oxide semiconductor layer 462 in which the concentration of hydrogen, moisture, hydride, or hydroxide is reduced can be formed (see FIG. 5E).

[0205]

A protective insulating layer or a planarization insulating layer for planarization may be provided over the transistor 460. Although not illustrated, an opening that reaches the source or drain electrode layer 465b is formed in the gate insulating layer 452 and the protective insulating layer or the planarization insulating layer, and a wiring layer that is electrically connected to the source or drain electrode layer 465b is formed in the opening.

[0206]

In the transistor described in this embodiment, the conductive film used for the source and drain electrode layers is formed using the sputtering target described in Embodiment 1. The conductive film is formed in contact with the oxide

semiconductor film, so that impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film, which leads to an increase in the purity of the oxide semiconductor film. Further, moisture remaining in the reaction atmosphere is removed at the time of the formation of the oxide semiconductor film, so that the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Accordingly, the oxide semiconductor film can be stabilized.

[0207]

The purified oxide semiconductor layer is used in the transistor as described above, whereby a transistor in which off-state current is reduced can be provided.

[0208]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0209]

(Embodiment 4)

In this embodiment, an example of manufacturing a transistor with the use of the target in Embodiment 1 will be described. Note that the same portions as in Embodiment 2 or portions having functions similar to those in Embodiment 2, and steps for forming such portions may be similar to those in Embodiment 2, and description thereof will not be repeated. In each of transistors 425 and 426 described in this embodiment, a conductive film which is formed using the sputtering target described in Embodiment 1 can be used as a conductive film for the source or drain electrode layer 415a and the source or drain electrode layer 415b.

[0210]

The transistors in this embodiment will be described with reference to FIGS. 6A and 6B.

[0211]

FIGS. 6A and 6B each illustrate an example of a cross-sectional structure of the transistor. Each of the transistors 425 and 426 illustrated in FIGS. 6A and 6B is a transistor having a structure in which an oxide semiconductor layer is sandwiched between a conductive layer and a gate electrode layer.

[0212]

In FIGS. 6A and 6B, a silicon substrate is used as a substrate, and the

transistors 425 and 426 are provided over an insulating layer 422 that is formed over a silicon substrate 420.

[0213]

In FIG. 6A, a conductive layer 427 is provided between an insulating layer 407 and the insulating layer 422 provided over the silicon substrate 420, so as to overlap with at least the entire oxide semiconductor layer 412.

[0214]

Note that FIG. 6B illustrates an example in which a conductive layer between the insulating layer 422 and the insulating layer 407 is processed like a conductive layer 424 by etching and is overlapped with part of the oxide semiconductor layer 412, which includes at least the channel formation region.

[0215]

As the conductive layers 427 and 424, a metal material which can withstand the temperature of heat treatment performed later may be used; an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), an alloy including any of the above elements as a component, an alloy film containing a combination of any of these elements, nitride containing any of the above elements as a component, or the like can be used. In addition, the conductive layers 427 and 424 may each have a single-layer structure or a stacked-layer structure. For example, a single-layer structure of a tungsten layer, a stacked-layer structure including a tungsten nitride layer and a tungsten layer, or the like can be used.

[0216]

The conductive layers 427 and 424 may have the same potential as or have potential different from that of a gate electrode layer 411 of the transistors 425 and 426 and can function as a second gate electrode layer. In addition, the potential of the conductive layers 427 and 424 may be fixed potential such as GND or 0 V.

[0217]

The conductive layers 427 and 424 make it possible to control the electric characteristics of the transistors 425 and 426, respectively.

[0218]

The purified oxide semiconductor layer is used in the transistors as described

above, whereby transistors in which off-state current is reduced can be provided.

[0219]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0220]

(Embodiment 5)

In this embodiment, another example of a transistor manufactured using the target described in Embodiment 1 will be described. In a transistor 390 described in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0221]

FIGS. 7A to 7E illustrate examples of cross-sectional structures of the transistor in this embodiment. The transistor 390 illustrated in FIG. 7E is a bottom-gate transistor and is also called an inverted staggered transistor.

[0222]

Although the transistor 390 is described as a single-gate transistor, the transistor 390 can be manufactured as a multi-gate transistor including a plurality of channel formation regions as necessary.

[0223]

A process of manufacturing the transistor 390 over a substrate 394 will be described below with reference to FIGS. 7A to 7E.

[0224]

First, a conductive film is formed over the substrate 394 having an insulating surface, and then a gate electrode layer 391 is formed in a first photolithography step. End portions of the formed gate electrode layer are preferably in a tapered shape, in which case the coverage with a gate insulating layer that is stacked thereover can be improved. Note that a resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0225]

Although there is no particular limitation on a substrate that can be used as the

substrate 394 having an insulating surface, the substrate needs to have at least heat resistance high enough to withstand heat treatment performed later. A glass substrate made of barium borosilicate glass, aluminoborosilicate glass, or the like can be used as the substrate 394 having an insulating surface.

[0226]

In the case where a glass substrate is used and the temperature of the heat treatment performed later is high, a glass substrate whose strain point is higher than or equal to 730 °C is preferably used. As a material for the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that in general, when a glass substrate contains more barium oxide (BaO) than boron oxide, the glass substrate can be more practical and heat resistant. For that reason, a glass substrate containing BaO and $B_2O_3$ in which the amount of BaO is larger than that of $B_2O_3$ is preferably used.

[0227]

Note that a substrate formed of an insulator, such as a ceramic substrate, a quartz glass substrate, a quartz substrate, or a sapphire substrate, may be used instead of the above glass substrate. Alternatively, a crystallized glass substrate or the like can be used. Further alternatively, a plastic substrate or the like can be used as appropriate.

[0228]

An insulating film that serves as a base film may be provided between the substrate 394 and the gate electrode layer 391. The base film has a function of preventing diffusion of an impurity element from the substrate 394, and can be formed to have a single-layer structure or a stacked-layer structure using one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0229]

The gate electrode layer 391 can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy that contains any of these materials as a main component.

[0230]

As a two-layer structure of the gate electrode layer 391, the following

structures are preferable: a two-layer structure in which a molybdenum layer is stacked over an aluminum layer, a two-layer structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer and a molybdenum layer are stacked, and a two-layer structure in which a tungsten nitride layer and a tungsten layer are stacked. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable. Note that the gate electrode layer can be formed using a light-transmitting conductive film. As an example of the light-transmitting conductive film, light-transmitting conductive oxide or the like can be given.

[0231]

Next, a gate insulating layer 397 is formed over the gate electrode layer 391.

[0232]

The gate insulating layer 397 can be formed to have a single-layer structure or a stacked-layer structure using one or more of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, and an aluminum oxide layer by a plasma CVD method, a sputtering method, or the like. The gate insulating layer 397 is preferably formed by a sputtering method so that a large amount of hydrogen is prevented from being contained in the gate insulating layer 397. In the case of forming a silicon oxide film by a sputtering method, a silicon target or a quartz target is used as a target, and oxygen or a mixed gas of oxygen and argon is used as a sputtering gas. Alternatively, the sputtering target described in Embodiment 1 can be used as a sputtering target for forming the gate insulating layer.

[0233]

The gate insulating layer 397 can have a structure in which a silicon nitride layer and a silicon oxide layer are stacked over the gate electrode layer 391 in that order. For example, a silicon nitride layer ($SiN_y$ ($y > 0$)) with a thickness greater than or equal to 50 nm and less than or equal to 200 nm (50 nm in this embodiment) is formed as a first gate insulating layer by a sputtering method and a silicon oxide layer ($SiO_x$ ($x > 0$)) with a thickness greater than or equal to 5 nm and less than or equal to 300 nm (50 nm

in this embodiment) is stacked as a second gate insulating layer over the first gate insulating layer, whereby the gate insulating layer with a thickness of 100 nm is formed.

[0234]

Pretreatment for deposition is preferably performed so that hydrogen, hydroxyl groups, and moisture are contained as little as possible in the gate insulating layer 397 and an oxide semiconductor film 393 formed later. For example, the substrate 394 over which the gate electrode layer 391 is formed or the substrate 394 over which the gate electrode layer 391 and the gate insulating layer 397 are formed is preheated in a preheating chamber in a sputtering apparatus so that impurities such as hydrogen or moisture attached to the substrate 394 are eliminated and removed. The temperature of the preheating is higher than or equal to 100 °C and lower than or equal to 400 °C, preferably higher than or equal to 150 °C and lower than or equal to 300 °C. As an evacuation unit provided for the preheating chamber, a cryopump is preferably used. This preheating step can be omitted. This preheating may be performed in a similar manner on the substrate 394 over which layers up to and including a source electrode layer 395a and a drain electrode layer 395b are formed before formation of an oxide insulating layer 396.

[0235]

Next, the oxide semiconductor film 393 is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the gate insulating layer 397 (see FIG. 7A).

[0236]

Note that before the oxide semiconductor film 393 is formed by a sputtering method, dust attached to a surface of the gate insulating layer 397 is preferably removed by reverse sputtering in which plasma is generated by introduction of an argon gas. The reverse sputtering is a method in which voltage is applied to a substrate side, not to a target side, using an RF power source in an argon atmosphere and plasma is generated in the vicinity of the substrate so that a substrate surface is modified. Note that a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used instead of an argon atmosphere.

[0237]

The oxide semiconductor film 393 is formed by a sputtering method. As the oxide semiconductor film 393, the following can be used: an In-Ga-Zn-O-based oxide semiconductor film, an In-Sn-Zn-O-based oxide semiconductor film, an In-Al-Zn-O-based oxide semiconductor film, a Sn-Ga-Zn-O-based oxide semiconductor film, an Al-Ga-Zn-O-based oxide semiconductor film, a Sn-Al-Zn-O-based oxide semiconductor film, an In-Sn-O-based oxide semiconductor film, an In-Zn-O-based oxide semiconductor film, a Sn-Zn-O-based oxide semiconductor film, an Al-Zn-O-based oxide semiconductor film, an In-O-based oxide semiconductor film, a Sn-O-based oxide semiconductor film, or a Zn-O-based oxide semiconductor film. In this embodiment, the oxide semiconductor film 393 is formed by a sputtering method using an In-Ga-Zn-O-based oxide semiconductor target for film formation. The oxide semiconductor film 393 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas (typically, argon) and oxygen. In the case of using a sputtering method, the oxide semiconductor film may be formed using a target containing $SiO_2$ at greater than or equal to 2 wt% and less than or equal to 10 wt%.

[0238]

As a target for forming the oxide semiconductor film 393 by a sputtering method, a metal oxide target containing zinc oxide as a main component can be used. As another example of the metal oxide target, an oxide semiconductor target for film formation containing In, Ga, and Zn (the composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:1 (molar ratio)) or the like can be used. As the oxide semiconductor target for film formation containing In, Ga, and Zn, a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:2 (molar ratio) or a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:4 (molar ratio) can also be used. In addition, the filling factor of the oxide semiconductor target for film formation is greater than or equal to 90 % and less than or equal to 100 %, preferably greater than or equal to 95 % and less than or equal to 99.9 %. An oxide semiconductor film which is formed using an oxide semiconductor target for film formation, which has a high filling factor, is dense.

[0239]

The oxide semiconductor film 393 is formed over the substrate 394 in such a

manner that the substrate is held in a treatment chamber maintained at reduced pressure and is heated to room temperature or a temperature lower than 400 °C, then a sputtering gas from which hydrogen and moisture have been removed is introduced into the treatment chamber while moisture remaining therein is removed, and metal oxide is used as a target. In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$) (preferably also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced. Sputtering film formation is performed while moisture remaining in the treatment chamber is removed using a cryopump, whereby the substrate temperature in forming the oxide semiconductor film 393 can be in the range of room temperature to a temperature lower than 400 °C.

[0240]

As an example of the deposition condition, the following conditions are employed: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of oxygen flow: 100 %). Note that a pulsed direct-current (DC) power source is preferably used, in which case powder substances (also referred to as particles or dust) that are generated in deposition can be reduced and the thickness can be uniform. The oxide semiconductor film preferably has a thickness greater than or equal to 5 nm and less than or equal to 30 nm. Note that the appropriate thickness differs depending on the oxide semiconductor material, and the thickness may be set as appropriate depending on the material.

[0241]

Examples of a sputtering method include an RF sputtering method in which a high-frequency power source is used for a sputtering power source, a DC sputtering method in which a direct-current power source is used, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is

mainly used in the case where an insulating film is formed, and a DC sputtering method is mainly used in the case where a metal film is formed.

[0242]

In addition, there is also a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be formed to be stacked in the same chamber, or a film of plural kinds of materials can be formed by electric discharge at the same time in the same chamber.

[0243]

In addition, there are a sputtering apparatus provided with a magnet system inside the chamber and used for a magnetron sputtering method, or a sputtering apparatus used for an ECR sputtering method in which plasma generated with the use of microwaves is used without using glow discharge.

[0244]

Furthermore, as a deposition method using a sputtering method, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering method in which voltage is also applied to a substrate during deposition.

[0245]

Next, in a second photolithography step, the oxide semiconductor film is processed into an island-shaped oxide semiconductor layer 399 (see FIG. 7B). Note that a resist mask for forming the island-shaped oxide semiconductor layer 399 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0246]

In the case where a contact hole is formed in the gate insulating layer 397, the contact hole can be formed at the time of the formation of the oxide semiconductor layer 399.

[0247]

Note that the etching of the oxide semiconductor film 393 here may be performed by dry etching, wet etching, or both wet etching and dry etching.

[0248]

As an etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine ($Cl_2$), boron chloride ($BCl_3$), silicon chloride ($SiCl_4$), or carbon tetrachloride ($CCl_4$)) is preferably used.

[0249]

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon tetrafluoride ($CF_4$), sulfur hexafluoride ($SF_6$), nitrogen trifluoride ($NF_3$), or trifluoromethane ($CHF_3$)); hydrogen bromide (HBr); oxygen ($O_2$); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0250]

As the dry etching method, a parallel plate RIE (reactive ion etching) method or an ICP (inductively coupled plasma) etching method can be used. In order to etch the film into a desired shape, the etching conditions (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, and the like) are adjusted as appropriate.

[0251]

As an etchant used for wet etching, a mixed solution of phosphoric acid, acetic acid, and nitric acid, or the like can be used. Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0252]

The etchant used in the wet etching is removed together with the etched materials by cleaning. The waste liquid containing the etchant and the material etched off may be purified and the material may be reused. A material such as indium contained in the oxide semiconductor layer is collected from the waste liquid after the etching and is reused, so that the resources can be efficiently used and the cost can be reduced.

[0253]

The etching conditions (such as an etchant, etching time, and temperature) are adjusted as appropriate depending on the material so that the oxide semiconductor film can be etched into a desired shape.

[0254]

Note that before formation of a conductive film in the subsequent step, reverse sputtering is preferably performed so that a resist residue or the like attached to surfaces of the oxide semiconductor layer 399 and the gate insulating layer 397 is removed.

[0255]

Next, a conductive film is formed over the gate insulating layer 397 and the oxide semiconductor layer 399. The conductive film is formed by a sputtering method with the use of the sputtering target described in Embodiment 1. As examples of the material for the conductive film, an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W), an alloy containing any of the elements, an alloy film in which the elements are combined, and the like are given. Alternatively, one or more materials selected from manganese, magnesium, zirconium, beryllium, and thorium may be used. Further, the conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon; a two-layer structure of an aluminum film and a titanium film stacked thereover; a three-layer structure of a titanium film, an aluminum film stacked thereover, and a titanium film stacked thereover; and the like can be given. Alternatively, a film, an alloy film, or a nitride film which contains aluminum and one or more elements selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc) may be used. Note that a material having a low electronegativity is preferably used as the material for the conductive film.

[0256]

The conductive film formed using the target described in Embodiment 1 is used as the conductive film in this embodiment; thus, impurities such as moisture or hydrogen in the oxide semiconductor layer, the insulating layer, at an interface between the oxide semiconductor layer and the insulating layer, and in the vicinity thereof are absorbed or adsorbed by the conductive film. Thus, elimination of impurities such as moisture or hydrogen makes it possible to obtain an i-type (intrinsic) oxide semiconductor layer or an oxide semiconductor layer that is as close to an i-type oxide semiconductor layer as possible, and deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage, can be prevented from being promoted and off-state current can be reduced.

[0257]

In a third photolithography step, a resist mask is formed over the conductive film and the conductive film is selectively etched, so that a source electrode layer 395a and a drain electrode layer 395b are formed, and then the resist mask is removed (see FIG. 7C).

[0258]

Ultraviolet light, KrF laser light, or ArF laser light is used for light exposure for forming the resist mask in the third photolithography step. A channel length $L$ of a transistor that is completed later is determined by a distance between bottom ends of the source electrode layer and the drain electrode layer, which are adjacent to each other over the oxide semiconductor layer 399. Note that in the case where light exposure is performed so that a pattern with a channel length $L$ of less than 25 nm is formed, light exposure for forming the resist mask in the third photolithography step is performed using extreme ultraviolet with an extremely short wavelength of several nanometers to several tens of nanometers. Light exposure using extreme ultraviolet enables high resolution and deep depth of focus. Thus, the channel length $L$ of the transistor that is completed later can be greater than or equal to 10 nm and less than or equal to 1000 nm and the operation speed of a circuit can be increased and furthermore the value of off-state current is extremely small, so that lower power consumption can be achieved.

[0259]

Note that in order to prevent the oxide semiconductor layer 399 from being removed at the time of the etching of the conductive film, materials and etching conditions of the conductive film and the oxide semiconductor layer 399 are adjusted as appropriate.

[0260]

In this embodiment, a titanium film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used for the oxide semiconductor layer 399, and an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant of the titanium film.

[0261]

Note that, in the third photolithography step, only part of the oxide semiconductor layer 399 is etched in some cases, so that an oxide semiconductor layer

having a groove (a depressed portion) is formed. In addition, the resist mask for forming the source electrode layer 395a and the drain electrode layer 395b may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0262]

In order to reduce the number of photomasks and steps in the photolithography step, an etching step may be performed with the use of a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. A resist mask formed with the use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; thus, the resist mask can be used in a plurality of etching steps for processing into different patterns. Thus, a resist mask corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can also be reduced, whereby simplification of a process can be realized.

[0263]

Plasma treatment using a gas such as nitrous oxide ($N_2O$), nitrogen ($N_2$), or argon (Ar) may be performed to remove water and the like attached to an exposed surface of the oxide semiconductor layer. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and argon.

[0264]

In the case where the plasma treatment is performed, the oxide insulating layer 396 is formed, without being exposed to air, as an oxide insulating layer that serves as a protective insulating film in contact with part of the oxide semiconductor layer (see FIG. 7D). In this embodiment, the oxide insulating layer 396 is formed so as to be in contact with the oxide semiconductor layer 399 in a region where the oxide semiconductor layer 399 does not overlap with the source electrode layer 395a and the drain electrode layer 395b.

[0265]

In this embodiment, a silicon oxide layer containing a defect is formed as the oxide insulating layer 396 in such a manner that the substrate 394 over which layers up to and including the island-shaped oxide semiconductor layer 399, the source electrode

layer 395a, and the drain electrode layer 395b are formed is heated to room temperature or a temperature lower than 100 °C, a sputtering gas which contains high-purity oxygen and from which hydrogen and moisture have been removed is introduced, and a silicon target is used.

[0266]

For example, the silicon oxide film is formed with a pulsed DC sputtering method under the following conditions: the purity of a sputtering gas is 6N, a boron-doped silicon target (the resistivity is 0.01 Ωcm) is used, the distance between the substrate and the target (T-S distance) is 89 mm, the pressure is 0.4 Pa, the direct-current (DC) power is 6 kW, and the atmosphere is an oxygen atmosphere (the oxygen flow rate is 100 %). The thickness of the silicon oxide film is 300 nm. Note that as the target for forming the silicon oxide film, quartz (preferably synthetic quartz) can be used instead of the silicon target. As the sputtering gas, oxygen or a mixed gas of oxygen and argon is used.

[0267]

In that case, the oxide insulating layer 396 is preferably formed while moisture remaining in the treatment chamber is removed in order to prevent hydrogen, hydroxyl groups, or moisture from being contained in the oxide semiconductor layer 399 and the oxide insulating layer 396.

[0268]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide insulating layer 396 formed in the treatment chamber can be reduced.

[0269]

Note that as the oxide insulating layer 396, a silicon oxynitride layer, an aluminum oxide layer, an aluminum oxynitride layer, or the like can be used instead of the silicon oxide layer.

[0270]

Furthermore, heat treatment may be performed at 100 °C to 400 °C with the oxide insulating layer 396 and the oxide semiconductor layer 399 being in contact with each other. Since the oxide insulating layer 396 in this embodiment contains a large number of defects, with this heat treatment, impurities such as hydrogen, moisture, hydroxyl groups, or hydride contained in the oxide semiconductor layer 399 can be diffused into the oxide insulating layer 396, so that the impurities contained in the oxide semiconductor layer 399 are further reduced.

[0271]

Through the above-described steps, the transistor 390 including the oxide semiconductor layer 392 in which the concentration of hydrogen, moisture, hydroxyl groups, or hydride is reduced can be manufactured (see FIG. 7E).

[0272]

In the transistor described in this embodiment, the conductive film that is used as the source electrode layer and the drain electrode layer is formed using the sputtering target described in Embodiment 1. The conductive film is formed in contact with the oxide semiconductor film that is used as an active layer, whereby impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film and the purity of the oxide semiconductor film can be increased. In addition, moisture remaining in the atmosphere is removed in forming the oxide semiconductor film, whereby the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Thus, the oxide semiconductor film can be stabilized.

[0273]

A protective insulating layer may be provided over the oxide insulating layer. In this embodiment, a protective insulating layer 398 is formed over the oxide insulating layer 396. A silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, or the like is used as the protective insulating layer 398.

[0274]

As the protective insulating layer 398, a silicon nitride film is formed in such a manner that the substrate 394 over which layers up to and including the oxide insulating layer 396 are formed is heated to a temperature of 100 °C to 400 °C, a sputtering gas

which contains high-purity nitrogen and from which hydrogen and moisture have been removed is introduced, and a silicon target is used. Also in that case, in a manner similar to that of the oxide insulating layer 396, the protective insulating layer 398 is preferably formed while moisture remaining in the treatment chamber is removed.

[0275]

In the case where the protective insulating layer 398 is formed, the substrate 394 is heated to 100 °C to 400 °C at the time of the formation of the protective insulating layer 398, whereby hydrogen or moisture contained in the oxide semiconductor layer can be diffused into the oxide insulating layer. In that case, heat treatment does not have to be performed after the formation of the oxide insulating layer 396.

[0276]

In the case where the silicon oxide layer is formed as the oxide insulating layer 396 and the silicon nitride layer is stacked thereover as the protective insulating layer 398, the silicon oxide layer and the silicon nitride layer can be formed in the same treatment chamber using the same silicon target. First, the silicon oxide layer is formed in such a manner that a gas containing oxygen is introduced and a silicon target provided in the treatment chamber is used. Then, the silicon nitride layer is formed in such a manner that the gas is switched to a gas containing nitrogen and the silicon target used for the silicon nitride layer is used. The silicon oxide layer and the silicon nitride layer can be formed successively without being exposed to air; thus, impurities such as hydrogen or moisture can be prevented from being adsorbed on a surface of the silicon oxide layer. In that case, heat treatment (at 100 °C to 400 °C) is preferably performed so that hydrogen or moisture contained in the oxide semiconductor layer is diffused into the oxide insulating layer, after the silicon oxide layer is formed as the oxide insulating layer 396 and the silicon nitride layer is stacked thereover as the protective insulating layer 398.

[0277]

After the protective insulating layer is formed, heat treatment may be further performed at temperature higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air.

This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating layer. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened. This heat treatment enables a normally-off transistor to be obtained. Thus, the reliability of a semiconductor device can be increased.

[0278]

Further, moisture remaining in a reaction atmosphere is removed at the time of forming the oxide semiconductor layer that serves as a channel formation region over the gate insulating layer, whereby the concentration of hydrogen and hydride in the oxide semiconductor layer can be reduced

[0279]

Since the above-described steps are performed at a temperature of 400 °C or lower, the process can be applied to a manufacturing process using a glass substrate having a side longer than or equal to 1 m and a thickness less than or equal to 1 mm. In addition, since all of the above steps can be performed at a treatment temperature of 400 °C or lower, a display panel can be manufactured without consuming too much energy.

[0280]

As described above, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided.

[0281]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0282]

(Embodiment 6)

In this embodiment, another example of a transistor that is manufactured using the target described in Embodiment 1 will be described. In a transistor 310 described

in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0283]

FIGS. 8A to 8E illustrate an example of a cross-sectional structure of the transistor in this embodiment. The transistor 310 illustrated in FIGS. 8A to 8E is one of bottom-gate transistors and is also called an inverted staggered transistor.

[0284]

Although the transistor 310 is described as a single-gate transistor, a multi-gate transistor including a plurality of channel formation regions can be manufactured when needed.

[0285]

A process of manufacturing the transistor 310 over a substrate 300 will be described below with reference to FIGS. 8A to 8E.

[0286]

First, a conductive film is formed over the substrate 300 having an insulating surface, and then a gate electrode layer 311 is formed in a first photolithography step. Note that a resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0287]

Although there is no particular limitation on a substrate which can be used as the substrate 300 having an insulating surface, it is necessary that the substrate have at least heat resistance high enough to withstand heat treatment performed later. For example, a glass substrate made of barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0288]

In the case where the temperature of heat treatment performed later is high, a glass substrate whose strain point is higher than or equal to 730 °C is preferably used. As a glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that in the case where a larger amount of barium oxide (BaO) than boron oxide is contained, a more practical

heat-resistant glass substrate can be obtained. Therefore, a glass substrate containing a larger amount of barium oxide (BaO) than boron oxide ($B_2O_3$) is preferably used.

[0289]

Note that a substrate formed of an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate may be used instead of the above glass substrate. Alternatively, a crystallized glass substrate or the like can be used.

[0290]

An insulating film that serves as a base film may be provided between the substrate 300 and the gate electrode layer 311. The base film has a function of preventing diffusion of an impurity element from the substrate 300, and can be formed to have a single-layer or stacked-layer structure using one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0291]

Further, the gate electrode layer 311 can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material which contains any of these materials as its main component. The gate electrode layer may be formed by a sputtering method with the use of the sputtering target described in Embodiment 1.

[0292]

Further, the gate electrode layer 311 may have a single-layer structure or a stacked-layer structure of two or more layers. For example, as a two-layer structure of the gate electrode layer 311, the following structure is preferable: a structure in which a molybdenum layer is stacked over an aluminum layer, a structure in which a molybdenum layer is stacked over a copper layer, a structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, a structure in which a titanium nitride layer and a molybdenum layer are stacked, or a structure in which a tungsten nitride layer and a tungsten layer are stacked. As a three-layer structure, a structure in which a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer are stacked is preferable.

[0293]

Next, a gate insulating layer 302 is formed over the gate electrode layer 311.

[0294]

The gate insulating layer 302 can be formed to have a single layer of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer or a stacked layer thereof by a plasma CVD method, a sputtering method, or the like. For example, a silicon oxynitride layer may be formed by a plasma CVD method using $SiH_4$, oxygen, and nitrogen as a deposition gas. The thickness of the gate insulating layer 302 is greater than or equal to 100 nm and less than or equal to 500 nm. In the case of a stacked-layer structure, for example, a first gate insulating layer with a thickness greater than or equal to 50 nm and less than or equal to 200 nm and a second gate insulating layer with a thickness greater than or equal to 5 nm and less than or equal to 300 nm are stacked in that order.

[0295]

In this embodiment, a silicon oxynitride layer is formed to a thickness of less than or equal to 100 nm by a plasma CVD method as the gate insulating layer 302.

[0296]

Next, an oxide semiconductor film 330 is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the gate insulating layer 302.

[0297]

Note that before the oxide semiconductor film 330 is formed by a sputtering method, dust attached to a surface of the gate insulating layer 302 is preferably removed by reverse sputtering in which plasma is generated by introduction of an argon gas. Note that a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used instead of an argon atmosphere.

[0298]

As the oxide semiconductor film 330, the following can be used: an In-Ga-Zn-O-based oxide semiconductor film, an In-Sn-Zn-O-based oxide semiconductor film, an In-Al-Zn-O-based oxide semiconductor film, a Sn-Ga-Zn-O-based oxide semiconductor film, an Al-Ga-Zn-O-based oxide semiconductor film, a Sn-Al-Zn-O-based oxide semiconductor film, an In-Sn-O-based oxide semiconductor film, an In-Zn-O-based oxide semiconductor film, a Sn-Zn-O-based oxide semiconductor film, an Al-Zn-O-based oxide semiconductor film,

an In-O-based oxide semiconductor film, a Sn-O-based oxide semiconductor film, or a Zn-O-based oxide semiconductor film. In this embodiment, the oxide semiconductor film 330 is formed by a sputtering method with the use of an In-Ga-Zn-O-based oxide semiconductor target for film formation. A cross-sectional view at this stage is FIG. 8A. The oxide semiconductor film 330 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas (typically, argon) and oxygen. In the case of using a sputtering method, the oxide semiconductor film may be formed using a target containing $SiO_2$ at greater than or equal to 2 wt% and less than or equal to 10 wt%.

[0299]

As a target for forming the oxide semiconductor film 330 by a sputtering method, a metal oxide target containing zinc oxide as a main component can be used. As another example of the metal oxide target, an oxide semiconductor target for film formation containing In, Ga, and Zn (the composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:1 (molar ratio)) or the like can be used. As the oxide semiconductor target for film formation containing In, Ga, and Zn, a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:2 (molar ratio) or a target having a composition ratio of $In_2O_3$:$Ga_2O_3$:ZnO = 1:1:4 (molar ratio) can also be used. In addition, the filling factor of the oxide semiconductor target for film formation is greater than or equal to 90 % and less than or equal to 100 %, preferably greater than or equal to 95 % and less than or equal to 99.9 %. An oxide semiconductor film which is formed using an oxide semiconductor target for film formation, which has a high filling factor, is dense.

[0300]

As a sputtering gas used for forming the oxide semiconductor film 330, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0301]

The substrate is held in a treatment chamber maintained at reduced pressure and is heated to a temperature higher than or equal to 100 °C and lower than or equal to 600 °C, preferably a temperature higher than or equal to 200 °C and lower than or equal

to 400 °C. Film formation is performed while the substrate is heated, whereby the concentration of impurities contained in the oxide semiconductor film formed can be reduced. In addition, damage due to the sputtering can be reduced. Then, a sputtering gas from which hydrogen and moisture have been removed is introduced into the treatment chamber while moisture remaining therein is removed, and metal oxide is used as a target. In the above manner, the oxide semiconductor film 330 is formed over the gate insulating layer 302. In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$) (preferably also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced.

[0302]

As an example of the deposition condition, the following conditions are employed: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the proportion of oxygen flow: 100 %). Note that a pulsed direct-current (DC) power source is preferably used, in which case powder substances (also referred to as particles or dust) that are generated in deposition can be reduced and the thickness can be uniform. The oxide semiconductor film preferably has a thickness greater than or equal to 5 nm and less than or equal to 30 nm. Note that the appropriate thickness differs depending on the oxide semiconductor material, and the thickness may be set as appropriate depending on the material.

[0303]

Next, the oxide semiconductor film 330 is processed into an island-shaped oxide semiconductor layer in a second photolithography step. A resist mask for forming the island-shaped oxide semiconductor layer may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which

results in a reduction in manufacturing costs.

[0304]

Note that the etching of the oxide semiconductor film may be dry etching, without limitation to wet etching.

[0305]

The etching conditions (such as an etchant, etching time, and temperature) are adjusted as appropriate depending on the material so that the oxide semiconductor film can be etched into a desired shape.

[0306]

Next, first heat treatment is performed on the oxide semiconductor layer. Through the first heat treatment, the oxide semiconductor layer can be dehydrated or dehydrogenated. The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and heat treatment is performed on the oxide semiconductor layer at 450 °C in a nitrogen atmosphere for one hour, and then water and hydrogen are prevented from entering the oxide semiconductor layer with the oxide semiconductor layer not exposed to air, so that the oxide semiconductor layer 331 is obtained (see FIG. 8B).

[0307]

The heat treatment apparatus is not limited to an electric furnace and may be provided with a device that heats an object to be processed by thermal conduction or thermal radiation from a heater such as a resistance heater or the like. For example, an RTA (rapid thermal anneal) apparatus such as an LRTA (lamp rapid thermal anneal) apparatus or a GRTA (gas rapid thermal anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus with which heat treatment is performed using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as

argon is used.

[0308]

For example, as the first heat treatment, GRTA may be performed as follows: the substrate is transferred and put in an inert gas which has been heated to a temperature as high as 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables a high-temperature heat treatment in a short time.

[0309]

Note that in the first heat treatment, it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or the rare gas such as helium, neon, or argon which is introduced into a heat treatment apparatus be set to be 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0310]

Further, the oxide semiconductor layer might be crystallized to become a microcrystalline film or a polycrystalline film depending on the condition of the first heat treatment or the material for the oxide semiconductor layer. For example, the oxide semiconductor layer might be crystallized to become a microcrystalline oxide semiconductor film having a degree of crystallization of 90 % or more, or 80 % or more. Further, depending on the condition of the first heat treatment and the material for the oxide semiconductor layer, the oxide semiconductor layer might become an amorphous oxide semiconductor film containing no crystalline component. The oxide semiconductor layer may become an oxide semiconductor film in which a microcrystalline portion (with a grain diameter greater than or equal to 1 nm and greater than or less than 20 nm, typically greater than or equal to 2 nm and less than or equal to 4 nm) is mixed into an amorphous oxide semiconductor.

[0311]

The first heat treatment for the oxide semiconductor layer can be performed on the oxide semiconductor film 330 that has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out of the heating

apparatus after the first heat treatment, and then a photolithography step is performed.

[0312]

The heat treatment which has an effect of dehydrating or dehydrogenating the oxide semiconductor layer may be performed at any of the following timings: after the oxide semiconductor layer is formed; after a conductive film is stacked over the oxide semiconductor layer; after the conductive film is processed into a source electrode and a drain electrode; and after a protective insulating film is formed over the source electrode and the drain electrode.

[0313]

In the case where a contact hole is formed in the gate insulating layer 302, the formation of the contact hole may be performed before or after the dehydration or dehydrogenation of the oxide semiconductor film 330.

[0314]

In this embodiment, as a conductive film for forming a source electrode layer and a drain electrode layer, a conductive film formed using the sputtering target described in Embodiment 1 is provided. The conductive film is a conductive film in which the hydrogen concentration is reduced; thus, when the conductive film is provided in contact with the oxide semiconductor layer and heat treatment is performed, the purity of the oxide semiconductor layer can be further increased. Note that in the case where heat treatment is performed after the conductive film is formed, the conductive film preferably has heat resistance high enough to withstand the heat treatment. For example, the heating temperature is preferably higher than or equal to 100 °C and lower than 300 °C, more preferably 220 °C to 280 °C.

[0315]

Next, a conductive film 333 is formed over the gate insulating layer 302 and the oxide semiconductor layer 331 (see FIG. 8B). The conductive film is formed by a sputtering method with the use of the sputtering target described in Embodiment 1. As examples of the material for the conductive film, an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W), an alloy containing any of the elements, an alloy film in which the elements are combined, and the like are given. Alternatively, one or more materials selected from manganese, magnesium, zirconium, beryllium, and thorium may be used.

Note that a material having a low electronegativity, specifically a material having a lower electronegativity than hydrogen, is preferably used as a material for the conductive film, in which case an effect of extracting impurities such as hydrogen or moisture from the oxide semiconductor layer can be more effective. Further, the conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film containing silicon; a two-layer structure of an aluminum film and a titanium film stacked thereover; a three-layer structure of a titanium film, an aluminum film stacked thereover, and a titanium film stacked thereover; and the like can be given. Alternatively, a film, an alloy film, or a nitride film which contains aluminum and one or more elements selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc) may be used.

[0316]

The conductive film that is formed using the target described in Embodiment 1 is used as the conductive film 333 in this embodiment; thus, impurities such as moisture or hydrogen in the oxide semiconductor layer, at an interface between the oxide semiconductor layer and the conductive film, and in the vicinity thereof are absorbed or adsorbed by the conductive film. Thus, elimination of impurities such as moisture or hydrogen makes it possible to obtain an i-type (intrinsic) oxide semiconductor layer or an oxide semiconductor layer that is as close to an i-type oxide semiconductor layer as possible, and deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage, can be prevented from being promoted and off-state current can be reduced.

[0317]

In a third photolithography step, a resist mask is formed over the conductive film 333 and the conductive film 333 is selectively etched, so that a source electrode layer 315a and a drain electrode layer 315b are formed, and then the resist mask is removed (see FIG. 8C).

[0318]

Ultraviolet light, KrF laser light, or ArF laser light is used for light exposure for forming the resist mask in the third photolithography step. A channel length $L$ of a transistor that is completed later is determined by a distance between bottom ends of the

source electrode layer and the drain electrode layer, which are adjacent to each other over the oxide semiconductor layer 331. Note that in the case where light exposure is performed so that a pattern with a channel length $L$ of less than 25 nm is formed, light exposure for forming the resist mask in the third photolithography step is performed using extreme ultraviolet with an extremely short wavelength of several nanometers to several tens of nanometers. Light exposure using extreme ultraviolet enables high resolution and deep depth of focus. Thus, the channel length $L$ of the transistor that is completed later can be greater than or equal to 10 nm and less than or equal to 1000 nm and the operation speed of a circuit can be increased and furthermore the value of off-state current is extremely small, so that lower power consumption can be achieved.

[0319]

Note that in order to prevent the oxide semiconductor layer 331 from being removed at the time of the etching of the conductive film, materials and etching conditions of the conductive film and the oxide semiconductor layer 331 are adjusted as appropriate.

[0320]

In this embodiment, a titanium film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used for the oxide semiconductor layer 331, and an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant of the titanium film.

[0321]

Note that, in the third photolithography step, only part of the oxide semiconductor layer 331 is etched in some cases, so that an oxide semiconductor layer having a groove (a depressed portion) is formed. In addition, the resist mask for forming the source electrode layer 315a and the drain electrode layer 315b may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0322]

Further, an oxide conductive layer may be formed between the oxide semiconductor layer and the source and drain electrode layers. The oxide conductive layer and the metal layer for forming the source and drain electrode layers can be formed successively. The oxide conductive layer can function as a source region and a

drain region.

[0323]

The provision of the oxide conductive layer as the source and drain regions between the oxide semiconductor layer and the source and drain electrode layers makes it possible to decrease the resistance of the source and drain regions and to operate the transistor at high speed.

[0324]

In order to reduce the number of photomasks and steps in the photolithography step, an etching step may be performed with the use of a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. A resist mask formed with the use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; thus, the resist mask can be used in a plurality of etching steps for processing into different patterns. Thus, a resist mask corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can also be reduced, whereby simplification of a process can be realized.

[0325]

Next, plasma treatment using a gas such as nitrous oxide ($N_2O$), nitrogen ($N_2$), or argon (Ar) is performed. By this plasma treatment, water or the like attached to an exposed surface of the oxide semiconductor layer is removed. The plasma treatment may be performed using a mixed gas of oxygen and argon.

[0326]

After the plasma treatment, an oxide insulating layer 316 that serves as a protective insulating film and is in contact with part of the oxide semiconductor layer is formed without exposure to air.

[0327]

The oxide insulating layer 316 can be formed to a thickness of at least 1 nm by a method with which impurities such as water or hydrogen are not mixed into the oxide insulating layer 316, such as a sputtering method, as appropriate. When hydrogen is contained in the oxide insulating layer 316, entry of the hydrogen to the oxide semiconductor layer or extraction of oxygen in the oxide semiconductor layer by the

hydrogen is caused, thereby causing the backchannel of the oxide semiconductor layer to have lower resistance (to be n-type), so that a parasitic channel might be formed. Therefore, it is important that a formation method in which hydrogen is not used be employed in order to form the oxide insulating layer 316 containing as little hydrogen as possible.

[0328]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as the oxide insulating layer 316 by a sputtering method. The substrate temperature in the film formation may be higher than or equal to room temperature and lower than or equal to 300 °C, and is 100 °C in this embodiment. The formation of the silicon oxide film by a sputtering method can be performed in an atmosphere of a rare gas (typically, argon), an oxygen atmosphere, or an atmosphere containing oxygen and a rare gas (typically, argon). As a target, a silicon oxide target or a silicon target can be used. For example, with the use of a silicon target, a silicon oxide film can be formed by a sputtering method in an atmosphere containing oxygen and nitrogen. As the oxide insulating layer 316 which is formed in contact with the oxide semiconductor layer whose resistance is reduced, an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and $OH^-$ and blocks entry of these from the outside is used. Specifically, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0329]

In that case, the oxide insulating layer 316 is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor layer 331 and the oxide insulating layer 316.

[0330]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom

such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide insulating layer 316 formed in the treatment chamber can be reduced.

[0331]

As a sputtering gas used for forming the oxide insulating layer 316, a high-purity gas is preferably used in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0332]

Next, second heat treatment (preferably at higher than or equal to 200 °C and lower than or equal to 400 °C, for example, at higher than or equal to 250 °C and lower than or equal to 350 °C) is performed in an inert gas atmosphere or an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. By the second heat treatment, heat is applied while part of the oxide semiconductor layer (the channel formation region) is in contact with the oxide insulating layer 316.

[0333]

Through the above-described steps, first, the first heat treatment for dehydration or dehydrogenation of the formed oxide semiconductor film causes the oxide semiconductor film to be oxygen-deficient and to have lower resistance, that is, causes the oxide semiconductor film to be n-type (e.g., $n^-$ type). After that, by the second heat treatment in which heat is applied while the oxide insulating layer is in contact with the oxide semiconductor layer, oxygen is supplied to the oxide semiconductor layer 331 whose resistance is reduced by the first heat treatment, whereby an oxygen-deficient portion is repaired. As a result, a channel formation region 313 that overlaps with the gate electrode layer 311 has higher resistance (is i-type), and a high-resistance source region 314a that overlaps with the source electrode layer 315a and a high-resistance drain region 314b that overlaps with the drain electrode layer 315b are formed in a self-aligned manner. Through the above-described steps, the transistor 310 is manufactured (see FIG. 8D).

[0334]

Further, heat treatment may be performed at higher than or equal to 100 °C and

lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating film. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened. This heat treatment enables a normally-off transistor to be obtained. Thus, the reliability of a semiconductor device can be increased.

[0335]

The high-resistance drain region 314b (or the high-resistance source region 314a) is formed in a portion of the oxide semiconductor layer which overlaps with the drain electrode layer 315b (or the source electrode layer 315a), whereby the reliability of the transistor can be increased. Specifically, the formation of the high-resistance drain region 314b enables a structure in which the conductivity can be gradually varied from the drain electrode layer 315b to the channel formation region 313 via the high-resistance drain region 314b. Thus, in the case where the transistor is operated with the drain electrode layer 315b connected to a wiring for supplying a high power supply potential *VDD*, the high-resistance drain region serves as a buffer and local concentration of an electric field is less likely to occur even if high voltage is applied between the gate electrode layer 311 and the drain electrode layer 315b, whereby the withstand voltage of the transistor can be increased.

[0336]

Further, the high-resistance source region or the high-resistance drain region in the oxide semiconductor layer is formed in the entire thickness direction in the case where the oxide semiconductor layer is as thin as 15 nm or less. In contrast, in the case where the oxide semiconductor layer is as thick as 30 nm to 50 nm, the resistance of part of the oxide semiconductor layer, that is, a region of the oxide semiconductor layer, which is in contact with the source or drain electrode layer, and the vicinity

thereof is decreased, so that the high-resistance source region or the high-resistance drain region is formed and a region of the oxide semiconductor layer which is near the gate insulating layer can be made to be an i-type region.

[0337]

A protective insulating layer may be additionally formed over the oxide insulating layer 316. For example, a silicon nitride film is formed by an RF sputtering method. Since an RF sputtering method provides high productivity, it is preferably used as a film formation method of the protective insulating layer. As the protective insulating layer, an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and $OH^-$ and blocks entry of these from the outside is used; for example, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, an aluminum nitride oxide film, or the like is used. In this embodiment, as the protective insulating layer, a protective insulating layer 303 is formed using a silicon nitride film (see FIG. 8E).

[0338]

In this embodiment, as the protective insulating layer 303, a silicon nitride film is formed in such a manner that the substrate 300 over which layers up to and including the oxide insulating layer 316 are formed is heated to a temperature of 100 °C to 400 °C, a sputtering gas which contains high-purity nitrogen and from which hydrogen and moisture have been removed is introduced, and a silicon target is used. Also in that case, in a manner similar to that of the oxide insulating layer 316, the protective insulating layer 303 is preferably formed while moisture remaining in the treatment chamber is removed.

[0339]

A planarization insulating layer for planarization may be provided over the protective insulating layer 303.

[0340]

As described above, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided.

[0341]

This embodiment can be implemented in appropriate combination with any of

the structures of the other embodiments.

[0342]

(Embodiment 7)

In this embodiment, another example of a transistor that is manufactured using the target described in Embodiment 1 will be described. In a transistor 360 described in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0343]

FIGS. 9A to 9D illustrate an example of a cross-sectional structure of the transistor in this embodiment. The transistor 360 illustrated in FIGS. 9A to 9D is one of bottom-gate transistors called channel-protective (channel-stop) transistors and is also called an inverted staggered transistor.

[0344]

Although the transistor 360 is described as a single-gate transistor, a multi-gate transistor including a plurality of channel formation regions can be manufactured when needed.

[0345]

A process of manufacturing the transistor 360 over a substrate 320 will be described below with reference to FIGS. 9A to 9D.

[0346]

First, a conductive film is formed over the substrate 320 having an insulating surface, and then a gate electrode layer 361 is formed in a first photolithography step. Note that a resist mask may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask, which results in a reduction in manufacturing costs.

[0347]

The gate electrode layer 361 can be formed to have a single-layer or stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which contains any of these materials as a main component. Note that the gate electrode layer may be formed by a sputtering method with the use of the sputtering

target described in Embodiment 1.

[0348]

Next, a gate insulating layer 322 is formed over the gate electrode layer 361.

[0349]

In this embodiment, as the gate insulating layer 322, a silicon oxynitride layer is formed to a thickness of 100 nm or less by a plasma CVD method.

[0350]

Next, an oxide semiconductor film is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm over the gate insulating layer 322, and then the oxide semiconductor film is processed into an island-shaped oxide semiconductor layer in a second photolithography step. In this embodiment, the oxide semiconductor film is formed using an In-Ga-Zn-O-based oxide semiconductor target for film formation by a sputtering method.

[0351]

In that case, the oxide semiconductor film is preferably formed while moisture remaining in a treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is contained as little as possible in the oxide semiconductor film.

[0352]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced.

[0353]

As a sputtering gas used for forming the oxide semiconductor film, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0354]

Next, dehydration or dehydrogenation of the oxide semiconductor layer is

performed. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour, and then water and hydrogen are prevented from entering the oxide semiconductor layer with the oxide semiconductor layer not exposed to air; thus, the oxide semiconductor layer 332 is obtained (see FIG. 9A).

[0355]

Next, plasma treatment using a gas such as nitrous oxide ($N_2O$), nitrogen ($N_2$), or argon (Ar) is performed. By this plasma treatment, water or the like attached to an exposed surface of the oxide semiconductor layer is removed. The plasma treatment may be performed using a mixed gas of oxygen and argon.

[0356]

Next, an oxide insulating layer is formed over the gate insulating layer 322 and the oxide semiconductor layer 332. After that, in a third photolithography step, a resist mask is formed and the oxide insulating layer is selectively etched, so that an oxide insulating layer 366 is formed. After that, the resist mask is removed.

[0357]

In this embodiment, as the oxide insulating layer 366, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method. The substrate temperature in the film formation may be higher than or equal to room temperature and lower than or equal to 300 °C, and is 100 °C in this embodiment. The formation of the silicon oxide film with a sputtering method can be performed in an atmosphere of a rare gas (typically, argon), an oxygen atmosphere, or an atmosphere containing oxygen and a rare gas (typically, argon). As a target, a silicon oxide target or a silicon target can be used. For example, with the use of a silicon target, a silicon oxide film can be formed by a sputtering method in an atmosphere containing oxygen and nitrogen. As the oxide insulating layer 366 which is formed in contact with the oxide semiconductor layer whose resistance is reduced, an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and $OH^-$ and blocks entry of these from the

outside is used. Specifically, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0358]

In that case, the oxide insulating layer 366 is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor layer 332 and the oxide insulating layer 366.

[0359]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide insulating layer 366 formed in the treatment chamber can be reduced.

[0360]

As a sputtering gas used for forming the oxide insulating layer 366, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0361]

Next, second heat treatment may be performed in an inert gas atmosphere or an oxygen gas atmosphere (preferably at higher than or equal to 200 °C and lower than or equal to 400 °C, for example, at higher than or equal to 250 °C and lower than or equal to 350 °C). For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. By the second heat treatment, heat is applied while part of the oxide semiconductor layer (the channel formation region) is in contact with the oxide insulating layer 366.

[0362]

In this embodiment, the oxide semiconductor layer 332 which is provided with the oxide insulating layer 366 and is partly exposed is further subjected to heat

treatment in a nitrogen atmosphere or an inert gas atmosphere or under reduced pressure. By the heat treatment in a nitrogen atmosphere or an inert gas atmosphere or under reduced pressure, the resistance of the exposed region of the oxide semiconductor layer 332, which is not covered with the oxide insulating layer 366 can be reduced. For example, the heat treatment is performed at 250 °C in a nitrogen atmosphere for one hour.

[0363]

By the heat treatment performed on the oxide semiconductor layer 332 provided with the oxide insulating layer 366 in a nitrogen atmosphere, the resistance of the exposed region of the oxide semiconductor layer 332 is reduced, so that an oxide semiconductor layer 362 including regions with different resistances (indicated as a shaded region and a white region in FIG. 9B) is formed.

[0364]

Next, a conductive film is formed over the gate insulating layer 322, the oxide semiconductor layer 362, and the oxide insulating layer 366 with the use of the sputtering target described in Embodiment 1. After that, in a fourth photolithography step, a resist mask is formed and the conductive film is selectively etched, so that a source electrode layer 365a and a drain electrode layer 365b are formed, and then the resist mask is removed (see FIG. 9C).

[0365]

The conductive film that is formed using the target described in Embodiment 1 is used as the conductive film for forming the source electrode layer 365a and the drain electrode layer 365b in this embodiment; thus, impurities such as moisture or hydrogen in the oxide semiconductor layer, at an interface between the oxide semiconductor layer and the conductive film, and in the vicinity thereof are absorbed or adsorbed by the conductive film. Thus, elimination of impurities such as moisture or hydrogen makes it possible to obtain an i-type (intrinsic) oxide semiconductor layer or an oxide semiconductor layer that is as close to an i-type oxide semiconductor layer as possible, and deterioration of the characteristics of the transistor due to the impurities, such as a shift in the threshold voltage, can be prevented from being promoted and off-state current can be reduced.

[0366]

As examples of a material for the source electrode layer 365a and the drain electrode layer 365b, an element selected from aluminum (Al), chromium (Cr), copper (Cu), tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W), an alloy containing any of the elements, an alloy film in which the elements are combined, and the like are given. Further, the conductive film may have a single-layer structure or a stacked-layer structure of two or more layers.

[0367]

Through the above-described steps, first, the first heat treatment for dehydration or dehydrogenation of the formed oxide semiconductor film causes the oxide semiconductor film to be oxygen-deficient and to have lower resistance, that is, causes the oxide semiconductor film to be n-type (e.g., $n^-$ type). After that, by the second heat treatment in which heat is applied while the oxide insulating layer is in contact with the oxide semiconductor layer, oxygen is supplied to the oxide semiconductor layer 362 whose resistance is reduced by the first heat treatment, whereby an oxygen-deficient portion is repaired. As a result, a channel formation region 363 that overlaps with the gate electrode layer 361 has higher resistance (is i-type), and a high-resistance source region 364a that overlaps with the source electrode layer 365a and a high-resistance drain region 364b that overlaps with the drain electrode layer 365b are formed in a self-aligned manner. Through the above-described steps, the transistor 360 is manufactured.

[0368]

Further, heat treatment may be performed at higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating film. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened. This heat

treatment enables a normally-off transistor to be obtained. Thus, the reliability of a semiconductor device can be increased.

[0369]

The high-resistance drain region 364b (or the high-resistance source region 364a) is formed in a portion of the oxide semiconductor layer which overlaps with the drain electrode layer 365b (or the source electrode layer 365a), whereby the reliability of the transistor can be increased. Specifically, the formation of the high-resistance drain region 364b enables a structure in which the conductivity can be gradually varied from the drain electrode layer 365b to the channel formation region 363 via the high-resistance drain region 364b. Thus, in the case where the transistor is operated with the drain electrode layer 365b connected to a wiring for supplying a high power supply potential *VDD*, the high-resistance drain region serves as a buffer and local concentration of an electric field is less likely to occur even if high voltage is applied between the gate electrode layer 361 and the drain electrode layer 365b, whereby the withstand voltage of the transistor can be increased.

[0370]

A protective insulating layer 323 is formed over the source electrode layer 365a, the drain electrode layer 365b, and the oxide insulating layer 366. In this embodiment, the protective insulating layer 323 is formed using a silicon nitride film (see FIG. 9D).

[0371]

Note that an oxide insulating layer may be additionally formed over the source electrode layer 365a, the drain electrode layer 365b, and the oxide insulating layer 366, and a protective insulating layer 323 may be stacked over the oxide insulating layer.

[0372]

In the transistor described in this embodiment, moisture remaining in the reaction atmosphere is removed in forming the oxide semiconductor film, whereby the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Thus, the oxide semiconductor film can be stabilized.

[0373]

As described above, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided.

[0374]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0375]

(Embodiment 8)

In this embodiment, another example of a transistor that is manufactured using the target described in Embodiment 1 will be described. In a transistor 350 described in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0376]

FIGS. 10A to 10D illustrate an example of a cross-sectional structure of the transistor in this embodiment.

[0377]

Although the transistor 350 is described as a single-gate transistor, a multi-gate transistor including a plurality of channel formation regions can be manufactured when needed.

[0378]

A process of manufacturing the transistor 350 over a substrate 340 will be described below with reference to FIGS. 10A to 10D.

[0379]

First, a conductive film is formed over the substrate 340 having an insulating surface, and then a gate electrode layer 351 is formed in a first photolithography step. In this embodiment, as the gate electrode layer 351, a tungsten film is formed to a thickness of 150 nm by a sputtering method. Note that the gate electrode layer may be formed using the sputtering target described in Embodiment 1.

[0380]

Next, a gate insulating layer 342 is formed over the gate electrode layer 351. In this embodiment, as the gate insulating layer 342, a silicon oxynitride layer is formed to a thickness of 100 nm or less by a plasma CVD method.

[0381]

Next, a conductive film is formed over the gate insulating layer 342 with the use of the sputtering target described in Embodiment 1, a resist mask is formed over the

conductive film in a second photolithography step and the conductive film is selectively etched, so that a source electrode layer 355a and a drain electrode 355b are formed, and then the resist mask is removed (see FIG. 10A).

[0382]

Next, an oxide semiconductor film 345 is formed (see FIG. 10B). In this embodiment, the oxide semiconductor film 345 is formed using an In-Ga-Zn-O-based oxide semiconductor target for film formation by a sputtering method. The oxide semiconductor film 345 is processed into an island-like oxide semiconductor layer in a third photolithography step.

[0383]

In that case, the oxide semiconductor film 345 is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor film 345.

[0384]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide semiconductor film 345 formed in the treatment chamber can be reduced.

[0385]

As a sputtering gas used for forming the oxide semiconductor film 345, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0386]

Next, dehydration or dehydrogenation of the oxide semiconductor layer is performed. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus and first heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour, and then water and hydrogen are

prevented from entering the oxide semiconductor layer with the oxide semiconductor layer not exposed to air; thus, an oxide semiconductor layer 346 is obtained (see FIG. 10C).

[0387]

In this embodiment, as the conductive film for forming the source electrode layer and the drain electrode layer, a conductive film formed using the sputtering target described in Embodiment 1 is provided. The conductive film is a conductive film in which the hydrogen concentration is reduced; thus, when the conductive film is provided in contact with the oxide semiconductor layer and the first heat treatment is performed, impurities such as hydrogen or water in the oxide semiconductor layer is extracted by the conductive film, so that the purity of the oxide semiconductor layer can be increased.

[0388]

As the first heat treatment, GRTA may be performed as follows: the substrate is transferred and put in an inert gas which has been heated to a temperature as high as 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables a high-temperature heat treatment in a short time.

[0389]

An oxide insulating layer 356 that serves as a protective insulating film is formed in contact with the oxide semiconductor layer 346.

[0390]

The oxide insulating layer 356 can be formed to a thickness of at least 1 nm by a method with which impurities such as water or hydrogen are not mixed into the oxide insulating layer 356, such as a sputtering method, as appropriate. When hydrogen is contained in the oxide insulating layer 356, entry of the hydrogen to the oxide semiconductor layer or extraction of oxygen in the oxide semiconductor layer by the hydrogen is caused, thereby causing the backchannel of the oxide semiconductor layer to have lower resistance (to be n-type), so that a parasitic channel might be formed. For that reason, it is important that a formation method in which hydrogen is not used be employed in order to form the oxide insulating layer 356 containing as little hydrogen as possible.

[0391]

In this embodiment, as the oxide insulating layer 356, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method. The substrate temperature in the film formation may be higher than or equal to room temperature and lower than or equal to 300 °C, and is 100 °C in this embodiment. The formation of the silicon oxide film by a sputtering method can be performed in an atmosphere of a rare gas (typically, argon), an oxygen atmosphere, or an atmosphere containing oxygen and a rare gas (typically, argon). As a target, a silicon oxide target or a silicon target can be used. For example, with use of a silicon target, a silicon oxide film can be formed by a sputtering method in an atmosphere containing oxygen and nitrogen. As the oxide insulating layer 356 which is formed in contact with the oxide semiconductor layer whose resistance is reduced, an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and $OH^-$ and blocks entry of these from the outside is used. Specifically, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, or the like is used.

[0392]

In that case, the oxide insulating layer 356 is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor layer 331 and the oxide insulating layer 356.

[0393]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed; thus, the concentration of impurities in the oxide insulating layer 356 formed in the treatment chamber can be reduced.

[0394]

As a sputtering gas used for forming the oxide insulating layer 356, a high-purity gas is preferably used, in which impurities such as hydrogen, water,

hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0395]

Next, second heat treatment is performed in an inert gas atmosphere or an oxygen gas atmosphere (preferably at higher than or equal to 200 °C and lower than or equal to 400 °C, for example, at higher than or equal to 250 °C and lower than or equal to 350 °C). For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. By the second heat treatment, heat is applied while part of the oxide semiconductor layer (the channel formation region) is in contact with the oxide insulating layer 356.

[0396]

Through the above-described steps, after the heat treatment for dehydration or dehydrogenation is performed on the formed oxide semiconductor film to reduce the resistance of the oxide semiconductor film, an oxygen-deficient portion of the oxide semiconductor film is repaired. As a result, an oxide semiconductor layer 352 whose resistance is increased (an i-type oxide semiconductor layer) is formed. Through the above-described steps, the transistor 350 is manufactured.

[0397]

Further, heat treatment may be performed at higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours in the air. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating film. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened. This heat treatment enables a normally-off transistor to be obtained. Thus, the reliability of a semiconductor device can be increased.

[0398]

A protective insulating layer may be additionally formed over the oxide insulating layer 356. For example, a silicon nitride film is formed by an RF sputtering method. In this embodiment, as the protective insulating layer, a protective insulating layer 343 is formed using a silicon nitride film (see FIG. 10D).

[0399]

A planarizing insulating layer for planarization may be provided over the protective insulating layer 343.

[0400]

In the transistor described in this embodiment, the conductive film that is used as the source electrode layer and the drain electrode layer is formed using the sputtering target described in Embodiment 1. The conductive film is formed in contact with the oxide semiconductor film that is used as an active layer, whereby impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film and the purity of the oxide semiconductor can be increased. In addition, moisture remaining in the reaction atmosphere is removed in forming the oxide semiconductor film, whereby the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Thus, the oxide semiconductor film can be stabilized.

[0401]

As described above, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided. Further, the transistor described in this embodiment, in which off-state current is reduced is used in, for example, in a pixel in a display device so that a period in which a storage capacitor provided in the pixel can hold voltage can be increased. Thus, a display device which consumes less power in displaying a still image or the like can be provided.

[0402]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0403]

(Embodiment 9)

In this embodiment, another example of a transistor that is manufactured using the target described in Embodiment 1 will be described. In a transistor 380 described

in this embodiment, a conductive film formed using the sputtering target described in Embodiment 1 can be used as a conductive film for a source electrode and a drain electrode.

[0404]

In this embodiment, an example of a manufacturing process of a transistor, which is partly different from that of Embodiment 6, will be described with reference to FIG. 11. Since a manufacturing process of a transistor in FIG. 11 is the same as that of the transistor in FIGS. 8A to 8E except for some steps, the same reference numerals are used for the same portions, and detailed description of the same portions is not given.

[0405]

In accordance with Embodiment 6, a gate electrode layer 381 is formed over a substrate 370, and a first gate insulating layer 372a and a second gate insulating layer 372b are stacked. In this embodiment, a gate insulating layer has a two-later structure, in which a nitride insulating layer is used as the first gate insulating layer 372a and an oxide insulating layer is used as the second gate insulating layer 372b.

[0406]

As the oxide insulating layer, a silicon oxide layer, a silicon oxynitride layer, an aluminum oxide layer, an aluminum oxynitride layer, or the like can be used. As the nitride insulating layer, a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, an aluminum nitride oxide layer, or the like can be used.

[0407]

In this embodiment, the gate insulating layer has a structure in which a silicon nitride layer and a silicon oxide layer are stacked in this order over the gate electrode layer 381. A silicon nitride layer ($SiN_y$ ($y > 0$)) with a thickness greater than or equal to 50 nm and less than or equal to 200 nm (50 nm in this embodiment) is formed as the first gate insulating layer 372a by a sputtering method, and a silicon oxide layer ($SiO_x$ ($x > 0$)) with a thickness greater than or equal to 5 nm and less than or equal to 300 nm (100 nm in this embodiment) is stacked as the second gate insulating layer 372b over the first gate insulating layer 372a, whereby a gate insulating layer with a thickness of 150 nm is formed.

[0408]

Next, an oxide semiconductor film is formed and is processed into an island-shaped oxide semiconductor layer in a photolithography step. In this embodiment, the oxide semiconductor film is formed using an In-Ga-Zn-O-based oxide semiconductor target for film formation by a sputtering method.

[0409]

In that case, the oxide semiconductor film is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor film.

[0410]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed, whereby the concentration of impurities in the oxide semiconductor film formed in the treatment chamber can be reduced.

[0411]

As a sputtering gas used for forming the oxide semiconductor film, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0412]

Next, dehydration or dehydrogenation of the oxide semiconductor layer is performed. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 425 °C. Note that in the case where the temperature is higher than or equal to 425 °C, the heat treatment time may be one hour or less, whereas in the case where the temperature is lower than 425 °C, the heat treatment time is longer than one hour. Here, the substrate is put in an electric furnace that is a kind of heat treatment apparatus, and heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere, and then water and hydrogen are prevented from entering the

oxide semiconductor layer with the oxide semiconductor layer not exposed to air; thus, the oxide semiconductor layer is obtained. After that, cooling is performed by introduction of a high-purity oxygen gas, a high-purity nitrous oxide ($N_2O$) gas, or ultra-dry air (having a dew point of −40 °C or lower, preferably −60 °C or lower) into the same furnace. It is preferable that the oxygen gas and the nitrous oxide ($N_2O$) gas do not contain water, hydrogen, and the like. Alternatively, the purity of an oxygen gas or a nitrous oxide ($N_2O$) gas which is introduced into the heat treatment apparatus is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (that is, the impurity concentration of the oxygen gas or the nitrous oxide gas is 1 ppm or lower, preferably 0.1 ppm or lower).

[0413]

Note that a heat treatment apparatus is not limited to an electric furnace; for example, an RTA (rapid thermal anneal) apparatus such as an LRTA (lamp rapid thermal anneal) apparatus or a GRTA (gas rapid thermal anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. In addition, the LRTA apparatus may be provided with not only a lamp but also a device for heating an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater. GRTA refers to a method of heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used. The heat treatment may be performed at 600 °C to 750 °C for several minutes by an RTA method.

[0414]

Further, after the first heat treatment for dehydration or dehydrogenation, heat treatment may be performed at higher than or equal to 200 °C and lower than or equal to 400 °C, preferably higher than or equal to 200 °C and lower than or equal to 300 °C, in an atmosphere of an oxygen gas or a nitrous oxide ($N_2O$) gas.

[0415]

The first heat treatment for the oxide semiconductor layer can be performed on

the oxide semiconductor film that has not been processed into the island-shaped oxide semiconductor layer. In that case, the substrate is taken out of the heat apparatus after the first heat treatment, and then a photolithography step is performed.

[0416]

The entire oxide semiconductor film is made to contain an excess amount of oxygen through the above-described steps, whereby the oxide semiconductor film has higher resistance, that is, the oxide semiconductor film becomes an i-type oxide semiconductor film. Thus, an oxide semiconductor layer 382 the entire region of which is an i-type region is obtained.

[0417]

Next, a conductive film is formed over the gate insulating layers 372a and 372b and the oxide semiconductor layer 382. The conductive film is formed by a sputtering method with the use of the sputtering target described in Embodiment 1. Furthermore, a resist mask is formed over the conductive film in a photolithography step and the conductive film is selectively etched, so that a source electrode layer 385a and a drain electrode layer 385b are formed. Then, an oxide insulating layer 386 is formed by a sputtering method.

[0418]

In that case, the oxide insulating layer 386 is preferably formed while moisture remaining in the treatment chamber is removed so that hydrogen, hydroxyl groups, or moisture is prevented from being contained in the oxide semiconductor layer 382 and the oxide insulating layer 386.

[0419]

Note that in this embodiment, as the conductive film for forming the source electrode layer and the drain electrode layer, a conductive film formed using the sputtering target described in Embodiment 1 is provided. The conductive film is a conductive film in which the hydrogen concentration is reduced, and thus can extract impurities such as hydrogen or water in the oxide semiconductor layer or the oxide insulating layer. Note that metal having a lower electronegativity than hydrogen is used as a material used for the conductive film, so that a larger amount of impurities can be extracted.

[0420]

In order to remove moisture remaining in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the treatment chamber evacuated with a cryopump, for example, a hydrogen atom, a compound containing a hydrogen atom such as water ($H_2O$), and the like are removed, whereby the concentration of impurities in the oxide insulating layer 386 formed in the treatment chamber can be reduced.

[0421]

As a sputtering gas used for forming the oxide insulating layer 386, a high-purity gas is preferably used, in which impurities such as hydrogen, water, hydroxyl groups, or hydride are removed so that the concentration is approximately several parts per million or approximately several parts per billion.

[0422]

Through the above-described steps, the transistor 380 can be manufactured.

[0423]

Next, in order to reduce variation in the electric characteristics of the transistor, heat treatment (preferably at higher than or equal to 150 °C and lower than 350 °C) may be performed in an inert gas atmosphere or a nitrogen gas atmosphere. For example, the heat treatment is performed at 250 °C in a nitrogen atmosphere for one hour.

[0424]

Further, heat treatment may be performed at higher than or equal to 100 °C and lower than or equal to 200 °C for greater than or equal to 1 hour and less than or equal to 30 hours. In this embodiment, the heat treatment is performed at 150 °C for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from room temperature to a temperature higher than or equal to 100 °C and lower than or equal to 200 °C and then decreased to room temperature. This heat treatment may be performed under reduced pressure before the formation of the oxide insulating layer. When the heat treatment is performed under reduced pressure, the heat treatment time can be shortened. This heat treatment enables a normally-off transistor to be obtained. Thus, the reliability of a

semiconductor device can be increased.

[0425]

A protective insulating layer 373 is formed over the oxide insulating layer 386. In this embodiment, as the protective insulating layer 373, a silicon nitride film is formed to a thickness of 100 nm by a sputtering method.

[0426]

The protective insulating layer 373 and the first gate insulating layer 372a that are formed of nitride insulating layers do not contain impurities such as moisture, hydrogen, hydride, or hydroxide and have an effect of blocking entry of these impurities from the outside.

[0427]

Thus, in a manufacturing process after the formation of the protective insulating layer 373, entry of impurities such as moisture from the outside can be prevented. In addition, entry of impurities such as moisture from the outside can be prevented for a long time even after a device is completed as a semiconductor device; thus, the long-term reliability of the device can be improved.

[0428]

Alternatively, the insulating layers provided between the protective insulating layer 373 and the first gate insulating layer 372a that are formed of nitride insulating layers may be removed, so that the protective insulating layer 373 is in contact with the first gate insulating layer 372a.

[0429]

Thus, impurities such as moisture, hydrogen, hydride, or hydroxide in the oxide semiconductor layer are reduced to the minimum and entry of the impurities is prevented, so that the concentration of impurities in the oxide semiconductor layer can be kept low.

[0430]

A planarizing insulating layer for planarization may be provided over the protective insulating layer 373.

[0431]

In the transistor described in this embodiment, the conductive film that is used as the source electrode layer and the drain electrode layer is formed using the sputtering

target described in Embodiment 1. The conductive film is formed in contact with the oxide semiconductor film that is used as an active layer, whereby impurities such as hydrogen or water in the oxide semiconductor film are extracted by the conductive film and the purity of the oxide semiconductor film can be increased. In addition, moisture remaining in the reaction atmosphere is removed in forming the oxide semiconductor film, whereby the concentration of hydrogen and hydride in the oxide semiconductor film can be further reduced. Thus, the oxide semiconductor film can be stabilized.

[0432]

As described above, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided. Further, the transistor in which off-state current is reduced is used in, for example, a pixel in a display device, so that a period in which a storage capacitor provided in the pixel can hold voltage can be increased. Thus, a display device which consumes less power in displaying a still image or the like can be provided.

[0433]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0434]

(Embodiment 10)

In this embodiment, another example of a transistor that is manufactured using the target described in Embodiment 1 will be described. The transistor described in this embodiment can be used as the transistors described in Embodiments 2 to 9.

[0435]

In this embodiment, an example in which a light-transmitting conductive material is used for a gate electrode layer, a source electrode layer, and a drain electrode layer will be described. Other than the above, the transistor can be manufactured in a manner similar to those of the above embodiments, and description of the same parts or parts having functions and process similar to those in the above embodiments is not given. In addition, detailed description of the same parts is omitted.

[0436]

As materials for the gate electrode layer, the source electrode layer, and the drain electrode layer, a conductive material that transmits visible light can be used.

For example, any of the following metal oxides can be used: an In-Sn-O-based metal oxide; an In-Sn-Zn-O-based metal oxide; an In-Al-Zn-O-based metal oxide; a Sn-Ga-Zn-O-based metal oxide; an Al-Ga-Zn-O-based metal oxide; a Sn-Al-Zn-O-based metal oxide; an In-Zn-O-based metal oxide; a Sn-Zn-O-based metal oxide; an Al-Zn-O-based metal oxide; an In-O-based metal oxide; a Sn-O-based metal oxide; and a Zn-O-based metal oxide. The thickness thereof is set in the range of greater than or equal to 50 nm and less than or equal to 300 nm as appropriate. As a deposition method of the metal oxide used for the gate electrode layer, the source electrode layer, and the drain electrode layer, a sputtering method, a vacuum evaporation method (an electron beam evaporation method or the like), an arc discharge ion plating method, or a spray method is used. In the case where a sputtering method is employed, deposition is preferably performed using a target containing $SiO_2$ at greater than or equal to 2 wt% and less than or equal to 10 wt%, so that $SiO_x$ ($x > 0$) which inhibits crystallization is contained in the light-transmitting conductive film; in this way, the oxide semiconductor film can be prevented from being crystallized in heat treatment performed later.

[0437]

Note that the unit of the percentage of components in the light-transmitting conductive film is atomic percent, and the percentage of components is evaluated by analysis using an electron probe X-ray microanalyzer (EPMA).

[0438]

In a pixel in which the transistor is provided, when a pixel electrode layer, another electrode layer (such as a capacitor electrode layer), or a wiring layer (such as a capacitor wiring layer) is formed using a conductive film that transmits visible light, a display device having high aperture ratio can be realized. Needless to say, a gate insulating layer, an oxide insulating layer, a protective insulating layer, and a planarization insulating layer in the pixel are also preferably formed using a film that transmits visible light.

[0439]

In this specification, a film that transmits visible light means a film having a thickness that allows a visible light transmittance of 75 % to 100 %. In the case where

the film has conductivity, the film is also referred to as a transparent conductive film. Further, a conductive film which is semi-transparent to visible light may be used for metal oxide which is used for the gate electrode layer, the source electrode layer, the drain electrode layer, the pixel electrode layer, another electrode layer, or another wiring layer. The conductive film which is semi-transparent to visible light means a film having a visible light transmittance of 50 % to 75 %.

[0440]

When the transistor has light-transmitting properties as described above, the aperture ratio can be increased. In particular, for small liquid crystal display panels of 10 inches or smaller, high aperture ratio can be achieved even when the size of pixels is decreased in order to realize higher resolution of display images by, for example, increasing the number of gate wirings. Further, by using a light-transmitting film for components in a transistor, even when a group of high-density transistors is provided, high aperture ratio can be obtained and a sufficient area of a display region can be secured. Further, when a storage capacitor is formed using a material through a step that are the same as those of the component in the transistor, the storage capacitor can also have light-transmitting properties, which results in a further increase in the aperture ratio.

[0441]

Further, the purified oxide semiconductor layer is used in the transistor, whereby a transistor in which off-state current is reduced can be provided. Further, the transistor in which off-state current is reduced is used in, for example, a pixel in a display device, so that a period in which a storage capacitor provided in the pixel can hold voltage can be increased. Thus, a display device which consumes less power in displaying a still image or the like can be provided.

[0442]

This embodiment can be implemented in appropriate combination with any of the structures of the other embodiments.

[0443]

(Embodiment 11)

A variety of electronic devices can be completed using a semiconductor device such as the transistors described in Embodiments 2 to 10. In a transistor manufactured

using the target described in Embodiment 1, an oxide semiconductor layer whose purity is increased is used as an active layer; thus, off-state current can be reduced. In addition, a transistor which has less variation in the threshold voltage and high reliability can be obtained. Thus, electronic devices as end products can be manufactured with high throughput and high quality.

[0444]

In this embodiment, specific application examples to electronic devices are described with reference to FIGS. 16A to 16F. Note that examples of electronic devices include a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone handset (also referred to as a mobile phone or a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large game machine such as a pinball machine, and the like. Note that the semiconductor devices according to Embodiments 2 to 10 may be integrated to be mounted on a circuit board or the like so as to be incorporated in electronic devices, or can be used as a switching element of a pixel portion. The transistor described in Embodiments 2 to 10 has a small amount of off-state current and less variation in the threshold voltage, and thus can be favorably used in both a pixel portion and a driver circuit portion.

[0445]

FIG. 16A illustrates a laptop personal computer that includes any of the semiconductor devices according to Embodiments 2 to 10 and includes a main body 501, a housing 502, a display portion 503, keyboard 504, and the like.

[0446]

FIG. 16B is a portable information terminal (personal digital assistance (PDA)) that includes any of the semiconductor devices according to Embodiments 2 to 10. In a main body 511, a display portion 513, an external interface 515, operation buttons 514, and the like are provided. In addition, the personal information terminal includes a stylus 512 as an accessory for operation.

[0447]

FIG. 16C illustrates an e-book reader 520 as an example of a device that includes an electronic paper in which any of the semiconductor devices according to

Embodiments 2 to 10 is included. The e-book reader 520 includes two housings: a housing 521 and a housing 523. The housing 521 and the housing 523 are combined with a hinge 537 so that the e-book reader 520 can be opened and closed with the hinge 537 as an axis. Such a structure enables the e-book reader 520 to be used like a paper book.

[0448]

A display portion 525 and a display portion 527 are incorporated in the housing 521 and the housing 523, respectively. The display portion 525 and the display portion 527 may display one image or different images. In the structure where different images are displayed on the display portion 525 and the display portion 527, for example, the right display portion (the display portion 525 in FIG. 16C) can display text and the left display portion (the display portion 527 in FIG. 16C) can display images.

[0449]

FIG. 16C illustrates an example in which the housing 521 is provided with an operation portion and the like. For example, the housing 521 is provided with a power source 531, operation keys 533, a speaker 535, and the like. Pages can be turned with the operation keys 533. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. Furthermore, an external connection terminal (an earphone terminal, a USB terminal, a terminal that can be connected to various cables such as an AC adapter and a USB cable, or the like), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Further, the e-book reader 520 may have a function of an electronic dictionary.

[0450]

Further, the e-book reader 520 may send and receive information wirelessly. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[0451]

Note that electronic paper can be used for electronic devices in all fields as long as the electronic devices display data. An electronic paper can be applied to, for example, posters, advertisement in vehicles such as trains, display in a variety of cards such as credit cards, and the like as well as e-book readers.

[0452]

FIG. 16D illustrates a mobile phone that includes any of the semiconductor devices according to Embodiments 2 to 10. The mobile phone includes two housings: a housing 540 and a housing 541. The housing 541 is provided with a display panel 542, a speaker 543, a microphone 544, a pointing device 546, a camera lens 547, an external connection terminal 548, and the like. The housing 540 is provided with a solar cell 549 that charges the mobile phone, an external memory slot 550, and the like. In addition, an antenna is incorporated in the housing 541.

[0453]

The display panel 542 is equipped with a touch panel function. A plurality of operation keys 545 displayed as images are indicated by dashed lines in FIG. 16D. Note that the mobile phone includes a booster circuit for increasing voltage output from the solar cell 549 to voltage needed for each circuit. In addition to the above structure, a contactless IC chip, a small memory device, and the like can be incorporated.

[0454]

The display orientation of the display panel 542 changes as appropriate in accordance with the usage pattern. Further, the mobile phone is provided with the camera lens 547 on the surface on which the display panel 542 is provided, and thus it can be used as a video phone. The speaker 543 and the microphone 544 can be used for a video phone, recording, playback, and the like without being limited to verbal communication. Moreover, the housings 540 and 541 in a state where they are developed as illustrated in FIG. 16D can be slid so that one is overlapped over the other; therefore, the size of the portable information terminal can be reduced, which makes the portable information terminal suitable for being carried.

[0455]

The external connection terminal 548 is connectable to an AC adaptor and a variety of cables such as a USB cable, which enables charging of the mobile phone and data communication between the mobile phone a personal computer or the like. Moreover, a larger amount of data can be stored and moved by inserting a recording medium to the external memory slot 550. Further, in addition to the above functions, an infrared communication function, a television reception function, or the like may be provided.

[0456]

FIG. 16E illustrates a digital camera that includes any of the semiconductor devices according to Embodiments 2 to 10. The digital camera includes a main body 561, a display portion A 567, an eyepiece 563, an operation switch 564, a display portion B 565, a battery 566, and the like.

[0457]

FIG. 16F illustrates a television set that includes any of the semiconductor devices according to Embodiments 2 to 10. In a television set 570, a display portion 573 is incorporated in a housing 571. Images can be displayed on the display portion 573. Here, the housing 571 is supported by a stand 575.

[0458]

The television set 570 can be operated with an operation switch of the housing 571 or a separate remote controller 580. Channels and volume can be controlled with operation keys 579 of the remote controller 580 so that an image displayed on the display portion 573 can be controlled. Further, the remote controller 580 may be provided with a display portion 577 for displaying data output from the remote controller 580.

[0459]

Note that the television set 570 is preferably provided with a receiver, a modem, and the like. With the receiver, a general television broadcast can be received. Moreover, when the display device is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver, between receivers, or the like) information communication can be performed.

[0460]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

This application is based on Japanese Patent Application serial no. 2009-260238 filed with Japan Patent Office on November 13, 2009, the entire contents of which are hereby incorporated by reference.

# CLAIMS

1. A sputtering target which is used for forming a conductive film, comprising:

a sintered body of a metal material having lower electronegativity than an hydrogen,

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

2. The sputtering target according to claim 1, wherein the filling rate of the sputtering target is greater than or equal to 90 % and less than or equal to 100 %.

3. A sputtering target which is used for forming a conductive film, comprising:

a sintered body of at least one metal material selected from the group consisting of aluminum, copper, chromium, tantalum, titanium, molybdenum, and tungsten,

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

4. The sputtering target according to claim 3, wherein the filling rate of the sputtering target is greater than or equal to 90 % and less than or equal to 100 %.

5. A sputtering target which is used for forming a conductive film, comprising:

a sintered body of a metal material in which silicon, titanium, tantalum, tungsten, molybdenum, chromium, neodymium, scandium, or yttrium is mixed with aluminum at 0.1 at.% to 3 at.%,

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

6. The sputtering target according to claim 5, wherein the filling rate of the sputtering target is greater than or equal to 90 % and less than or equal to 100 %.

7. A transistor comprising:

a semiconductor layer; and

a conductive film in contact with the semiconductor layer,

wherein the conductive film comprises a sintered body of a metal material having lower electronegativity than hydrogen, and

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

8. The transistor according to claim 7, wherein the conductive film is a source electrode or a drain electrode.

9. A transistor comprising:

a semiconductor layer; and

a conductive film in contact with the semiconductor layer,

wherein the conductive film comprises a sintered body of at least one metal material selected from the group consisting of aluminum, copper, chromium, tantalum, titanium, molybdenum, and tungsten, and

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

10. The transistor according to claim 9, wherein the conductive film is a source electrode or a drain electrode.

11. A transistor comprising:

a semiconductor layer; and

a conductive film in contact with the semiconductor layer,

wherein the conductive film comprises a sintered body of a metal material in which silicon, titanium, tantalum, tungsten, molybdenum, chromium, neodymium, scandium, or yttrium is mixed with aluminum at 0.1 at.% to 3 at.%, and

wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

12. The transistor according to claim 11, wherein the conductive film is a source electrode or a drain electrode.

13. A method for manufacturing a sputtering target, comprising the steps of:
forming a sintered body of a metal material by baking the metal material;
forming a target with a desired shape by machining the sintered body of the metal material;
cleaning the target; and
performing heat treatment on the cleaned target.

14. The method for manufacturing the sputtering target according to claim 13, wherein the metal material is at least one selected from the group consisting of aluminum, copper, chromium, tantalum, titanium, molybdenum, and tungsten.

15. The method for manufacturing the sputtering target according to claim 13, wherein the sintered body contains aluminum mixed silicon, titanium, tantalum, gungsten, molybdenum, chromium, neodymium, scandium, or yttrium at 0.1 at.% to 3 at.%.

16. The method for manufacturing the sputtering target according to claim 13, wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

17. The method for manufacturing the sputtering target according to claim 13, wherein the filling rate of the sputtering target is greater than or equal to 90 % and less than or equal to 100 %.

18. A method for manufacturing a sputtering target, comprising the steps of:
forming a sintered body of a metal material by baking the metal material;
forming a target with a desired shape by machining the sintered body of the

metal material;

cleaning the target;

performing heat treatment on the cleaned target; and

attaching the target to a backing plate.

19. The method for manufacturing the sputtering target according to claim 18, wherein the metal material is at least one selected from the group consisting of aluminum, copper, chromium, tantalum, titanium, molybdenum, and tungsten.

20. The method for manufacturing the sputtering target according to claim 18, wherein the sintered body contains aluminum mixed silicon, titanium, tantalum, gungsten, molybdenum, chromium, neodymium, scandium, or yttrium at 0.1 at.% to 3 at.%.

21. The method for manufacturing the sputtering target according to claim 18, wherein the concentration of hydrogen contained in the sintered body is lower than or equal to $1 \times 10^{16}$ atoms/cm$^3$.

22. The method for manufacturing the sputtering target according to claim 18, wherein the filling rate of the sputtering target is greater than or equal to 90 % and less than or equal to 100 %.

23. The method for manufacturing the sputtering target according to claim 18, wherein the backing plate is formed using copper, titanium, a copper alloy, or a stainless steel alloy.

FIG. 1A

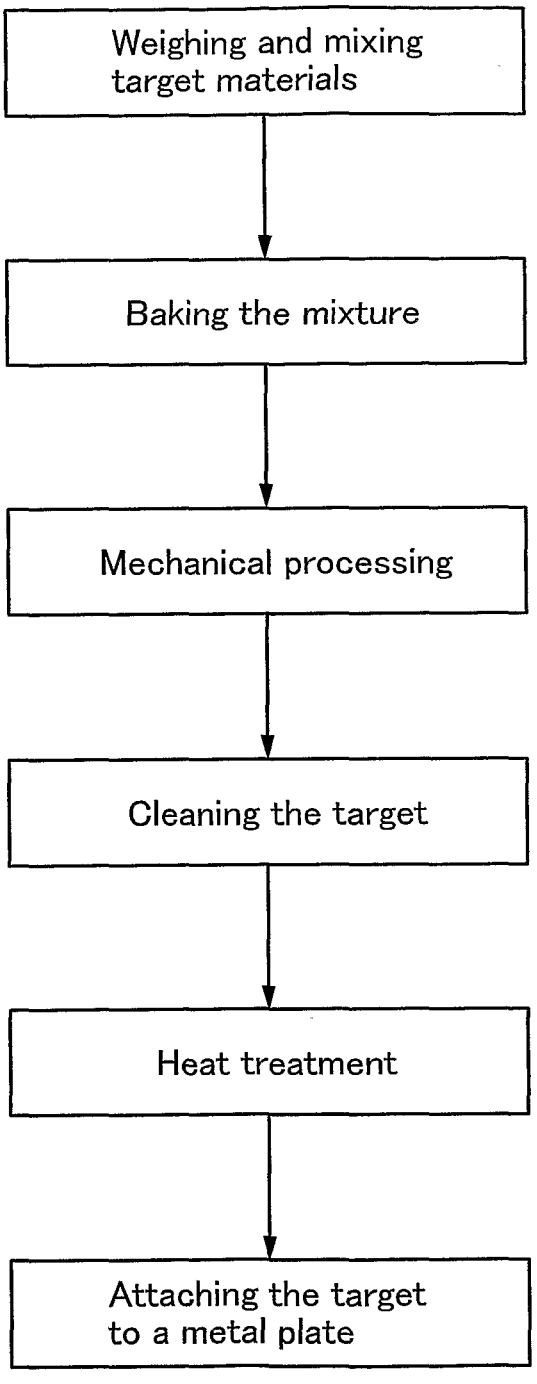



FIG. 1B

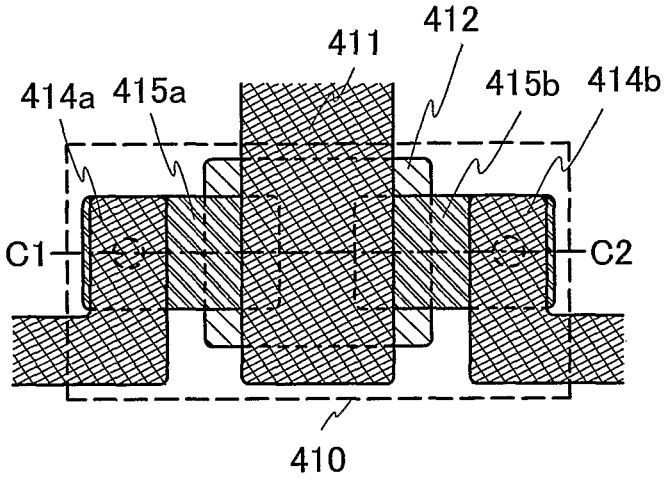
FIG. 1C

FIG. 1D

FIG. 1E

FIG. 1F

FIG. 2A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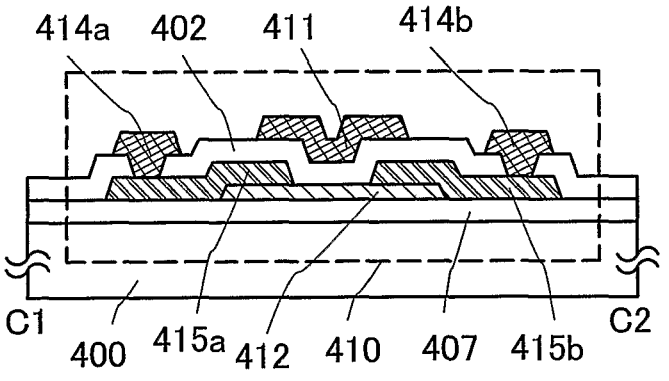
C1
C2
410

FIG. 2B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415b
C2

FIG. 3A

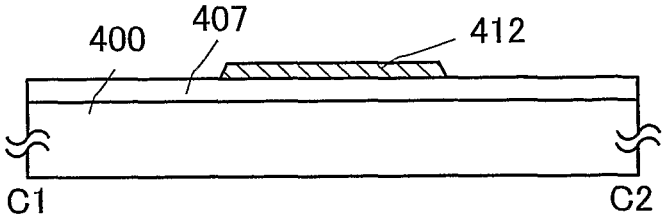


FIG. 3B

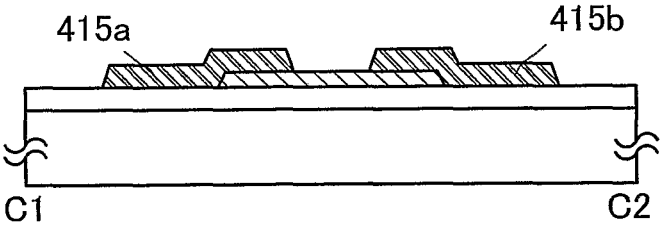


FIG. 3C

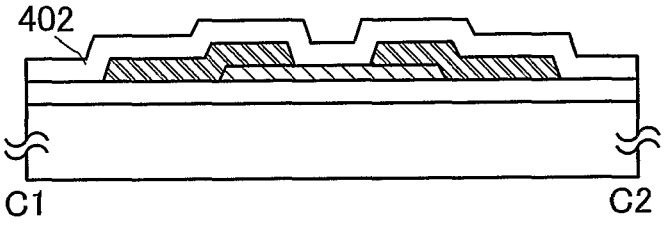


FIG. 3D

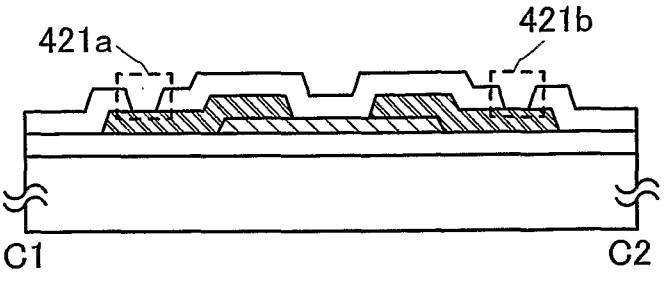


FIG. 3E

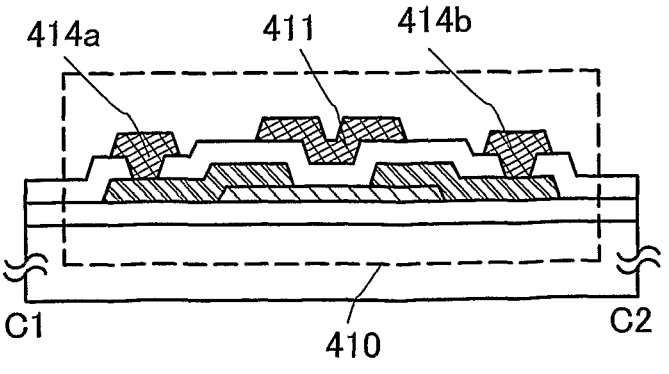

FIG. 4A

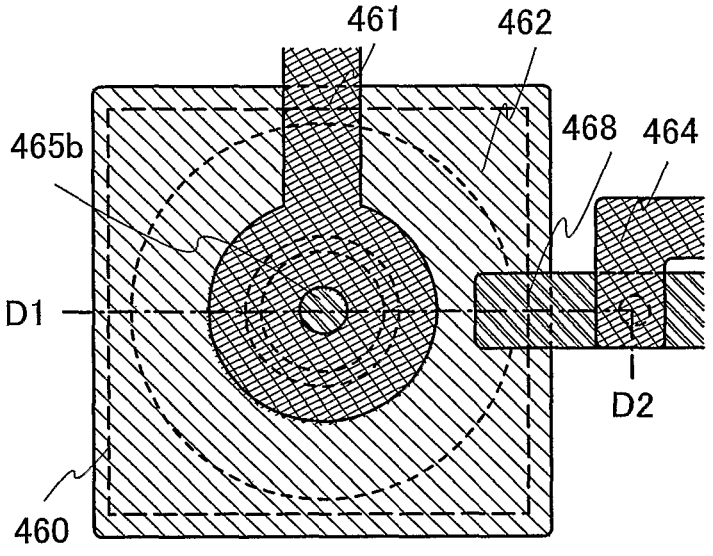
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FIG. 4B

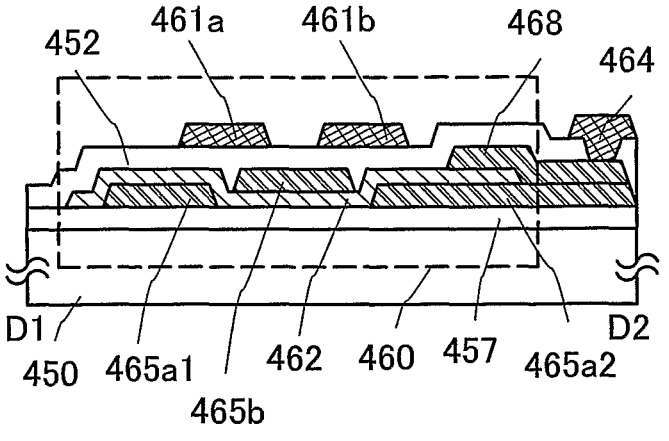
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FIG. 5A

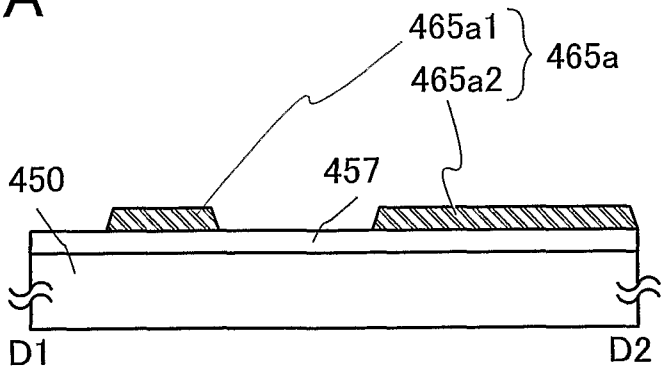


FIG. 5B

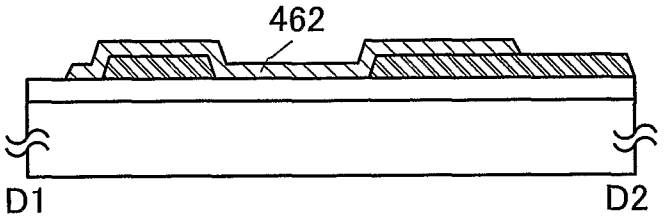


FIG. 5C

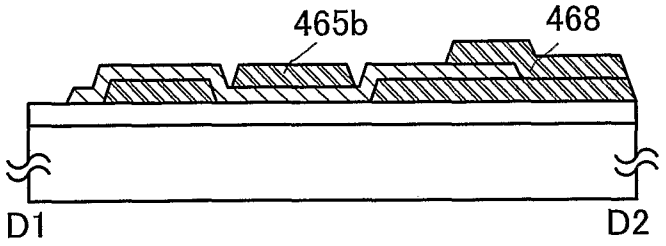


FIG. 5D

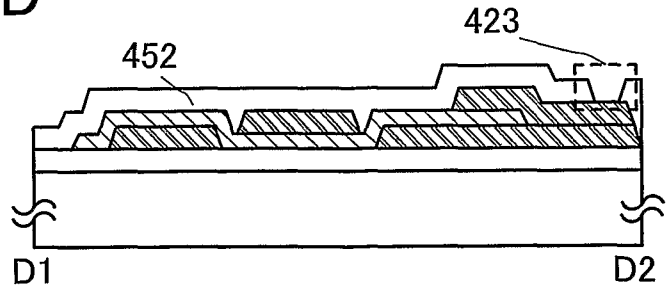


FIG. 5E

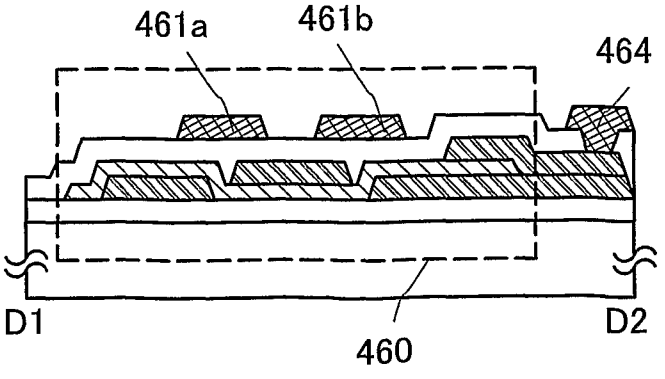

FIG. 6A

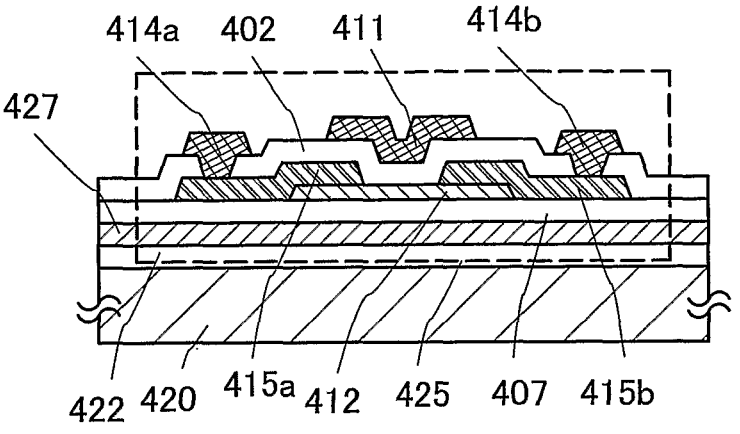
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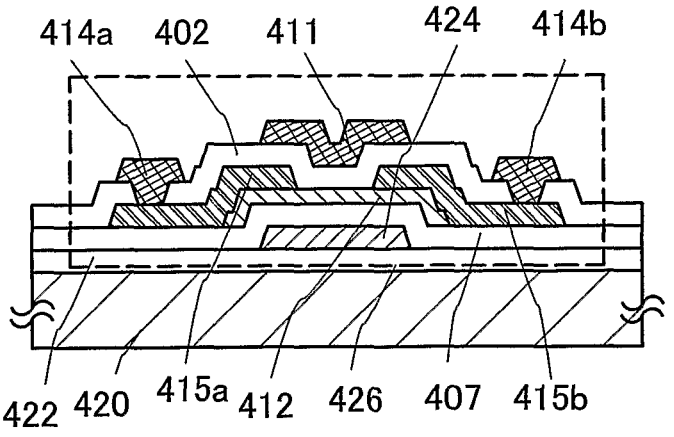
FIG. 6B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415b

FIG. 7A

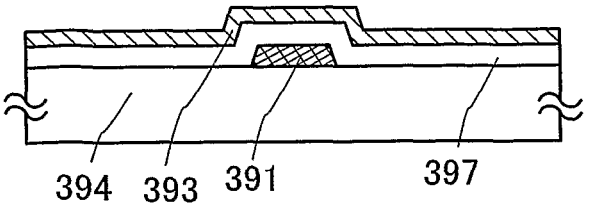



FIG. 7B

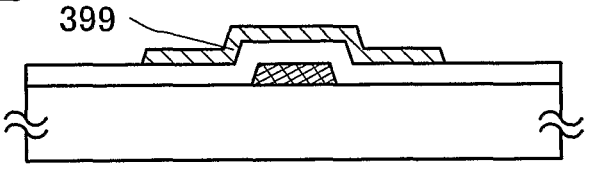



FIG. 7C

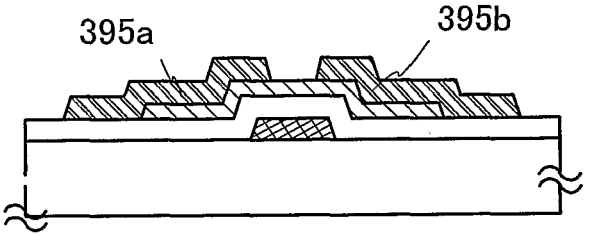



FIG. 7D

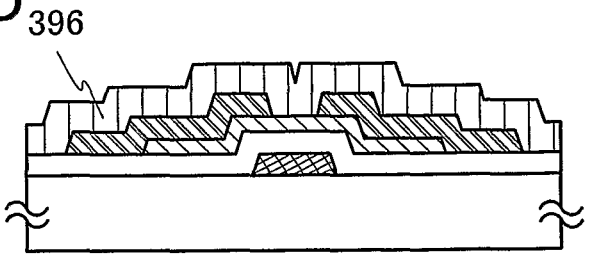



FIG. 7E

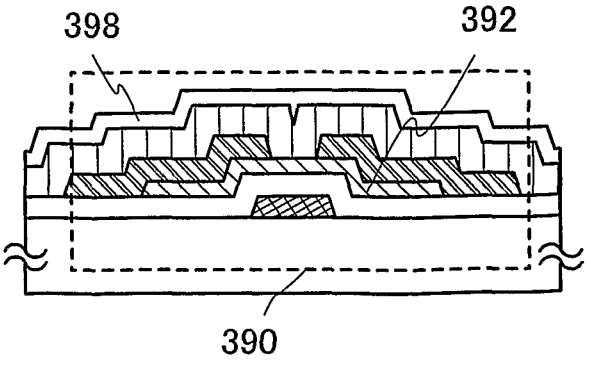


FIG. 8A

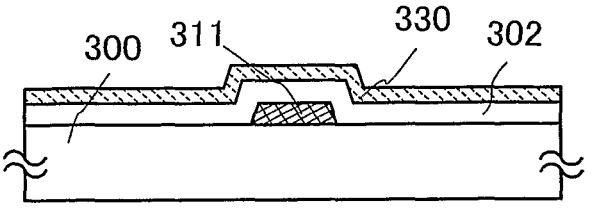



FIG. 8B

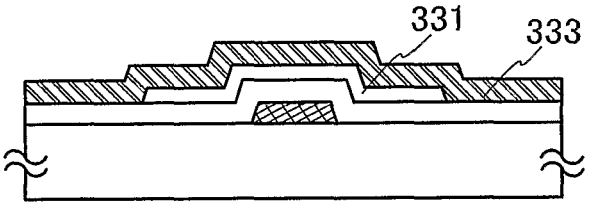



FIG. 8C

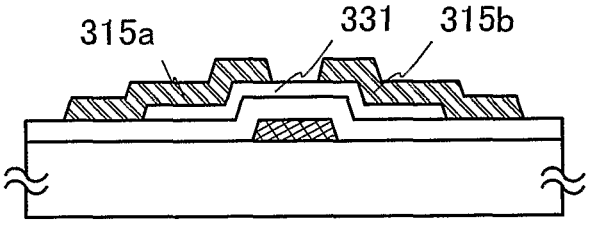



FIG. 8D

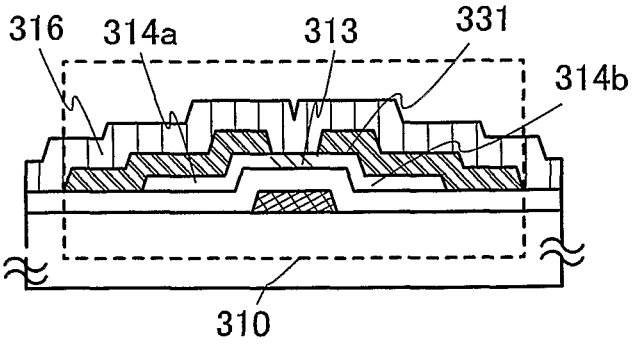



FIG. 8E

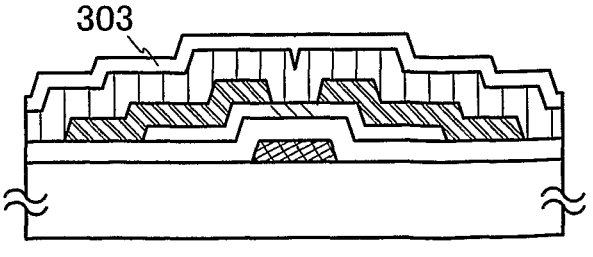


FIG. 9A

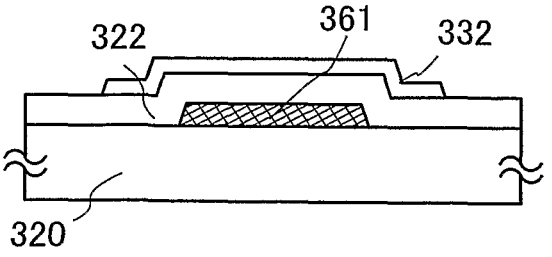



FIG. 9B

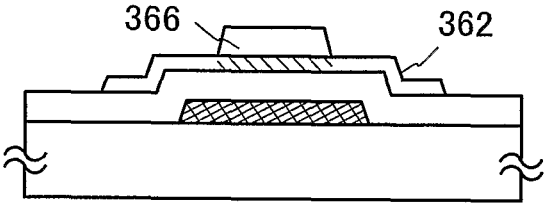



FIG. 9C

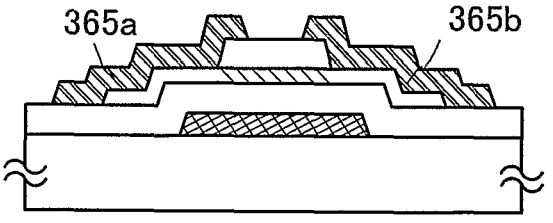



FIG. 9D

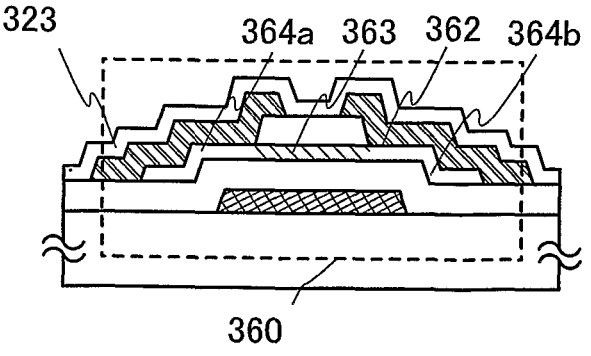


FIG. 10A

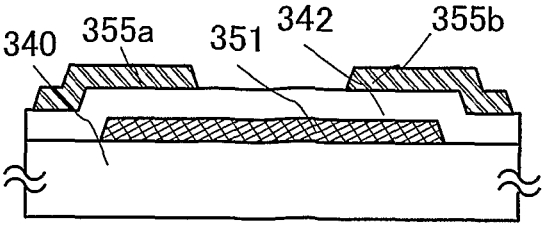



FIG. 10B

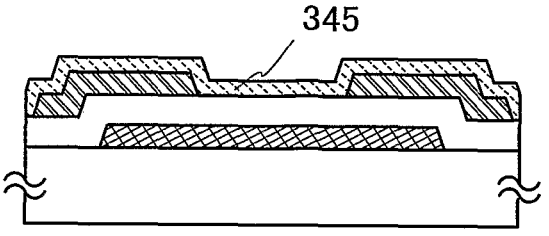



FIG. 10C

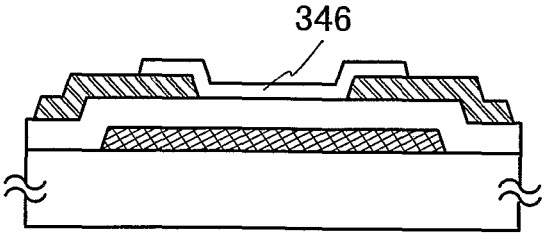



FIG. 10D

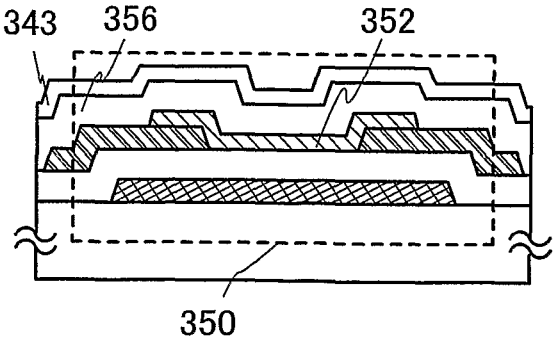


FIG. 11

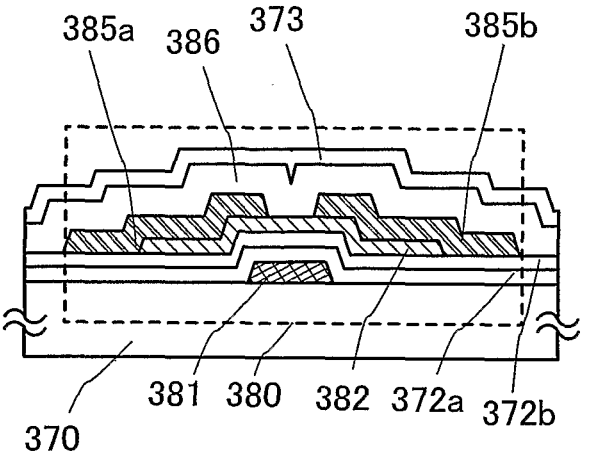


FIG. 12

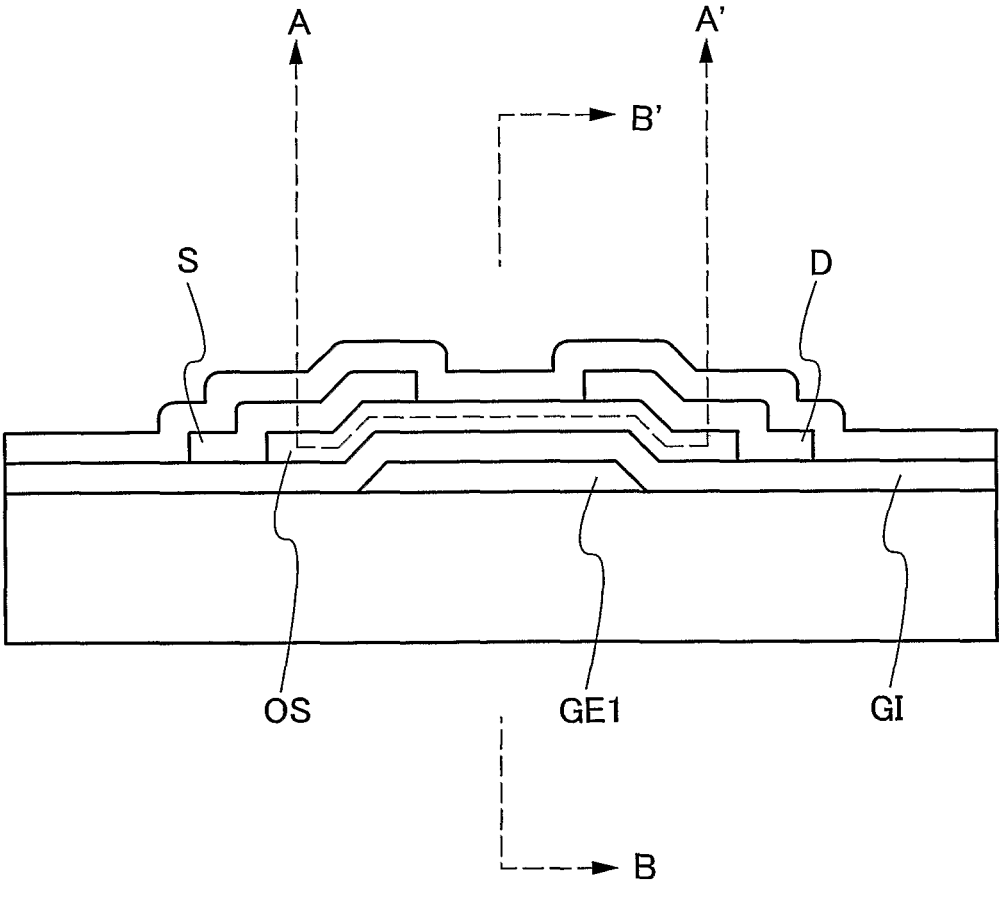


FIG. 13

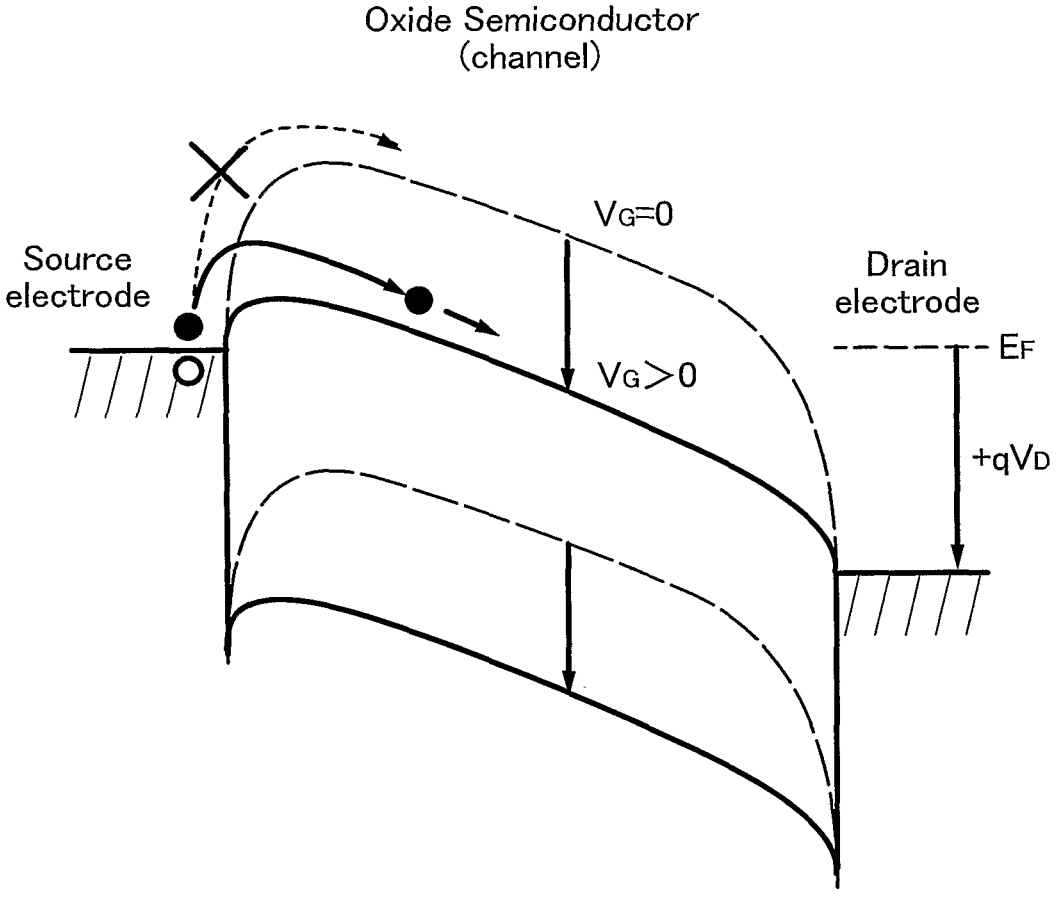
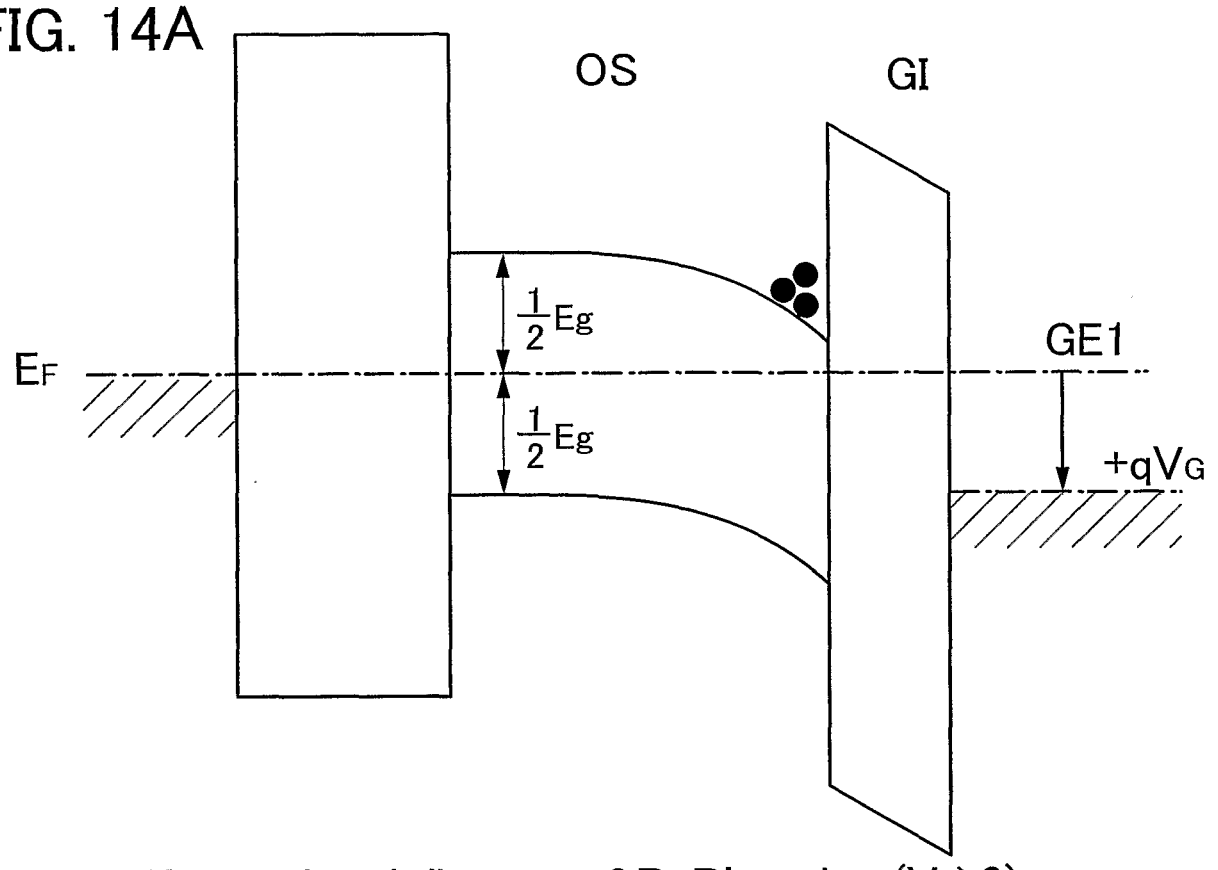
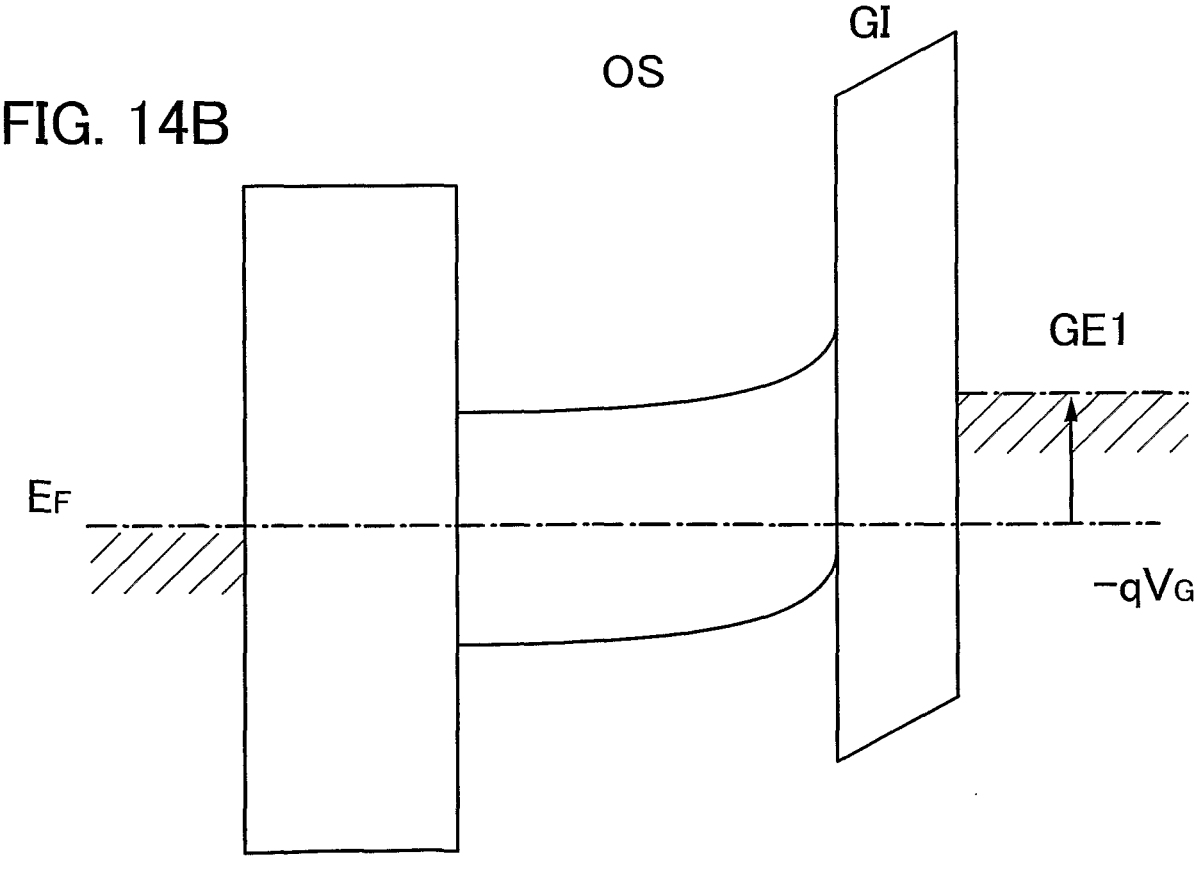

Oxide Semiconductor
(channel)
Source
electrode
VG=0
VG>0
Drain
electrode
EF
+qVD

FIG. 14A




Energy band diagram of B–B'section ($V_G$>0)

FIG. 14B




Energy band diagram of B–B'section ($V_G$<0)

FIG. 15

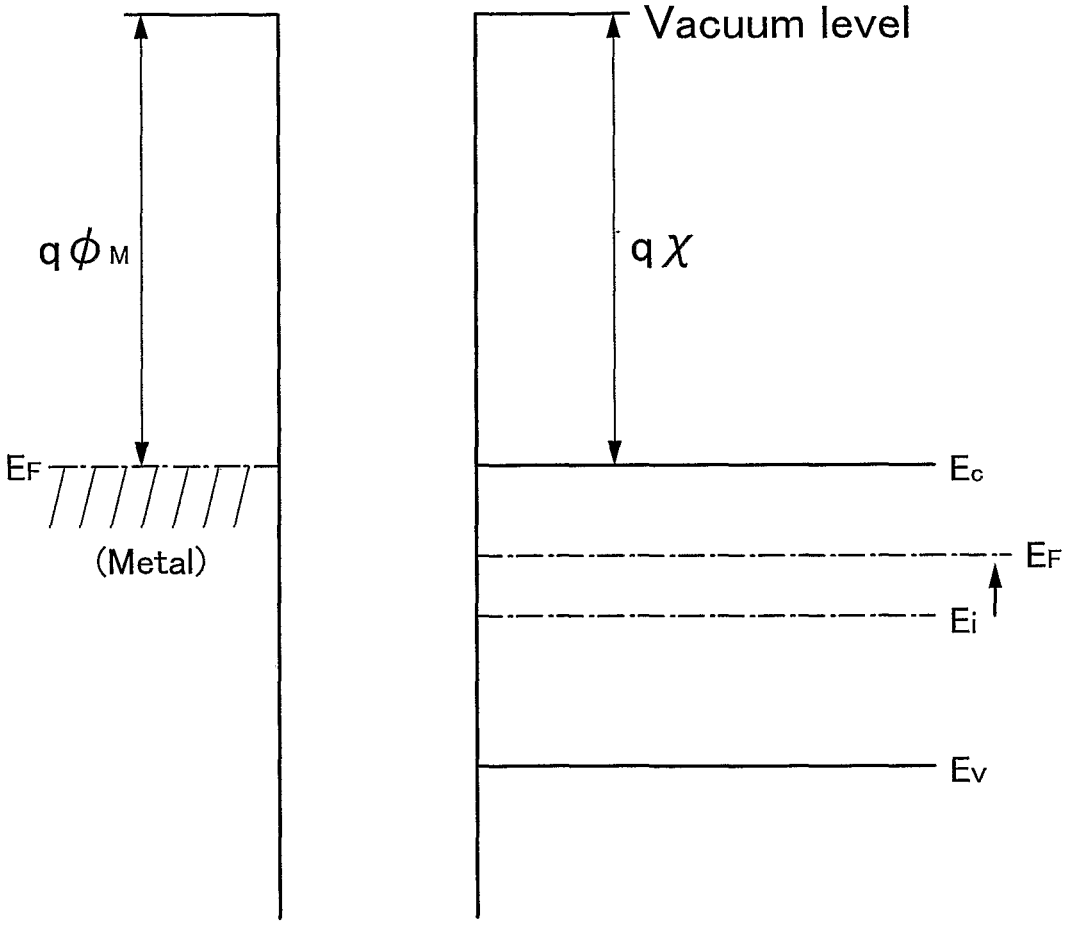


FIG. 16A

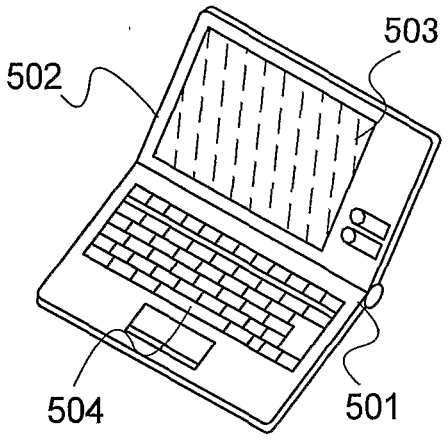



FIG. 16B

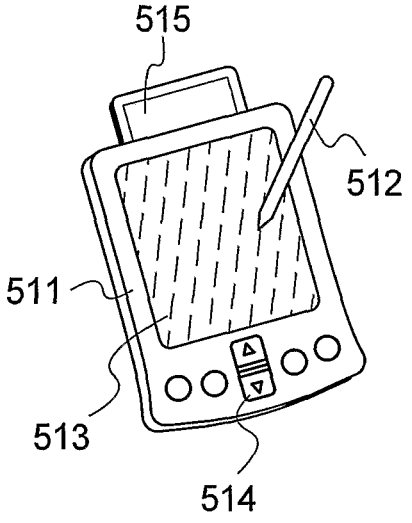



FIG. 16C

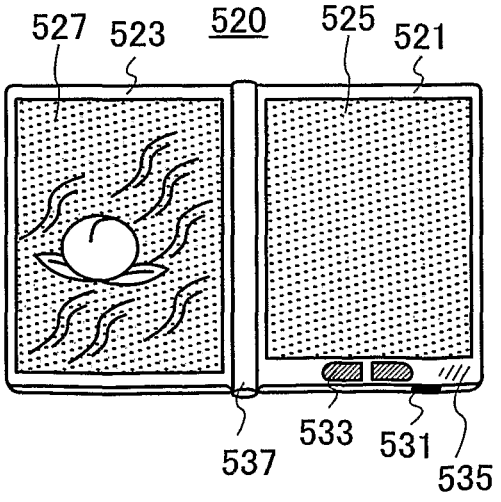



FIG. 16D

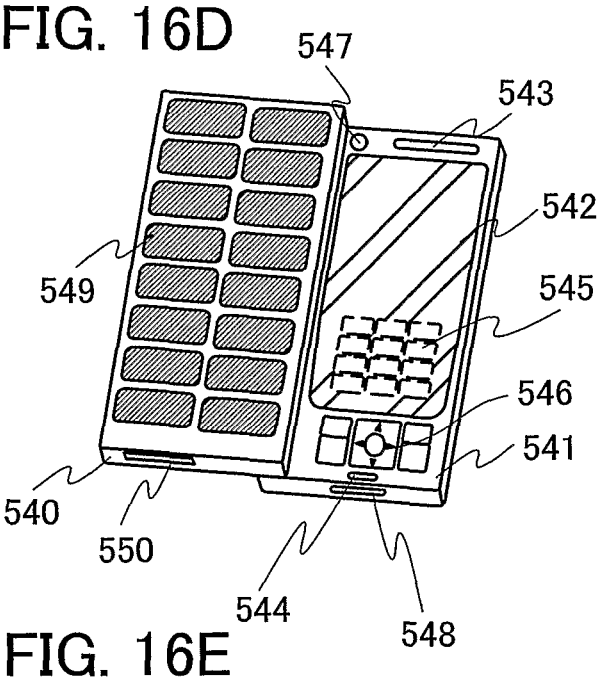



FIG. 16E

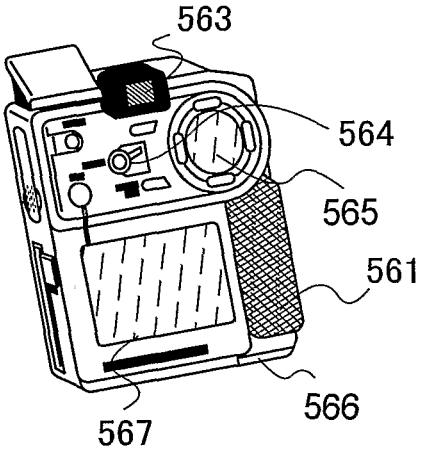
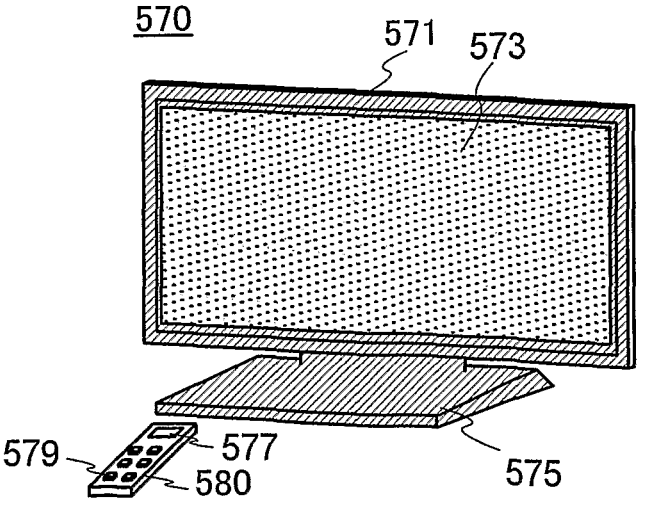



FIG. 16F



REFERENCE NUMERALS

300: substrate, 302: gate insulating layer, 303: protective insulating layer, 310: transistor, 311: gate electrode layer, 313: channel formation region, 314a: high-resistance source region, 314b: high-resistance drain region, 315a: source electrode layer, 315b: drain electrode layer, 316: oxide insulating layer, 320: substrate, 322: gate insulating layer, 323: protective insulating layer, 330: oxide semiconductor film, 331: oxide semiconductor layer, 332: oxide semiconductor layer, 333: conductive film, 340: substrate, 342: gate insulating layer, 343: protective insulating layer, 345: oxide semiconductor film, 346: oxide semiconductor layer, 350: transistor, 351: gate electrode layer, 352: oxide semiconductor layer, 355a: source electrode layer, 355b: drain electrode layer, 356: oxide insulating layer, 360: transistor, 361: gate electrode layer, 362: oxide semiconductor layer, 363: channel formation region, 364a: high-resistance source region, 364b: high-resistance drain region, 365a: source electrode layer, 365b: drain electrode layer, 366: oxide insulating layer, 370: substrate, 372a: gate insulating layer, 372b: gate insulating layer, 373: protective insulating layer, 380: transistor, 381: gate electrode layer, 382: oxide semiconductor layer, 385a: source electrode layer, 385b: drain electrode layer, 386: oxide insulating layer, 390: transistor, 391: gate electrode layer, 392: oxide

semiconductor layer, 393: oxide semiconductor film, 394: substrate, 395a: source electrode layer, 395b: drain electrode layer, 396: oxide insulating layer, 397: gate insulating layer, 398: protective insulating layer, 399: oxide semiconductor layer, 400: substrate, 402: gate insulating layer, 407: insulating layer, 410: transistor, 411: gate electrode layer, 412: oxide semiconductor layer, 414a: wiring layer, 414b: wiring layer, 415a: source electrode layer or drain electrode layer, 415b: source electrode layer or drain electrode layer, 420: silicon substrate, 421a: opening, 421b: opening, 422: insulating layer, 423: opening, 424: conductive layer, 425: transistor, 426: transistor, 427: conductive layer, 450: substrate, 452: gate insulating layer, 457: insulating layer, 460: transistor, 461: gate electrode layer, 462: oxide semiconductor layer, 464: wiring layer, 465a: source electrode layer or drain electrode layer, 465b: source electrode layer or drain electrode layer, 465a1: source electrode layer or drain electrode layer, 465a2: source electrode layer or drain electrode layer, 468: wiring layer, 501: main body, 502: housing, 503: display portion, 504: keyboard, 512: stylus, 513: display portion, 514: operation button, 515: external interface, 520: e-book reader, 521: housing, 523: housing, 525: display portion, 527: display portion, 531: power source, 533: operation key, 535: speaker, 537: hinge, 540: housing, 541: housing, 542: display panel, 543: speaker, 544: microphone, 545: operation key, 546: pointing device, 547: camera lens, 548: external connection terminal, 549: solar cell,

550: external memory slot, 561: main body, 563: eyepiece, 564: operation switch, 565: display portion B, 566: battery, 567: display portion A, 570: television set, 571: housing, 573: display portion, 575: stand, 577: display portion, 579: operation key, and 580: remote controller.

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/068797

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. C23C14/34(2006.01)i, H01L21/336(2006.01)i, H01L29/786(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. C23C14/00-14/58, H01L21/336, H01L29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y<br>A | WO 97/013885 A1<br>(Kabushiki Kaisha Toshiba) 1997.04.17,<br>claim 12, p11l26-p12l16, examples 4-8<br>& JP 2004-260194 A & JP 2006-100822 A<br>& JP 2006-111969 A & JP 2006-111970 A<br>& JP 4137182 B & JP 2009-149997 A<br>& JP 2010-31378 A & US 6329275 B1<br>& EP 855451 A1 & EP 1553205 A1 | 1-6<br>13-23<br>7-12 |
| Y | JP 2003-277924 A<br>(Sumitomo Metal Mining Co., Ltd.) 2003.10.02,<br>claims 1 and 6, paragraphs [0031] and [0032]<br>(Family: none) | 13-23 |

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 05.01.2011 | 18.01.2011 |

| Name and mailing address of the ISA/JP | Authorized officer |
|---|---|
| **Japan Patent Office**<br>3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan | WAKATSUCHI, Masayuki 4G 3774<br>Telephone No. +81-3-3581-1101 Ext. 3416 |

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/JP2010/068797

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | JP 2003-213407 A<br>(Nippon Mining & Metals Co., Ltd.) 2003.07.30,<br>claims 15 and 16, paragraph [0011]<br>& WO 2003/062488 A | 13-23 |
| Y | JP 11-050244 A<br>(Ryoka-Matthey Co., Ltd.) 1999.02.23,<br>claim 2, paragraph [0017]<br>(Family: none) | 13-23 |
| A | JP 2007-123861 A<br>(Semiconductor Energy Laboratory Co., Ltd.)<br>2007.05.17, the whole document<br>& JP 2009-21612 A & JP 2009-260378 A<br>& US 2007/0072439 A1 & US 2008/0308796 A1<br>& US 2008/0308797 A1 & US 2008/0308804 A1<br>& US 2008/0308805 A1 & US 2008/0308806 A1<br>& US 2009/0008639 A1 & US 2010/0136743 A<br>& EP 1770788 A2 & EP 1995787 A2 & EP 1998373 A2<br>& EP 1998374 A2 & EP 1998375 A2<br>& CN 1941299 A & CN 101335212 A<br>& CN 101335274 A & CN 101335275 A<br>& CN 101335276 A & CN 101335293 A<br>& CN 101335304 A & CN 101552210 A<br>& CN 101651105 A | 1-23 |
| A | JP 2007-096055 A<br>(Semiconductor Energy Laboratory Co., Ltd.)<br>2007.04.12, the whole document<br>(Family: none) | 1-23 |
| A | JP 10-219480 A<br>(Texas Instruments Inc.) 1998.08.18,<br>the whole document<br>& US 6673400 B1 & US 2004/0036168 A1<br>& EP 837502 A2 | 1-23 |

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/JP2010/068797

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:
The invention described as claim 1 does not have any special technical feature because the feature of claim 1 is not noble in view of D1 (WO97/013885 A1).
Therefore, this application involves multiple inventions; the main invention composed of claims 1 and 2, and some other inventions claims 3-23.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☑ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.