

[54] **DIGITAL PHASE SHIFTER**

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[51] Int. Cl. **H03h 7/18**

[58] Field of Search..... 307/295, 320, 262;
333/31 R, 24.1

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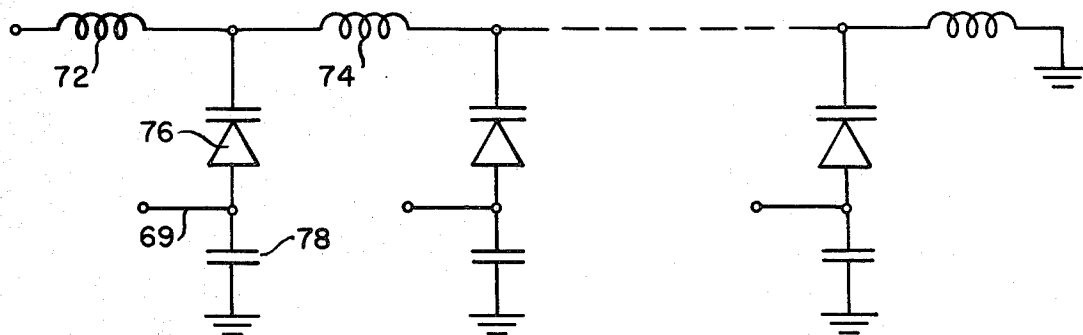
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[57] **ABSTRACT**

A low dissipation, digital, phase shifter comprising a plurality of quadrature hybrid circuits, each quadrature hybrid being loaded with a plurality of reactive-impedance circuits. These reactive-impedance circuits each comprise a varactor diode, a capacitor connecting the anode of the varactor to ground, a first inductor connected between the cathode of the varactor and an input to the quadrature hybrid, and a second inductor connected between the cathode of the varactor and ground. These capacitor and inductors act to linearize the reactive impedance seen by the quadrature hybrid.

4 Claims, 9 Drawing Figures



TRANSMITTING ANTENNA

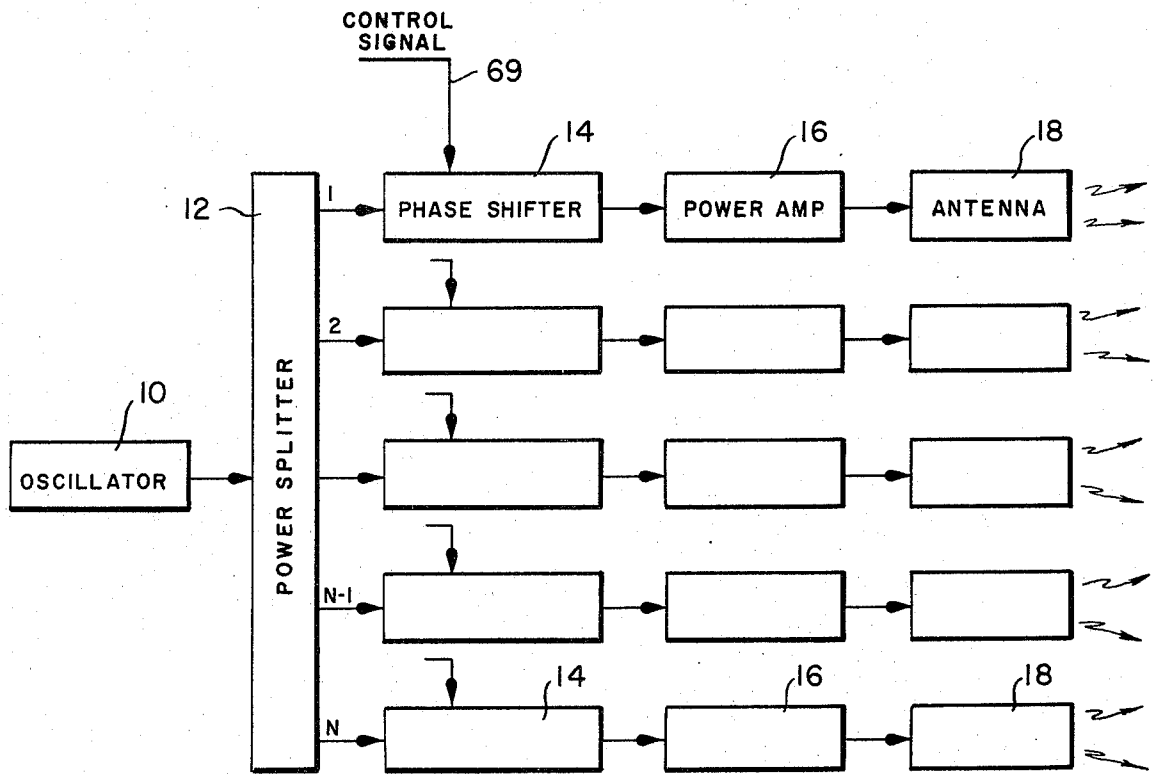


FIG. 1a.

RECEIVING ANTENNA

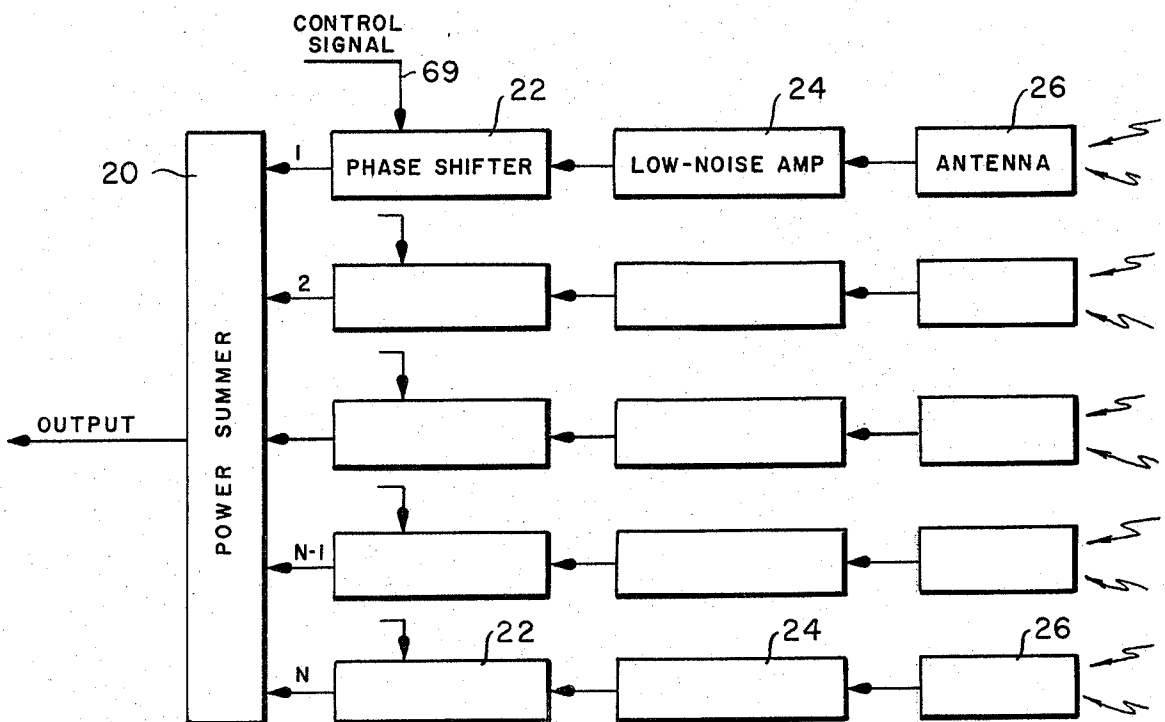
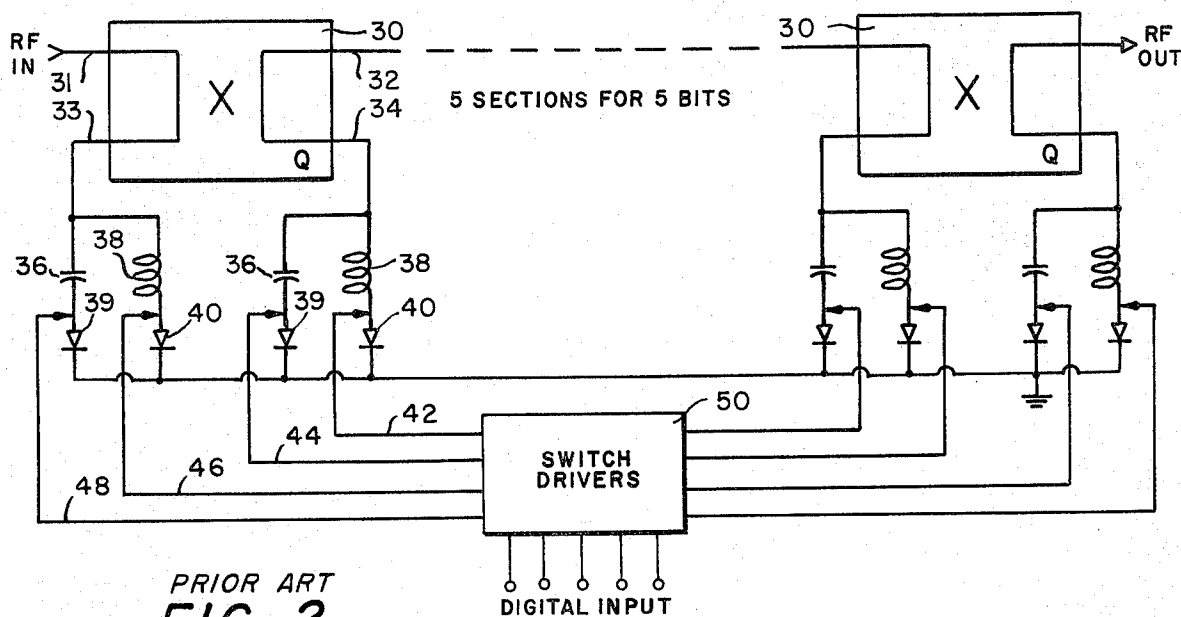


FIG. 1b.



PRIOR ART
FIG. 2.

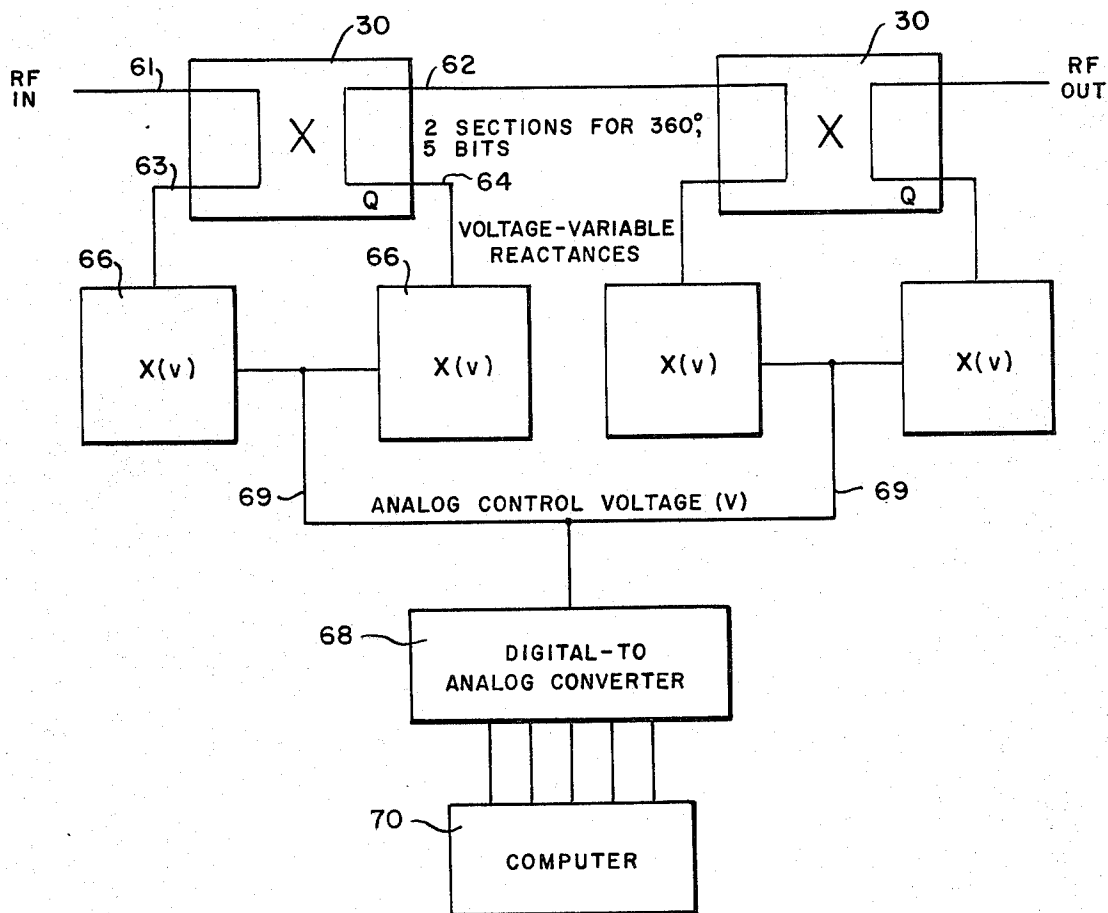
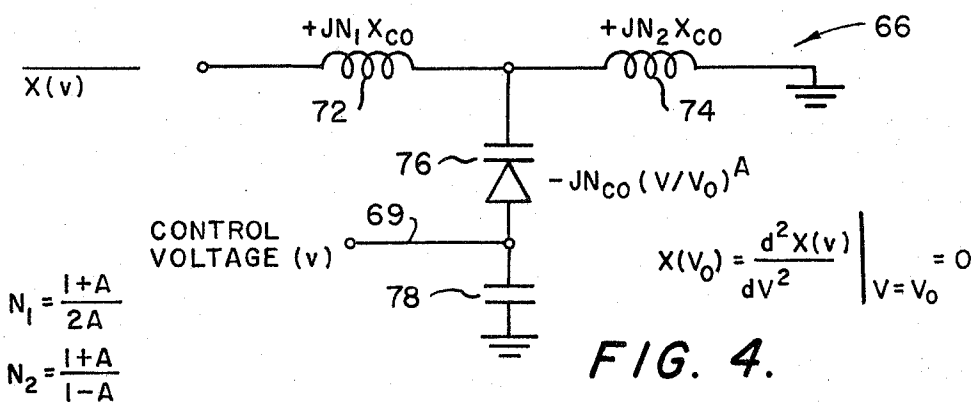
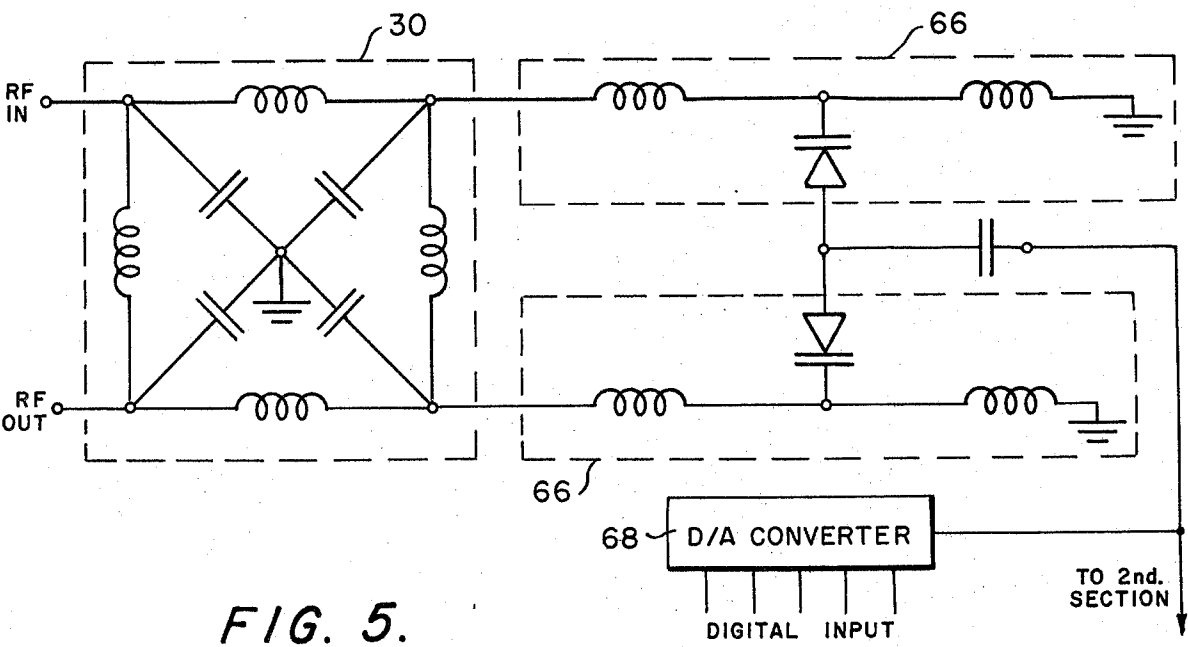
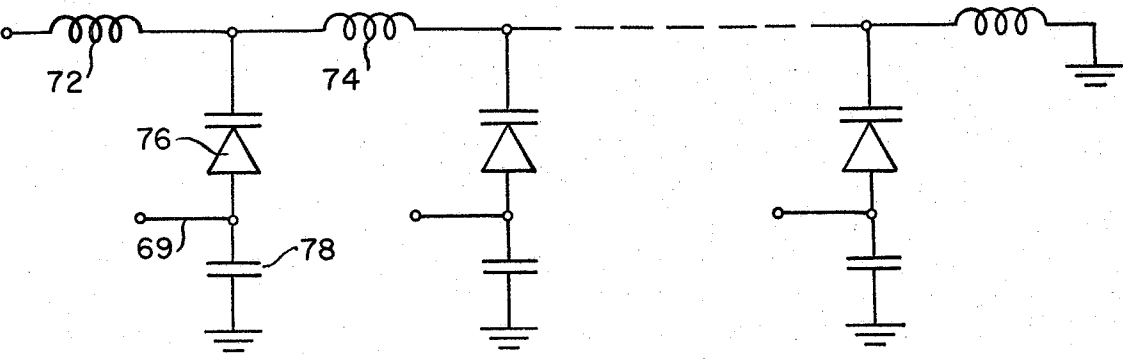


FIG. 3.



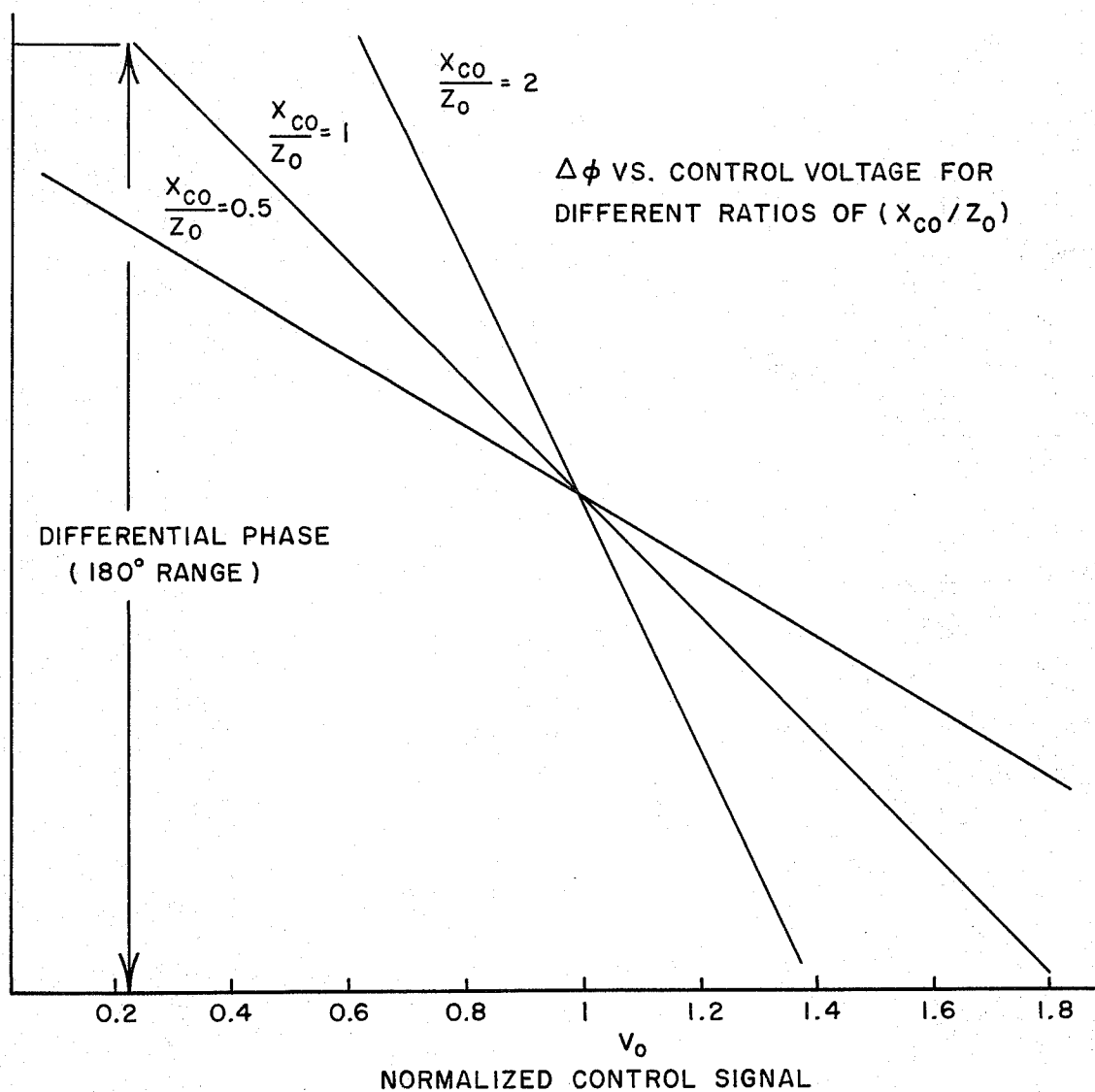


FIG. 7.

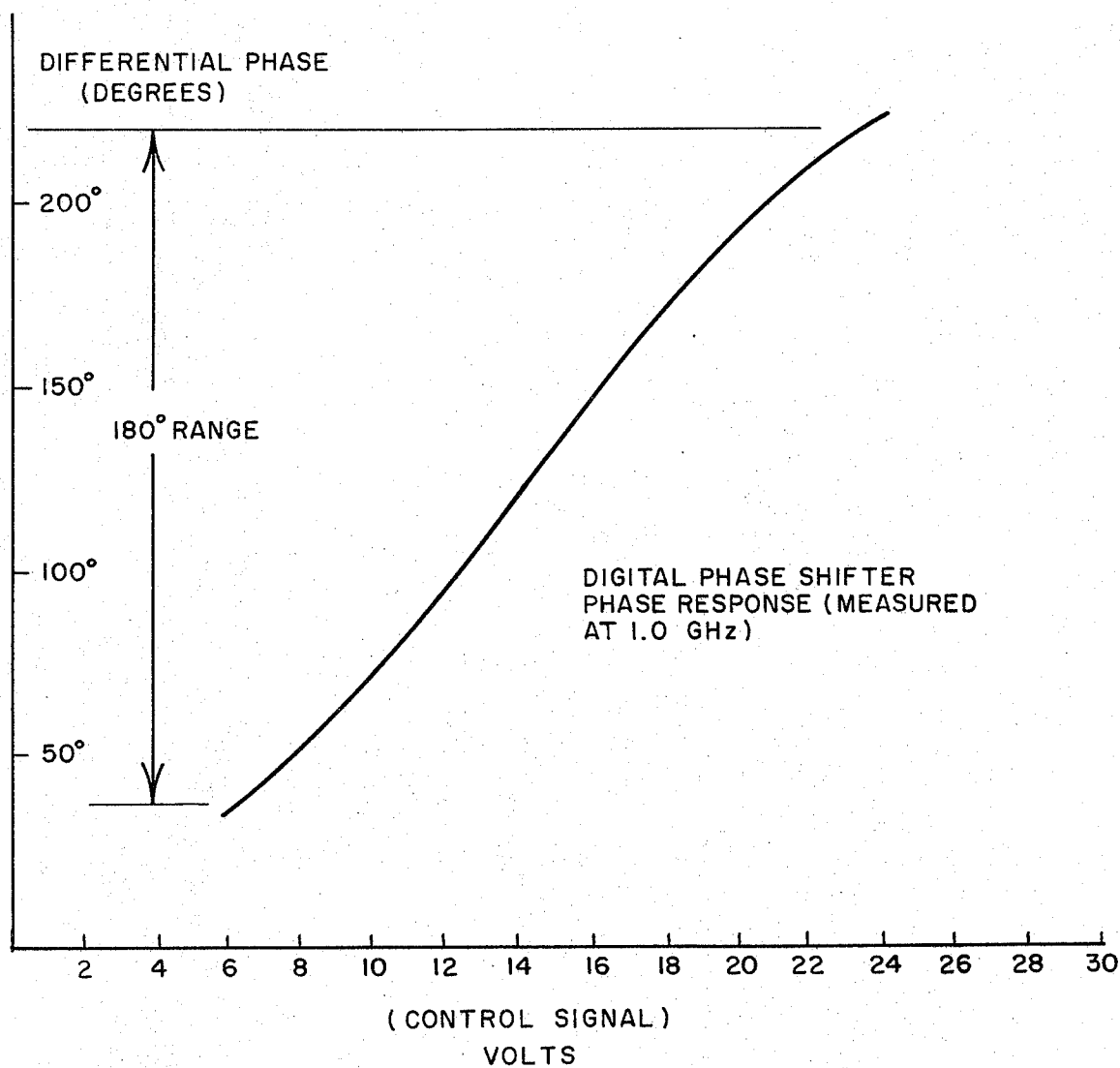


FIG. 8.

DIGITAL PHASE SHIFTER

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to phased arrays and, in particular, to a digital phase-shifter circuit to be used in a phased array.

2. Description of the Prior Art.

There are a large number of possible applications for phased arrays. Examples of such applications are for use in phased array antennas and for use in phase modulators. Such applications generally require large and very accurately controlled phase shifts.

The type of phase shifter used in the past in these applications was the hybrid-type, reflective, diode-switched phase shifter. This phase shifter is a well-documented device and finds uses in phased array applications as a digital phase bit. A 5-bit phase shifter of this type with its associated drive circuitry typically will dissipate about $\frac{1}{2}$ watt of control power when the different diodes used to vary the reactance in the phase shifter are being switched on and off. Such a power dissipation can be significant when this type of phase shifter is used in phased-array applications since thousands of phase shifters are used in each array. Thus for more efficient arrays, phase shifters are desired which require considerably less control power.

Analog phase shifters using varactor diodes as the line terminations have substantially lower power requirements and have been available for some years. But the highly non-linear tuning characteristic of the varactor phase shifter has previously prevented its use in phased-array applications where large and accurately controlled phase shifts are required. Such applications generally require a digitally controlled phase shifter. But in order to use a varactor phase shifter as a digitally controlled phase shifter, the tuning characteristic of the circuit must be linearized such that a control voltage can be successfully taken from a digital-to-analog converter and used to control the phase shifter. The circuit of the present invention has been successfully designed so as to linearize the tuning characteristic of a varactor phase shifter so that the control voltage can be digitally controlled.

SUMMARY OF THE INVENTION

Briefly, the present invention makes it possible to use varactor diodes with their low power dissipation as reactive loads on a quadrature-hybrid phase shifter network even in phased array applications where large and accurately controlled phase shifts are required. The phase shift of these varactor diodes can now be digitally controlled. This is done by adding a linearizing network consisting of capacitors and inductors to the varactor load circuit. This network linearizes the tuning characteristic of the varactor diode so that the varactor control voltage can be taken directly from a digital-to-analog converter and used to control the phase shift.

OBJECTS OF THE INVENTION

An object of the present invention is to considerably reduce the control power required to control a phase shifter.

A further object of this invention is to linearize the tuning characteristic of a varactor diode phase shifter.

A still further object is to digitally control a varactor diode phase shifter such that large and accurately controlled phase shifts can be obtained.

Other objects, advantages and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1a is a block diagram illustrating a phased array transmitter application. FIG. 1b is a block diagram illustrating a phased-array receiver application.

FIG. 2 is a block diagram of a prior art high dissipation phase shifter.

FIG. 3 is the basic block diagram of the phase shifter of the present invention.

FIG. 4 is a schematic diagram of a linearizing network that can be utilized in the present invention.

FIG. 5 is a schematic diagram of an embodiment of the digital phase shifter of the present invention.

FIG. 6 is a schematic of another embodiment of a linearizing network of the present invention.

FIG. 7 is a plot of $\Delta\phi$ vs. control voltage for different ratios of X_{co}/Z_o .

FIG. 8 is a plot of the phase response of the digital phase shifter shown in FIG. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1 (a and b) show, as an example, one type of phased-array application, a phased-array antenna. FIG. 1a shows a transmitting antenna system. The oscillator 10 provides the basic frequency. The power splitter 12 acts to provide the same impedance to the oscillator 10 at all frequencies of interest at each antenna line from 1 to N. Each antenna line from 1 to N is identical. The frequency from the oscillator 10 is phase-shifted in accordance with the control signal from line 69 on that particular phase shifter. It is then amplified in the amplifier 16 and radiated by the antenna 18.

In FIG. 1b, the receiving antenna acts in the conventional manner to pick up the signal at the antenna 26, amplify the signal in the amplifier 24, phase-shift it in the phase shifter 22, and sum the outputs of all the receiver lines 1 to N in the power summer 20.

FIG. 2 shows the prior art, high-dissipation, hybrid-type, reflective phase shifter previously used in phased arrays, as shown in FIG. 1. This phase shifter operates as follows: The radio frequency to be phase shifted is brought into the quadrature hybrid 30 by line 31. Quadrature hybrids are well known and an example of one is shown in FIG. 5 and labeled 30. This device acts to keep the impedance levels into and out of the device at some constant level. (It preserves the characteristic impedance over a broad bandwidth). The device operates by combining, in correct phase and amplitude, the reflections from the different reactance elements used to load it and steering or guiding these combined reflections to the output 32 of the device. The quadrature hybrid always has a 90° phase shift plus whatever phase shift the reactive load provides. Thus each quadrature hybrid can provide up to 180° in phase shift.

Depending on what phase shift is desired, either lines 42 and 46, or lines 44 and 48 are energized to bias either diodes 40 or diodes 39 respectively into conduction. If diodes 40 are biased on, then the two inductors 38 act as the termination to the line 32 and the radio-

frequency wave is phase-shifted by a phase which is a function of the magnitude of the reactance on the inductors 38. If diodes 39 are biased on, then the two capacitors 36 act as the termination to the input line 32. Thus the radio frequency is phase-shifted by a phase which is a function of the magnitude of the reactance on the capacitors 36.

The actual energization of the lines 42, 44, 46, and 48 is controlled by a 5-bit digital input. This digital input is decoded by switch driver 50 to determine the appropriate diodes to be biased into conduction. Then the outputs from switch driver 50 bias the various diodes in accordance with this decoded digital input.

FIG. 3 shows the basic block diagram of the phase shifter of the invention. The circuit consists of a quadrature hybrid 30 which again functions to preserve a characteristic impedance over a broad bandwidth. Thus the device again operates to combine the reflections from the different reactance elements used to load it in correct phase and amplitude. The quadrature hybrid always has a 90° phase shift in addition to whatever phase shift is provided by its reactive load. Thus each quadrature hybrid can provide up to 180° in phase shift.

Two voltage-variable reactance circuits 66 act as the reactive load on each quadrature hybrid. These reactance circuits 66 are varied by control voltages from line 69. The control voltages on line 69 are determined in a computer 70. In a radar application, for example, the variable reactance circuits 66 would be set so as to give the proper phase shift in the direction in which the phased-array antenna beam is desired to point at that particular time.

When the computer 70 has determined the proper setting for each reactance circuit in order to have a lobe in the desired direction, it provides a digital word containing this information to the input of a digital-to-analog converter 68. The D/A converter 68 changes the digital word to an analog control voltage, which is then applied on line 69 to the variable reactance networks 66.

Since each quadrature hybrid circuit with its respective loads can provide a possible 180° shift in phase, the combination of two quadrature hybrid circuits as shown in FIG. 3 can provide a possible 360° shift in phase.

In order to linearize the phase shift vs. voltage characteristic of a quadrature, hybrid phase shifter, the load circuits 66 for this quadrature hybrid must be specially designed. The equation for the differential phase shift through the quadrature hybrid phase shifter is:

$$(1) \quad \Delta\phi = 2 \tan^{-1} \frac{X(V)}{Z_o}$$

$X(V)$ = reactance of the reactive load circuit

Z_o = characteristic impedance of the hybrid

In order to linearize the phase shift vs. voltage characteristic over some voltage range V_o , two conditions are imposed on the reactive load circuit 66 at the voltage V_o .

$$(2) \quad X(V_o) = 0$$

$$(3) \quad \left. \frac{d^2X}{dV^2}(V) \right|_{V=V_o} = 0$$

These conditions force $\Delta\phi$ to vary about certain inflection points. The ratio $X(V_o)/Z_o$ can be selected to achieve the largest range of operation consistent with the realizable circuit elements, bandwidth, and losses.

There are many networks, both distributed and lumped, which yield to conditions (2) and (3). The network chosen for the device shown in FIG. 4 utilizes a varactor diode as the voltage-variable reactance to minimize drive power, and utilizes lumped circuit elements to minimize size.

The varactor diode 76 of FIG. 4 has its anode connected to ground through a capacitor 78. The capacitor 78 acts to provide an R.F. ground to the varactor 76. Two inductors 72 and 74, one connected between the cathode of the varactor 76 and ground, and the other connected between the cathode of varactor 76 and the input from the quadrature hybrid circuit 30, act to linearize the reactive impedance seen by the quadrature hybrid circuit. The values of the two inductances are picked in accordance with equations (2) and (3).

Application of conditions (2) and (3) to the network of FIG. 4 results in:

$$(4) \quad N_1 = \frac{1+A}{2A}$$

$$(5) \quad N_2 = \frac{1+A}{1-A}$$

where A is the varactor slope coefficient, and N_1 and N_2 are ratios of the inductor reactances to that of the varactor at the nominal control voltage V_o . V_o is defined here as being the sum of an applied voltage and the varactor contact potential. X_{co} is the varactor reactance.

The expression for differential phase is then

$$(6) \quad \tan \left(\frac{\Delta\phi}{2} \right) = \left(\frac{X_{co}}{Z_o} \right) \left(\frac{1+A}{2A} \right) \left[\left(\frac{V}{V_o} \right)^A - 1 \right]$$

$$\left[\left(\frac{1-A}{1+A} \right) \left(\frac{V}{V_o} \right)^A - 1 \right]$$

A plot of this plot function, FIG. 7, shows that best linearity is achieved when X_{co}/Z_o is about 1 to 1.5 for control voltages varying symmetrically about V_o .

Thus the reactive impedance seen by the quadrature hybrid circuit will vary in a linear manner when an analog control voltage is applied from line 69 to the anode of varactor 76.

The complete network, including a lumped quadrature hybrid, is shown in FIG. 5.

The measured performance of a single 180° section as in FIG. 5 is shown in FIG. 8. It is seen that the center 180° section departs from a straight line by no more than an amount which is equivalent to the accuracy of a 5-bit digital phase shifter.

The total dissipation of the device is that of the D-A converter, which is for example, about 60 milliwatts for a commercial 5-bit device with five microsecond rise time. This compares favorably with the 500 milliwatt

power dissipation typical of the diode switched phase shifters previously used in phased arrays.

The useful bandwidth of this device is about 10 percent when the simplest form of hybrid is used. This percentage can be increased by using a multi-section hybrid and revising the phase shift network.

If more linearity is required in the phase shifter, a number of identical linearizing network as shown in FIG. 4 can be connected in cascade. This cascade connection would consist of removing ground from inductor 74 and connecting it to another inductor and the cathode of another varactor diode as shown in FIG. 6. Thus almost any degree of linearity could be attained depending only on the number of cascaded linearizing networks used in each variable reactance network 66.

Obviously many modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed is:

1. A digital phase-shifter circuit capable of providing 360° phase shifts for use in phased array applications, comprising:

first and second quadrature hybrid means, each having four terminals;

first and second voltage-variable reactance means connected respectively to the second and third terminals of said four terminals of said first quadrature hybrid means;

third and fourth voltage-variable reactance means connected to the second and third terminals respectively of said second quadrature hybrid means, said voltage-variable reactance means acting as reactive loads on their respective quadrature hybrid means,

each of said quadrature hybrid means in combination with their respective voltage-variable-reactance means acting to shift the phase of a input signal by 90° plus the phase shift due to the reactive load on said quadrature hybrid means; and

digital-to-analog converter means acting to receive a digital input and convert said digital input into an analog control voltage, said analog control voltage being applied to each of said voltage-variable reactance means and acting to vary the reactances of said voltage-variable reactance means in accordance with said digital input,

a first terminal of said first quadrature hybrid means acting to receive an input signal, a fourth terminal of said first quadrature hybrid means connected to the first terminal of said second quadrature hybrid means and acting to apply the phase-shifted signal to said second quadrature hybrid means, a fourth terminal of said second quadrature hybrid means providing an output signal with the desired phase shift,

said voltage-variable reactance means comprising:

a varactor diode;

a capacitor connected between the anode of said varactor diode and ground potential and acting to provide an A.C. ground to said varactor diode;

a first inductor connected between the cathode of said varactor diode and ground;

a second inductor connected between the cathode of said varactor diode and an input from

said quadrature hybrid means, said inductors acting to linearize the reactive impedance seen by said quadrature hybrid means; and

means to apply an analog control voltage at the anode of said varactor diode in order to vary the reactance of said varactor diode.

2. A digital phase shifter circuit capable of providing 360° phase shifts for use in phased array applications, comprising:

first and second quadrature hybrid means, each having four terminals;

first and second voltage-variable reactance means connected respectively to the second and third terminals of said four terminals of said first quadrature hybrid means;

third and fourth voltage-variable reactance means connected to the second and third terminals respectively of said second quadrature hybrid means, said voltage-variable reactance means acting as reactive loads on their respective quadrature hybrid means,

each of said quadrature hybrid means in combination with their respective voltage variable reactance means acting to shift the phase of a input signal by 90° plus the phase shift due to the reactive load on said quadrature hybrid means; and

digital-to-analog converter means acting to receive a digital input and convert said digital input into an analog control voltage, said analog control voltage being applied to each of said voltage-variable reactance means and acting to vary the reactances of said voltage-variable reactance means in accordance with said digital input,

a first terminal of said first quadrature hybrid means acting to receive an input signal, a fourth terminal of said first quadrature hybrid means connected to the first terminal of said second quadrature hybrid means and acting to apply the phase-shifted signal to said second quadrature hybrid means, a fourth terminal of said second quadrature hybrid means providing an output signal with the desired phase shift,

said voltage-variable reactance means comprising linearizing circuits connected in cascade, each of said linearizing circuits comprising:

a varactor diode;

a capacitor connected between the anode of said varactor diode and ground potential and acting to provide an A.C. ground to said varactor diode;

a first inductor connected at one end to the cathode of said varactor diode, the other end of the first inductor of the first linearizing network of said cascade being connected to said quadrature hybrid means, the other end of the first inductor of the second and subsequent linearizing circuits being connected to the cathode of the varactor diode of the last preceding network;

a second inductor connected between the cathode of the varactor diode of the last linearizing circuit in said cascade and ground potential; and

means to apply an analog control voltage at the anode of each of said varactor diodes in order to vary the reactance of said varactor diodes.

3. A quadrature, hybrid phase shifter circuit having
a linear phase shift comprising, in combination:
a quadrature, hybrid phase shifter having four ports,
the first and fourth being for an input and an output
signal respectively;
a first varactor linearizing network comprising
a first lumped inductance, connected at one end to
the third port of said phase shifter,
a second lumped inductance connected at one end
to the other end of said first lumped inductance
and at the other end to ground, and
a varactor having its cathode connected to the con-
nection between said first and second induc-
tances;
a second varactor linearizing network comprising
a third lumped inductance, connected at one end
to the fourth port of said phase shifter;
a fourth lumped inductance connected at one end
to the other end of said third lumped inductance
and at the other end to ground;
a second varactor having its cathode connected to
the connection between said third and fourth in-
ductances; and
means connected to the cathodes of said varactors
for connecting a control voltage thereto.
4. A quadrature, hybrid phase shifter as in claim 3,

further comprising:
a first lumped capacitance connected between the
anode of said first varactor and ground potential;
a second lumped capacitance connected between the
anode of said second varactor and ground poten-
tial; and
wherein the equation for the differential phase shift
through said phase shifter is

$$\Delta\phi = 2 \tan^{-1} \frac{X(V)}{Z_o}$$

where
 $X(V)$ = reactance of the reactive linearizing networks
 Z_o = characteristic impedance of the hybrid phase
shifter
and the following conditions are imposed on the linear-
izing networks at a nominal control voltage V_o ,

$$\left. \frac{d^2 X(V)}{dV^2} \right|_{V=V_o} = 0$$

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