Title: A METHOD FOR FABRICATING A SEMICONDUCTOR PACKAGE, AND THE USE OF A NON-CONTACT UPWARD JETTING SYSTEM IN THE FABRICATION OF A SEMICONDUCTOR PACKAGE

Abstract: A method for fabricating a semiconductor package, comprising the steps of: a) providing a semiconductor chip having a bottom surface to which one or more solder contact points are attached; b) applying a curable epoxy composition upwards to at least one part of the bottom surface and/or to at least one of the solder contact points of the semiconductor chip by means of a non-contact jetting system; c) placing the coated semiconductor chip onto a circuit board or a carrier substrate; d) coupling the one or more solder contact points to the circuit board or the carrier substrate and curing the curable epoxy composition. The use of a non-contact upward jetting system in the fabrication of a semiconductor package is also disclosed.
A METHOD FOR FABRICATING A SEMICONDUCTOR PACKAGE, AND THE USE OF A NON-CONTACT UPWARD JETTING SYSTEM IN THE FABRICATION OF A SEMICONDUCTOR PACKAGE

Technical Field

The present invention relates to a novel deposition method to apply solder joint protection materials such as epoxy flux onto the bottom surface of a IC package, such as BGA (Ball Grid Array), CSP (Chip-Scale Package), WLP (Wafer-Level Package), PoP (Package-on-Package), and LGA (Land Grid Array), to overcome problems associated with current package dipping process, spraying material or coating material on PCB (Printed Circuit Board) substrate or the bottom package of PoP package.

Background Art

To protect the solder joints of the BGAs and LGAs from early drop-test failures on mobile electronic devices, various forms of solder joint protection materials have been used to protect solder joints from impact shock. Epoxy flux is one of the solder joint protection materials, and has the following advantages compared to conventional capillary underfill.

1. It can be cured with the solder reflow process to eliminate the dispense and cure steps of capillary underfills.

2. It can be cured with the solder reflow process to enable the implementation of the one-part EMI (electromagnetic interference) shield without the use of a low temperature solder and a second low temperature reflow process. One-piece EMI shield reduces the over-all height of the shield (compared to a 2-piece fence & cover EMI shield).

3. It has small fillet spread, and thus enables high density component layout of modern mobile devices.

However, the biggest downside of the epoxy flux is in its inability to protect the entire solder bumps owing to the limitations of current application methods listed below:

Method 1. Dipping method: That the IC package is dipped into a reservoir of epoxy flux wiped to a controlled height.

Method 2. Deposition of material on circuit board: That the material is either sprayed, printed, dispensed, etc., onto the circuit board, prior to attaching the component.

The first method, dipping method, has package pick up problems and solder smearing problems, while the second method -- spraying or coating on circuit board -- has solder smearing problem and moisture induced voids problem.

Based on previous negative result for LGA dipping process, the insert machine vender developed a tailor-made nozzle to maximize the pick up force on the dipped parts. It however could not completely solve the pick up failures.

Moreover, the engineer attempted to reduce the dipping depth for LGA, but the problem persisted.
The present invention uses an upside-down jetting process to shoot material to the back of the package. The process can produce an accurate coating with pro-grammed pattern onto each I/O pad of LGA or into the empty spaces between the balls of BGAs. The process will overcome the package pick up problem associated with dipping technology because of high tack force of the epoxy flux. It will also overcome solder smearing since the quantity and pattern can be programmed.

To avoid pick up failure, current dipping depth is limited to max.70% of the BGA ball height. As a result, only the bottom ball joint is protected, while the top is not. Because of this, drop test performance of epoxy flux has been reported to be inferior to capillary underfill that fills the entire ball height. The jetting from bottom method, if properly programmed, can achieve 100% coverage of the ball joints and give similar protection as capillary underfill.

Summary of Invention

It is therefore an object of the present invention to provide a novel method, by which the prior art problems as mentioned above can be overcome.

This object is achieved by a method for fabricating a semiconductor package, comprising the steps of:

a) providing a semiconductor chip having a bottom surface to which one or more solder contact points are attached;

b) applying a curable epoxy composition upwards to at least one part of the bottom surface and/or to at least one of the solder contact points of the semiconductor chip by means of a non-contact jetting system;

c) placing the coated semiconductor chip onto a circuit board or a carrier substrate;

d) coupling the one or more solder contact points to the circuit board or the carrier substrate and curing the curable epoxy composition.

According to another aspect of the invention, the use of a non-contact upward jetting system in the fabrication of a semiconductor package is provided.

Brief Description of Drawings

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become more apparent and the invention itself will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein:

Figure 1 shows a conventional dipping process for a BGA;

Figure 2 shows the schematic view of the non-contact upward jetting system according to the present invention;

Figure 3 and 4 show the operation and the structure of the upward jetting valve according to the present invention.
Detailed Description of Preferred Embodiments

The present invention relates to a method for fabricating a semiconductor package, comprising the steps of:

a) providing a semiconductor chip having a bottom surface to which one or more solder contact points are attached;

b) applying a curable epoxy composition upwards to at least one part of the bottom surface and/or to at least one of the solder contact points of the semiconductor chip by means of a non-contact jetting system;

c) placing the coated semiconductor chip onto a circuit board or a carrier substrate;

d) coupling the one or more solder contact points to the circuit board or the carrier substrate and curing the curable epoxy composition.

a) Providing a semiconductor chip

The semiconductor chip can be selected from the group consisting of BGA, CSP, WLP, PoP and LGA. One or more solder contact points are attached to the bottom surface of the semiconductor chip.

b) Upwards applying a curable epoxy composition by means of a non-contact upward jetting system

In an embodiment of the method according to the present invention, the non-contact upward jetting system may comprise a means to pressurize the epoxy composition; an operating valve system to control the dispense of the curable epoxy composition via outlet means 1 attached to the valve system, wherein the valve system is driven by a piezoelectric actuation means 3 especially to provide a possibility for a high frequency dispense of the curable epoxy composition (see Fig. 2).

The present invention makes use of the upward jetting capability of modern jetting valve such as but not limited to EFD picoDot to jet material to the desired spots on the back of the package with programmed pattern (see Figs. 3 and 4). This will solve the problems associated with the package dipping process or with PCB spraying or coating process.

The operating valve system of the non-contact upward jetting system may comprise a nozzle plate 10 with a nozzle as the outlet means 1; a sealing ball 9 for opening and closing the nozzle, being in contact with the piezoelectric actuation means 3; wherein nozzle plate 10 and sealing ball 9 are configured and arranged to each other in a way that the nozzle is closed by the sealing ball 9, preventing flow of the curable epoxy composition and when the sealing ball 9 is raised and/or distanced with respect to the nozzle plate 10 via the piezoelectric actuation means 3, the curable epoxy composition flows through the nozzle and is dispensed.

The nozzle plate 10 and/or the sealing ball 9 can be preferably made of a ceramic or alloy steel material.

The piezoelectric actuation means 3 may comprise two piezoelectric actuators.
The valve system may comprise an upper part with the piezoelectric actuation means 3 and a lower part with the nozzle plate 10 and the sealing ball 9, wherein a means for providing a thermal insulation 8 is provided between the upper part and the lower part, preferably a thermal insulation air gap.

The valve system may comprise preferably located in the lower part a fluid inlet 4 for the curable epoxy composition to connect the valve system with the means to pressurize the curable epoxy composition; a fluid path 5 to provide a connection between the fluid inlet 4 and the nozzle for the curable epoxy composition; a heating device 6 to provide a heating possibility for the valve system as well as a measuring device 7 for the measurement of the parameters of the curable epoxy composition and/or the valve system, preferably at least one temperature measuring sensor.

The valve system may comprise preferably located in the upper part an integrated counting means, preferably built as an integrated electronic counter 2, especially for the cycles and/or the power-on time.

In an embodiment of the method according to the present invention, the incident angle for applying the curable epoxy composition to the bottom surface of the semiconductor chip is less than 20°, preferably less than 10°, more preferably less than 5°.

In an embodiment of the method according to the present invention, the curable epoxy composition is applied by a pressure from about 10 psi to about 30 psi.

In an embodiment of the method according to the present invention, the distance between the non-contact jetting system and the bottom surface of the semiconductor chip is from about 0.8 mm to 5 mm.

In an embodiment of the method according to the present invention, the curable epoxy composition is applied at a temperature from about 40°C to about 75°C.

In an embodiment of the method according to the present invention, the curable epoxy composition has a viscosity from about 3000 mPa·s to about 30000 mPa·s at 25 °C.

In an embodiment of the method according to the present invention, the curable epoxy composition comprises at least one epoxy resin, at least one diluting agent, at least one curing agent, and at least one accelerator.

As the at least one epoxy resin, all the epoxy resins known in the prior art, for example U.S. Patent Application Publication No. 2011/0241228 A1, which is incorporated herein by reference in its entirety, can be used, so long as they are bifunctional or greater. Preferably used among these, from the viewpoint of viscosity reduction, low water absorption and high heat resistance, are bisphenol A-type epoxy resins, bisphenol F-type epoxy resins, naphthalene skeleton-containing polyfunctional epoxy resins, dicyclopentadiene skeleton-containing polyfunctional epoxy resins and triphenylmethane skeleton-containing polyfunctional epoxy resins: These epoxy resins may be either liquid or solid at 25 °C, but when solder is hot melted for connection, a solid epoxy resin used preferably has a melting point or softening point lower than the melting point of the solder. These epoxy resins may also be used alone or in combinations of two or more.
As the at least one curing agent, acid anhydrides commonly known in the prior art, for example U.S. Patent Application Publication No. 2011/0241228 A1, which is incorporated herein by reference in its entirety, can be used. Particularly preferred among these from the viewpoint of heat resistance and humidity resistance are methyltetrahydrophthalic anhydride, methylhexahydrophthalic anhydride, endomethylenenetetrahydrophthalic acid, methylendomethylenenetetrahydrophthalic acid, 3,4-dimethyl-6-(2-methyl-1-propenyl)-4-cyclohexene-1,2-dicarboxylic anhydride, 1-isopropyl-4-methyl-bicyclo[2.2.2]oct-5-ene-2,3-dicarboxylic anhydride, ethyleneglycol bistrimellitinate and glycerol trisanhydrotrimellitate. Any of these may be used alone or in mixtures of two or more.

The proportion of the at least one epoxy resin to the at least one curing agent is not particularly restricted, and can be determined by a person skilled in the art. The amount of the at least one curing agent is preferably 0.5 - 1.5 and more preferably 0.7 - 1.2, as the equivalent ratio to the epoxy resin (the ratio of the number of epoxy groups and the number of carboxyl groups generated from the acid anhydride = number of epoxy groups / number of carboxyl groups). If the equivalent ratio is smaller than 0.5, excessive carboxyl groups will remain, the water absorption may be increased and the moisture-proof reliability may be reduced; and if the equivalent ratio is larger than 1.5, the curing may not proceed sufficiently.

The at least one diluting agent used can be preferably selected from the group consisting of alcohols, phenols and carboxylic acids. An alcohol used here is preferably a compound with a two or more alcoholic hydroxyl groups in the molecule. A phenol used here is preferably a compound with at least two phenolic hydroxyl groups. Carboxylic acids used here include aliphatic carboxylic acids and aromatic carboxylic acids. These compounds may be used alone or in combinations of two or more.

The amount of the at least one diluting agent is preferably 0.1 - 15 parts by weight, more preferably 0.5 - 10 parts by weight and even more preferably 1 - 10 parts by weight, with respect to 100 parts by weight as the total of the at least one epoxy resin and the at least one curing agent. If the amount of the at least one diluting agent is less than 0.1 part by weight, a sufficient effect of removing the oxide layer on the solder surface may not be exhibited; and if it exceeds 15 parts by weight, the carboxyl groups and epoxy resin in the flux agent may react, potentially lowering the storage stability. These compounds may be used alone or in combinations of two or more.

As the at least one accelerator, quaternary phosphonium salts commonly known in the prior art, for example U.S. patent No. 7,074,738, which is incorporated herein by reference in its entirety, can be used.

The amount of the at least one accelerator is preferably 0.01 - 10 parts by weight and more preferably 0.1 - 5 parts by weight, with respect to 100 parts by weight as the total of the at least one epoxy resin and the at least one curing agent. If the amount of the at least one accelerator is less than 0.01 part by weight, the curability will be reduced, potentially lowering the connection reliability; and if it is greater than 10 parts by weight, the storage stability may be reduced.

The curable epoxy composition may optionally comprise a filler, such as organic filler or inorganic filler, to adjust the viscosity or control the properties of the cured product.
c) Placing the coated semiconductor chip onto a circuit board or a carrier substrate

In an embodiment of the method according to the present invention, the one or more solder contact points are encapsulated by the curable epoxy composition. In particular, the semiconductor chip coated in step b) can be placed onto a circuit board or a carrier substrate in a spaced apart relationship wherein a gap between the semiconductor chip and the circuit board or carrier substrate is formed by the one or more solder contact points which are encapsulated by the curable epoxy composition thereby forming a semiconductor package assembly.

In addition, the semiconductor chip and the circuit board or carrier substrate can be aligned and pressed together.

d) Coupling and curing

In an embodiment of the method according to the present invention, the semiconductor package assembly can be subjected to conditions sufficient to reflow the one or more solder contact points within the gap and to cure the curable epoxy composition wherein the one or more solder contact points meet the circuit board or the carrier substrate within the gap.

In particular, the semiconductor package assembly can be heated at a temperature at or above the melting point of the solder contact points, so that the semiconductor chip and the circuit board or carrier substrate are coupled together. The diluting agent in the curable epoxy composition of the invention may cause removal of the oxide layer on the surface of the solder contact points by reductive reaction, so that the solder contact points can reflow smoothly and a joint is formed by metal bonding.

Advantageous Effects of the Upward Jetting Process

1. On leadless packages such as LGA, current dipping process frequently leads to LGA pick up failures. The upward jetting process according to the present invention makes no direct contact with epoxy flux reservoir and can address pick up issues.

2. The upward jetting process according to the present invention can produce precise, programmable coating only on the I/O pads of LGA; versus coating the entire back of LGA with dipping process. This overcomes solder paste smearing issue on the PCB during placement, and prevents electrical short failures.

3. On BGA packages, dipping process can practically coat up to only 70% of the solder ball height. Higher coating levels result in pickup failures. Because of this, epoxy flux cannot reach and protect the top joint of the solder balls resulting in poorer drop test performance compared to capillary underfills. The upward jetting process according to the present invention can jet material only in between the balls to coat the entire ball giving comparable drop test performance as capillary underfills.
4. Enable pattern control to achieve accurate outline and volume for various parts, flexible and wide process window against traditional dipping process which normally has a unique dipping depth for one side of PCB.

5. In summary, the upward jetting process according to the present invention enables accurate deposition of epoxy flux onto the back of the package with precise volume control. This overcomes the difficulty of using capillary underfill to fill the tiny solder gap of LGA, avoids pickup failures of BGA and LGA with epoxy flux dripping process, allows 100% ball height coating of epoxy flux for BGA to achieve comparable drop-test performance of capillary underfill.

The present invention allows epoxy flux to become the main stream solder joint protection choice, which in turns eliminates the dispense and cure process of capillary underfill, solves the tight space dispensing and overflowing issues of capillary underfill, and enables incorporation of one-piece EMI shield process with normal solder reflow (without the need of additional low-temperature solder print and reflow process for 2-piece EMI shield).

As LGA and BGA are typical representatives of the semiconductor packages, the effects of the inventive upward jetting process for CSP, WLP and PoP can be anticipated based on the results as stated in Example 1 (LGA) and Example 2 (BGA) below.

The present invention further relates to the use of a non-contact upward jetting system in the fabrication of a semiconductor package.

The following non-limiting examples illustrate various features and characteristics of the present invention, which is not to be construed as limited thereto.

**Comparative Example 1: Dipping Process for LGA**

LGA package had only I/O pads on its bottom and no solder balls. It presented a big challenge to the current dipping application process in that when the package was dipped into the epoxy flux reservoir and the epoxy flux came into contact with the entire bottom of LGA, the tacky epoxy flux worked against the pick up force and caused pick up failures. With dipping process, the entire bottom of the LGA was fully covered by epoxy flux. When attaching the LGA onto the board, the epoxy flux dispersed the wet solder paste that was preprinted onto the connecting pads of the circuit board and caused electrical failures.

**Example 1: Upward Jetting Process for LGA**

In the upward jetting process according to the present invention, a jetting head (EFD PICO DOT Jet System model: 774 MV-100) was used, and the operating parameters were as follows:

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<th>Parameter</th>
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<td>Needle size:</td>
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<td>Dispense speed:</td>
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<td>Cycle time:</td>
<td>25 sec./unit</td>
</tr>
<tr>
<td>Glue viscosity:</td>
<td>8000 cps@2 rpm</td>
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Using the upward jetting process, the part had no direct contact with the epoxy flux reservoir, and the upward jetting process according to the present invention can address the pick up issue. The upward jetting process was programmed to produce an accurate pattern of epoxy flux coating that matched the I/O pads of LGA, and thereby, the solder dispersion issue were overcome.

Comparative Example 2: Dipping Process for BGA (Fig. 1)

BGA package had solder balls on its bottom and the epoxy flux was supposed to coat and protect the entire ball height plus the solder joints on the top and bottom of the ball to prevent early drop test failures. Conventional dipping process can only dip up to max 70% of the ball height according to field data. Higher dipping depth had too high the wetting force from the epoxy flux on the balls and resulted in pick up failures. Failing to coat the entire ball height left the top part of the ball and the top joints unprotected and resulted in early drop test failures.

Example 2: Upward Jetting Process for BGA

The same jetting head and operating parameters as Example 1 were used for BGA. The upward jetting process was programmed to deposit sufficient materials to fill the empty space between solder balls and provide 100% coverage. This allowed the protection of the top joints and gave comparable drop test performance as capillary underfill.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. The attached claims and their equivalents are intended to cover all the modifications, substitutions and changes as would fall within the scope and spirit of the invention.
CLAIMS

1. A method for fabricating a semiconductor package, comprising the steps of:
   a) providing a semiconductor chip having a bottom surface to which one or more solder contact points are attached;
   b) applying a curable epoxy composition upwards to at least one part of the bottom surface and/or to at least one of the solder contact points of the semiconductor chip by means of a non-contact jetting system;
   c) placing the coated semiconductor chip onto a circuit board or a carrier substrate;
   d) coupling the one or more solder contact points to the circuit board or the carrier substrate and curing the curable epoxy composition.

2. The method of claim 1, wherein the incident angle for applying the curable epoxy composition to the bottom surface of the semiconductor chip is less than 20°.

3. The method of claim 1 or 2, wherein the curable epoxy composition is applied by a pressure from about 10 psi to about 30 psi.

4. The method of any one of claims 1 to 3, wherein the distance between the non-contact jetting system and the bottom surface of the semiconductor chip is from about 0.8 mm to 5 mm.

5. The method of any one of claims 1 to 4, wherein the curable epoxy composition is applied at a temperature from about 40°C to about 75°C.

6. The method of any one of claims 1 to 5, wherein the curable epoxy composition comprises at least one epoxy resin, at least one diluting agent, at least one curing agent, and at least one accelerator.

7. The method of any one of claims 1 to 6, wherein the curable epoxy composition has a viscosity from about 3000 mPa·s to about 30000 mPa·s at 25°C.

8. The method of any one of claims 1 to 7, wherein in step c) the one or more solder contact points are encapsulated by the curable epoxy composition.

9. Use of a non-contact upward jetting system in the fabrication of a semiconductor package.
Fig. 1  Conventional dipping process for a BGA

Fig. 2  Schematic view of the non-contact upward jetting system according to the present invention
Fig. 3  The operation of the upward jetting valve according to the present invention

Fig. 4  The structure of the upward jetting valve according to the present invention
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/60(2006.01); H01L 23/498(2006.01); H05K 1/18(2006.01); H05K 3/34(2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L; H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPDOC, WPI, CNABS, CNKI; semiconductor, chip, packaging, epoxy, solder, jet+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

SPECIAL CATEGORIES OF CITED DOCUMENTS:

- Document defining the general state of the art which is not considered to be of particular relevance
- “F” earlier application or patent but published on or after the international filing date
- “G” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- “G” document referring to an oral disclosure, use, exhibition or other means
- “P” document published prior to the international filing date but later than the priority date claimed
- “P” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- “X” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- “E” document member of the same patent family

Date of the actual completion of the international search: 28 August 2014
Date of mailing of the international search report: 11 September 2014

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Form PCT/ISA/210 (second sheet) (July 2009)
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