



(51) International Patent Classification:
H03K 5/22 (2006.01)

(21) International Application Number:
PCT/CN2015/096170

(22) International Filing Date:
1 December 2015 (01.12.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/567,068 11 December 2014 (11.12.2014) US

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(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

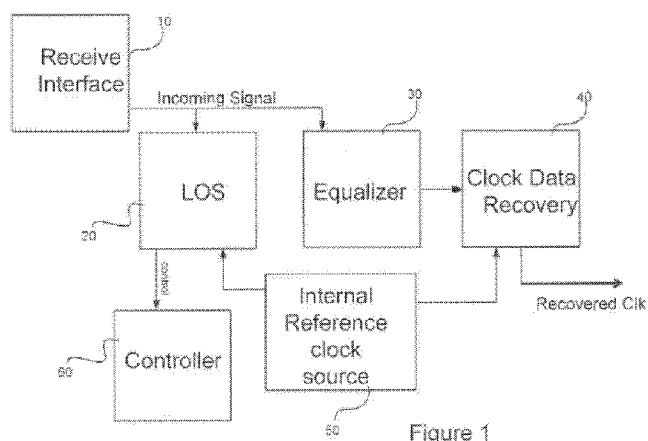
Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a
patent (Rule 4.17(ii))

Published:

— with international search report (Art. 21(3))

(54) Title: SYSTEM AND METHOD FOR DETECTING LOSS OF SIGNAL



(57) Abstract: Apparatus and methods are taught for quickly determining whether a Loss of Signal (LOS) condition has occurred for a receiver which includes an internal reference clock, a LOS circuit and a Clock and Data Recovery (CDR) circuit. The CDR circuit recovers the clock and data of an incoming signal. However, the LOS circuit can determine whether a received incoming signal includes an active signal, independent of said CDR circuit such that it samples said incoming signal utilizing said internal reference clock to determine a loss of signal prior to said CDR recovering the clock of said incoming signal. The LOS circuit includes an analog voltage threshold stage which samples the incoming signal, and produces at least one sample stream indicative of transitions in the incoming signal. The LOS circuit further includes a digital transition stage which counts transitions in order to discriminate between an active signal and noise.

SYSTEM AND METHOD FOR DETECTING LOSS OF SIGNAL

CROSS REFERENCE TO RELATED APPLICATION

[0001] This patent application claims priority to U.S. Patent Application No. 14/567,068, filed on the 11th of December, 2014 and entitled “SYSTEM AND METHOD FOR DETECTING LOSS OF SIGNAL”, which is hereby incorporated by reference herein as if reproduced in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to systems for detecting the loss of a signal.

BACKGROUND

[0003] Receivers designed to receive transmitted signals often need to determine whether a signal they are supposed to receive from a transmitter is present. This can be a challenge, as the receiver may still “receive” a “signal” which is not actually an active signal transmitted by a transmitter, but instead constitutes noise. Loss of Signal (LOS) circuits exist which attempt to detect a loss of signal.

[0004] However, there is a need for an improved LOS circuit which can quickly detect such a LOS condition.

SUMMARY

[0005] Aspects of the disclosure provide a system and method for quickly determining whether a Loss of Signal (LOS) condition has occurred.

[0006] A first aspect of the disclosure provides a receiver which includes a signal receive interface for receiving an incoming signal, an internal reference clock source, and an LOS circuit. The internal reference clock source produces an internal reference clock signal which is asynchronous to a clock rate of said incoming signal. For example, the internal reference clock signal need not be locked in frequency or phase to a clock signal which generated any active signal present in said incoming signal. The LOS circuit samples the incoming signal utilizing said internal reference clock signal to determine whether a loss of signal condition has occurred.

[0007] An embodiment includes a clock recovery circuit, for example a Clock and Data Recovery (CDR) circuit. The CDR circuit recovers the clock and data of an incoming signal. However, the LOS circuit can determine whether a received incoming signal includes an active signal, by sampling the incoming signal utilizing the internal reference clock to determine a loss of signal without requiring the clock recovery circuit recover the clock of said incoming signal. In an embodiment the LOS circuit includes two stages, an analog threshold stage and a digital transition stage. The analog threshold stage samples the incoming signal, and produces a sample stream indicative of transitions in the incoming signal. The digital transition stage counts transitions in the sample stream in order to discriminate between an active signal and a LOS condition. In an embodiment, the analog threshold stage is configured to sample the incoming signal to produce samples indicative of transitions which occur when the signal level of the incoming signal crosses both a first reference threshold, and a second reference threshold. To improve the robustness of such a system, an embodiment produces at least one additional sample stream, sampled with a phase shifted internal reference clock, to increase the likelihood that transitions which occur are detected by the system.

[0008] Another aspect of the disclosure provides for an LOS circuit which includes an analog threshold stage and a digital transition stage to process an incoming signal. The analog threshold stage utilizes a reference clock which is asynchronous to a clock rate of the incoming signal to sample the incoming signal, and produces at least one sample stream indicative of transitions in the incoming signal. The digital transition stage counts transitions in the at least one sample stream in order to discriminate between an active signal and a LOS condition. Such an LOS circuit can be used in a receiver which includes an internal reference clock and a Clock and Data Recovery circuit (CDR) for recovering the clock of an incoming signal. Such an LOS circuit is configured to operate independent of said CDR circuit and determines whether a loss of signal condition exists or not prior to said CDR recovering said clock of said incoming signal.

[0009] Another aspect of the disclosure provides for a method of detecting a Loss of Signal (LOS) condition carried out by a receiver. Such a method includes sampling an incoming signal, using an asynchronous internal reference clock internal to the receiver, for transitions which occur when the signal level of the incoming signal crosses both a first and second reference threshold. The method then counts the number of transitions within a period of time and compares the counted number of

transitions with a threshold to discriminate between an active signal and a LOS condition. The asynchronous internal reference clock is asynchronous to a clock which generated an active signal if one is present in the incoming signal. For example, the asynchronous clock need not be synchronized in phase or frequency to a clock which generated any such active signal.

5 [0010] The foregoing and other objects, features, aspects and advantages of the present disclosure will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings which description is by way of example only.

BRIEF DESCRIPTION OF DRAWINGS

10 [0011] Figure 1 is a block diagram illustrating a receiver according to an embodiment;

[0012] Figure 2 is a block diagram illustrating an embodiment of the Loss of Signal (LOS) circuit of Figure 1;

[0013] Figure 3a is a signal diagram which illustrates a first signal;

[0014] Figure 3b is a diagram illustrating the comparator output corresponding to Figure 3a;

15 [0015] Figure 4a illustrates another signal which has a low frequency data pattern;

[0016] Figure 4b is a diagram illustrating the comparator output corresponding to Figure 4a;

[0017] Figure 5a illustrates a noise signal;

[0018] Figure 5b is a diagram illustrating the comparator output corresponding to Figure 5a;

[0019] Figure 6 is a block diagram illustrating schematically another embodiment of an LOS circuit;

20 [0020] Figure 7 conceptually illustrates how transitions are sampled and counted, utilizing idealized signal outputs for a single path, according to an embodiment;

[0021] Figure 8 is a flow chart illustrating a method of detecting a LOS condition carried out by a receiver, according to an embodiment.

DESCRIPTION OF EMBODIMENTS

[0022] Embodiments provide Loss of Signal (LOS) detection systems and methods which can distinguish a valid (i.e., an active) signal from noise (which for simplicity will be used in this specification to include an invalid signal, noise, or a non-existing signal). Embodiments will be
30 discussed with respect to implementations particularly suited for high-speed backplane

environments, in which the received signal amplitude can be relatively small, while crosstalk noise can be relatively high. However, the principles discussed herein are not limited to backplane environments, and can be applicable generally to receivers which require LOS.

[0023] Figure 1 is a block diagram illustrating a receiver according to an embodiment. The receiver includes a receive interface 10 which forwards an incoming signal to a LOS circuit 20 and an Equalizer 30. The receiver also includes a clock recovery circuit, for example Clock and Data Recovery (CDR) circuit 40, and an internal reference clock source 50. The Equalizer 30, for example a continuous-time linear equalizer, operates in a conventional manner to reverse distortion (e.g., inter-symbol interference) incurred during transmission through the channel. It should be appreciated that not all receivers will require an equalizer, depending on the transmission medium involved. For embodiments which do not require an equalizer, the incoming signal may be forwarded to both the LOS 20 and the CDR 40. In this embodiment, the LOS circuit 20 processes the incoming signal in parallel to the Equalizer 30, and before the CDR 40. In other words, the LOS Circuit 20 can determine a LOS condition without first requiring the receiver to either equalize the signal or recover the incoming signal clock. This allows for faster LOS detection than prior art systems which perform LOS as part of, or after, CDR.

[0024] The LOS circuit 20 determines if the received incoming signal 10 includes an active signal (as opposed to simply noise). LOS circuit 20 is configured to operate independently of said CDR circuit 40 such that it samples said incoming signal utilizing an internal reference clock signal received from the internal reference clock source 50 to determine a loss of signal based on an incoming signal that has not been processed by the CDR circuit 40. As a result, in some embodiments the LOS determination may be made prior to said CDR 40 recovering said clock of said incoming signal. While only a single incoming signal is shown, it should be appreciated that embodiments, like the further embodiments discussed below, can operate for receivers which are configured to receive differential incoming signals with positive and negative components. Internal reference clock signal refers to a clock signal derived from an internal clock component, without needing to be locked in frequency or phase to the clock of the incoming signal. The clock component may produce an initial clock signal which is processed (e.g., upconverted or divided) to produce the internal reference clock signal of a desired rate.

[0025] Depending on the application, the receiver may also include one or more termination blocks, not shown, to match the receiver impedance to the transmission line(s), in order to minimize reflections back to the transmitter. As should be appreciated, for differential signaling, both the positive and negative signal components should be terminated.

5 [0026] The LOS output is sent to receiver controller 60, which can send appropriate alarms, and take appropriate remedial action when a LOS condition is determined. One advantage of such an embodiment is that it can detect a LOS condition faster than prior art systems which detect a LOS after CDR, and can therefore respond earlier than such prior art systems.

[0027] Figure 2 is a block diagram illustrating an embodiment of the LOS circuit of Figure 1. The
10 embodiment of Figure 2 is discussed with respect to an example of LOS detection for a receiver configured to receive a differential signal. However, the system is not limited to differential signaling. The LOS circuit in this example includes two stages. The first stage is an analog threshold voltage stage 210 that samples said incoming signal, and produces a sample stream indicative of transitions in the incoming signal. The second stage is a digital transition stage 250
15 that counts transitions in the sample stream in order to discriminate between an active signal and noise.

[0028] The analog stage 210 includes a level comparator with hysteresis 220, which compares the incoming signal against a first threshold and second threshold (which in some embodiments may be the positive and negative values of a single threshold). In this embodiment, due to the
20 differential signaling, comparator 220 receives the differential plus (p) and minus (m) inputs Rx_{inp} and Rx_{inm} .

[0029] In an embodiment, the comparator 220 produces an output indicative of when the voltage of said incoming signal crosses the reference voltages. As the comparator 220 has both a positive and negative reference voltage (V_{lev}), a transition occurs as the change in the voltage of the signal
25 crosses both the positive and negative reference voltages. We will discuss transitions in more detail below. The output of the comparator will stay constant (either 1 or 0, depending on its previous state) until a voltage transition occurs, at which point it will switch values, and remain at that new value until the next transition occurs. The output of the comparator is sampled by a Data Flip-Flop (DFF) 230, to produce a sample stream indicative of the transitions that occur in the
30 incoming signal. The DFF 230 samples the comparator output based on an internal reference

clock (Clk) 235, which is asynchronous to the clock of the incoming signal. The Clk 235 is said to be asynchronous, as it does not need to be synchronized (either in frequency or phase) to the clock of the incoming signal.

[0030] The output from DFF 230 is a digital sample stream, which is then processed by the digital transition stage 250. The digital transition stage 250 includes a transition counter (with reset) 240, which counts transitions in the sample stream output received from the DFF 230. The counter 240 counts the number of times the sample stream changes (from a 1 to 0 or from 0 to 1) within a period of time (between resets). The transition count comparator 260 compares the counted number of transitions with a threshold to discriminate between an active signal and noise. If the number of transitions between resets exceeds the threshold, then an active signal is presumed. Otherwise, a LOS is detected, resulting in a LOSDet alarm being output.

[0031] Figures 3 through 5 are signal diagrams which illustrate three different signals, and are used to discuss the comparator output for each signal. Figure 3a illustrates a signal 300, and Figure 3b illustrates the corresponding comparator output. The comparator 220 has Positive voltage threshold 320 of +100mV and a negative voltage threshold 330 of -100mV. The comparator output will be zero for signals that start below the negative threshold 330, until a transition occurs and the signal voltage crosses the positive threshold. Accordingly, at 305 the comparator output remains as zero. It is illustrative to note that at position 307, the signal voltage has crossed both the negative threshold 330 and the 0mV level to have a positive signal voltage. However the comparator output remains at zero due to the hysteresis resulting from the positive and negative voltage thresholds. As the signal value drops from 307, the comparator output remains zero at 308. Position 309 is noteworthy as it shows a transition about to take place. At this point, the signal, which was below the negative threshold, is increasing and about to cross the positive threshold. The transition occurs at 310, as the signal voltage has now crossed both negative threshold 330 and positive threshold 320. Accordingly, the comparator output switches to 1 after this transition, and remains at 1 for the remainder of this Figure. Thus, the comparator output is 1 when the signal is above the positive threshold at 312. The comparator output remains at 1 at position 315 (despite the signal value dropping to a negative value) and 318 (despite the signal value again crossing the 0mV level) due to hysteresis, as the signal has not had another transition (i.e., the signal has not

dropped below the negative threshold 330, having previously exceeded the positive threshold 320).

[0032] Figure 4a illustrates another signal 350 which has a low frequency data pattern with transitions at positions 352, 354, 356 and 358, and Figure 4b illustrates the corresponding

5 comparator output. The comparator output will be 1 at 351 and remain as 1 until transition 352, at which point the comparator output will switch to 0 once the signal drops below the negative threshold (having already crossed the positive threshold). The comparator output will then remain at 0 until transition 354, at which point the comparator output will switch to 1, and remain at 1 until transition 356, at which point the comparator output will switch to 0. The comparator output will
10 then remain at 0 until transition 358, at which point the comparator output will switch to 1. Figure 5a illustrates a noise signal, and the corresponding comparator output is illustrated in Figure 5b. Although the noise crosses the positive threshold at positions 380 and 382, the signal never crosses both the positive and negative thresholds. Accordingly the comparator output will remain at 1 throughout as no transitions occur.

15 [0033] Figure 6 is a block diagram illustrating another embodiment of a LOS circuit. This embodiment includes a second path for sampling the comparator output, in order to increase the robustness of the apparatus. In Figure 6, the lower path shows a second DFF 610 which samples the output from comparator 220 using a clock (Clk_{ϕ}) shifted in phase by phase shifter 605. Phase shifter 605 can be a simple delay line, a variable delay line, an inverter, or any other phase shifting
20 circuitry known in the art. In some embodiments a 90 or 180 degree phase shift may be utilized representing a quarter or half clock cycle respectively. When a half clock cycle is desired, an inverter may be used to implement the 180 degree phase shift. However it should be appreciated that other phase shifts can be used.

[0034] The second DFF 610 produces a second sampling stream which adds robustness to the
25 system, by reducing the probability that the system will fail to detect a valid transition, as the sampling at either phase can potentially detect a transition that sampling at the other phase may miss. It should also be understood that more than two paths may be provided, with each path using a clock shifted by a different phase.

[0035] For example, two transitions separated by less than one clock cycle may not be detected
30 by a single DFF due to the sampling frequency. The second path introduces a second sampling of

the comparator output, such that if one path co-incidentally samples a symbol at the eye edge, then the other path will likely sample the symbol other than at the eye edge, to increase the likelihood of transition detection. In addition, as the DFF only detects transitions which are sampled at the rising edge of the clock signal, transitions which occur between clock cycles may not be detected. Thus, the second path, which samples with a phase shifted reference clock, samples the comparator output at different points, potentially detecting transitions which may be missed by use of only a single path. This will be discussed below, with reference to Figure 7.

[0036] Each path in Figure 6 includes a Demux element 620, 640. These elements are optional, depending on the speed of the signals being received, and the processing power of the digital components. For fast signals, the Demux element 620 acts as a serial-to-parallel converter, converting the sample stream received from DFF 230 into a plurality (N) of sample streams, using a clock rate equal to the Clk divided by N (clock divider not shown). This allows for a transition counter (with reset) 640 which can handle N parallel sample streams, which may be cheaper than a single counter which can operate at a sufficiently high speed to process the entire output from DFF 230 in a serial stream. Alternatively, N transition counters could each be used for one of the sample streams. The LOS circuit having a single path could likewise utilize such a Demux to accommodate faster input signal bandwidths, according to another embodiment. If this is the case, the transition counter, for example the transition counter 240 in Figure 2, should count transitions in the parallel streams.

[0037] Transition counter (with reset) 640 counts the transitions which occur in the sample stream output from DFF 230, between resets. Transition counter (with reset) 645 counts the transitions which occur in the sample stream output from DFF 610, between resets. The higher transition count 650 is passed to a transition count comparator 660, which compares the number of transitions (per period between resets) with a threshold set to discriminate between an active signal and noise.

[0038] Figure 7 conceptually illustrates how transitions are sampled and counted, utilizing idealized signal outputs for a single path. It should be noted that Figure 7 is conceptual in nature, and should not be taken to represent actual signals. In Figure 7, a conceptual output from the comparator (with hysteresis) is shown 710. The internal reference clock signal, used to sample the comparator output, is shown at 720. A sample stream after sampling by the DFF is shown at 730.

The pulses shown at 740 indicate where transitions are detected, and these detected transitions are counted by the transition counter 240. It should be noted that these pulses 740 do not represent any real signal, and are not actual outputs of either the DFF or the transition counter – but are merely included to help illustrate what is counted by the transition counter 240. Transition counter 240 counts changes (from 0 to 1 or from 1 to 0) in the sample stream output from DFF. Each such change increments the counter until a reset occurs, at which point the counter value is set to zero and starts incrementing again, as illustrated at 750 and 760.

[0039] Each change in the comparator output represents a transition (meaning the signal has crossed both the positive and negative voltage thresholds of the comparator). In Figure 7 the dashed vertical lines (except for lines 722, 724 and 726) represent the rising edges of the clock signal. The dashed vertical lines 705 show one rising edge of the clock signal, and the corresponding sampling of the comparator output. Each such dashed vertical line represents a point where the DFF samples the comparator output. The output of the DFF changes if the comparator output at consecutive samples has changed, and remains the same if the comparator output at consecutive samples remains the same.

[0040] It should be appreciated that Figure 7 conceptually illustrates a signal with rapid transitions (as can be seen by the many changes in the comparator output), in order to illustrate that not every one of these transitions need be counted. It is not necessary for the LOS to validly detect and count every transition, especially for a rapidly changing signal, as a rapidly changing comparator output would tend to indicate there is an active signal. The threshold of the transition count comparator 260 or 660 is configured such that the number of transitions actually detected and counted between resets is a good test of whether an active signal exists.

[0041] As stated, it is not necessary for the LOS circuit to detect and count every transition, especially for an active signal with many transitions, in order for the LOS circuit to validly determine that an active signal is present. However, the second path in Figure 6 can help the robustness of the LOS circuit to detect and count transitions which do occur. This can be beneficial for detecting when an LOS condition does exist. With reference to Figure 7, region 735 helps illustrate how the second path can help the robustness of the system. In this region, no transitions are detected by the DFF 230, despite several transitions occurring in the comparator output. This is due to the rising edge of the clock failing to detect a transition as each consecutive

sampling is the same in this region (all zeroes). However, a second path sampling at the rising edge of the phase shifted clock represented by dashed vertical lines 722, 724 and 726, corresponding to comparator peak (1 value) at 712, trough (0 value) at 714 and peak (1 value) at 716, would detect (and count) a transition in this region.

[0042] Embodiments of a receiver incorporating a LOS circuit as described herein can include a controller 60 for taking appropriate action once a LOS condition has been reported. For example, such a controller 60 can send an alarm to the transmitter, or initiate a protection switch or restoration, depending on the situation and network. Advantageously, such a receiver can take such action faster than prior art systems, as the receiver does not need to wait for the CDR block to fail to recover the clock of the signal to determine the LOS condition exists. Further, the LOS circuit is fast, and relatively cheap in terms of components and power consumption. Indeed, as discussed above, embodiments can be configured that need not even detect every transition, which may offer a simpler architecture than receivers which need to decode every bit before a LOS condition can be detected. Further, embodiments can use relatively low power in order to discriminate between an active signal and a LOS condition. Such embodiments may be useful for systems which use non-continuous transmissions, or where power or heat dissipation is an issue. The LOS can quickly determine the presence of a signal, and activate the relatively higher power CDR portion of the receiver only when needed. Another advantage of some embodiments is that the LOS circuit can discriminate between a weak signal (with a relatively large amount of noise) and a LOS, which has been a problem for some prior art LOS circuits, including those which rely on a peak detector or power detector (also called a root-mean-square power detector).

[0043] Figure 8 illustrates a method of detecting a LOS condition carried out by a receiver, according to an embodiment. An incoming signal is sampled for transitions which occur when the signal level of the signal crosses both a first reference threshold and a second reference threshold 810. This sampling is done using an asynchronous internal reference clock (internal to the receiver), which need not be synchronized in phase or frequency to a clock which generated said signal (if present). The number of transitions within a period of time are counted 820 and compared with a threshold 830. If the counted number exceeds the threshold, then an active signal is deemed present. Otherwise, a LOS condition is declared 840. In some embodiments, the second reference threshold is the negative value of the first reference threshold. In some embodiments the

signal level is measured by measuring the voltage of the signal, and comparing the measured voltage against first and second reference voltage thresholds.

[0044] The methods and devices described herein are generally applicable to receivers which attempt to differentiate signals from noise, and in particular where noise typically is bounded by upper and lower voltage thresholds, but for which active signals cross said thresholds.

Embodiments may be of particular value for receivers embodied in a card in networking or computer equipment which includes a plurality of cards connected by a backplane, in which the backplane is a source of crosstalk noise, in which case the reference voltages can be selected to differentiate between an active signal and said crosstalk noise. Embodiments may also be implemented in receivers for optical, cable, and other transmission systems. The LOS circuit can be embodied in FPGA, ASIC, CMOS, DSP or other chip, which can be used with a receiver or incorporated into a receiver, which may itself incorporate one or more processors and other chips.

[0045] Although the present invention has been described with reference to specific features and embodiments thereof, it is evident that various modifications and combinations can be made

thereto without departing from the invention. The specification and drawings are, accordingly, to be regarded simply as an illustration of the invention as defined by the appended claims, and are contemplated to cover any and all modifications, variations, combinations or equivalents that fall within the scope of the present invention.

CLAIMS

1. A receiver comprising:

a signal receive interface for receiving an incoming signal;

an internal reference clock source for producing an internal reference clock signal,

said internal reference clock signal being asynchronous to a clock rate of said incoming signal;
and

a loss of signal (LOS) circuit which samples said incoming signal utilizing said internal reference clock signal to determine whether a loss of signal condition has occurred.

2. The receiver as claimed in claim 1 wherein said LOS circuit comprises:

an analog threshold stage which samples said incoming signal, and produces at least one sample stream indicative of transitions in said incoming signal; and

a digital transition stage which counts transitions in said at least one sample stream in order to discriminate between an active signal and a loss of signal condition.

3. The receiver as claimed in claim 2 wherein a transition occurs when a signal value of said incoming signal crosses a first reference threshold and a second reference threshold.

4. The receiver as claimed in claim 3 wherein said analog stage produces first and second sample streams, wherein the second sample stream is sampled using a phase shifted version of the internal reference clock signal; and wherein said digital transition stage includes a counter for counting transitions in each of said first and second sample streams.

5. The receiver as claimed in claim 4 wherein said digital transition stage further comprises a comparator for comparing the counted transitions in said first and second sample streams.

6. The receiver as claimed in claim 5 wherein said analog threshold stage comprises:

a level comparator for comparing said input signal with said first and second reference thresholds;

a first circuitry coupled to the output of said comparator and said internal reference clock signal for sampling the output from the comparator; and

a second circuitry coupled to the output of said comparator and the phase shifted version of the internal reference clock signal for sampling the output from said comparator.

5

7. The receiver as claimed in claim 6 wherein said digital transition stage comprises:

a first transition counter element which counts transitions in samples received from said first circuitry;

10 a second transition counter element which counts transitions in samples received from said second circuitry; and

a transition count comparator which compares counted transitions within a period of time with a threshold and provides an output signal indicative of whether said incoming signal includes an active signal.

- 15 8. The receiver as claimed in claim 7 wherein said level comparator is a level comparator with hysteresis and wherein said first circuitry comprises a first data flip flop and wherein said second circuitry comprises a second data flip flop.

9. The receiver as claimed in claim 7 wherein said analog threshold stage further comprises:

20 a first demux element for converting the serial sample stream from the first circuitry into a first plurality of parallel sample streams; and

a second demux element for converting the serial sample stream from the second circuitry into a second plurality of parallel sample streams;

and wherein,

25 said first transition counter element counts transitions in said first plurality of parallel sample streams; and

said second transition counter element counts transitions in said second plurality of parallel sample streams.

10. The receiver as claimed in claim 9 embodied in a card in networking equipment which includes a plurality of cards connected by a backplane, and said backplane is a source of crosstalk noise, and wherein said first and second reference thresholds are selected to differentiate between an active signal and said crosstalk noise.

5

11. The receiver as claimed in claim 3 wherein said receiver further comprises a clock recovery circuit for recovering the clock of said incoming signal, and said LOS circuit operates independently of said clock recovery circuit.

10 12. A loss of signal (LOS) circuit comprising:

an analog threshold stage which samples an incoming signal, and produces at least one sample stream indicative of transitions in said incoming signal; and

a digital transition stage which counts transitions in said at least one sample stream in order to discriminate between an active signal and a LOS condition;

15 wherein said analog threshold stage samples said incoming signal utilizing a reference clock which is asynchronous to a clock rate of said incoming signal.

13. The LOS circuit as claimed in claim 12 wherein said analog threshold stage is configured to sample said incoming signal to produce samples indicative of transitions which occur when the signal level of said incoming signal crosses both a first reference threshold, and a second reference threshold.

20

14. The LOS circuit as claimed in claim 13 wherein said analog stage produces at least one additional sample stream which is sampled by a phase shifted reference clock in order to increase likelihood that at least one sample detects a transition; and wherein said digital transition stage includes a counter for counting transitions in each of said sample streams, and a comparator for comparing the counted transitions in said sample streams in order to discriminate between an active signal and noise.

25

30 15. The LOS circuit as claimed in claim 14 wherein said analog threshold stage comprises:

a level comparator for comparing said input signal with said first and second reference thresholds;

a first circuitry coupled to the output of said comparator and said internal reference clock signal for sampling the output from the comparator with said internal reference clock;
5 and

a second circuitry which is also coupled to the output of said comparator and said internal reference clock signal via a phase shifter for sampling the output from said comparator with a phase shifted reference clock signal.

10 16. The LOS circuit as claimed in claim 15 wherein said digital transition stage comprises:

a first transition counter element which counts transitions in samples received from said first circuitry;

a second transition counter element which counts transitions in samples received from said second circuitry; and

15 a transition count comparator which compares counted transitions within a period of time with a threshold and provides an output signal indicative of whether said incoming signal includes an active signal.

17. The LOS circuit as claimed in claim 16 wherein said analog threshold stage further comprises:

20 a first demux element for converting the serial sample stream from the circuitry into a first plurality of parallel sample streams; and

a second demux element for converting the serial sample stream from the second circuitry into a second plurality of parallel sample streams;

and wherein,

25 said first transition counter element counts transitions in said first plurality of parallel sample streams; and

said second transition counter element counts transitions in said second plurality of parallel sample streams.

18. The LOS circuit as claimed in claim 17 wherein said level comparator is a level comparator with hysteresis and wherein said first circuitry comprises a first data flip flop and wherein said second circuitry comprises a second data flip flop.

5 19. A method of detecting a Loss of Signal (LOS) condition carried out by a receiver comprising:
sampling an incoming signal, using an asynchronous internal reference clock internal
to the receiver, for transitions which occur when the signal level of the incoming signal crosses
both a first reference threshold and a second reference threshold;
counting the number of transitions within a period of time; and
10 comparing said counted number of transitions with a threshold to discriminate
between an active signal and a LOS condition;
wherein said asynchronous internal reference clock is asynchronous to a clock which
generated an active signal if present.

15 20. The method as claimed in claim 19 wherein said sampling produces a pair of sample streams,
one of which is sampled by a phase shifted internal reference clock in order to increase
likelihood that at least one of each pair of samples detects a transition; and wherein said
counting counts transitions in each of said pair of sample streams.

20 21. The method as claimed in claim 20 wherein said sampling comprises sampling the output of a
level comparator with hysteresis which compares said incoming signal with said reference
voltage thresholds.

25 22. The method as claimed in claim 21 wherein said sampling is carried out by a first Flip Flop
coupled to the output of said comparator and said internal reference clock signal for sampling
the output from the comparator with said internal reference clock and by a second Flip Flop
coupled to the output of said comparator and said phase shifted internal reference clock signal
for sampling the output from the comparator with said phase shifted internal reference clock.

23. The method as claimed in claim 21 wherein said counting comprises counting the transitions in each of said pair of sample streams; and wherein said comparing comprises first comparing the count of each sample stream to produce a total count equal to the higher of number of transitions within said pair of sample streams, and then comparing said total count with said threshold to discriminate between an active signal and a LOS condition.

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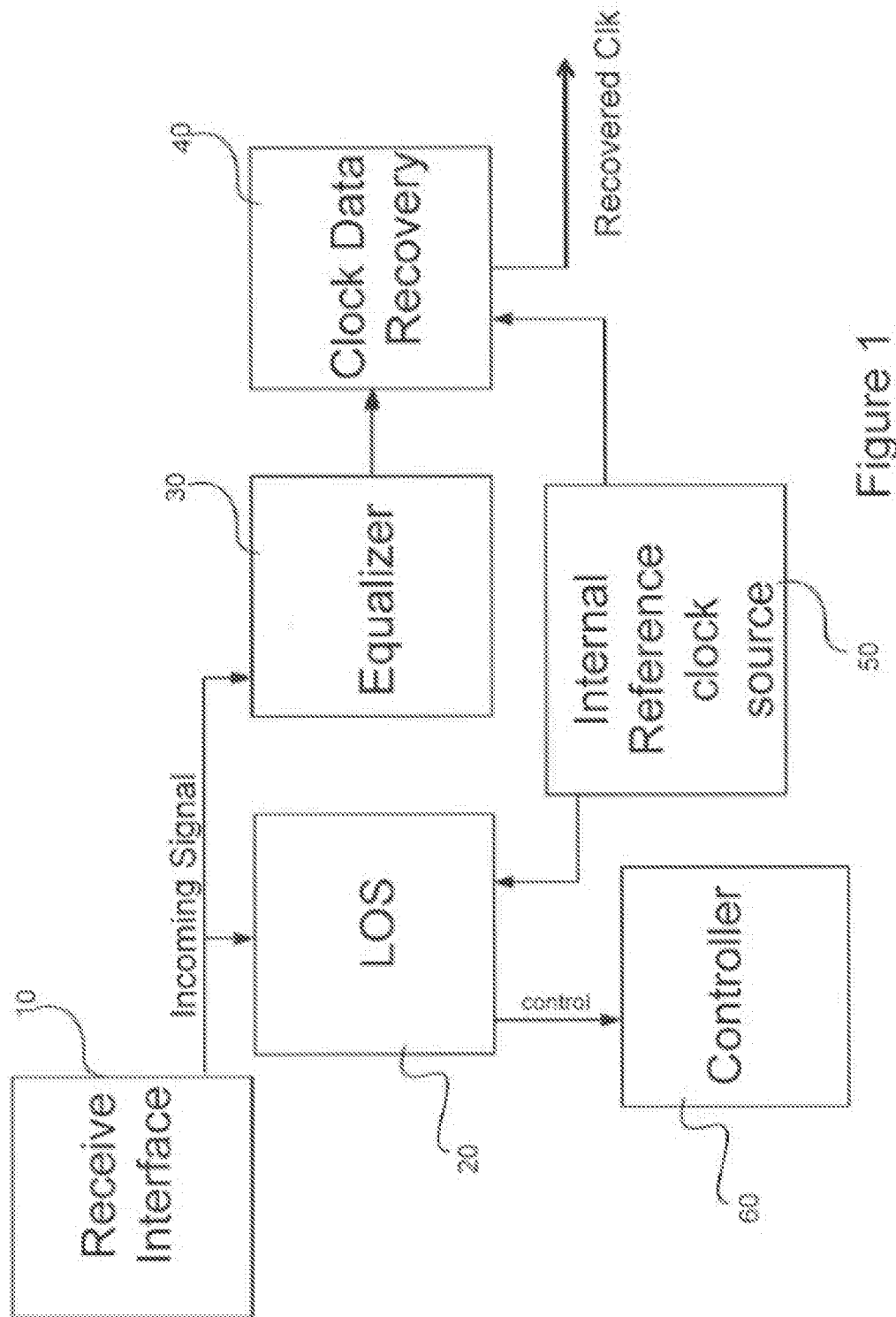


Figure 1

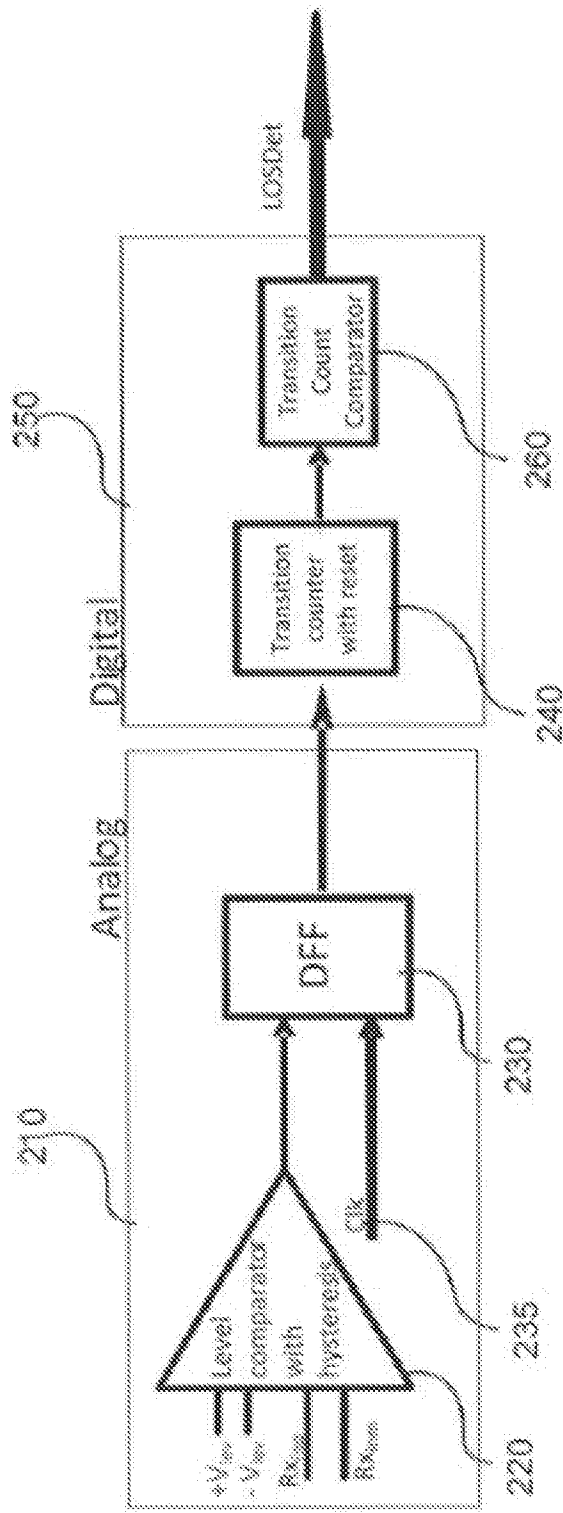


Figure 2

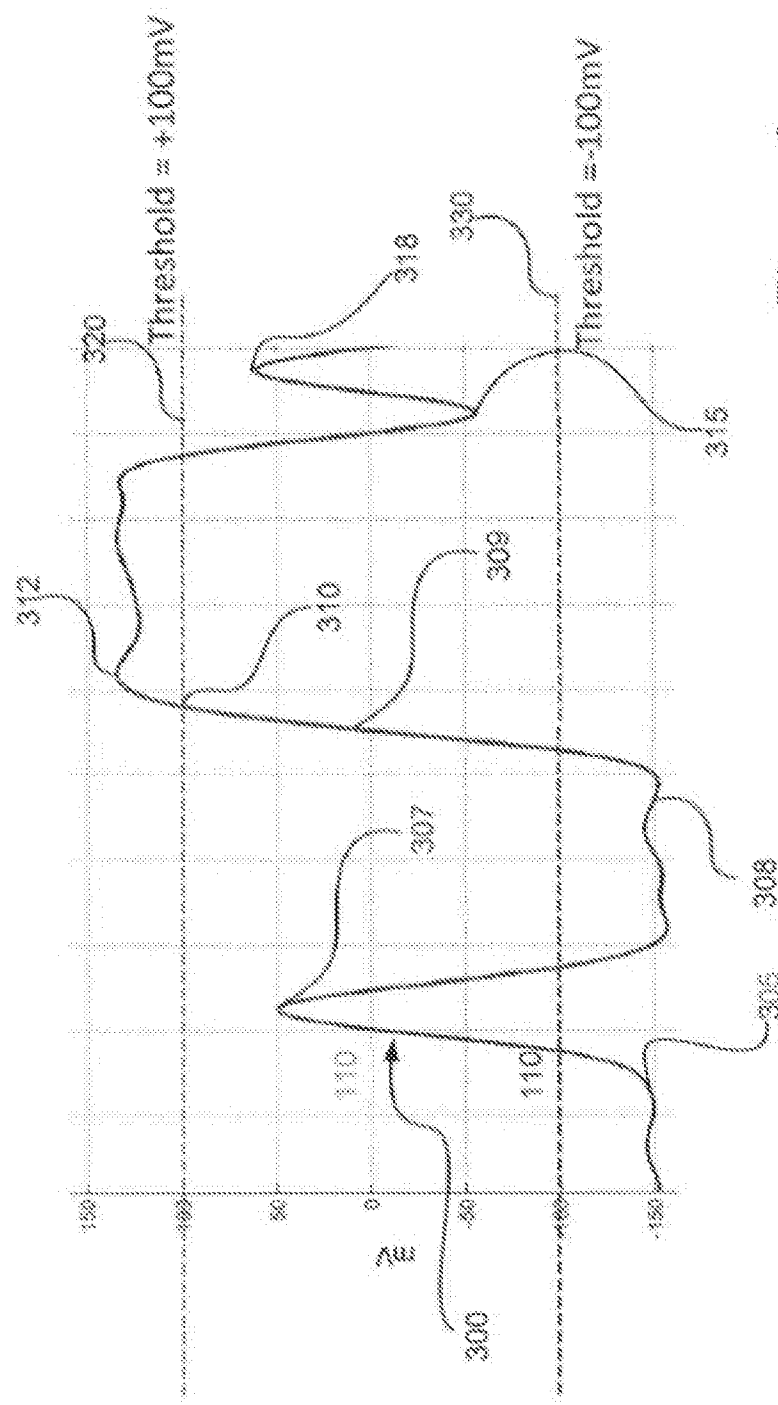


Figure 3a

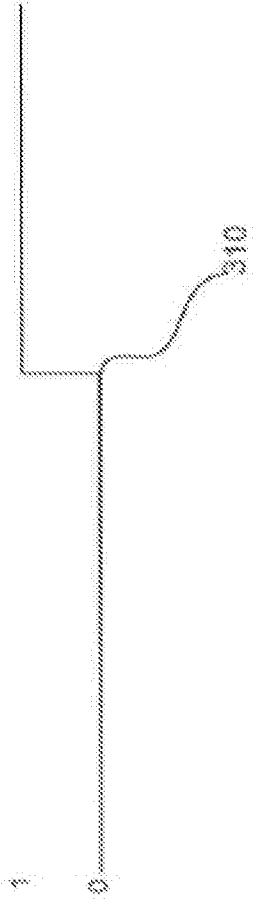


Figure 3b

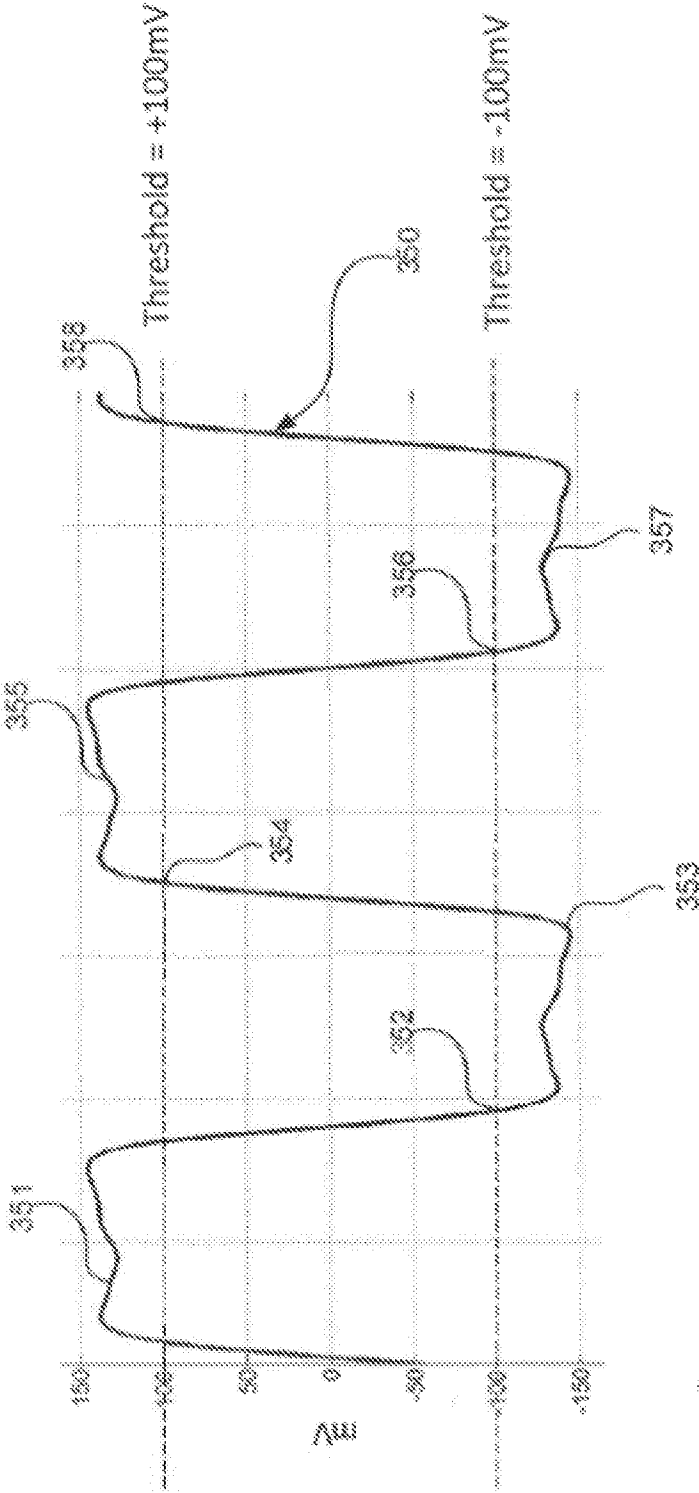


Figure 4a

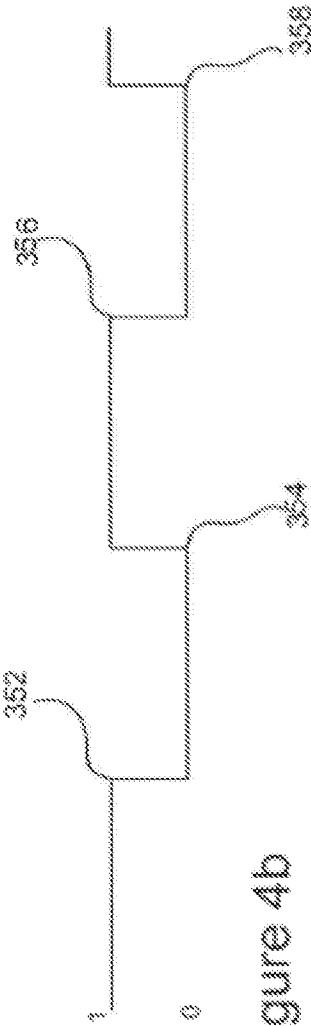


Figure 4b

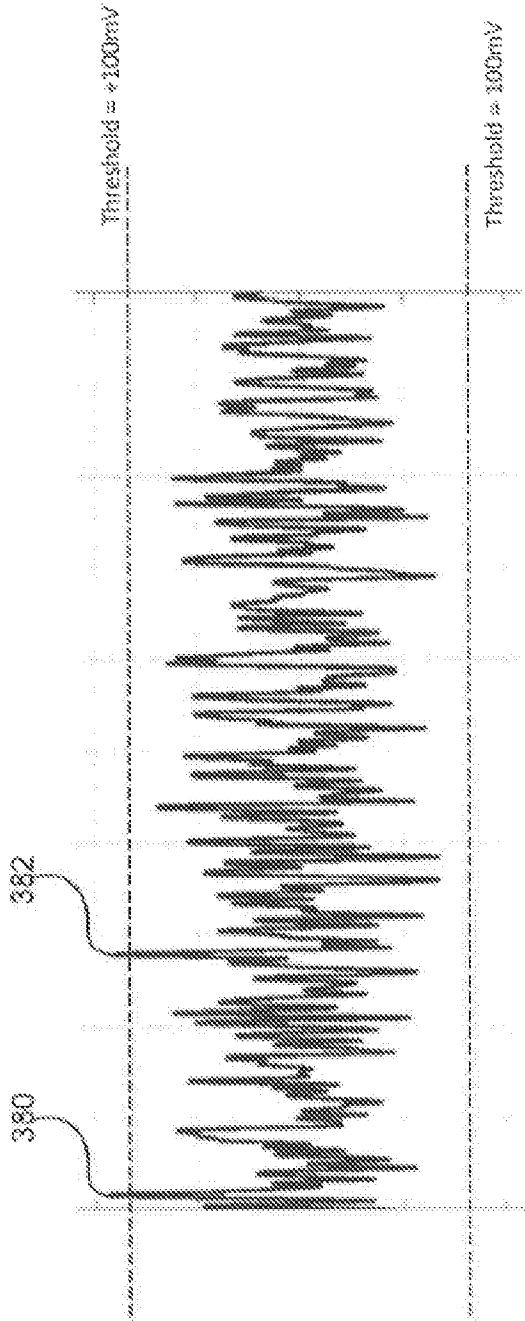


Figure 5a

1 _____

Figure 5b

0

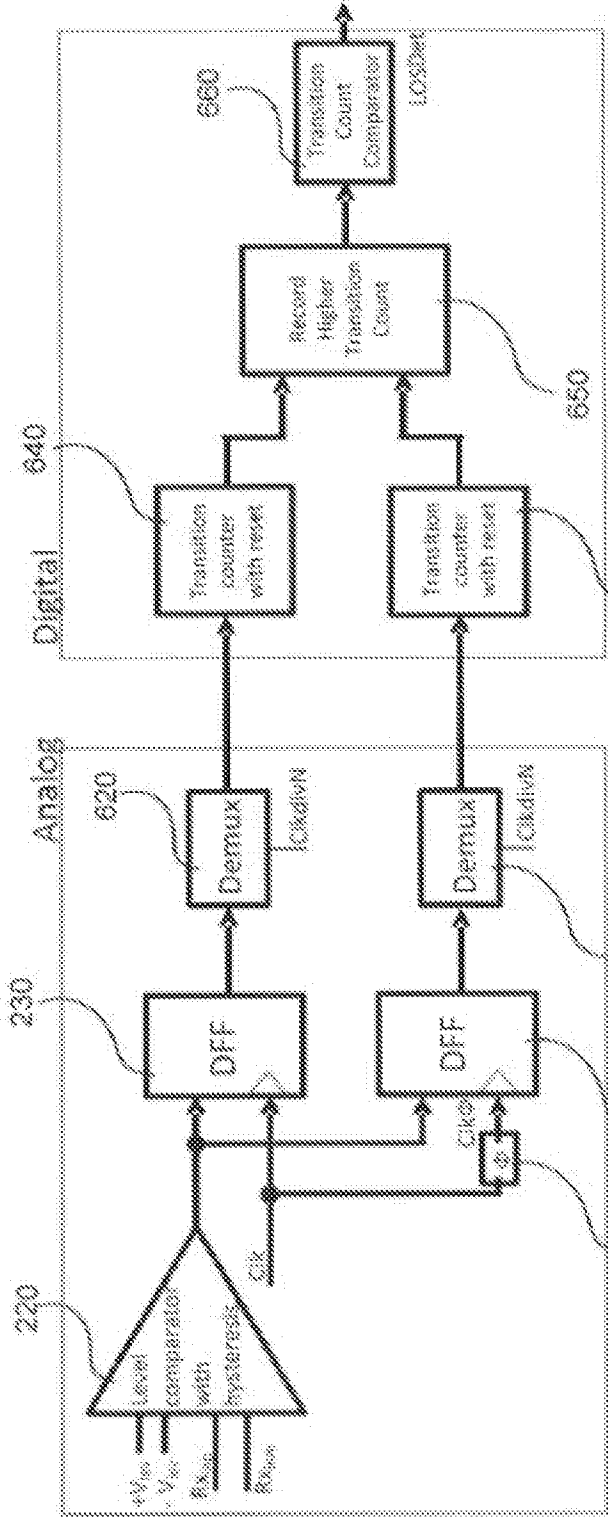


Figure 6

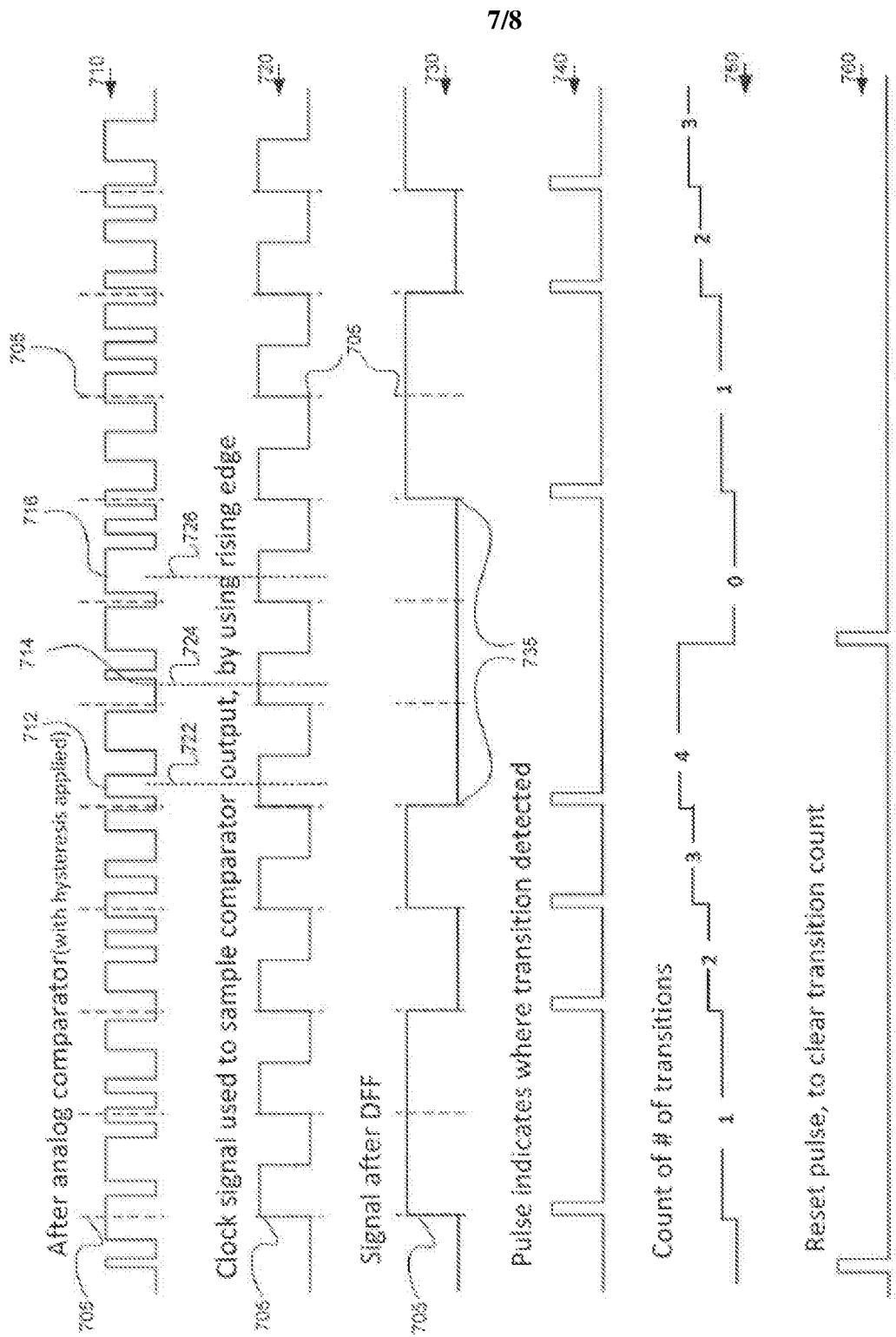
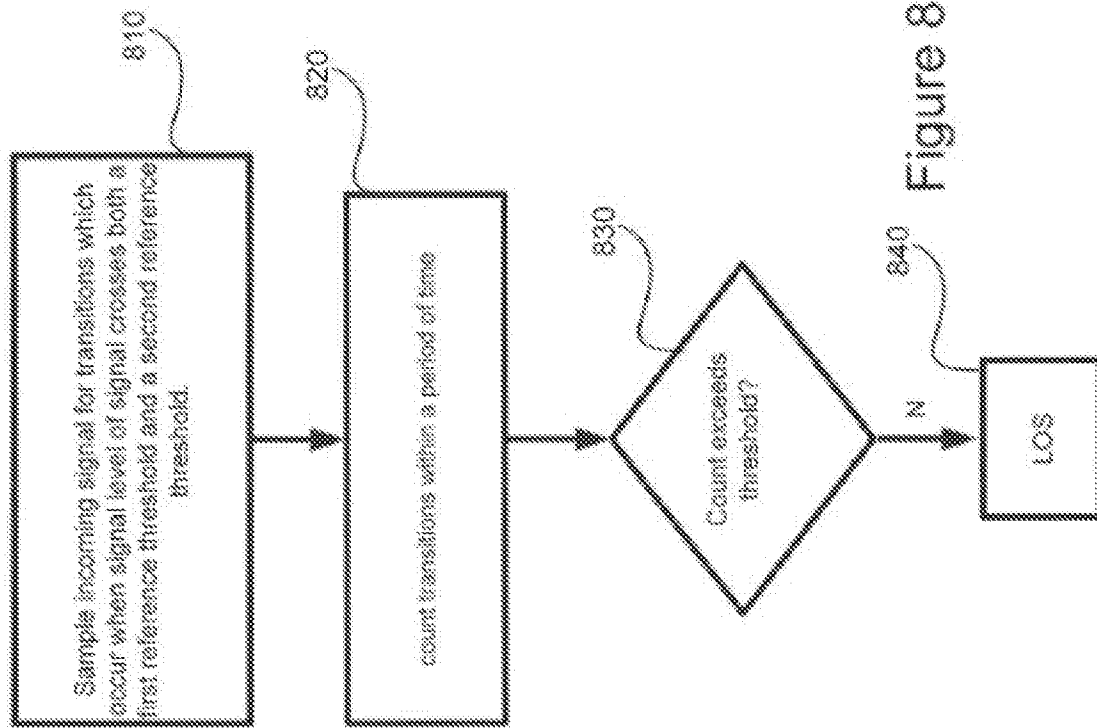


Figure 7

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/096170

A. CLASSIFICATION OF SUBJECT MATTER

H03K 5/22(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K, H04L, H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: LOS detect+ sampl??? Analog digital signal noise threshold clock asynchronous rate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7254169 B1 (SILICON LAB., INC.) 07 August 2007 (2007-08-07) description, column 2, line 58 to column 4, line 53, figures 1-2	1
Y	US 7254169 B1 (SILICON LAB., INC.) 07 August 2007 (2007-08-07) description, column 2, line 58 to column 4, line 53, figures 1-2	2-23
Y	US 6377082 B1 (AGERE SYSTEMS GUARDIAN CORP.) 23 April 2002 (2002-04-23) description, column 4, line 25 to column 5, line 11, figures 3-4	2-23
A	US 6489803 B1 (SILICON LAB., INC.) 03 December 2002 (2002-12-03) the whole document	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

19 February 2016

Date of mailing of the international search report

03 March 2016

Name and mailing address of the ISA/CN

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Telephone No. (86-10)62413855

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2015/096170

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US	7254169	B1	07 August 2007	None	
US	6377082	B1	23 April 2002	None	
US	6489803	B1	03 December 2002	None	