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(71) Applicant *(for all designated States except US)*: **INFINEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Strasse 53, 81669 Munich (DE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **MA, Fan, Yung** [SG/SG]; 66 Jalan Girang, 359235 Singapore (SG).

(74) Agents: **HEINZE, Ekkehard** et al.; Meissner, Bolte & Partner GbR, P.O. Box 86 06 24, 81633 Munich (DE).

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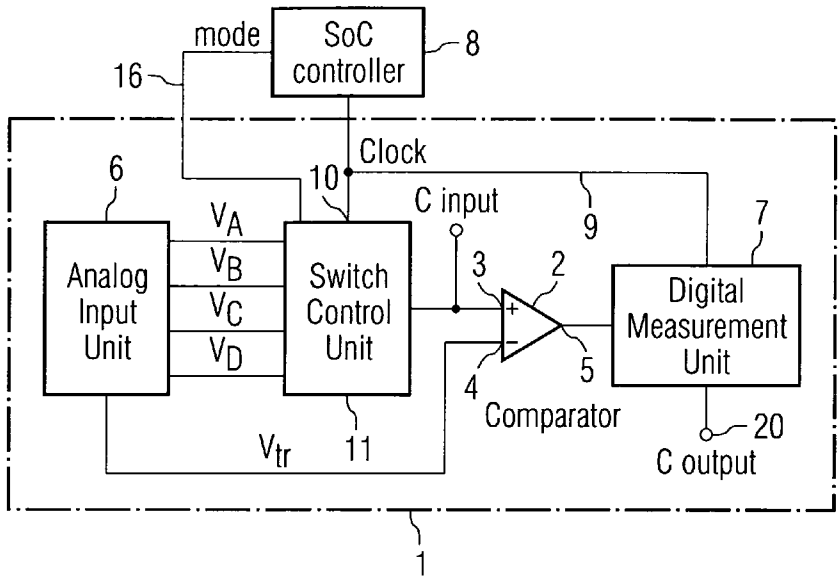
(54) **Title:** ON-CHIP TEST CIRCUIT FOR AN EMBEDDED COMPARATOR



(57) **Abstract:** A semiconductor chip comprising an embedded comparator is provided with an on-chip test circuit for the comparator. The test circuit comprises an analog input unit which, during a test mode of the chip, produces a range of analog voltage signals that are applied to a first input of the comparator and a threshold voltage signal that is applied to a second input of the comparator. A switch control unit is provided to control the application of a predetermined sequential pattern of these analog voltage signals to the first input of the comparator in synchrony with a clock signal supplied to the switch control unit during a predetermined test period. A digital measurement unit is provided to receive output signals from the comparator during the test period in response to said input patterns, to compare the output signals with the clock signal, and to measure and to store data relating thereto.

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Description

On-chip test circuit for an embedded comparator

The present invention relates to the testing of a comparator embedded in a System-on-Chip (SoC) product and, in particular, relates to a semiconductor chip with an on-chip test circuit for a comparator embedded in the chip.

Complex SoC products, for example products for analog voltage detection and for joystick control, often contain embedded comparators. The performance of these comparators needs to be tested to detect manufacturing faults and to ensure that the products function according to their specifications. Conventional methods of testing involve either reliance on functional testing wherein the whole circuit of which the comparator forms a part is tested or the implementation of a special test mode wherein the input and output of the comparator are made accessible at chip pins in order that the an off-chip test circuit can be used to test the functioning of the comparator.

However, neither of these methods is entirely satisfactory. Functional testing wherein the whole of a comparator-containing circuit is tested may not be able to test the comparator itself sufficiently. Many different tests may have to be devised in an attempt to test operation of the comparator and this is time consuming and, therefore, costly.

In contrast, off-chip testing of a comparator via a test mode involves either the use of additional chip pins, where the total number for any given chip circuitry may be limited, or analog multiplexing control, which is required to share access to analog I/O pins. Also, in order to test a high performance comparator which has a small input voltage resolution and a high speed, high performance and high cost test instruments are required. Delays associated with off-chip connection loading limit the frequency of input test signals and high

speed buffers are therefore required to drive the outputs off-chip. These buffers limit the testing accuracy and increase test costs. In addition, the loading caused by such analog test-paths may degrade the functional performance of the embedded comparator under test.

The aim of the present invention is to provide a semiconductor chip with an on-chip test circuit for an embedded comparator which can be used to overcome or mitigate many of the problems outlined above in conventional testing methods.

According to a first aspect of the present invention there is provided a semiconductor chip comprising an embedded comparator with first and second inputs and an output, and an on-chip test circuit for the comparator, the test circuit comprising
an analog input unit adapted to produce a range of analog voltage signals for application to said first input of said comparator during a test mode of the chip and a threshold voltage signal for application to said second input of said comparator;
a switch control unit adapted to control application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator over time in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit adapted to receive output signals from said comparator during said predetermined test period in response to said input pattern, to compare same with said clock signal, and to store data relating to said output signals and said comparison.

Preferably, the analog input unit comprises a resistor divider. Advantageously, the resistor divider comprises a chain of four resistors that is tapped at its ends and between each of the resistors to provide four analog voltage signals and the threshold voltage signal which can be set by resistor ratios.

Preferably also, the tapping point at middle-point of resistor chain provides the threshold voltage.

Preferably also, the resistor divider is adapted such that it is only supplied with an output voltage power supply during the test mode of the chip and is otherwise isolated during normal operation of the comparator.

Preferably also, the switch control unit comprises a plurality of switches and a control generator for controlling the individual operation of each of these switches by non-overlapping control signals. Advantageously, each switch controls the application of one of the range of analog voltage signals to said first input of said comparator.

Preferably also, the semiconductor comprises a digital controller producing a clock signal and the switch control unit comprises a non-overlap clock generator that controls operation of the control generator and that is adapted to receive the clock signal from the digital controller.

Preferably also, the non-overlap clock generator uses the clock signal from the digital controller to produce other clock signals that are in synchrony with the clock signal from the digital controller and that are used to produce non-overlapping control signals which are applied sequentially with a frequency which is twice that of the clock signal frequency.

Preferably also, the control generator is adapted to operate in one of a plurality of different test modes and in a normal operation mode and can be switched between these various modes by the digital controller.

Preferably also, in at least one of the test modes two analog voltage signals, one higher and the other lower than the threshold voltage, are applied alternately to said first input

of said comparator such that each larger voltage that is higher or lower than the threshold voltage is followed by a smaller voltage that is respectively lower or higher than the threshold voltage with a frequency which is twice that of the clock signal frequency.

Advantageously, one of the test modes is an overdrive test mode wherein all the analog voltage signals produced by the analog input unit are applied in sequence to said first input of said comparator such that each larger voltage that is higher or lower than the threshold voltage is followed by a smaller voltage that is respectively lower or higher than the threshold voltage.

Preferably also, the control generator comprises a decoder adapted to receive signals from the digital controller and linked to a plurality of 4-input multiplexers each of which is adapted to produce one of said control signals in response to said signals from said non-overlap clock generator.

Preferably also, the digital measurement unit comprises a digital counter that counts the positive edge transitions of the output signals from said comparator during said predetermined test period.

Preferably also, the digital measurement unit comprises a control circuit that compares the number of positive edge transitions counted by the digital counter with the number of input transitions in the same predetermined test period.

Preferably also, the control circuit is linked to a test status register which is used to store a pass/fail indicator that shows whether the number of positive edge transitions counted by the digital counter is the same as the number of input transitions in the same predetermined test period.

According to a second aspect of the present invention there is provided a method of on-chip testing a comparator embedded in

a semiconductor chip, the method comprising the provision of an on-chip test circuit wherein, during a test mode of the chip,
an analog input unit produces a range of analog voltage signals that are applied to said first input of said comparator and a threshold voltage signal that is applied to said second input of said comparator;
a switch control unit controls the application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit receives output signals from said comparator during said predetermined test period in response to said input pattern, compares same with said clock signal, and stores data relating to said output signals and said comparison.

Preferred embodiments of the present invention will now be described by way of example with reference to the accompanying drawings.

Fig.1 is a schematic block circuit diagram of one embodiment of a combined comparator and a test circuit therefore for incorporation in a system-on-a-chip in accordance with the present invention;

Fig. 2 is a circuit diagram of an analog input unit forming part of the test circuit shown in Fig. 1;

Figs 3a and 3b are alternative embodiments of the analog input unit shown in Fig. 2;

Fig. 4 is a block circuit diagram of a switch control unit forming part of the test circuit shown in Fig. 1;

Fig. 5 is a series of graphs illustrating clock signals and control signals produced by the switch control unit in each of three different test modes;

Fig. 6 is a series of graphs illustrating the voltage signals input to a first input of the comparator over time by the analog input unit in response to the control signals shown in Fig. 5 in each of the same three different test modes;

Fig. 7 is a block diagram showing an embodiment of a control generator forming part of the switch control unit shown in Fig. 4 illustrating the way each of the three different test modes can be implemented; and

Fig. 8 is a block circuit diagram showing an embodiment of digital measurement unit forming part of the test circuit shown in Fig. 1.

The block circuit diagram shown in Fig. 1 illustrates one embodiment of a combined comparator and test circuit therefore that can be implemented on a single semiconductor chip. The combined circuit 1, as indicated within the dashed lines, comprises a comparator 2 having first and second inputs, namely a noninverting input terminal 3 and an inverting input terminal 4, and an output terminal 5.

During normal operation of the chip and therefore of the comparator 2, the noninverting input terminal 3 is supplied with a voltage signal C_{input} and the inverting input is supplied with a threshold or trip voltage signal V_{tr} by an analog input unit 6 that forms part of the test circuit. The output signal, C_{output}, from the output terminal 5 of the comparator 2 is supplied to a digital measurement unit 7 that also forms part of the test circuit. As described below, during normal operation of the comparator 2, the unit 7 outputs C_{output} unchanged but during a test mode C_{output} is analyzed in order that operation of the comparator 2 can be assessed.

To this end, the semiconductor chip on which the combined circuit 1 is implemented includes circuitry (not shown) to isolate the test circuit during normal operation of the comparator 2 when it is not needed and also circuitry to control and to supervise operation of the test circuit during a test mode. The latter circuitry is preferably provided by a digital controller 8 forming part of the microcontroller for the SoC. This digital controller 8 also provides a clock signal that is supplied during a test mode via inputs 9 and 10 respectively to the digital measurement unit 7 and to a switch control unit 11 that also forms part of the test circuit. The comparator 2 may be strobed or non-strobed. In the former case, the clock signal supplied during the test mode needs to be synchronized with the strobe signal by the digital controller 8.

The analog input unit (AIU) 6 is adapted to generate precise analog voltages V_A, V_B, V_C, V_D relative to the trip voltage V_{tr}. During a test mode, these analog voltages are applied to the noninverting input terminal 3 of the comparator 2 via the switch control unit 11 that applies the voltages to the input terminal 3 in a predetermined repeating pattern over time in synchrony with the clock signal. To this end, the analog input unit 6 preferably comprises a resistor divider 12, as shown in Fig. 2, that is connected between output and lower-voltage analog sources V_{DDA} and V_{SSA} respectively.

In the illustrated embodiment the resistor divider 12 comprises a chain of four resistors comprising two identical resistors R_1 and two resistors R_2 and R_3 arranged in series. The chain is tapped at its ends and between each of the resistors to provide the four analog voltages V_A V_B, V_C, V_D and the trip voltage V_{tr}. The tapping point at middle of resistor chain provides the trip voltage V_{tr}. Hence, resistors R_1 and R_2, R_1 and R_3 are arranged in series symmetrically on either side of the middle tapping point such that $R_T=2R_1+R_2+R_3$ where R_T is the total resistance.

In this way, the accuracy of the input voltages is controlled by resistor matching and the resistor ratio R_1/R_T is used to generate small input voltages V_B and V_C to test the comparator's resolution. V_A and V_D are used to apply large input voltages to the comparator 2. The threshold voltage is set by resistors ratio $(R_1+R_3)/R_T$. It will be appreciated that additional voltages could also be generated by the resistor chain if required.

As shown in Fig. 4 and as described in more detail below, the voltages V_A, V_B, V_C, V_D are applied to the input terminal 3 of the comparator 2 via switches S_1, S_2, S_3, S_4 respectively that form part of the switch control unit 11. The RC delay of this analog input signal path affects the speed of the comparator testing. The resistance of the resistance divider 12 and the switches S_1, S_2, S_3, S_4 together with the input capacitance of the comparator 2 and any parasitic capacitances all contribute to the RC delay.

To increase the speed of the testing, larger switches S_1, S_2, S_3, S_4 are needed along with a reduction in the value of the resistor divider 12, which will increase the power. In order to minimize the resistor divider 12 power during normal operation of the chip and therefore of the comparator 2 the output voltage V_{DDA} may be applied to the resistor divider 12 via a pin 13 only during test mode, as shown in Fig. 3a. Alternatively, as shown in Fig. 3b, a switch S_p is provided to isolate the resistor divider 12 during normal operation but this will affect the accuracy of the testing.

The switch control unit 11 controls the application of the voltages V_A, V_B, V_C, V_D in predetermined patterns to the noninverting input terminal 3 of the comparator 2 via the switches S_1, S_2, S_3, S_4. An embodiment of switch control unit 11 will now be described in more detail with reference to Fig. 4 where it can be seen that the unit 11 comprises a control generator 14 that controls operation of the switches S_1, S_2,

S_3, S_4 via switch control signals A, B, C, D, respectively. The control signals A, B, C, D are arranged to be non-overlapping in the manner shown to prevent shorting of any analog input voltages from the analog input unit 6.

The operation of the control generator block 14 is determined by a non-overlap clock generator 15 which receives the clock signal from the digital controller 8 via input 10. This clock signal is also supplied independently to the control generator 14. The non-overlap clock generator 15 uses the clock signal to produce two clock signals $\varnothing_1$ and $\varnothing_2$ that each comprise pulses of reduced pulse width relative to the main clock signal and in synchrony with the main clock pulses and the periods between the clock pulses respectively.

The control generator 14 is adapted to operate in one of three different test modes, namely Overdrive, Large Drive and Small Drive, or in a normal operation mode. A 2-bit mode input 16 is supplied by the digital controller 8 to the control generator 14 to switch it between these various modes and normal operation. The differences between the control signals generated in each of the three different test modes will now be described with reference to Fig. 5.

At the top of Fig. 5 are four clock pulses that are used to produce the control signals A, B, C, D in each of the three test modes, namely Overdrive, Large Drive and Small Drive. The control signals themselves in each of these test modes are as shown in the underlying graphs. The four clock pulses comprise the main clock signal at the top, a clock signal T, which simply comprises the main clock signal divided by two, and the clock signals $\varnothing_1$ and $\varnothing_2$ as described above.

In the Overdrive test mode, the control signals A, B, C, D are produced in the sequence A, C, D, B at similar intervals with respect to each other such that the frequency of each signal is equivalent to half the frequency of the clock signals $\varnothing_1$ and $\varnothing_2$ but with the same pulse width and in synchrony with these

signals. In the Large Drive test mode, control signals B and C are inactive and the control signals A and D are each produced with the same pulse width and in synchrony with the clock signals $\varnothing_1$ and $\varnothing_2$ respectively. In contrast, in the Small Drive test mode the control signals A and D are inactive and the control signals B and C are each produced with the same pulse width and in synchrony with the clock signals $\varnothing_1$ and $\varnothing_2$ respectively.

The resulting voltage input C_{input}-V_{tr} applied to the comparator 2 via the switches S_1, S_2, S_3, S_4 controlled by the control signals A, B, C, D in each of these three test modes is as shown in Fig. 6. It can be seen here that in the Overdrive test mode all four of the voltages V_A, V_B, V_C, V_D are applied in the sequence V_A, V_C, V_D, V_B such that each of the two larger voltages, V_A, V_D, is followed by the smaller voltage, V_C, V_B respectively, that is lower or higher than the trip voltage V_{tr}. The voltages V_A, V_B, V_C, V_D are applied sequentially with a frequency which is twice that of the clock signal frequency. This forces the comparator 2 to switch rapidly from state to state as the signal crosses the trip voltage in order that its overdrive recovery can be assessed. In contrast, in the Large Drive test mode only the larger voltages V_A and V_D are applied alternately to the comparator 2, whereas in the Small Drive test mode the smaller voltages V_B and V_C are applied alternately to the comparator 2. Again, in both cases the voltages are applied sequentially with a frequency which is twice that of the clock signal frequency. In normal mode when comparator testing is not needed, all the control signals (A,B,C,D) are inactive.

In should be noted that the non-overlap clock generator 15 is a well-known standard circuit and will not be described in further detail. Likewise, the circuit producing the clock signal T, which comprises the main clock signal divided by two, will also not be described in detail.

However, an embodiment of control generator 14 capable of implementing the three different test modes described above is shown in Fig. 7. In this generator 14, four 4-input multiplexers MUX1, MUX2, MUX3, MUX4 are linked to a decoder 17 which receives the 2-bit mode input 16 from the digital controller 8 that determines whether the control generator adopts one of the three test modes or normal operation mode. This then causes the decoder to output an appropriate signal, namely one of the signals S0, S1, S2 or S3 respectively, to the multiplexers MUX1-MUX4 in response. The multiplexers MUX1, MUX2, MUX3, MUX4 each have four inputs A0, A1, A2, A3 linked to the clock generator 15 and the clock signal T circuit for receipt of the clock pulse signals $\varnothing_1$, $\varnothing_2$ and T to produce the control signals A, B, C, D in response to the receipt of the appropriate signals from the decoder 17 as shown in Fig. 7.

Hence, in each of the three test modes different predetermined patterns of the voltage are applied to the comparator 2 over time in synchrony with the clock signal for a predetermined test period. This enables the comparator resolution, over-drive recovery and speed to be tested by analyzing C_{output} during the test modes in the digital measurement unit 7.

In this unit 7, an embodiment of which will now be described with reference to Fig. 8, digital circuits are used to measure the comparator output response. First, the output signal from the output terminal 5 of the comparator 2 is fed to a digital buffer 18 of the unit 7 by connecting the output terminal 5 of the comparator 2 directly to the unit 7 via its input terminal 19. The output from the buffer 18 is linked directly to an output terminal 20 of the unit 7 which therefore outputs the comparator output signal C_{output} directly for use by other circuitry of the chip during both normal operation and when in a test mode.

However, in a test mode, the output from the buffer 18 is also processed internally in the unit 7 via a gate 21 controlled by a control circuit 22 linked to the clock input 9. The gate 21

feeds the comparator output signal C_{output} to a digital counter 23 that counts the positive edge transitions of the signal. The output from the counter 23 can be read by the SoC digital controller 8. The control circuit 22 is also used to reset the counter 23 and to set the counting interval, for example N clock cycles.

For a known number of input transitions in N cycles, there should be corresponding number of output transitions from the comparator 2 otherwise the comparator 2 has a speed performance problem. Hence, by counting every positive comparator output edge every clock cycle, the output from the counter 23 can be checked and a test status register 24 used to store a pass/fail indicator that shows whether the comparator 2 is operating correctly in this regard. The control circuit 22 can be used to reset indicators in the register 24.

Hence, the invention provides a combined comparator and test circuit therefore that can be implemented on a single semiconductor chip to overcoming or substantially mitigating many of the problems outlined above encountered when using conventional testing methods. It will be appreciated, however, that the embodiments of the various parts of the invention described above are examples only and many variations and modifications are possible without departing from the scope of the present invention.

Claims

1. A semiconductor chip comprising an embedded comparator with first and second inputs and an output; and an on-chip test circuit for the comparator, the test circuit comprising
an analog input unit adapted to produce a range of analog voltage signals for application to said first input of said comparator during a test mode of the chip and a threshold voltage signal for application to said second input of said comparator;
a switch control unit adapted to control application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit adapted to receive output signals from said comparator during said predetermined test period in response to said predetermined input pattern, to compare same with said clock signal, and to store data relating to said output signals and said comparison.

2. A semiconductor chip as claimed in Claim 1, wherein the analog input unit comprises a resistor divider.

3. A semiconductor chip as claimed in Claim 1, wherein the switch control unit comprises a plurality of switches and a control generator for controlling the individual operation of each of these switches by non-overlapping control signals.

4. A semiconductor chip as claimed in Claim 3, wherein each switch controls the application of one of the range of analog voltage signals to said first input of said comparator.

5. A semiconductor chip as claimed in Claim 1, wherein the digital measurement unit comprises a digital counter that counts the positive edge transitions of the output signals from said comparator during said predetermined test period.

6. A semiconductor chip as claimed in Claim 5, wherein the digital measurement unit comprises a control circuit that compares the number of positive edge transitions counted by the digital counter with the number of input transitions in the same predetermined test period.

7. A semiconductor chip as claimed in Claim 6, wherein the control circuit is linked to a test status register which is used to store a pass/fail indicator that shows whether the number of positive edge transitions counted by the digital counter is the same as the number of input transitions in the same predetermined test period.

8. A semiconductor chip comprising an embedded comparator having first and second inputs and an output; and an on-chip test circuit for the comparator, the test circuit comprising a resistor divider adapted to produce a range of analog voltage signals for application to said first input of said comparator during a test mode of the chip and a threshold voltage signal for application to said second input of said comparator;
a switch control unit adapted to control application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit adapted to receive output signals from said comparator during said predetermined test period in response to said predetermined input pattern, to compare same with said clock signal, and to store data relating to said output signals and said comparison.

9. A semiconductor chip as claimed in Claim 8, wherein the resistor divider comprises a chain of four resistors that is tapped at its ends and between each of the resistors to provide four analog voltage signals and the threshold voltage signal.

10. A semiconductor chip as claimed in Claim 9, wherein the tapping point at middle-point of resistor chain provides the threshold voltage.

11. A semiconductor chip as claimed in Claim 8, wherein the resistor divider is adapted such that it is only supplied with an output voltage power supply during the test mode of the chip and is otherwise isolated during normal operation of the comparator.

12. A semiconductor chip comprising an embedded comparator having first and second inputs and an output; an on-chip microcontroller adapted to produce a clock signal; and an on-chip test circuit for the comparator, the test circuit comprising
an analog input unit adapted to produce a range of analog voltage signals for application to said first input of said comparator during a test mode of the chip and a threshold voltage signal for application to said second input of said comparator;
a switch control unit adapted to control application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator over time in synchrony with said clock signal during a predetermined test period; and
a digital measurement unit adapted to receive output signals from said comparator during said predetermined test period in response to said predetermined input pattern and to store data relating to said output signals that can be read by said microcontroller.

13. A semiconductor chip as claimed in Claim 12, wherein the switch control unit comprises a plurality of switches, a control generator for controlling the individual operation of each of these switches by non-overlapping control signals, and a non-overlap clock generator that is adapted to receive the clock signal from the microcontroller and to produce modified clock signals that control operation of the control generator.

14. A semiconductor chip as claimed in Claim 13, wherein the modified clock signals are in synchrony with the clock signal from the microcontroller and are used to produce non-overlapping control signals which are applied sequentially to the control generator with a frequency which is twice that of the clock signal frequency.

15. A semiconductor chip as claimed in Claim 13, wherein the control generator comprises a decoder that is adapted to receive signals from the microcontroller and that is linked to a plurality of 4-input multiplexers each of which is adapted to produce one of said control signals in response to said signals from said non-overlap clock generator.

16. A semiconductor chip comprising an embedded comparator having first and second inputs and an output; an on-chip microcontroller adapted to produce a clock signal; and an on-chip test circuit for the comparator, the test circuit comprising
an analog input unit adapted to produce a range of analog voltage signals for application to said first input of said comparator during a test mode of the chip and a threshold voltage signal for application to said second input of said comparator;
a plurality of switches each adapted to control the application of one of said analog voltage signals to said first input of said comparator;
a control generator for controlling the individual operation of each of these switches by non-overlapping control signals in a predetermined sequential pattern in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit adapted to receive output signals from said comparator during said predetermined test period in response to said predetermined input pattern and to store data relating to said output signals that can be read by said microcontroller.

17. A semiconductor chip as claimed in Claim 16, wherein the control generator is adapted to operate in one of a plurality of different test modes and in a normal operation mode and can be switched between these various modes by the digital controller.

18. A semiconductor chip as claimed in Claim 17, wherein in at least one of the test modes two analog voltage signals, one higher and the other lower than the threshold voltage, are applied alternately to said first input of said comparator such that each larger voltage that is higher or lower than the threshold voltage is followed by a smaller voltage that is respectively lower or higher than the threshold voltage with a frequency which is twice that of the clock signal frequency.

19. A semiconductor chip as claimed in Claim 17, wherein one of the test modes is an overdrive test mode wherein all the analog voltage signals produced by the analog input unit are applied in sequence to said first input of said comparator such that each larger voltage that is higher or lower than the threshold voltage is followed by a smaller voltage that is respectively lower or higher than the threshold voltage.

20. A method of on-chip testing a comparator embedded in a semiconductor chip, the method comprising the provision of an on-chip test circuit wherein, during a test mode of the chip, an analog input unit produces a range of analog voltage signals that are applied to said first input of said comparator and a threshold voltage signal that is applied to said second input of said comparator;
a switch control unit controls the application of a predetermined sequential pattern of said analog voltage signals to said first input of said comparator in synchrony with a clock signal supplied to said switch control unit during a predetermined test period; and
a digital measurement unit receives output signals from said comparator during said predetermined test period in response

to said input patterns, compares same with said clock signal, and stores data relating to said output signals and said comparison.

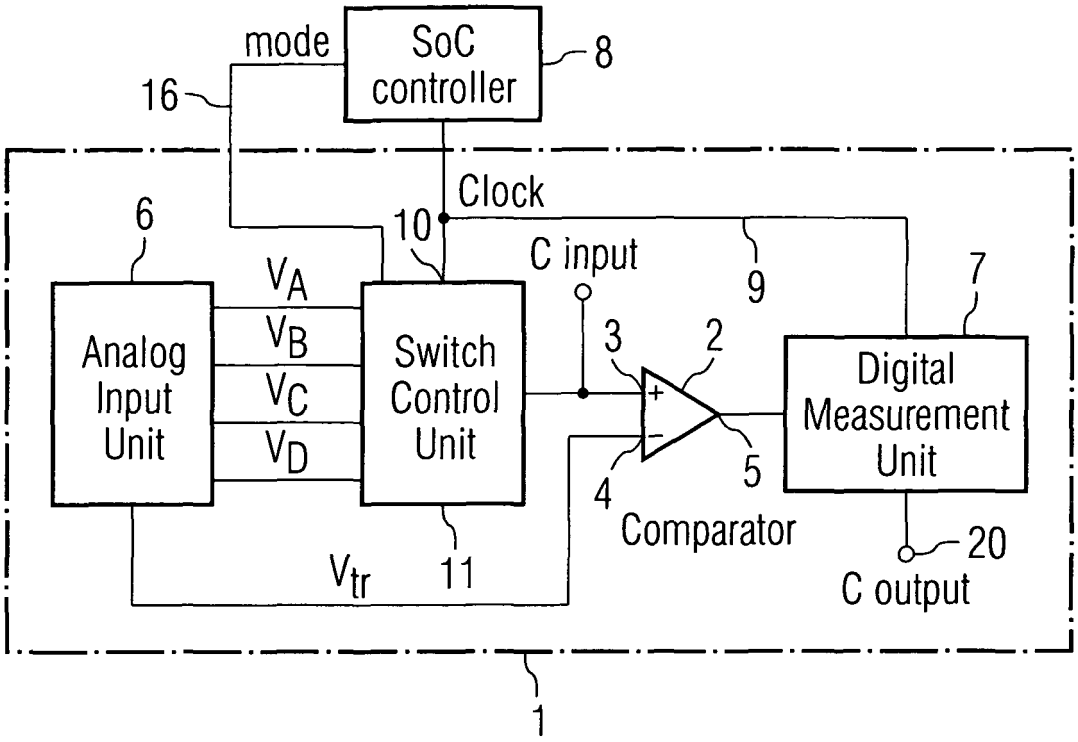
21. A method as claimed in Claim 20, wherein the switch control unit comprises a plurality of switches which are each operated by non-overlapping control signals.

22. A method as claimed in Claim 20, wherein the digital measurement unit counts the positive edge transitions of the output signals from said comparator during said predetermined test period.

23. A method as claimed in Claim 22, wherein the digital measurement unit compares the number of positive edge transitions counted during said predetermined test period with the number of input transitions input to said comparator by said switch control unit in the same predetermined test period.

24. A method as claimed in Claim 23, wherein a test status register is used to store a pass/fail indicator that shows whether the number of positive edge transitions is the same as the number of input transitions input to said comparator by said switch control unit in the same predetermined test period.

FIG 1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SoC controller
8
16
Clock
6
10
C input
9
7
V_A
V_B
V_C
V_D
Analog Input Unit
Switch Control Unit
3
2
Digital Measurement Unit
4
5
Comparator
20
C output
V_{tr}
11
1

FIG 2

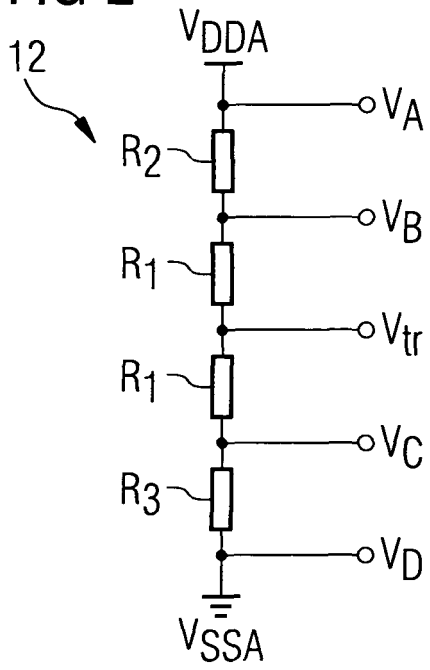

12
V_{DDA}
V_A
R_2
V_B
R_1
V_{tr}
R_1
V_C
R_3
V_D
V_{SSA}

FIG 3A

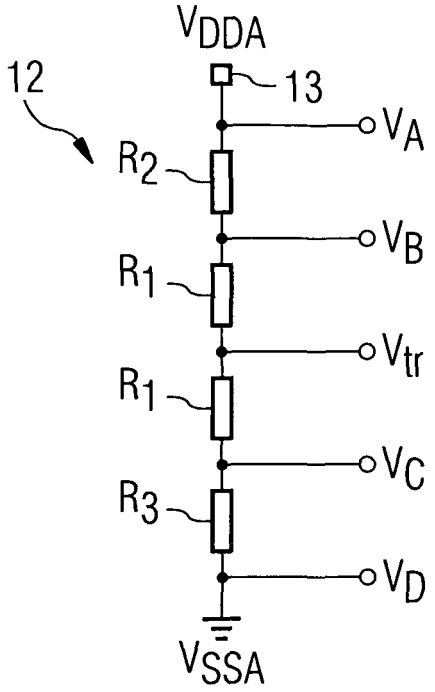


FIG 3B

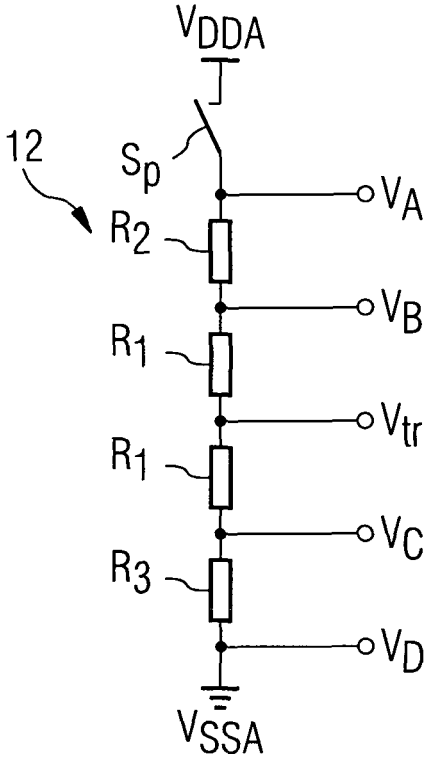


FIG 4

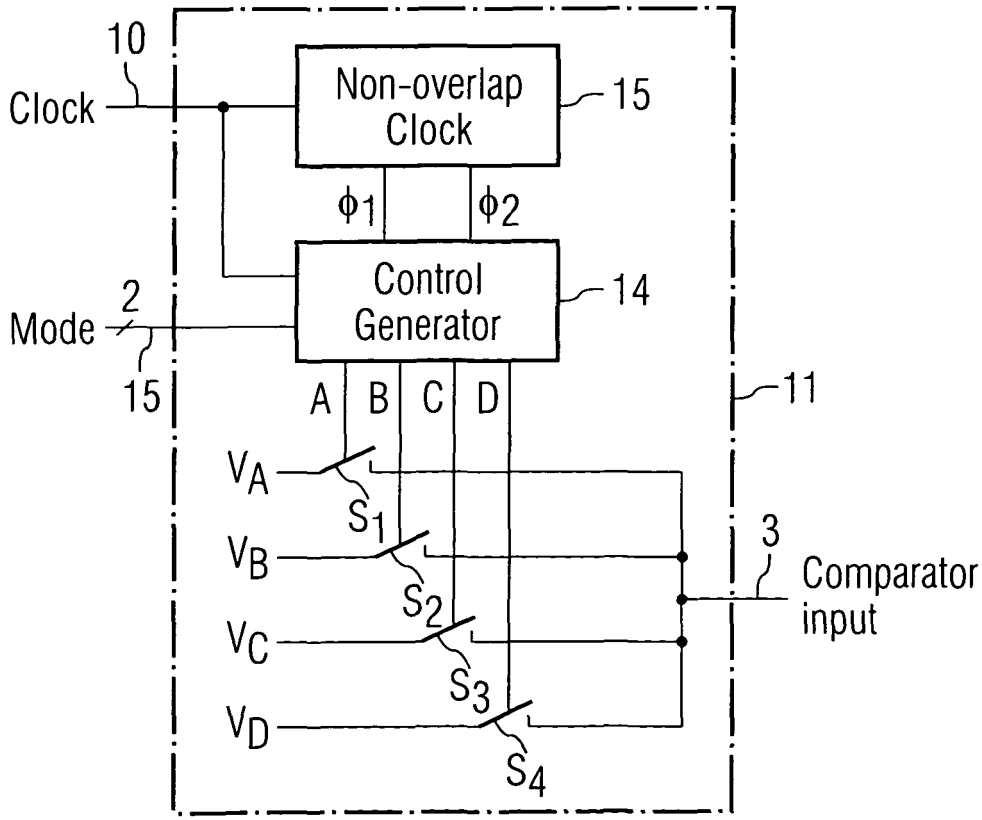
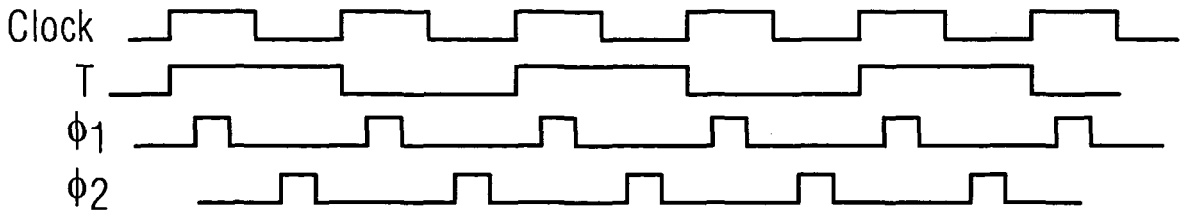
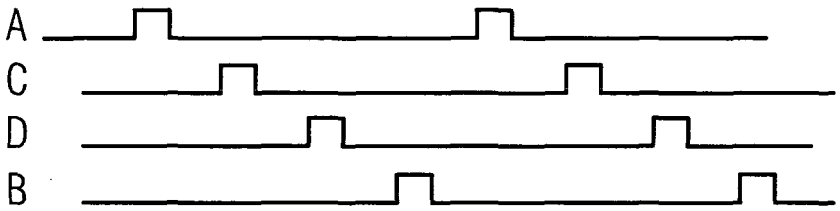


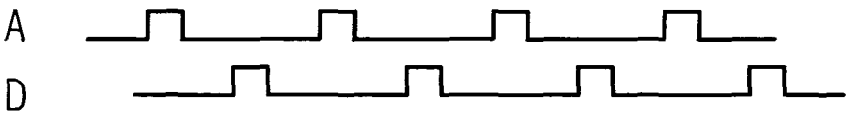
FIG 5



Overdrive Mode

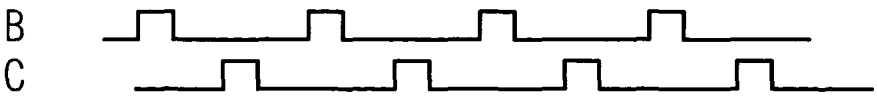


Large Drive Mode



B and C inactive

Small Drive Mode



A and D inactive

FIG 6

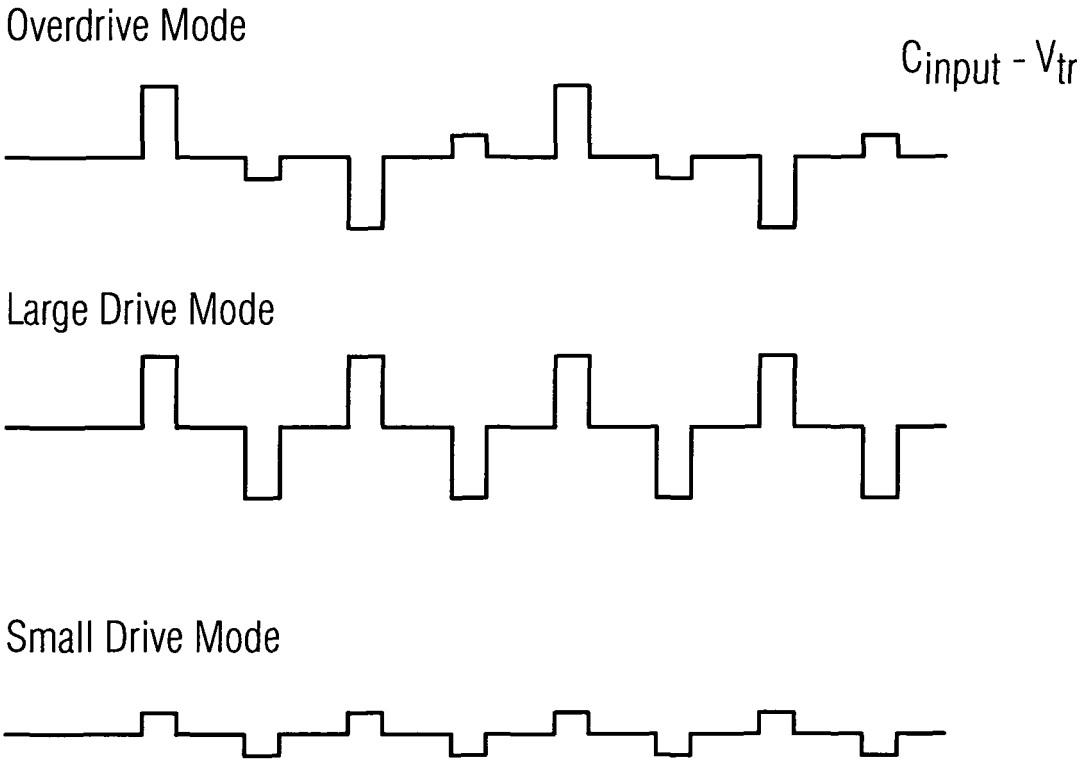

Overdrive Mode
$C_{input} - V_{tr}$
Large Drive Mode
Small Drive Mode

FIG 7

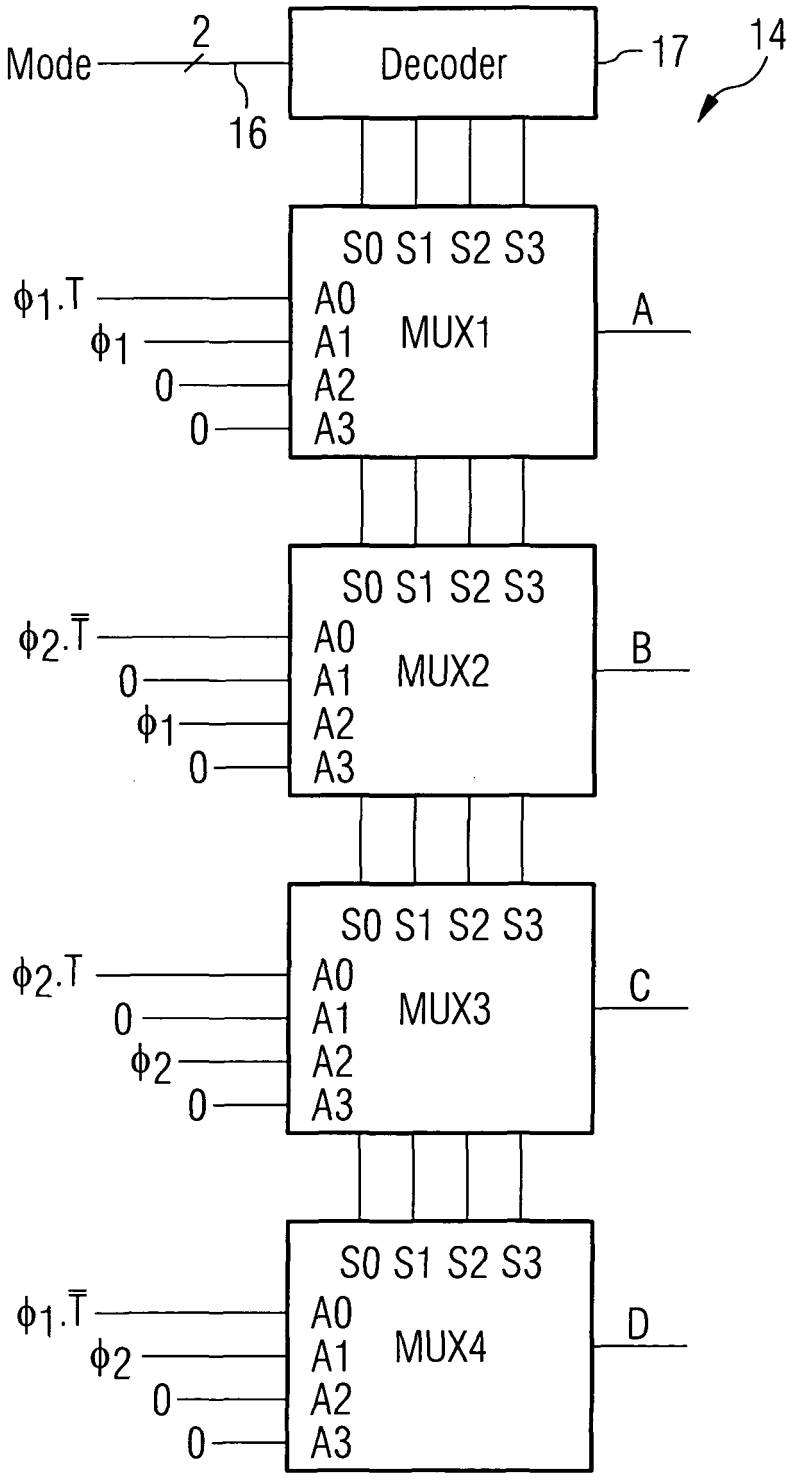
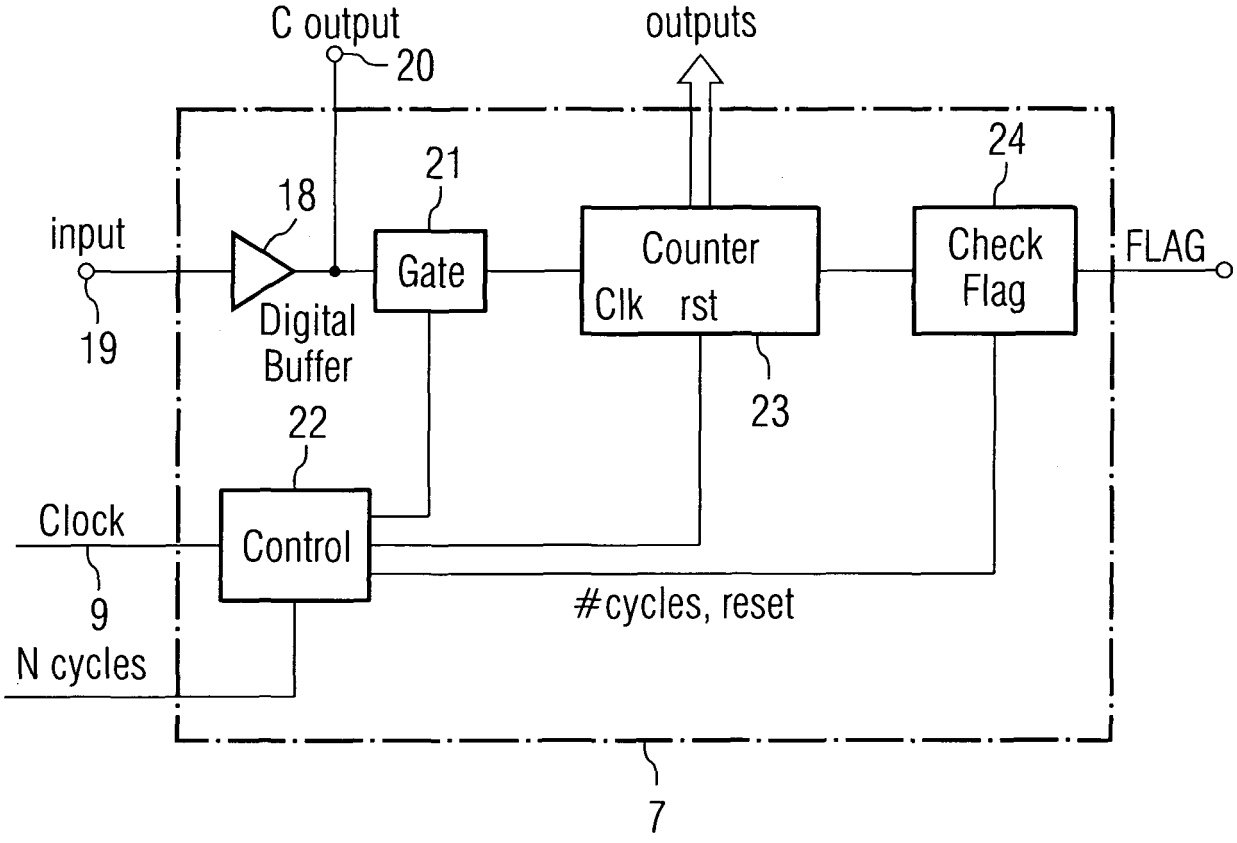

Mode
2
16
Decoder
17
14
S0 S1 S2 S3
A0
A1
A2
A3
MUX1
A
$\phi_1.T$
ϕ_1
0
0
S0 S1 S2 S3
A0
A1
A2
A3
MUX2
B
$\phi_2.\overline{T}$
0
ϕ_1
0
S0 S1 S2 S3
A0
A1
A2
A3
MUX3
C
$\phi_2.T$
0
ϕ_2
0
S0 S1 S2 S3
A0
A1
A2
A3
MUX4
D
$\phi_1.\overline{T}$
ϕ_2
0
0

FIG 8


C output
20
outputs
24
21
18
input
Gate
Counter
Clk rst
Check
Flag
FLAG
19
Digital
Buffer
23
22
Clock
Control
9
#cycles, reset
N cycles
7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/007022

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R31/3193

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 09 015301 A (NIPPON ELECTRIC IC MICROCOMPUT) 17 January 1997 (1997-01-17) abstract	1-24
A	US 2001/026173 A1 (SCHNEIDER RALF [DE] ET AL) 4 October 2001 (2001-10-04) abstract; claims 1-11; figures 1,2 paragraphs [0007] - [0018]	1-24
A	US 6 691 271 B1 (KANEHIRA YUSUKE [JP] ET AL) 10 February 2004 (2004-02-10) abstract; claims 1-13; figures 1-16 column 2, line 9 - column 5, line 37	1-24
A	US 2005/240842 A1 (YONAGA TAKERU [JP]) 27 October 2005 (2005-10-27) abstract; claims 1-13; figures 1-10 paragraphs [0006] - [0010]	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 May 2007	01/06/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nadal, Rafael

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/007022

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