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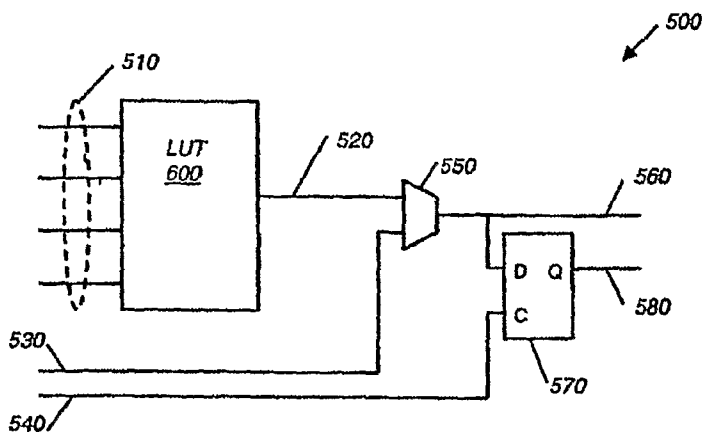
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(54) Title: FPGA ARCHITECTURE AT CONVENTIONAL AND SUBMICRON SCALES



(57) Abstract: Reconfigurable logic devices (500) and methods of programming the devices are disclosed. The logic device includes a look-up table (600, 600') (LUT) and at least one storage element (570) configured for sampling LUT output signals (520). The LUT (600, 600') comprises a plurality of input signals (510), an array of programmable impedance devices (110) operably coupled to the input signals (510), and the LUT output signals (520). Each programmable impedance devices (110) in the array includes a first electrode (120) operably coupled to one of the input signals (520), a second electrode (130) disposed to form a junction (150) wherein the second electrode (130) at least partially overlaps the first electrode (120), and

a programmable material (140) disposed between the first electrode (120) and the second electrode (130). The programmable material (140) operably couples the first electrode (120) and second electrode (130) such that each programmable impedance device (110) exhibits a non-volatile programmable impedance. The array may be configured as a one-dimensional array (700, 700') or two-dimensional array (610, 610').

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# INTERNATIONAL SEARCH REPORT

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**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H03K19/177 G11C13/02

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, IBM-TDB, INSPEC

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 072 716 A (JACOBSON JOSEPH M [US] ET AL) 6 June 2000 (2000-06-06) the whole document	1-13
A	WO 2005/093870 A (THIN FILM ELECTRONICS ASA [NO]; SANDBERG MATS [SE]; NORDAL PER-ERIK [N] 6 October 2005 (2005-10-06) the whole document	1-13
A	US 2004/238864 A1 (TRIPSAS NICHOLAS H [US] ET AL) 2 December 2004 (2004-12-02) the whole document	1-13
A	WO 2005/053027 A (INFINEON TECHNOLOGIES AG [DE]; SEZI RECAI [DE]; WALTER ANDREAS [DE]; E) 9 June 2005 (2005-06-09) the whole document	1-13
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Further documents are listed in the continuation of Box C.

See patent family annex.

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- \*Z\* document member of the same patent family

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No PCT/US2007/002805
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