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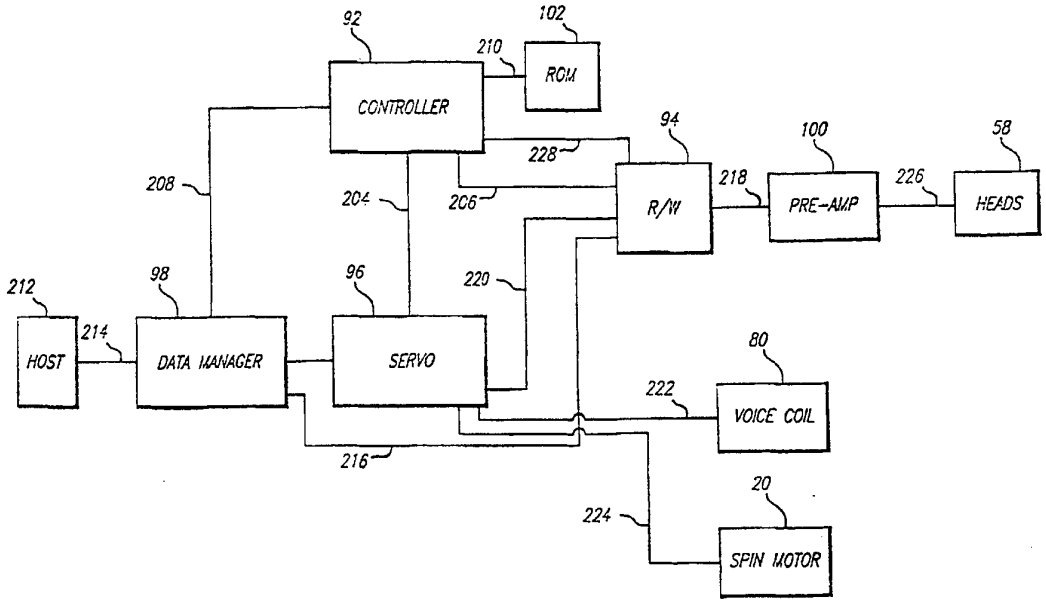

(57) Abstract

An electronic architecture that provides a portable hard disk drive that can meet the type II PCMCIA specification and which can efficiently operate with a 3.3 V power supply.

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SYSTEM ARCHITECTURE FOR HDD

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an electronic architecture for a hard disk drive.

2. DESCRIPTION OF RELATED ART

Most computer systems contain a massive memory storage device such as a hard disk drive. Hard disk drive units include a magnetic disk that is capable of storing a large amount of binary information. The magnetic disk is typically coupled to a hub that is rotated by an electric motor, commonly referred to as a spin motor. The drive unit also has a head that magnetizes and senses the magnetic field of the disk. The head is typically located at the end of a cantilevered actuator arm which can pivot about a bearing assembly mounted to the base plate of the disk drive. The actuator arm has a coil which cooperates with a magnet mounted to the base plate. Providing a current to the coil creates a torque on the arm and moves the head relative to the disk. The coil and magnet are commonly referred to as a voice coil motor or VCM. The actuator arm, motors and other components of a typical disk drive unit are relatively small and fragile, and are therefore susceptible to damage when subjected to excessive external shock loads or vibration. For this

reason, hard disk drives are usually rigidly mounted to the housing of the computer system by screws or other fastening means.

Hard disk drives contain programs and other information that are vital to the user. It is sometimes desirable to transfer such information to a different computer system. Transferring programs from a hard disk typically requires loading the information onto a floppy disk, or sending such information over a phone line. Such methods can be time consuming, particularly if the program is long, or there is a large amount of data. There have been developed portable hard disk drives which can be plugged into a slot in the computer. To reduce the amount of possible component damage to the drive unit, the housing and disk assembly are constructed to be quite rugged. These rugged assemblies are typically heavy and bulky, and generally impractical to carry and store.

The Personal Computer Memory Card International Association (PCMCIA) has recently promulgated specifications for portable memory cards which can be plugged into slots within a computer. The PCMCIA standard includes a type I format, a type II format and a type III format, each format being distinguished by a different card thickness. Memory can be added to a computer by merely plugging in an additional card. Similarly, a modem or facsimile (FAX) card can be added to a system with the push of the hand. The standardized format of the cards allow a user to plug the memory card of one computer into another computer, regardless of the type or make of either system.

The standardized PCMCIA cards are approximately the size of a credit card and include a connector which mates with a corresponding connector in the computer. The small size of the card provides an electronic assembly that is easy to carry and store. It is very desirable to have a hard disk drive unit which conforms with the PCMCIA format, so

that the disk drive can be readily carried and plugged into an existing slot of a computer. Such a hard disk card must be rugged enough to withstand the large shock loads that may be applied to the drive unit, such as by dropping the card onto a hard surface. The existence of such a card would also allow the user to accumulate memory in the same manner that floppy disk are used today.

Hard disk drive units contain a number of integrated circuits that control the operation of the drive. The circuits typically include a read/write channel that is coupled to the transducers of the actuator arm assembly. The read/write channel is connected to a interface controller which is coupled to the host computer. The interface controller is coupled to a random access memory device that is used as a buffer to store data transferred between the disk and the host.

Disk drives also contain circuitry that provide current to the voice coil to maintain the head(s) on the center of a track (servo routine) and to move the head(s) from track to track (seek routine). Additionally, a disk drive typically contains circuitry to commutate the motor, and to insure that the motor and disk rotate at a uniform speed.

The operation of the above described circuits is typically controlled by a microprocessor based controller. Conventional disk drive also contain a separate circuit which interfaces the controller with the other circuits. This chip is commonly referred to as glue logic. U.S. Patent No. 4,979,056 issued to Squires et al., discloses a hard disk architecture which has a microprocessor based controller that controls the operation of the interface controller, read/write channel, actuator and spin motor circuitry. The Squires system utilizes an embedded servo format which stores the servo information in the same sector of a track as the data. During each sector the processor services the voice coil and spin motor

circuitry of the drive. The processor employs a hierarchy that allows the spin motor and the voice coil to be serviced in conjunction with the transfer of data between the host computer and the disk. Although a Squires type system provides a controller based system to efficiently transfer data between the disk and the host, such systems typically require a large amount of electrical components that must be mounted onto a printed circuit board.

U.S. Patent No. 4,933,785 issued to Morehouse et al. and U.S. Patent No. 5,025,335 issued to Stefansky et al., disclose conventional hard disk drives which have a printed circuit board mounted to a disk drive housing commonly referred to as a HDA. The HDA is typically sealed and contains the disk, actuator arm and spin motor of the assembly. The HDA may also contain a pre-amplifier that is connected to the heads of the drive. The remaining electrical components (interface controller, read/write channel, actuator circuitry, etc.) are located on the external printed circuit board. The circuit board extends along the entire length and width of the HDA. Therefore the thickness of the overall assembly is determined by the thickness of the HDA, the thickness of the printed circuit board and the height of the electrical components.

Application Serial No. 07/975,008 filed on November 13, 1992 and assigned to the same assignee as the present application, discloses a hard disk drive which contains a 1.8 inch diameter disk and meets the type III requirements of the PCMCIA specifications. Like the Morehouse and Stefansky patents, the '008 application contains a printed circuit board that extends across the length and width of the HDA. It has been found that using such a board arrangement will not provide a disk drive that

meets the type II PCMCIA specification. It is desirable to provide a hard disk drive assembly which meets the type II PCMCIA specifications.

Portable disk drives that meet the PCMCIA specifications can be used in portable laptop computers. Some laptop computers are designed to run on a 3.3 V power supply. Conventional computer electronics are designed to operate with a 5.0 V power supply. It has been found that it takes more time to access a volatile memory devices that is supplied with only 3.3 V of power. The longer access time slows down the performance of any processor that is utilizing the memory device. It would therefore be desirable to have an electronic architecture for a hard disk drive which can run on 3.3 V without degrading the performance of the drive.

SUMMARY OF THE INVENTION

The present invention is an electronic architecture which can be entirely contained within a hard disk drive that meets the type II PCMCIA specifications. The disk drive contains a low profile spin motor that rotates a disk. The rotation of the spin motor is controlled by spin motor circuitry within a servo chip. The disk rotates relative to an actuator arm assembly which has transducers that store and retrieve information from the disk. The actuator arm is rotated by a voice coil that is controlled by actuator circuitry within the servo chip.

The disk drive has an outer housing and a connector which allows the drive to be plugged into a host computer. The transducers are coupled to a read/write chip which transfers information between the disk and the host computer through a data manager chip. The data manager; read/write and servo chips are all controlled by a controller chip. All of the electrical components of the drive are mounted to a single printed circuit board. The circuit board is approximately one-third the length of the housing and is located between the disk and the connector. The reduction in board length allows the circuit board to be placed in the same plane as the disk and therefore does not add to the thickness of the overall assembly. The compact assembly provides a hard disk drive which meets the type II PCMCIA thickness requirements.

The controller chip contains a core processor and a state machine that controls the operation of the drive. The core microprocessor is a product commonly referred to as a reduced instruction set chip ("RISC") which has a dual bus architecture that allows the processor to execute fetching, decoding, reading and execution routines in parallel. The processor of the present invention requires fewer memory fetches for a

given function, than processors used in hard disk drives of the prior art. The reduction in memory fetches allows the overall system to be used in a system that contains a 3.3 V power supply.

It is therefore an object of the present invention to provide a hard disk drive that will meet the type II PCMCIA specifications.

It is also an object of the present invention to provide an electronic architecture which will reduce the size of the printed circuit board of a hard disk drive assembly.

It is also an object of the present invention to provide an electronic architecture for a hard disk drive that can operate with a 3.3 V power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a perspective view of a hard disk drive of the present invention;

Figure 2 is a top cross-sectional view of the hard disk drive;

Figure 3 is a bottom view of the cover of the hard disk drive;

Figure 4 is a cross-sectional view of the actuator arm assembly;

Figure 5 is a cross-sectional view of the hard disk drive showing the printed circuit board and the connector of the drive;

Figure 6 is a cross-sectional view of the spin motor;

Figure 7 is a bottom view of the printed circuit board;

Figure 8 is a schematic of the system architecture of the disk drive;

Figure 9 is a schematic of the data manager chip of the system;

Figure 10 is a schematic of the servo chip of the system;

Figure 11 is a representation of a sector of the disk;

Figure 12 is a schematic of the controller chip of the system;

Figure 13 is a schematic of the R/W chip of the system;

Figures 14a-g are flowcharts of the operation of the disk drive.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 1 shows a hard disk drive 10 of the present invention. The disk drive 10 is constructed as a card which can be plugged into a host computer (not shown). The unit 10 includes a housing 12 and a connector 14. In the preferred embodiment, the housing has the dimensions of 85.6 x 54.0 x 5.0 millimeters. The dimensions conform with the specifications issued by the Personal Computer Memory Card International Association (PCMCIA) for a type II electronic card. The PCMCIA is an association that has promulgated a specification which list dimensions and other requirements for a standard electronic card. Each computer that conforms with the PCMCIA specification will contain slots that can receive a standardized card. With such a standard, electronic cards of one computer can be readily plugged into another computer, regardless of the model or make of the systems. A copy of the PCMCIA standard can be obtained by writing to the Personal Computer Memory Card International Association at 1030 G East Duane Avenue, Sunnyvale, California 94086.

The PCMCIA standard includes three types of cards which each have varying thicknesses. A type I card is approximately 3.3 millimeters thick, a type II card is approximately 5.0 millimeters thick and a type III card is approximately 10.5 millimeters thick. The computer has a plurality of adjacent slots that are wide enough to receive a type II card. Both the type I and II cards occupy a single slot, while the type III card occupies two slots. Each computer slot contains a 68 pin connector that is typically mounted to a motherboard to provide an interconnect to the computer system. The PCMCIA standards were originally established for

memory and/or logic cards including internal modem and facsimile boards. The present invention provides a hard disk drive unit that can conform to the PCMCIA type II card format.

In the preferred embodiment, the connector 14 of the card assembly 10 has 68 pins which can mate with the 68 pin connector located in the computer. The connector 14 is typically constructed from a dielectric material that has a plurality of sockets 16 which mate with pins (not shown) located in the computer connector. The connector has certain pins designated for power, ground and data. As required by the PCMCIA specification, the sockets dedicated to ground are longer than the sockets dedicated to power, and the sockets dedicated to power are longer than the sockets dedicated to data. Such an arrangement allows the card to be plugged into an operating "live" system, without creating voltage spikes or power surges within the card.

Referring to Figures 2-7, the hard disk drive contains a disk 18 that is rotated by a spin motor 20. The disk 18 is typically constructed from a metal, glass, ceramic or composite substrate that is covered with a magnetic coating as is known in the art. As shown in Fig. 6, the spin motor 20 includes a hub 22 coupled to a spindle magnet 24 by a pair of conical bearings 26. Within the hub 22 is a stator 28 and a number of windings 30 which cooperate with magnets 32 attached to the inner surface of the hub 22. Providing a current to the windings 30 creates a magnetic flux which passes through the magnets 32 and induces a rotation of the hub 22 and the disk 18. The hub 22 has a pair of tapered inner surfaces 34 which slide along corresponding tapered surfaces 36 of the conical bearings 26. Between the tapered hub surfaces 36 and bearings 26 is a thin layer of fluid which allows relatively frictionless rotation between the two members 22 and 26. Between the conical

bearings 26 is a space 38 which provides a reservoir for the bearing fluid. The bearing fluid is preferably a ferro-fluid lubricant which is maintained between the hub 22 and bearings 26 by the magnetic flux of the spindle magnet 24. The conical bearings 26 provide a low profile spin motor 20 which can withstand the type shock loads that could be applied to a hand held computer and/or disk drive.

The disk 18 is clamped against a hub shoulder 40 by a disk clamp 42. The disk clamp 42 is preferably constructed from a thermoplastic material that is ultrasonically melted onto the motor 20. The thermoplastic flows into a plurality of grooves 44 located in the hub 22. The plastic in the grooves 44 prevent movement of the disk 18 in the z axis. A portion of the clamp 42 also flows into a space between the inner diameter of the disk 18 and the hub 22 to prevent lateral movement of the disk 18.

The fixed spindle 24 is captured by a pair of caps 45 and 46. The bottom cap 45 is mounted to a base plate 48 by a layer of adhesive 50. In the preferred embodiment the adhesive is a material sold by Minnesota Manufacturing & Minning Co. ("3M") under the designation AF46. The film 50 is also used to mount the lower conical bearing 26 to the cap 45. The upper cap 46 is mounted to the fixed spindle 24. In the preferred embodiment, the cap 46 and cover 52 are coupled together by an adhesive viscoelastic film material 54 mounted on the cover 52. The viscoelastic material 54 compensates for tolerances between the height of the motor 20 and the space between the base plate 48 and cover 52. The viscoelastic 54 also dampens shock and vibrational loads applied to the motor 20.

As shown in Fig. 2, the disk 18 rotates relative to an actuator arm assembly 56 which has a pair of transducers 58 commonly referred to as heads. The transducers 58 contain a coil (not shown) which can magnetize and sense the magnetic field of each corresponding adjacent surface of the disk 18. Each head 58 is supported by a flexbeam 60 that is attached to an actuator arm 62. In the preferred embodiment, each flexbeam 60 is constructed from one or more conductive plates (not shown) that are separated by a relatively elastic dielectric material (not shown). The metal plates may provide a conductive path for the signals that are sent to the transducers 58. The heads 58 each contain a slider (not shown) which cooperate with the air stream produced by the rotation of the disk 18 to create an air bearing between the surface of the disk and the transducer. The air bearing lifts the head 58 off of the surface of the disk 18. The flexbeams are constructed to be flexible enough to allow the heads to be separated from the disk surface by the air bearings and take up the disk 18 and motor 20 axial runout. The heads 58 can be constructed to provide either horizontal or vertical recording.

The flexbeams 60 are inserted into slots of the actuator arms 62 by an adhesive. In the preferred embodiment, the adhesive can be cured by a primer, heat, or a UV light source. The actuator arms 62 are preferably constructed from a silicon carbide which is both light and strong. The actuator arms 62 pivot about a bearing assembly 66. As shown in Fig. 4, the bearing assembly 66 includes a bearing block 68 which extends from the base plate 48. Referring to Fig. 2, the actuator arms 62 have a triangular shaped roller bearing 70 which extends into a V shaped slot 72 in the block 68. The roller bearing 70 is pressed into contact with the block 68 by a C shaped spring clip 74. The apex of the roller bearing 70 engages the apex of the slot 72 such that the bearing rolls relative to the

block 68 when the actuator arms 62 are rotated about the bearing assembly 66. The roller bearing of the present invention provides a low profile bearing assembly that produces a relatively small amount of friction and which can withstand the typical shock loads applied to a hand held disk drive.

At the end of the actuator arms 62 is a magnet 76 located between a pair of stationary coils 78. The magnet has north (N) and south (S) poles, so that when a current is sent through the coils in one direction the north pole experiences a force perpendicular to the coils, and when current is provided in an opposite direction the south pole experiences a force in the same direction. The magnet and coils, commonly referred to as a voice coil motor or VCM 80, rotate the actuator arms 62 and move the heads 58 relative to the disk 18. As shown in Fig. 4, the coils 78 are mounted to a C shaped shield plate 82 that is constructed from a ferrite material which provides a return path for the magnetic flux, and maintains the flux in the area of the voice coil 80.

As shown in Figs. 2 and 5, the connector 14 is located at one end of the housing 12 and is captured by indent surfaces 84 in the base plate 48 and cover 52. The indent surfaces 84 prevent the connector 14 from moving in any direction relative to the housing 12. The connector sockets 16 each have tails 86 that are soldered to conductive surface pads 88 on a printed circuit board 90 (PCB). As shown in Fig. 4, the printed circuit board 90 is supported by the base plate 48 and contains all of the electrical components required to operate the disk drive assembly 10.

As shown in Fig. 7, mounted to the printed circuit board 90 is a controller chip 92, a read/write channel chip 94 and a servo chip 96. Each chip is housed within an integrated circuit package that is soldered

to the board 90 by conventional techniques well known in the art. As shown in Fig. 2, the opposite side of the circuit board 90 contains a data manager chip 98, a pre-amplifier chip 100 and a read only memory (ROM) chip 102. The board 90 also contains passive elements such as resistors 104 and capacitors 106 to complete the electrical system of the drive assembly. The board 90 is located between the disk 18 and the connector 14. As shown in Fig. 5, the printed circuit board 90 is located in a plane essentially parallel with the disk 18. Locating the board 90 essentially "in-plane" with the disk 18 reduces the overall thickness of the disk drive assembly.

As shown in Fig. 2, the printed circuit board 90 is coupled to the actuator arm assembly 56 by a flexible circuit board 108. The flexible circuit board 108 is typically constructed from polyimide sheets commonly sold under the trademark KAPTON, which encapsulate conductive traces that extend throughout the circuit. One end of the flexible circuit 108 has contact pads 110 that are soldered or ultrasonically to the flexbeam 60. As shown in Fig. 5, the opposite end of the circuit 108 has contact pads that are pressed into operative contact with corresponding pads on the printed circuit board 90 by clamp down strips 116 located on the cover plate 52. The clamp down strips 116 are adapted to apply a pressure to the contact pads of the flexible circuit 108 when the cover plate 52 is attached to the base plate 48. The clamp down strips 116 provide a means of coupling/decoupling the flexible circuit 108 to the printed circuit board 90 without having to solder together the two members. As shown in Fig. 2, the disk drive assembly also contains flexible circuits 126 and 128 that couple the printed circuit board 90 to the coils 78 of the voice coil 80 and the windings 30 of the spin motor 20, respectively. The flexible circuits 126 and 128 have

contact pads that are pressed into contact with corresponding pads on the circuit board 90 by clamp down strips 116.

As shown in Figs. 3 and 4, mounted to the cover 52 is an elastomeric seal 122 that is pushed against a corresponding surface 124 in the base plate 48. The elastomer 122 seals the disk 18, spin motor 20 and actuator arm assembly 56 in an area which is commonly referred to as the HDA 126. The cover plate 52 is attached to the base plate 48 by a clamp 128. The clamp 128 has a number of spring tabs 130 which extend into corresponding slots 132 in the plates 48 and 52. The clamp 128 may have an elastomeric strip 134 which absorbs external shock and vibrational loads that are applied to the edges of the disk drive assembly 10. The disk drive 10 is typically loaded into a host computer so that the edges of the card are supported by the computer housing. Any shock or vibrational loads applied to the computer are therefore typically transmitted to the disk drive through the edge of the drive. The elastomeric strip 134 dampens these loads to prevent damage or an interruption to the operation of the drive. The clamp provides a means for attaching the base plate 48 to the cover 52 without using screws or other equivalent fastening means. The elimination of threaded fasteners assist in the reduction of the overall height of the assembly. As shown in Figs. 2 and 3, the cover 52 has a rectangular pin 136 that is inserted into a corresponding groove 138 in the base plate 48 to align the two members 48 and 52.

The base plate 48 has a filter chamber 140 which contains a breather filter 142 located external to the HDA 126. The base plate 48 has a slot 142 which provides fluid communication between the HDA 126 and the chamber 140. When the pressure of the air within the HDA 126 is lower than the ambient air outside of the drive 10, the differential

pressure will pump air past the clamp 128, through the interface of the cover 52 and base plate 48 and into the HDA area 126 and base 48. This HDA area 126 is in fluid communication with the filter chamber 140 which also is in fluid communication with the HDA. The pumped air flows into the HDA 126 through the filter chamber 140. Hydrocarbon, acid-gas and other impurities in the air are captured by the breather filter 142. The breather filter may also have a humidity control element.

The disk drive assembly 10 also has a recirculation filter 146 that removes impurities within the HDA. The recirculation filter 146 is located in the center of chamber separated from the HDA by a wall 146. The filter 146 separates an upstream chamber 150 from a downstream chamber 151. Rotation of the disk 18 induces a flow of air into the upper chamber 152, through the filter 146, into the lower chamber 146 and back into the HDA area 126 of the disk 18. The disk drive may also have an environmental control assembly 180 constructed from materials that absorb hydrocarbons, acid-gas and water.

Figure 8 shows a schematic of the system architecture of the hard disk drive assembly 10. The system controls the operation of the disk drive. Data is typically stored on a magnetic disk 12 along annular tracks concentric with the diameter of the disk. In the preferred embodiment, the disk is 1.8 inches in diameter. Although a 1.8 inch disk is described, it is to be understood that the present invention can be used with disks having other diameters such as 1.3", 2.5", 3.5", etc. For a 1.8" disk, the system will typically store data on 130 tracks per disk surface. Each track contains a plurality of servo sectors. Each sector is capable of storing up to 768 bytes of data. The total assembly is capable of storing up to 130 Mbytes of data.

As shown in Fig. 8, the system 10 includes the data manager chip 98, the controller chip 92, the servo chip 96 and the read/write ("R/W") chip 94. The system also has the read only memory ("ROM") device 102 coupled to the controller 92, and the pre-amplifier circuit ("pre-amp") 100 connected to the heads 58 and the R/W chip 94. The controller 92 is coupled to the servo 96 and R/W 94 chips through serial lines 204 and 206, respectively. The controller 92 is coupled to the data manager 98 by address/data bus 208 and to the ROM 202 by instruction bus 210. The data manager 98 is coupled to a host 212 by address/data bus 214 and to the R/W chip 94 by data bus 216. The R/W chip 94 is connected to the pre-amplifier chip by lines 218. The servo chip 96 is coupled to the R/W chip 94 through servo lines 220. The servo chip 96 is also connected to the voice coil 80 and spin motor 20 through lines 222 and 224, respectively. The pre-amp chip 100 is connected to the heads 58 through lines 226. The controller 92 is also coupled to the R/W chip 94 by raw data line 228. The serial lines and address/data busses contain control signal lines which are needed to transfer information between the respective chips. Although the term line is used through this specification, it is to understood that the term line may include multiple lines.

As shown in Figure 9, the data manager 98 is coupled to the host 212 by a host interface controller circuit 230. The interface controller 230 contains hardware to interface with the host 212 by providing return handshakes, etc. in accordance with the host protocol. In the preferred embodiment, the interface controller 230 complies with the PCMCIA protocol. The interface controller 230 is coupled to a random access memory (RAM) device 232 through data bus 234. The RAM 232 provides a data buffer to store the data transferred between the host 212 and the

disk 18. In the preferred embodiment, the RAM can store up to 4.0 Kbytes of data. 3.5 Kbytes of memory is typically dedicated to storing data transferred between the host and the disk. The remaining 0.5 Kbytes of memory provide a scratch pad which is typically dedicated to storing certain predetermined disk drive characteristics. When each disk drive is assembled, various characteristics of the drive unit are determined and stored on the disk. When the disk drive is powered up, the controller performs an initialization routine. Part of the routine retrieves the drive characteristics from the disk and stores the same in the scratch pad portion of the RAM.

The management of the RAM 232 is controlled by a memory controller circuit 236 which provides addresses to the memory device 232 on address bus 238 and an enable control signal on line 240. The memory controller circuit 236 receives access request from the interface controller circuit through lines 242. The controller circuit 236 also receives access request from a disk controller circuit 244 through lines 246. The disk controller circuit 244 provides an interface between the disk manager chip 98 and the R/W chip 94. The disk controller circuit 244 receives read/write control signals on lines 248 from the interface circuit 236 which are relay to the R/W chip 94 on read and write gate lines 250 and 252. The interface, memory and disk controller circuits is also connected to the controller chip 92 through lines 254, 256 and 258.

The memory controller 256 controls the storage and retrieval of data between the RAM 232 and interface controller circuit 230, between the RAM 232 and the disk controller circuit 244 and between the controller chip 92 and the data manager chip 98. The RAM 232 and controller chip 92 are coupled together by dedicated data bus 208. The controller chip provides addresses and a data manager chip select (DM

CS) control signal when the controller chip 92 wants access to the RAM 232.

To write data onto the disk 18, the host 212 initially provides a write request that is received by the interface controller circuit 230, which executes the requisite handshaking sequence. The interface controller circuit 230 generates an access request to the memory controller circuit 236 to store the logical addresses and data from the host to the memory buffer 232. The memory controller circuit 236 then stores the data in the buffer 232 in accordance with a memory mapping scheme. The interface controller circuit 230 generates a HOSTINT interrupt signal that is sent to the controller chip 92.

After acknowledging the HOSTINT signal, the controller chip 92 will request access to the RAM 232 to read the logical addresses provided by the host 212. The controller chip 92 converts the logical addresses to physical disk addresses. The controller chip 92 may then initiate a seek routine to move the heads 58 to the proper location on the disk 18. When the voice coil 80 has moved the transducers 58 to the desired disk sector, the controller chip 92 provides a Z sector signal to the data manager 98. Upon receiving the Z sector signal, the disk controller circuit 244 provides a data access request to the memory controller circuit 236. The memory controller circuit 236 initiates a write sequence onto the disk 18 by placing the corresponding contents of the RAM 232 onto the bus 216.

To read data, the host 212 provides a read request that is received by the interface controller circuit 230. The requested logical addresses are stored in the buffer 232. A HOSTINT signal is generated and the logical addresses are retrieved by the controller chip 92. The controller chip 92 converts the physical addresses to the actual sectors on the disk

and then initiates a seek routine to move the actuator arm, accordingly. When the transducers are above the proper disk location, the controller chip 92 provides a Z sector signal to the data manager 98. The disk controller circuit 244 then generates a memory access request to the memory controller circuit 236 which enables the RAM 232. Data is then transferred from the R/W chip 94 to the buffer 232 through the disk controller circuit 244. The memory controller circuit 236 then transfers the data from the RAM 232 to the host 212 through the interface controller circuit 230.

As shown in Figure 10, the servo chip 96 contains a voice coil control circuit 270 and a spin motor control circuit 272 to drive the voice coil 80 and spin motor 20, respectively. The servo chip 96 is coupled to the controller chip 92 by a bi-directional 16 bit synchronous serial port 274. The serial port 274 is coupled to a digital to analog (Dac) converter by lines 278. The Dac 278 contains a spin motor Dac port 280, a voice coil Dac port 282 and an analog to digital (Ad) Dac port 284.

The voice coil port provides three signals Vvcmoffset, Vvcmtrack and Vcm gain range to the voice control circuit 270 on lines 288-292. The three signals are summed within a summing circuit 294. The Vvcmoffset signal provides the bias voltage for the voice coil 80. The Vvcmtrack signal provides a secondary voltage signal, that will vary the bias signal to more accurately control the driving signal of the voice coil 80. The Vcm gain range signal is another secondary signal that provides a higher resolution of the bias signal and is typically employed during a servo routine of the drive. The amplitudes of the Vcm signals are determined by a 8 bit data stream which is provided by the controller chip 92 to the voice coil port 280 through the bi-directional serial port 274. The data command is accompanied by a 7 bit address and a

read/write bit which are decoded by the serial port. The data is directed to the appropriate Dac port in accordance with the contents of the 7 bit address.

The summation circuit 294 provides a signal to an operational amplifier 296 which biases a driver circuit 298. The driver circuit 298 is connected to the coils 78 of the voice coil through pins VcmP 300 and VcmN 302. The voice coil control circuit 270 also contains a current sensor 304 which is fed back to the operational amplifier 296 to provide a direct current control of the current supplied to the voice coil 80.

The spin motor port 280 provides signals Vspnoffset, Vspntrack and Vspn gain range to the spin motor control circuit 272 through lines 306-310. The signals are received by the spin motor circuit which contains essentially the same components, summation circuit 312, op-amp 314, driver circuit 316 and current sensor 318, as the voice coil circuit 270. The summing circuit sums the Vspin( ) signals as described above. Like the voice coil signals, the offset signal provides a bias voltage and the other signals provide an adjustment of the bias voltage. The driver circuit 316 is connected to the windings of the spin motor through pins A, B and C on lines 320-324, respectively. The driver circuit 316 is controlled by spindle control logic 326 which sequentially enables the proper combination of drivers of the output lines A, B and C after receiving a commutation advance signal provided by the controller chip 92 on the Vcomm line 328. Each time a commutation advance signal Vcomm is provided, the control logic 326 sequentially enables the correct drivers, so that a current is provided to the spin motor in the proper combination of lines A, B or C.

The spin motor control circuit 272 has a back emf sensor 330 connected to the lines A, B and C and the center tap (CT) of the motor on line 332. The sensor 330 provides a back emf signal to a comparator 334 which compares the signal to a reference voltage. The comparator 334 provides a Vphase signal to the controller chip 92 on line 336. The controller chip 92 utilizes the Vphase signal to commutate the spin motor 20 through the Vcomm line 328. In the preferred embodiment, the driver circuit 316 has additional lines SpnGa, SpnGb and SpnGc which can be connected to additional drivers to increase the current level provided to the motor. This feature allows the servo chip 96 to be used in disk drives which contain additional disk that require higher rotating torque.

The servo chip 96 has an analog multiplexer 338 which receives various input signals. The signals are multiplexed to an analog to digital (Adc) converter 340 which utilizes the digital to analog circuits of the Dac converter 276. The Adc includes a comparator 342, and a serial approximation register (SAR) 344 which generates a series of 8-bit data strings.

In operation, the multiplexer 338 provides an analog signal to the comparator 342. The SAR 344 generates successive 8 bit words that are sent to the Ad DAC port 284 which converts the word to an analog comparator signal. The analog comparator signal is compared with the analog signal from the multiplexer 338. The first word has the most significant bit set to 1 and all other bits set to 0. If the most significant bit is greater than the analog signal, then a bit 1 is provided to the serial port 274. The SAR 344 generates the next 8 bit word which is again converted to an analog signal and compared by the comparator 342. The new word has the next least significant bit set to 1. This routine is

continued until 8 bits are provide to the serial port 274 to define the amplitude of the analog signal. The serial port 274 then sends the bits to the controller chip 92 through the serial line 304.

The multiplexer 338 receives input signals Vbemf and Vispn from the back emf sensor 330 and current sensor 318 on lines 346 and 348, respectively. A-B and C-D servo signals from the R/W chip 94 are provided to the multiplexer 338 through lines 350 and 352. The output signal Vivcm of the voice coil current sensor 304 is provided to the multiplexer 338 on line 354. These feedback signals are transmitted to the controller chip 92 through the Adc 340 and the serial port 274.

The voice coil control circuit 270 positions the heads 58 relative to the disk in response to commands from the controller chip 92. The controller chip 92 and control circuit 270 move the actuator pursuant to either a seek routine or a servo routine. In a seek routine the heads 58 are moved from a first track location on the disk to a second track location on the disk. The servo routine is used to maintain the transducers 58 on the centerlines of the tracks.

In the preferred embodiment, the disk 18 contains embedded servo information. Figure 11 shows a typical sector on a track of a disk. Each sector initially contains a servo field followed by an ID field. The ID field includes a header address that identifies the sector. The ID field is followed by a data field and error correction code information. The ECC field is followed by another ID field which identifies a subsequent data field D1 that contains a fraction of the data of data field D0.

The servo field initially contains a write to read field and than an automatic gain control (AGC) field that is followed by a period of no data (DC gap). At the end of the DC gap is a sync pulse. The servo field also includes a gray code to identify the particular cylinder (tracks) of the

sector and a number of servo bursts A, B, C and D. Servo bursts A and B have an outer edge at the centerline of the track. Servo burst C is centrally located on the centerline of the track for even numbered tracks. Servo burst D has a bottom edge located at the top edge of servo burst C. The position of the transducer relative to the centerline of the track can be determined by reading the amplitudes of servo bursts A-D. The AGC field is used to set the reference voltage value of the servo bursts.

The sync pulse is identified as the first voltage transition that is sensed after a predetermined number of clock cycles having no transitions after the AGC field. For example, after the transducer senses the AGC field, three clock cycles may occur without any voltage transitions, before detection of the sync pulse. As an alternate scheme, the beginning of the gray code may provide a voltage transition which signifies the sync pulse.

Figure 12 shows a schematic of the controller chip 92 which contains a core microprocessor 360. In the preferred embodiment, the core is a modified version of a processor sold by Texas Instruments Inc. ("TI") under the part designation DSP TMS320C25. The processor 360 operates with less instruction sets than a conventional hard disk drive controller such as the controller chip sold by Intel Corp. under the family designation 80C196. The decrease in instruction sets results in less memory access request. The processor block 360 includes RAM memory (not shown). Conventional RAM devices operate with a 5.0 V nominal power supply. It is desirable to provide a hard disk drive that will run on 3.3 V nominal, a voltage level that is commonly used in portable laptop computers. Conventional RAM devices respond to processor memory access request at a slower speed when operating at 3.3 V, than when the RAM device is operating at 5.0 V. The slower RAM speed degrades the

performance of the processor. Utilizing a processor which requires fewer memory access request for a given function provides a system that can operate on 3.3 V without appreciably affecting the performance of the processor.

The DSP microprocessor has two separate internal busses (not shown) for transferring instructions and data. The dual bus architecture allows the processor to execute fetching, decoding, reading and execution routines in parallel. The pipeline feature of the DSP significantly increases the performance of the processor. The DSP processor has on board memory that functions as both registers and a RAM device.

The controller chip also has supporting "on-chip" hardware coupled to the processor 360. The supporting hardware includes a bi-directional 16 bit synchronous serial port 362 that is coupled to the servo 96 and R/W chips 94 through the serial lines 204 and 206. The serial port 362 is also connected to the processor 360 through bus 364. The serial port 362 contains registers that provide a buffer between the processor 360 and the chips 94 and 96. The port 362 also generates chip select signals for the R/W chip 94 and the servo chip 96 in response to addresses provided by the processor 360. The serial port 362 is connected to a register file 366.

The controller chip 96 has a state machine 368 which contains a gray code circuit 370, servo strobe circuit 372, burst demod circuit 374, automatic gain control (AGC) circuit 376 and a write disable circuit 378. The burst demod 374 controls the operation of the other circuits through lines 380. The demod circuit 374 is connected to a timer circuit 382 through line 384. Both the gray code circuit 370 and the

burst demod circuit 376 are connected to a raw data line 328 to receive raw data from the R/W chip 94.

The timer circuit 382 has a number of timers, one of which "times out" prior to the servo burst of a sector. When the pre-servo timer times out, the timer circuit 382 provides an AGC signal to the AGC circuit 376 on line 386. The AGC signal enables the AGC circuit 376, which enables the automatic gain control circuitry of the R/W chip 94 through line 388. The timer circuit 382 also provides a search signal to the burst demod 374 on line 384. The search signal enables the burst demod 374 to begin searching for the sync pulse within the servo burst of the sector. Upon receipt of the search signal, the burst demod 374 enables an internal sync mark field when no signal transitions (from the raw data line 228) occur within a predetermined number of clock cycles. If a transition occurs within a predetermined time after the field is enabled, the burst demod 374 generates a H sector signal which signifies the detection of a sync pulse.

The H sector signal is provided to a Z sector circuit 392 on line 394 and to the processor 360 on line 390. The H sector signal from the demod circuit 374 sets a pair of timers within the z sector circuit 392. The z sector circuit 392 provides a z sector signal to the data manager 98 and R/W 94 chips on line 258 when a timer "times out". There is preferably a timer for each data field Do and D1. The z sector circuit 392 only generates a z sector signal if the circuit 392 has been enabled by the processor 360 through enable line 396.

The burst demod 374 circuit enables the gray code circuit 372 after detection of the sync pulse. The gray code circuit 372 contains shift registers which store the gray code provided on the raw data line 228. The gray code is then stored in a dedicated address in the register file 366 through bus 398, for subsequent retrieval by the processor 360. The detection of the sync pulse also sets an internal timer in the burst demod 374. When the timer times out the burst demod 374 disables the gray code circuit 370 and enables the servo strobe circuit 372. The servo strobe circuit 372 sends out a series of two bit signals on line 399, to enable internal circuits within the R/W chip 94 to provide the A-B and C-D signals to the servo chip 96. The A-B and C-D signals are then sent to the register file 366 through the Adc converter 340 and the serial ports 374 and 362.

When the timer 382 generates the search signal, the burst demod 374 also enables the write disable circuit 378. The write enable line 252 from the data manager chip 98 is routed to the preamp 100 through the write disable circuit 378, so that the write disable circuit 378 can disable the write signal and prevent writing of data onto the disk. The write disable circuit 378 disables the write signal during the servo burst to prevent any writing of data onto the servo field. The write disable circuit 378 is also enabled by a shock sensor (not shown) through line 400. The shock sensor provides an enabling signal when the disk drive is accelerated beyond a predetermined value. The shock sensor and write disable circuit 378 prevent writing of data when the drive is subjected to an excessive shock.

The controller chip 92 contains a interface module 402 that is coupled to the processor 360 and register file 366 through busses 404 and 406. The interface module 402 provides a memory map between the

processor 260 and the register file 366. The modular interface 402 allows the supporting on-chip hardware to be coupled to different types of processors. The module 402 is coupled to a decoder 408 through line 410. The decoder 408 decodes addresses provided by the processor 360 to enable chip select control signals ROM and DM that select either the ROM 102 or data manager chip 98 through lines 412 and 256.

The controller chip 92 contains an oscillator 412 which receives a clock signal from a system clock on line 414. The oscillator 412 provides a clocking signal to clock circuit 416 on line 418. The clock circuit 416 provides clocking signals for the R/W chip 94, data manager chip 98, servo chip 96, microprocessor 360 and the support hardware of the

controller 92 on lines 420-428. In the preferred embodiment, the oscillator 412 generates a 30 MHz clock signal. The oscillator 412 is connected to a sleep circuit 430 through line 432. The sleep circuit 430 disables the oscillator 412 when an INTb signal is provided to the circuit 430 on line 434. The INTb signal is typically provided by the host processor (not shown). The host processor typically provides the sleep signal when a disk access request has not been generated for a predetermined time interval, by setting a bit within a register of the register file 366.

The support hardware also contains a spin circuit 436 which is connected to the servo chip 96 through the Vphase and Vcomm lines 336 and 328. The spin circuit 436 is connected to both the register file 366 and the processor 360 by lines 438 and 440. When the spin circuit 336 receives a Vphase signal, the circuit 436 provides an interrupt signal to the processor 360 on the SPININT line 440. The Vphase signal also sets an internal Vcomm timer within the spin circuit 436. Additionally,

the spin block circuit 436 also reads a dedicated register(s) in the register file 366. The contents of the register file 366 provide a time interval between when the spin circuit 436 receives the Vphase signal and when the circuit 436 generates the Vcomm signal for the spin control circuit 272 of the servo module 96.

The processor 360 has a continuously running internal timer (not shown). When the processor 360 acknowledges the SPININT pin 440 and the line is activated by the spin circuit 436, the processor 360 reads the time of the internal timer and the value of the Vcomm timer in the spin circuit 436. The Vcomm timer value signifies the amount of time elapsed between the reception of the Vphase signal and the acknowledgment by the processor 360 of the SPININT interrupt signal. The Vcomm time is subtracted from the time value of the internal processor timer. The resulting time is compared to a theoretical time to determine if there is an error in the speed of the spin motor 20. The spin motor 20 typically has 12 poles wherein there are created 36 Vphase signals per revolution.

In the alternative, the speed of the spin motor 20 can be measured by counting the number of pulses between the end of the AGC field and the beginning of the DC gap. In this embodiment, a time field of microseconds is created between the end of the AGC field and the beginning of the DC gap of each disk sector. This time field contains a predetermined number of pulses. After a sync pulse is detected, a spin timer 383 is set. The spin timer 383 times out at the end of the AGC field of the next sector. The timer 383 enables a counter 375 in the burst demod 374 by activating pin 385. The counter 375 counts the number of pulse detected by the transducer. The number of pulses is then stored in the register file 366. After the processor 360 completes

the voice coil 80 routine, the processor 360 retrieves the number of pulses counted by the counter 375 and compares the count to a nominal value. If the count is different than the nominal value, the processor 360 generates a digital command that is sent to the servo module 96 to either speed up or slow down the spin motor 20. The processor 360 also changes the timer 383 so that the timer 383 will time out at exactly the end of the AGC field of the next sector. In this manner the processor insures that the counter 375 always begins counting at the end of the AGC field, thereby insuring an accurate spin motor control error value.

The processor acknowledges the interrupt signals H sector, SPININT, HOSTINT and DISKINT in accordance with a hierarchy that responds to the H sector interrupt first (voice coil subtask), SPININT interrupt signal second (spin motor subtask) and then either the HOSTINT or DISKINT interrupt signals (data subtask). Accordingly, when the burst demod 374 detects a sync pulse signal, a pulse is sent to the processor 360 on the H sector line 390. Upon receiving the H sector signal the processor 360 may initiate a servo routine. The processor 360 initially reads the registers within the register file 366 that contain the gray code information. The processor 360 determines the cylinder location of the head 58 and then writes data containing voice coil control information to the serial port 362. The serial port 362 then sends the data to the servo chip 96. If the gray code corresponds to a desired track location (eg. for a read or write of data from the disk) the processor enables the Z sector circuit 392 through the enable line 396.

After the gray code is read, the processor 360 contain the A-B and C-D servo information. The servo burst information is processed by the processor 360 to determine the location of the head 58 relative to the centerline of the track. The processor 360 then writes data to the serial

port 362 for subsequent transmittal to the servo chip 96. If the processor 360 is in a seek routine the servo information is not fetched from the register file 366.

After the servo routine, the processor acknowledges any SPININT signal from the spin circuit 436 and computes the difference between the actual motor speed and the theoretical motor speed. In the preferred embodiment, the processor stores the error values of each sector and computes a mean spin motor error each revolution of the disk. The processor 360 then writes control data to the servo chip 96 through the serial port 362 to control the speed of the spin motor 20, typically during an index sector that occurs once per revolution of the disk 18.

After the spin routine the processor 360 acknowledges any HOSTINT or DISKINT interrupt signals. If the HOSTINT pin is active the processor 360 retrieves the logical addresses stored in the buffer 232 of the data manager 98. The processor 360 converts the logical addresses to actual sector locations on the disk. The processor 360 initiates a seek routine if the heads 58 are not above the desired track. Once the head reaches a desired sector of the head, the controller chip 92 provides the Z sector signal to the data manager 98 which then transfer, data with the R/W chip 94. An active DISKINT signal indicates the end of a data transfer or an error in the process of transferring data. The register file 366 typically has a error bit that is set when an error has occurred. The processor 360 reads the error bit and performs an error correction routine if there is an error.

Figure 13 shows a schematic of the R/W chip 94. The R/W chip 94 contains a bi-directional 16 bit synchronous serial port 450 that is coupled to the serial port 362 of the controller chip 92. The serial port 450 is coupled to a controller circuit 452 through line 454. The

controller 452 is connected to a multiplexer 456 through line 458. The multiplexer 456 multiplexes the various lines of the heads in accordance with instructions received from the controller chip 92 through the serial port 450 and the controller circuit 452.

The R/W chip 94 has a data port 460 that is coupled to a detection circuit 462 through bus 464. The detection circuit 462 is coupled to the multiplexer 456 and controller circuit 452 by lines 466 and 468, respectively. The circuit 462 detects transitions in the voltage provided by the transducers and provides a digital output to the data port 246 through line 370. The R/W chip 94 has a decoder 472 connected to the servo strobe circuit 372 of the controller chip 92. The decoder 472 is coupled to a servo burst circuit 474 through line 476. The decoder 472 enables the servo burst circuit 474 in response to pulses received from the servo strobe. The servo burst circuit 474 provides the servo signals A-B and C-D to the servo chip 96 on lines 350 and 352.

In the preferred embodiment, the R/W chip 94 is an integrated circuit similar to a product sold by Silicon Systems Inc. ("SSI") under the part designation 32P4730. The pre-amplifier chip is preferably a conventional integrated circuit sold by TI under the part designation TLV2234.

Figures 14a-g provide a flowchart of a typical operating sequence of the disk drive. In processing block 500 the host 212 has provided the disk drive with a request to write data to logical addresses A0-A63. The other condition is a head position at the end of a sector of the disk. In block 502 the data manager 98 stores the physical addresses and data from the host into the RAM buffer 232 and activates the HOSTINT interrupt signal. As the disk spins the servo field of a sector the approaches the head. In block 404, the search timer of the timer circuit

382 times out and provides the search signal and H sector signal to the burst demod circuit 374 and processor 360, respectively. The AGC circuit is also enabled to provide a control signal to the R/W chip 94 to initiate automatic gain control in block 506.

Along a parallel path the spin motor control circuit of the servo chip 96 generates a Vphase signal that is received by the spin circuit 436 of the controller chip 92 in block 508. The spin circuit 436 generates a SPININT interrupt signal for the processor 360 and initiates an internal timer in block 510. The spin circuit 436 also accesses the register file 366 to determine the time interval between the Vphase signal and the generation of the Vcomm signal. In block 512, the spin circuit 336 generates the Vcomm signal after the predetermined time interval.

After block 506, the burst demod circuit 374 reads raw data from the R/W chip 94 and enables the gray code circuit 370 upon the detection of the sync pulse in block 514. In block 516, the burst demod circuit 374 disables the gray code circuit 370 and enables the servo strobe circuit 372, which provides servo strobe pulses to the R/W chip 94. The R/W chip 94 provides the servo signals A-B and C-D to the servo chip 96 in block 518. The servo chip 96 converts the analog servo signals to digital data strings, which are transmitted to the controller chip 92 and stored in the register file 366 in blocks 518 and 520. The ID field of the servo burst is subsequently stored in the register file 366 in block 522.

In processing block 524, the processor 360 acknowledges the H sector interrupt signal. In decision block 526, the processor 360 determines whether the disk drive is in a seek routine. If the drive is in a seek routine, the processor reads the contents of the register file 366 which contain the gray code information, in processing block 528. In

blocks 530-531, the processor 360 compares the gray code data with a desired track location, computes a seek current and generates a write command which is transmitted to the servo chip 96 through the serial ports 274 and 362. If the disk is in a servo routine the processor 360 reads the contents of the register file 366 which contain the servo burst information in processing block 534. The servo burst information is used to determine whether the heads 58 are on the centerline of the tracks and to calculate a voice coil correction command. in processing block 537-8. The processor 360 then generates a write command containing voice coil control data to the servo chip 96 through the serial ports in block 532. The digital voice coil control data is converted to analog signal by the Dac of the servo chip and provided to the voice coil to move the actuator arm and heads of the assembly.

In block 538, the processor 260 acknowledges the SPININT interrupt signal, if one exists. The processor 360 reads the processor internal timer and the Vcomm timer of the spin circuit 436 to compute the time interval between the Vphase signals in processing block 540 and adds the time interval to an accumulated time. In accordance with decision block 542, if the number of interrupts equals one revolution, a spin correction command is computed and the processor 360 generates a write command to the servo chip 96 through the serial ports in processing blocks 544 and 546. The spin correction command is calculated from the difference between a reference time and the accumulated time. The accumulative time is reset to zero in block 547. A new time interval value is also stored in the register file 366 for subsequent use by the spin circuit 436. The write command is transmitted to the servo chip which converts the digital string into analog signals which are provided to the spin motor control circuit. If

the number of interrupts does no equal a revolution, the accumulative time is stored by the processor 360 in block 548.

In processing block 550, the processor 360 acknowledges the HOSTINT interrupt signal from the data manager 98. The processor 360 then retrieves the physical addresses from the buffer 332 within the data manager 98 and the ID field data in the register file 366 in processing block 552. In block 554, the processor 360 converts the logical addresses to actual sector locations. In accordance with decision block 556, if the heads 58 are not above the actual sector location, the processor 360 initiates a seek routine and generates a write command to the servo chip 96 to move the voice coil in processor block 558. The actuator arm is moved until the head is in the proper track. The processor 360 continually reads gray code until the actual sector location is adjacent to the head. In block 560, the processor 360 enables the Z sector circuit 392 which activates the Z sector pin after the servo field of the sector. The activation of the Z sector pin initiates a write of data from the data manager 98 to the R/W chip 94, which writes the data into the data field of the sector in processing block 562.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. An electronic architecture for a hard disk drive that can be coupled to an external device, comprising:

a disk that stores information;

a spin motor that rotates said disk;

an actuator arm assembly that can transfer information with said disk;

a data manager chip that transfers information with the external device;

a read/write chip that transfers information between said actuator arm assembly and said data manager chip;

a servo module chip that controls said actuator arm assembly and said spin motor; and,

a controller chip that controls said data manager chip, said read/write chip and said servo module chip, said controller chip including a core processor which has a dual bus architecture that can execute fetching, decoding, reading and executing task in parallel.

2. The architecture as recited in claim 1, wherein said controller chip provides digital commands to said servo module chip to control said spin motor and said actuator arm assembly.

3. The architecture as recited in claim 2, wherein said servo module chip contains a voice coil control circuit that provides an analog voice coil control signal to a voice coil of said actuator arm assembly, and a spin motor control circuit that provides an analog spin motor control signal to said spin motor.

4. The architecture as recited in claim 3, wherein said servo module chip includes a digital to analog converter to convert said digital commands from said controller chip to analog input signals that are provided to said voice coil and spin motor control circuits.

5. The architecture as recited in claim 1, wherein said servo module chip contains an analog to digital converter to convert analog feedback signals provided to said servo module chip from said read/write chip and convert said analog feedback signals to digital signals that are transmitted to said controller chip.

6. The architecture as recited in claim 5, wherein said analog feedback signals include servo burst signals.

7. The architecture as recited in claim 1, wherein said controller chip includes a burst demod circuit that senses a sync pulse within a sector of said disk.

8. The architecture as recited in claim 1, wherein said controller chip includes a gray code circuit that stores gray code information from a sector of said disk.

9. The architecture as recited in claim 1, wherein said controller chip includes a servo circuit that stores servo burst signals from a sector of said disk.

10. The architecture as recited in claim 1, wherein said controller chip includes a spin motor circuit that commutates said spin motor.

11. The architecture as recited in claim 10, wherein said spin motor circuit includes timer circuits coupled to said core processor to control a speed of said disk.

12. The architecture as recited in claim 1, wherein said controller chip is coupled to said servo module chip by a serial line and a synchronous serial bit port in each chip.

13. The architecture as recited in claim 1, wherein said chips operate with 3.3 V power.

14. An electronic architecture for a hard disk drive that can be coupled to an external device, comprising:

a disk that stores information;

a spin motor that rotates said disk;

an actuator arm assembly that can transfer information with said disk and that has a voice coil that can move a transducer relative to said disk;

a data manager chip that transfers information with the external device;

a read/write chip that transfers information between said transducer and said data manager chip;

a servo module chip that contains a voice coil control circuit that controls said voice coil and a spin motor control circuit that controls said spin motor, said servo module chip further having a digital to analog

converter for converting digital command signals to analog input signals that are provided to said voice coil and said spin motor control circuit; and,

a controller chip that controls said data manager chip, said read/write chip and said servo module chip, said controller chip being capable of providing digital command signals to said servo module chip to control said spin motor and said actuator arm assembly.

15. The architecture as recited in claim 14, wherein said controller chip includes a core processor which has a dual bus architecture that can execute fetching, decoding, reading and executing task in parallel.

16. The architecture as recited in claim 15, wherein said servo module chip contains an analog to digital converter to convert analog feedback signals provided to said servo module chip from said read/write chip and convert said analog feedback signals to digital signals that are transmitted to said controller chip.

17. The architecture as recited in claim 16, wherein said controller chip includes a burst demod circuit that senses a sync pulse within a sector of said disk.

18. The architecture as recited in claim 17, wherein said controller chip includes a gray code circuit that stores gray code information from a sector of said disk.

19. The architecture as recited in claim 18, wherein said controller chip includes a servo circuit that stores servo burst signals from a sector of said disk.

20. The architecture as recited in claim 19, wherein said controller chip includes a spin motor circuit that commutates said spin motor.

21. The architecture as recited in claim 20, wherein said spin motor circuit includes timer circuits coupled to said core processor to control a speed of said disk.

22. The architecture as recited in claim 21, wherein said controller chip is coupled to said servo module chip by a serial line and a synchronous serial bit port in each chip.

23. The architecture as recited in claim 22, wherein said chips operate with 3.3 V power.

24. The architecture as recited in claim 23, wherein said analog feedback signals include servo burst signals.

25. An electronic architecture for a hard disk drive that can be coupled to an external device, comprising:

disk means for storing information;

spin motor means for rotating said disk means;

actuator arm assembly means for transferring information with said disk means;

data manager means for transferring information with the external device;

read/write chip means for transferring information between said actuator arm assembly means and said data manager means;

servo module means for controlling said actuator arm assembly means and said spin motor means; and,

controller means for controlling said data manager means, said read/write means and said servo module means, said controller means includes core processing means having a dual bus architecture that can execute fetching, decoding, reading and executing task in parallel.

26. The architecture as recited in claim 25, wherein said controller means provides digital commands to said servo module means to control said spin motor means and said actuator arm assembly means.

27. The architecture as recited in claim 26, wherein said servo module means contains voice coil control circuit means for providing an analog voice coil control signal to a voice coil of said actuator arm assembly means and spin motor control circuit means for providing an analog spin motor control signal to said spin motor means.

28. The architecture as recited in claim 27, wherein said servo module means includes digital to analog converter means for converting said digital commands from said controller means to analog input signals that are provided to said voice coil and spin motor control circuits means.

29. The architecture as recited in claim 25, wherein said servo module means contains analog to digital converter means for converting analog feedback signals provided to said servo module means from said read/write means and converting said analog feedback signals to digital signals that are transmitted to said controller means.

30. The architecture as recited in claim 29, wherein said analog feedback signals include servo burst signals.

31. The architecture as recited in claim 25, wherein said controller means includes burst demod circuit means for sensing a sync pulse within a sector of said disk means.

32. The architecture as recited in claim 25, wherein said controller means includes gray code circuit means for storing gray code information from a sector of said disk means.

33. The architecture as recited in claim 25, wherein said controller means includes servo circuit means for storing servo burst signals from a sector of said disk means.

34. The architecture as recited in claim 25, wherein said controller means includes spin motor circuit means for commutating said spin motor means.

35. The architecture as recited in claim 34, wherein said spin motor circuit means includes timer circuit means coupled to said core processing means to control a speed of said disk means.

36. The architecture as recited in claim 25, wherein said controller means is coupled to said servo module means by a serial line and a pair of synchronous serial bit ports.

37. The architecture as recited in claim 25, wherein said controller means operates with 3.3 V power.

38. An electronic architecture for a hard disk drive that can be coupled to an external device, comprising:

disk means for storing information;

spin motor means for rotating said disk means;

actuator arm assembly means for transferring information with said disk means, said actuator arm assembly means including a voice coil that can move a transducer relative to said disk means;

data manager means for transferring information with the external device;

read/write means for transferring information between said transducer and said data manager means;

servo module means containing voice coil control circuit means for controlling said voice coil spin motor control circuit means for controlling said spin motor means, said servo module means further having digital to analog converter means for converting digital command signals to analog input signals that are provided to said voice coil and said spin motor control circuit means; and,

controller means for controlling said data manager means, said read/write means and said servo module means, said controller means being capable of providing digital command signals to said servo module

means to control said spin motor means and said actuator arm assembly means.

39. The architecture as recited in claim 38, wherein said controller means includes core processing means which has a dual bus architecture that can execute fetching, decoding, reading and executing task in parallel.

40. The architecture as recited in claim 39, wherein said servo module means contains analog to digital converter means for converting analog feedback signals provided to said servo module means from said read/write means and converting said analog feedback signals to digital signals that are transmitted to said controller means.

41. The architecture as recited in claim 40, wherein said controller means includes burst demod circuit means for sensing a sync pulse within a sector of said disk means.

42. The architecture as recited in claim 41, wherein said controller means includes gray code circuit means for storing a gray code information from a sector of said disk means.

43. The architecture as recited in claim 42, wherein said controller means includes servo circuit means for storing servo burst signals from a sector of said disk means.

44. The architecture as recited in claim 43, wherein said controller means includes spin motor circuit means for commutating said spin motor means.

45. The architecture as recited in claim 44, wherein said spin motor circuit means includes timer circuit means coupled to said core processing means to control a speed of said disk means.

46. The architecture as recited in claim 45, wherein said controller means is coupled to said servo module means by a serial line and a pair of synchronous serial bit ports.

47. The architecture as recited in claim 46, wherein said controller means operates with 3.3 V power.

48. The architecture as recited in claim 47, wherein said analog feedback signals include servo burst signals.

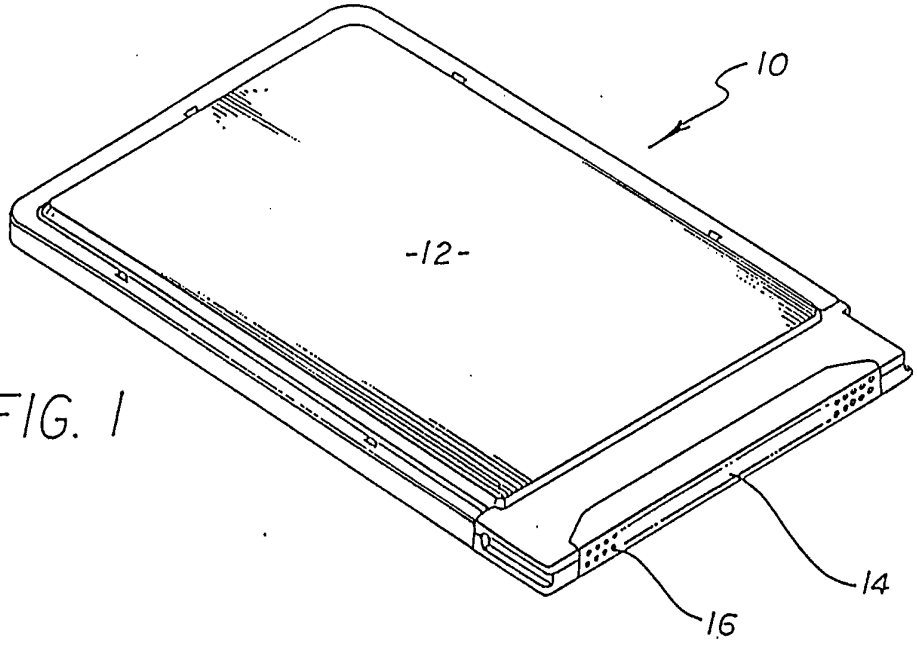


FIG. 1

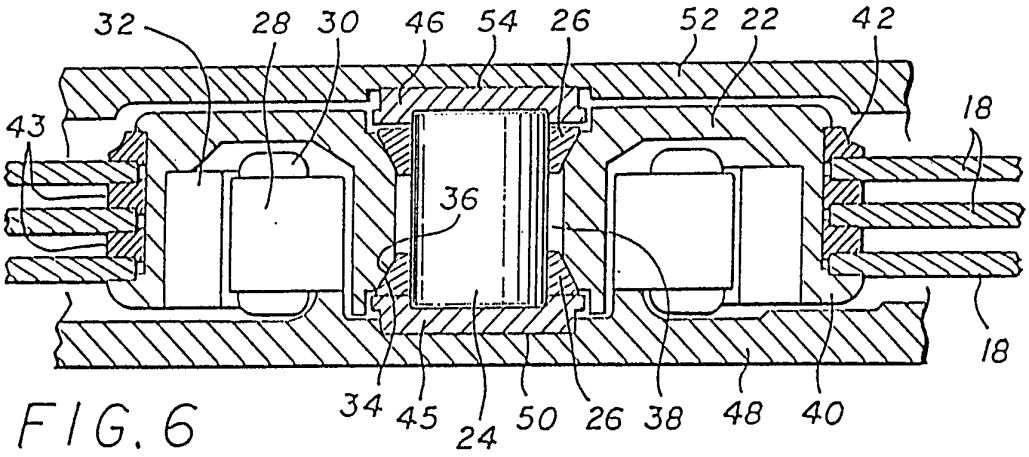


FIG. 6

FIG. 7

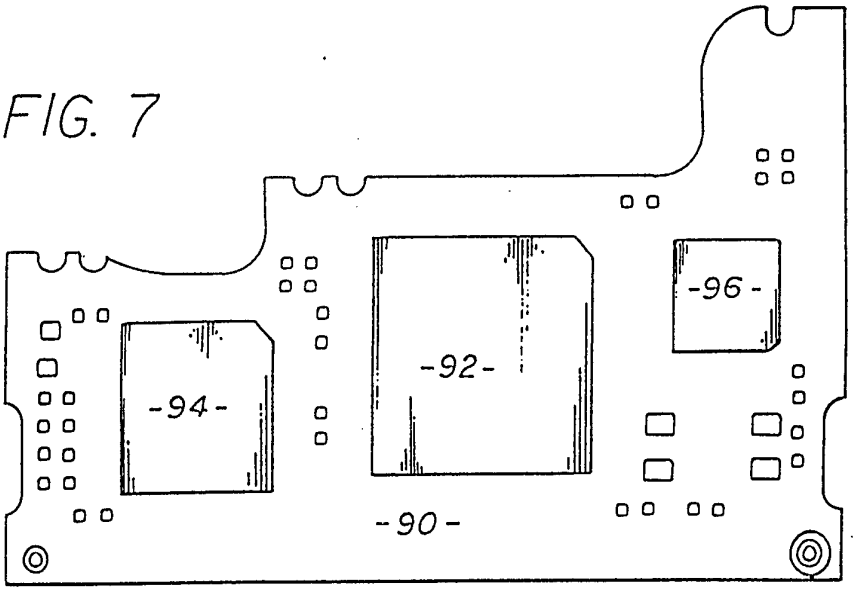


FIG. 2

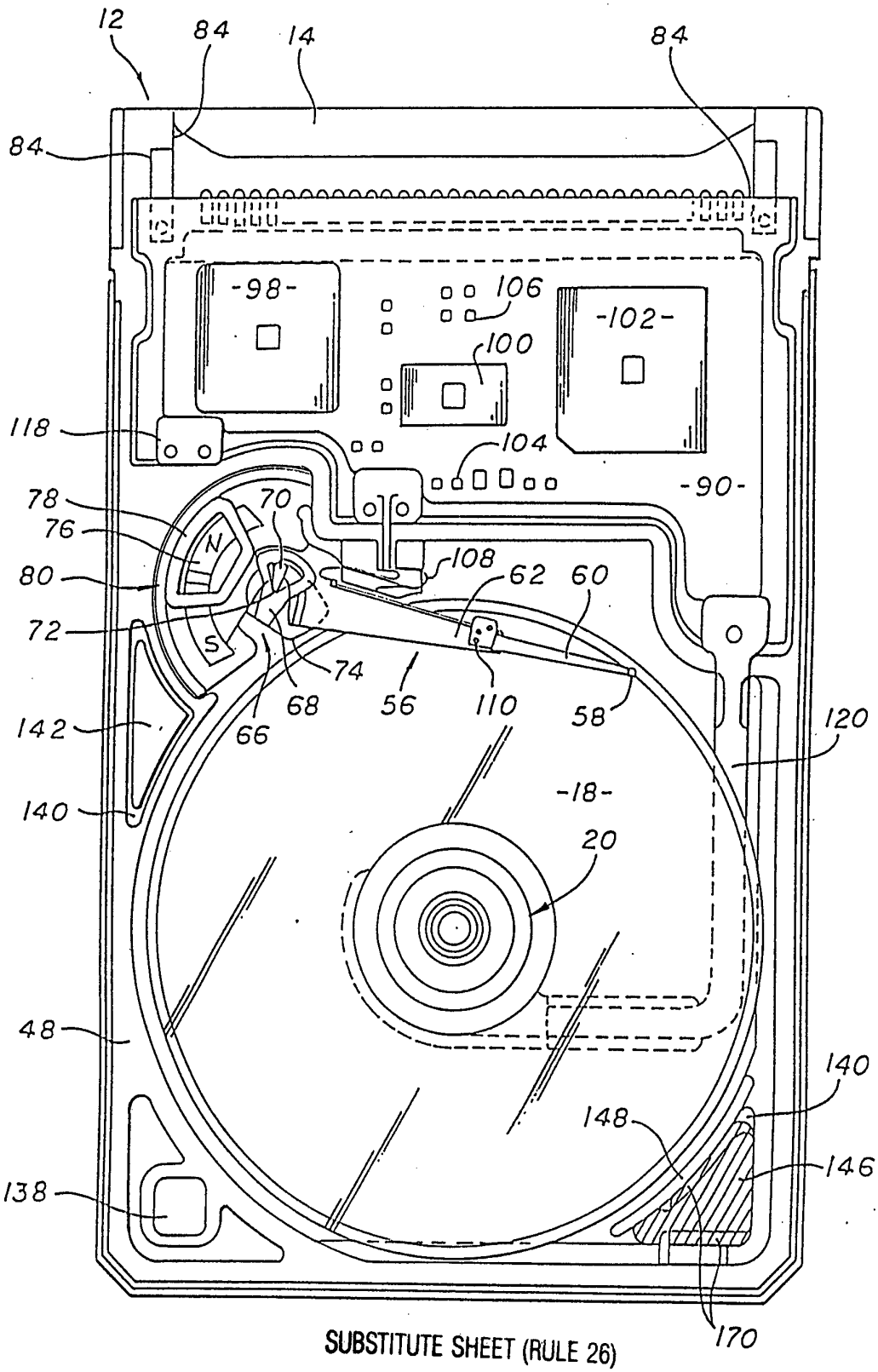
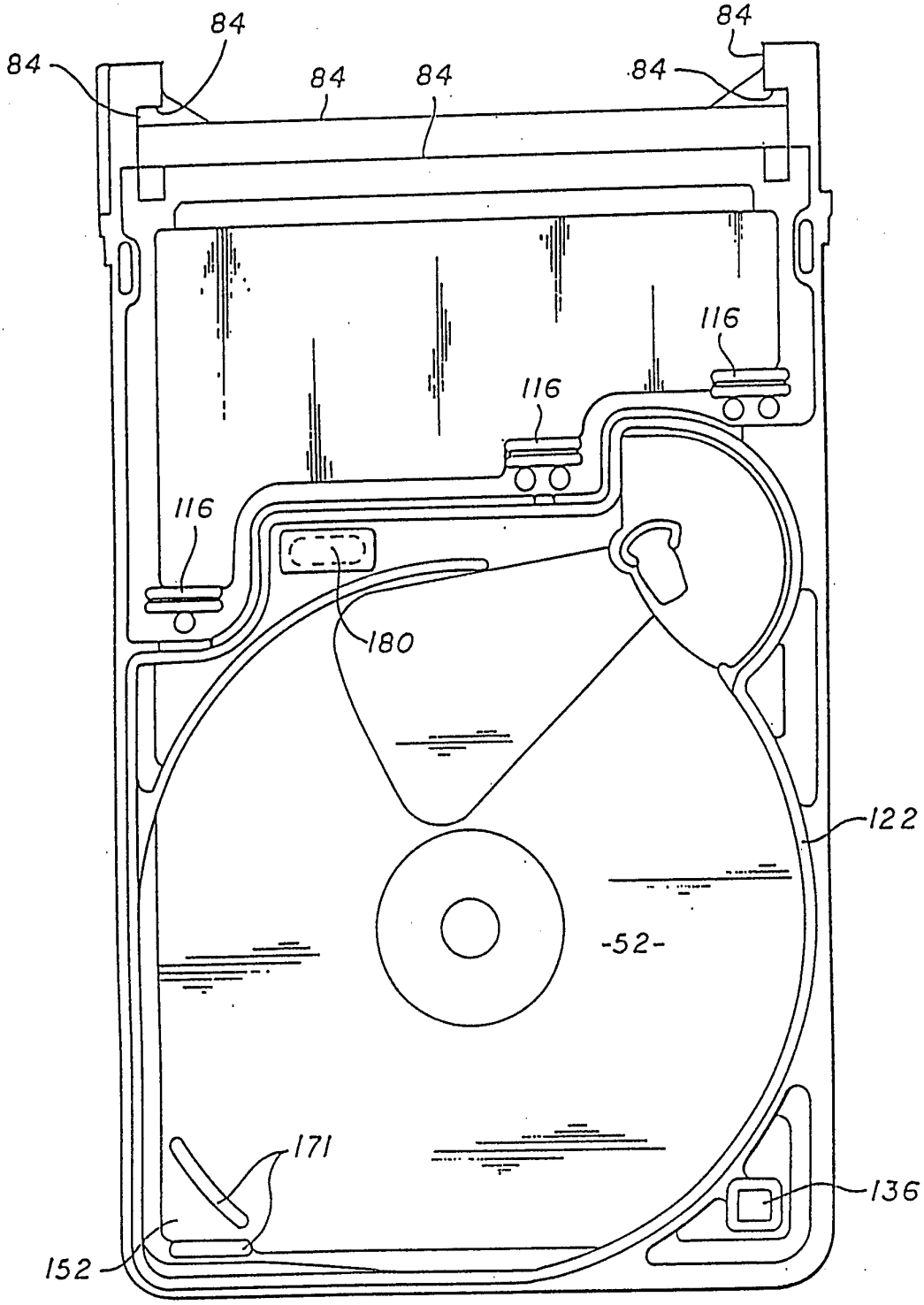

12
84
14
84
84
-98-
106
-102-
100
118
104
-90-
78
70
76
N
108
62
60
80
72
S
74
68
56
110
58
142
66
120
-18-
140
20
48
140
148
146
138
170

FIG. 3



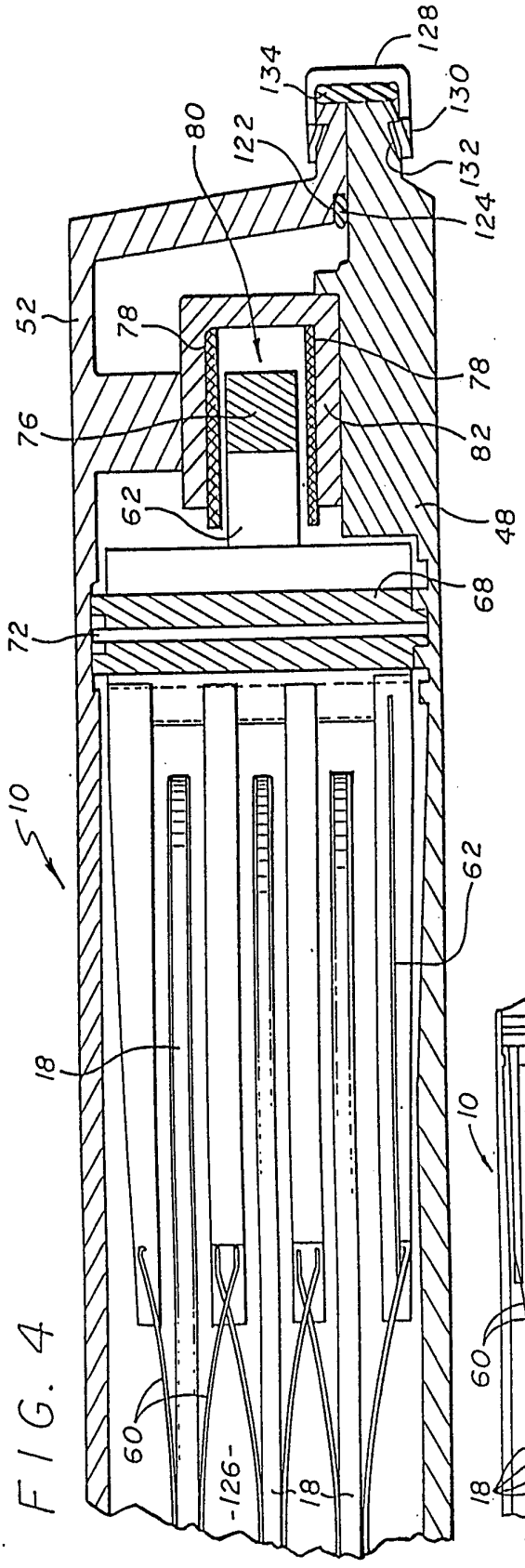


FIG. 4

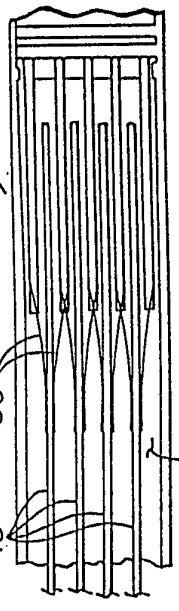


FIG. 4A

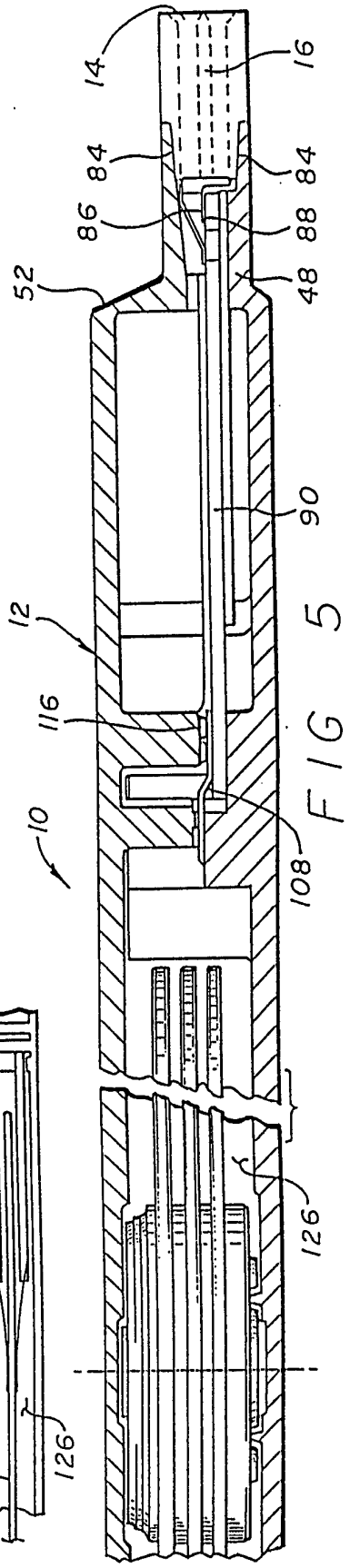


FIG 5

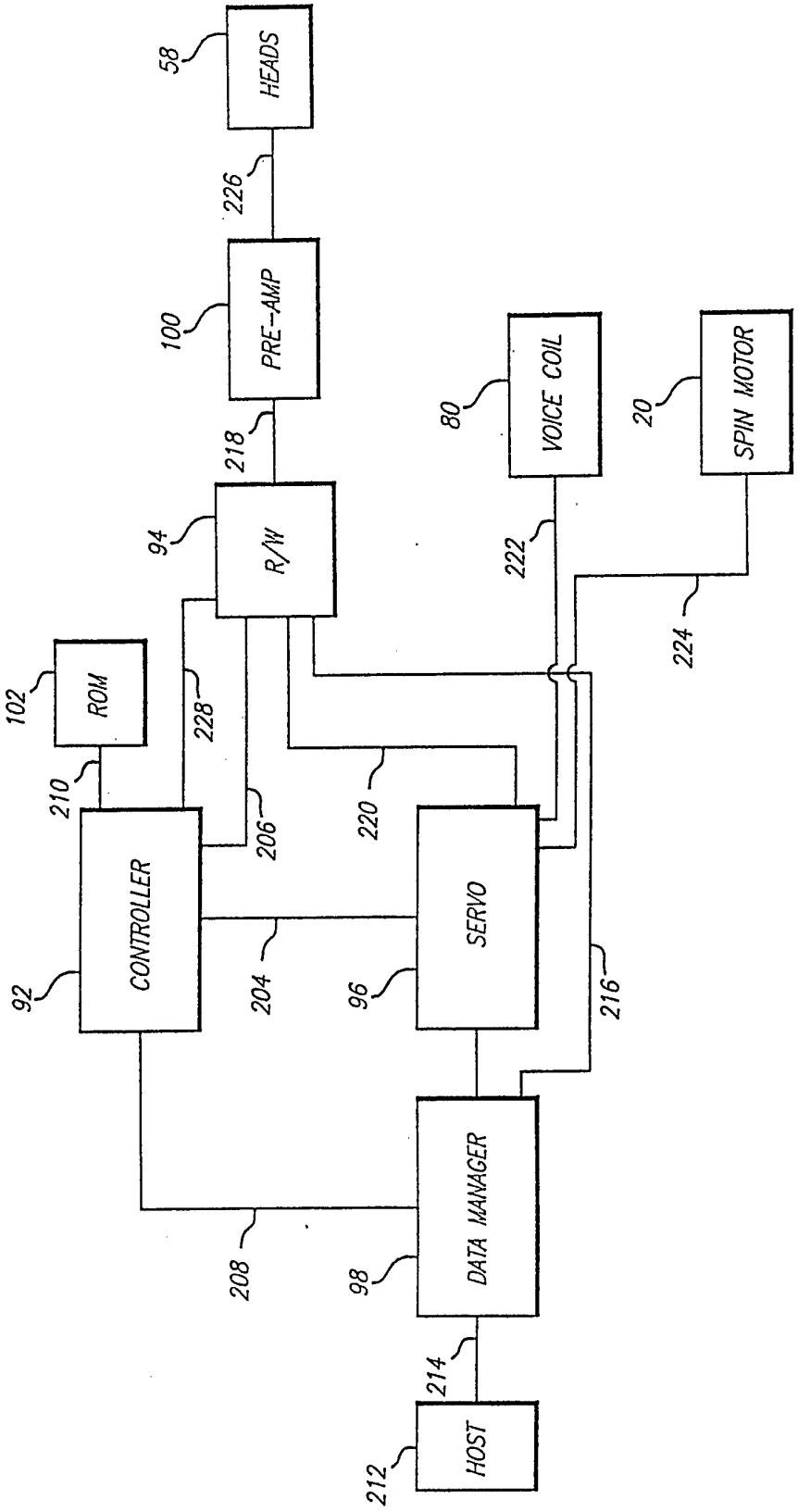

58
HEADS
226
100
PRE-AMP
218
80
VOICE COIL
20
SPIN MOTOR
94
R/W
222
224
102
ROM
228
210
206
220
CONTROLLER
SERVO
92
204
96
216
208
98
DATA MANAGER
214
212
HOST

FIG. 8

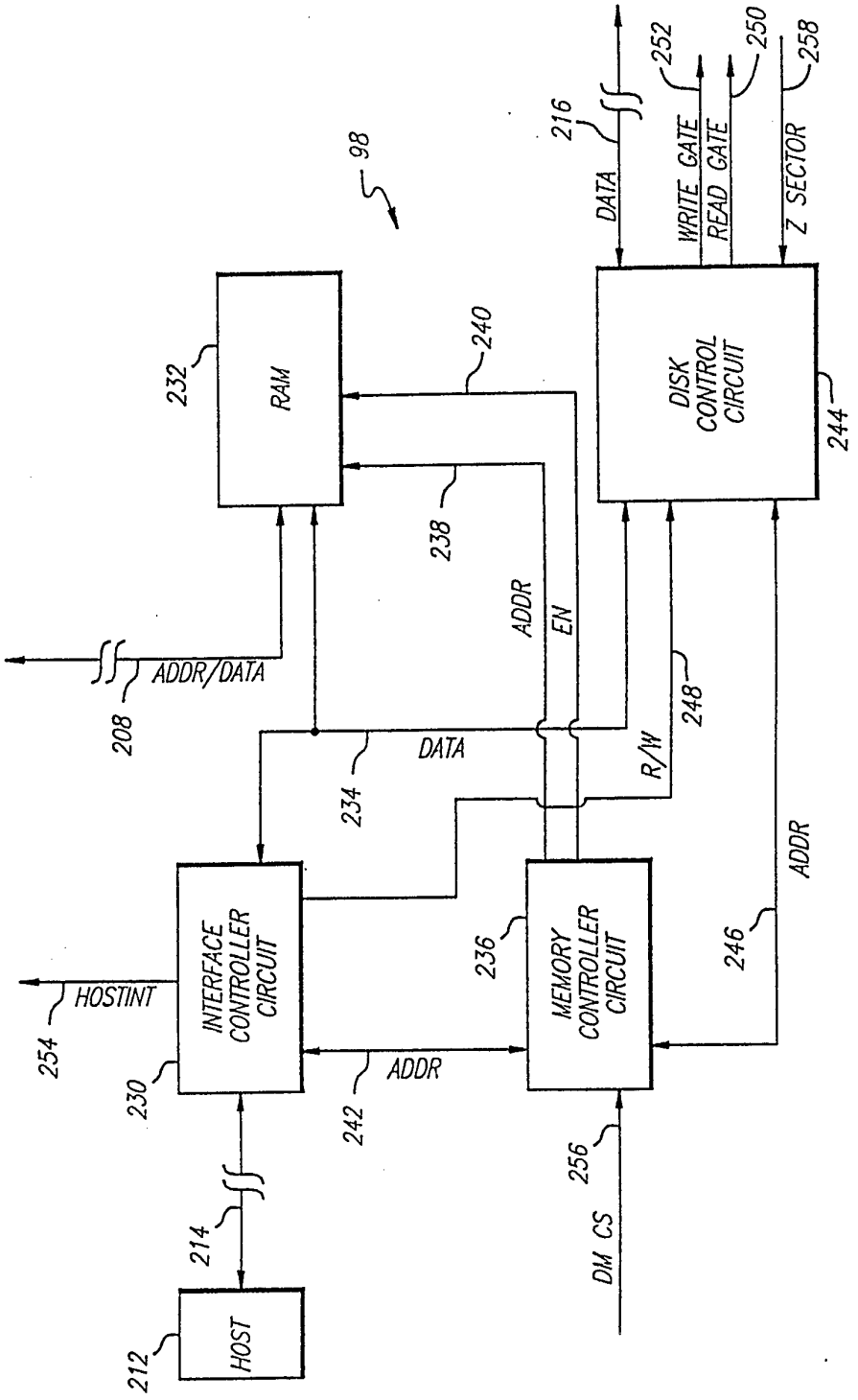

98
216
DATA
252
WRITE GATE
250
READ GATE
258
Z SECTOR
232
RAM
240
DISK CONTROL CIRCUIT
244
238
ADDR
EN
ADDR/DATA
208
DATA
234
R/W
248
INTERFACE CONTROLLER CIRCUIT
MEMORY CONTROLLER CIRCUIT
236
246
ADDR
HOSTINT
254
230
ADDR
242
256
DM CS
214
HOST
212

FIG. 9

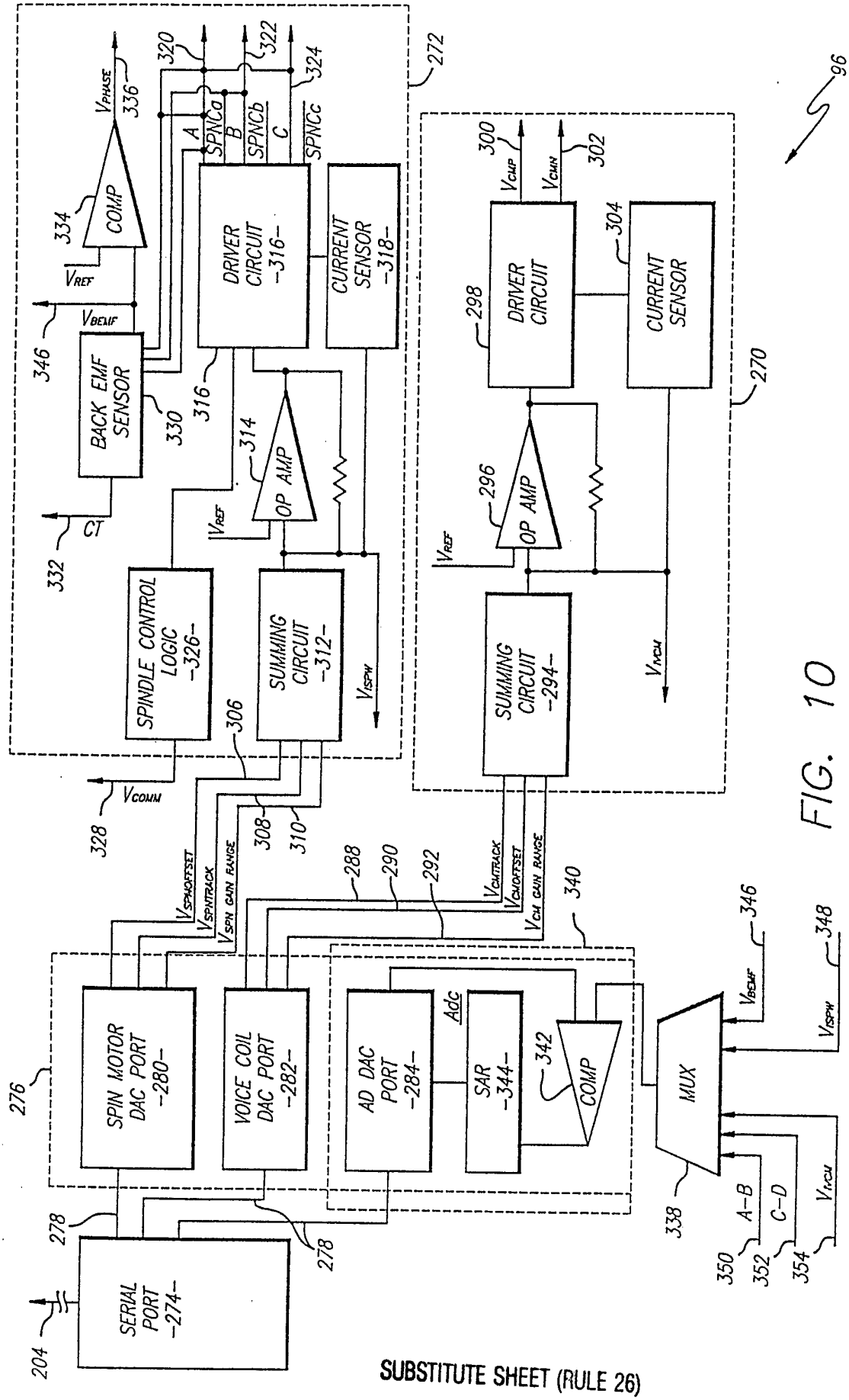

SERIAL PORT -274-
SPIN MOTOR DAC PORT -280-
VOICE COIL DAC PORT -282-
AD DAC PORT -284-
SAR -344-
COMP
MUX
SPINDLE CONTROL LOGIC -326-
SUMMING CIRCUIT -312-
OP AMP
BACK EMF SENSOR
DRIVER CIRCUIT -316-
CURRENT SENSOR -318-
COMP
DRIVER CIRCUIT
CURRENT SENSOR
OP AMP
SUMMING CIRCUIT -294-
A-B
C-D
A
B
C
SPNCa
SPNCb
SPNCc
CT
VREF
VBEMF
VPHASE
VCOMM
VISPW
VCMP
VCMN
VCMTRACK
VCMOFFSET
VCM GAIN RANGE
VSPNOFFSET
VSPNTRACK
VSPN GAIN RANGE
Adc
204
276
278
288
290
292
296
298
300
302
304
306
308
310
314
316
320
322
324
330
332
334
336
338
340
342
346
348
350
352
354
270
272
96

FIG. 10

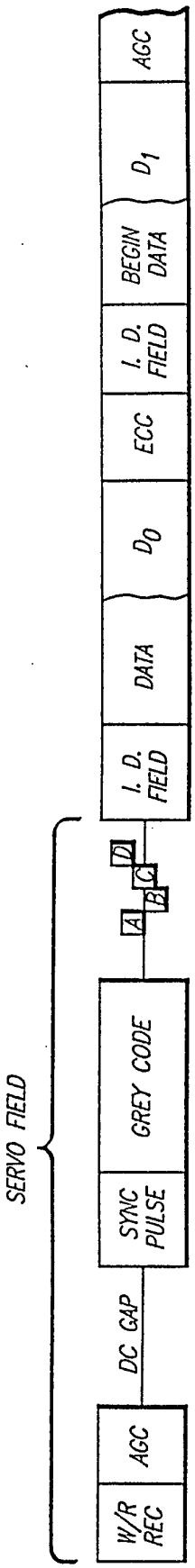

SERVO FIELD
W/R REC
AGC
DC GAP
SYNC PULSE
GREY CODE
A
B
C
D
I. D. FIELD
DATA
D_0
ECC
I. D. FIELD
BEGIN DATA
D_1
AGC

FIG. 11

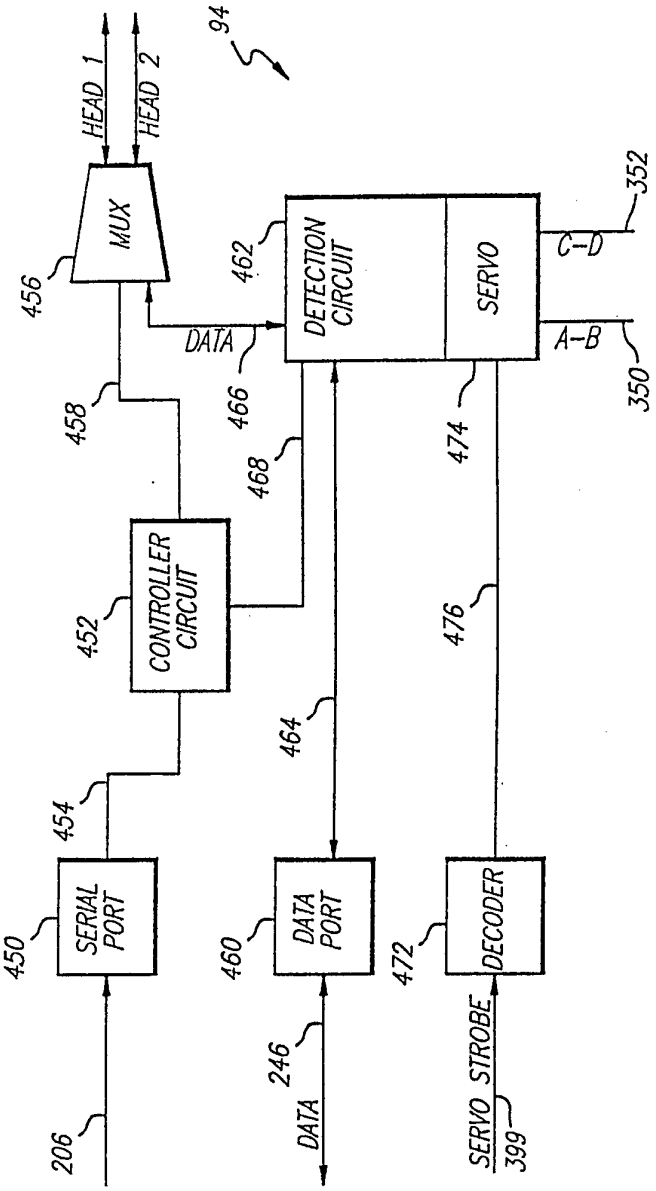

94
HEAD 1
HEAD 2
MUX
456
DETECTION CIRCUIT
462
SERVO
352
C-D
A-B
350
DATA
458
466
468
474
CONTROLLER CIRCUIT
452
476
464
454
SERIAL PORT
450
DATA PORT
460
DECODER
472
206
246
DATA
SERVO STROBE
399

FIG. 13

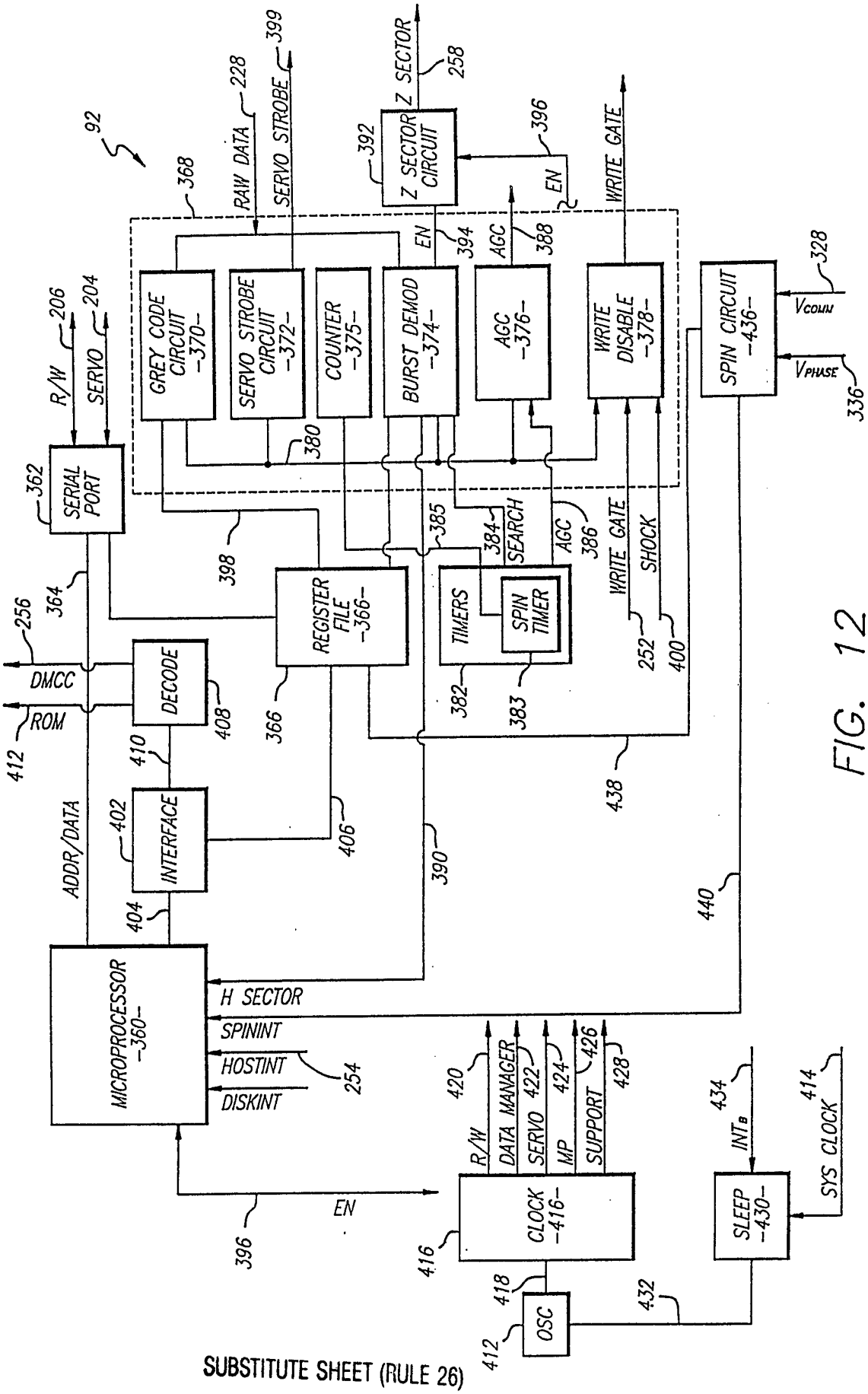

92
368
RAW DATA
228
SERVO STROBE
399
Z SECTOR
258
392
Z SECTOR CIRCUIT
396
EN
394
AGC
388
WRITE GATE
328
206
204
R/W
SERVO
GREY CODE CIRCUIT -370-
SERVO STROBE CIRCUIT -372-
COUNTER -375-
BURST DEMOD -374-
AGC -376-
WRITE DISABLE -378-
SPIN CIRCUIT -436-
V_{COIL}
V_{PHASE}
336
380
362
SERIAL PORT
398
385
384
SEARCH
AGC
386
WRITE GATE
SHOCK
364
256
REGISTER FILE -366-
TIMERS
SPIN TIMER
252
400
DMCC
ROM
412
DECODE
408
366
382
383
410
438
ADDR/DATA
402
INTERFACE
406
390
440
404
MICROPROCESSOR -360-
H SECTOR
SPININT
HOSTINT
DISKINT
254
420
R/W
DATA MANAGER
422
SERVO
424
MP
426
SUPPORT
428
434
INT_B
414
SYS CLOCK
EN
396
CLOCK -416-
SLEEP -430-
416
418
OSC
412
432

FIG. 12

FIG. 14a

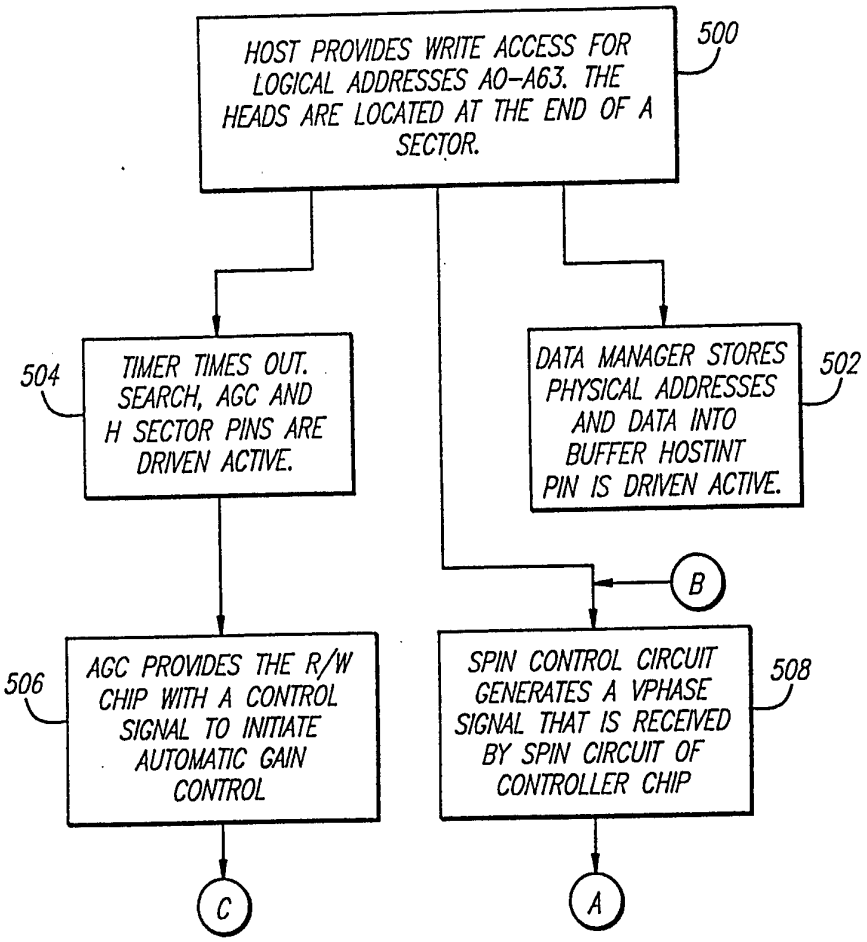


FIG. 14b

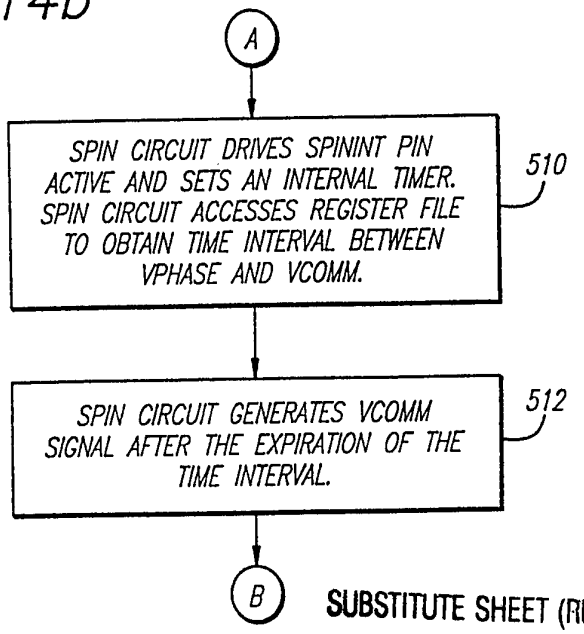


FIG. 14c

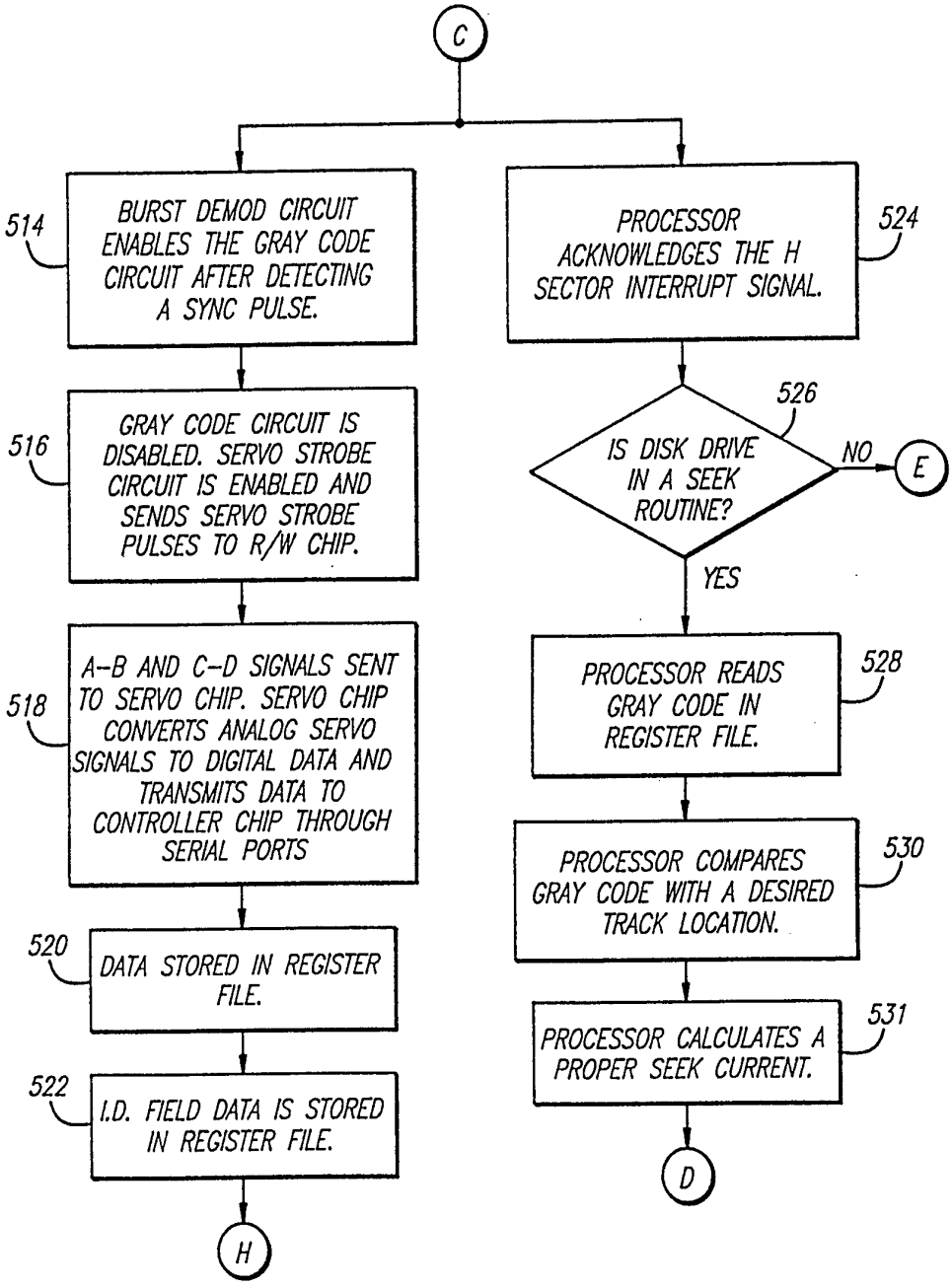

C
514
BURST DEMOD CIRCUIT ENABLES THE GRAY CODE CIRCUIT AFTER DETECTING A SYNC PULSE.
516
GRAY CODE CIRCUIT IS DISABLED. SERVO STROBE CIRCUIT IS ENABLED AND SENDS SERVO STROBE PULSES TO R/W CHIP.
518
A-B AND C-D SIGNALS SENT TO SERVO CHIP. SERVO CHIP CONVERTS ANALOG SERVO SIGNALS TO DIGITAL DATA AND TRANSMITS DATA TO CONTROLLER CHIP THROUGH SERIAL PORTS
520
DATA STORED IN REGISTER FILE.
522
I.D. FIELD DATA IS STORED IN REGISTER FILE.
H
524
PROCESSOR ACKNOWLEDGES THE H SECTOR INTERRUPT SIGNAL.
526
IS DISK DRIVE IN A SEEK ROUTINE?
NO
E
YES
528
PROCESSOR READS GRAY CODE IN REGISTER FILE.
530
PROCESSOR COMPARES GRAY CODE WITH A DESIRED TRACK LOCATION.
531
PROCESSOR CALCULATES A PROPER SEEK CURRENT.
D

FIG. 14d

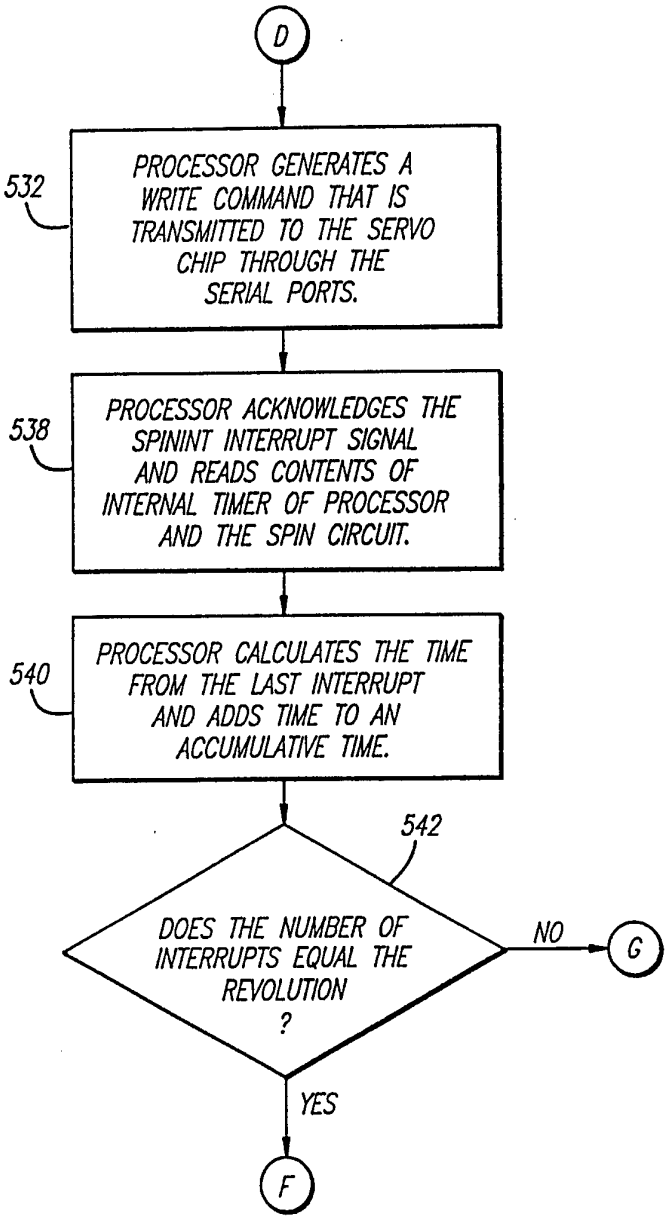

D
532
PROCESSOR GENERATES A WRITE COMMAND THAT IS TRANSMITTED TO THE SERVO CHIP THROUGH THE SERIAL PORTS.
538
PROCESSOR ACKNOWLEDGES THE SPININT INTERRUPT SIGNAL AND READS CONTENTS OF INTERNAL TIMER OF PROCESSOR AND THE SPIN CIRCUIT.
540
PROCESSOR CALCULATES THE TIME FROM THE LAST INTERRUPT AND ADDS TIME TO AN ACCUMULATIVE TIME.
542
DOES THE NUMBER OF INTERRUPTS EQUAL THE REVOLUTION ?
NO
G
YES
F

FIG. 14e

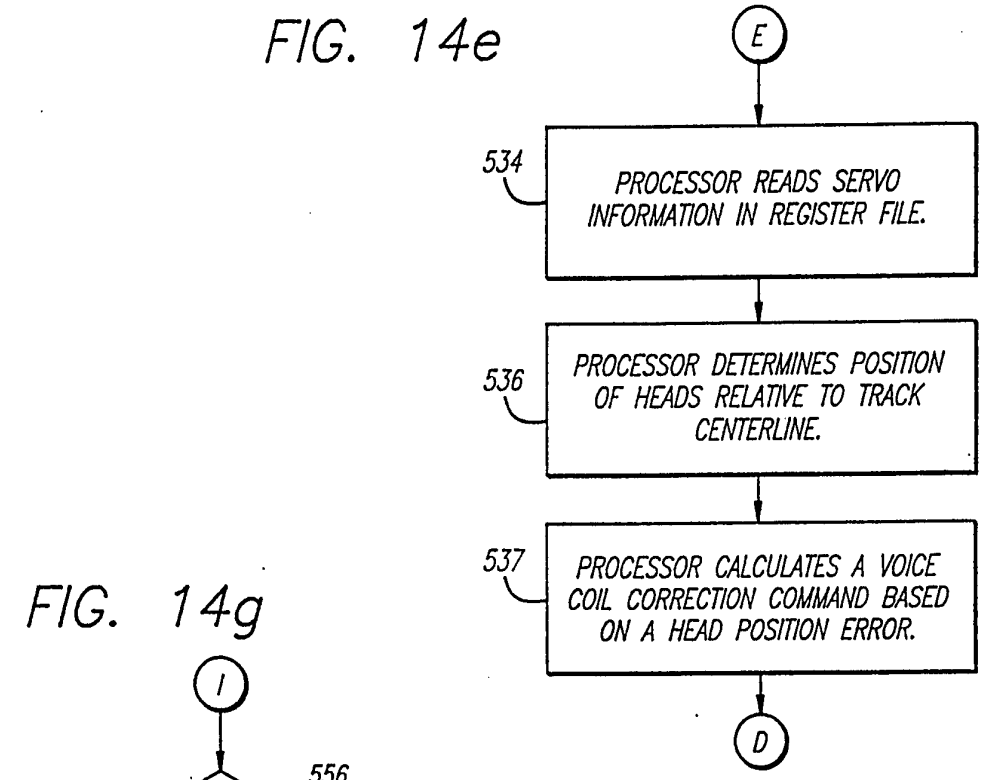


FIG. 14g

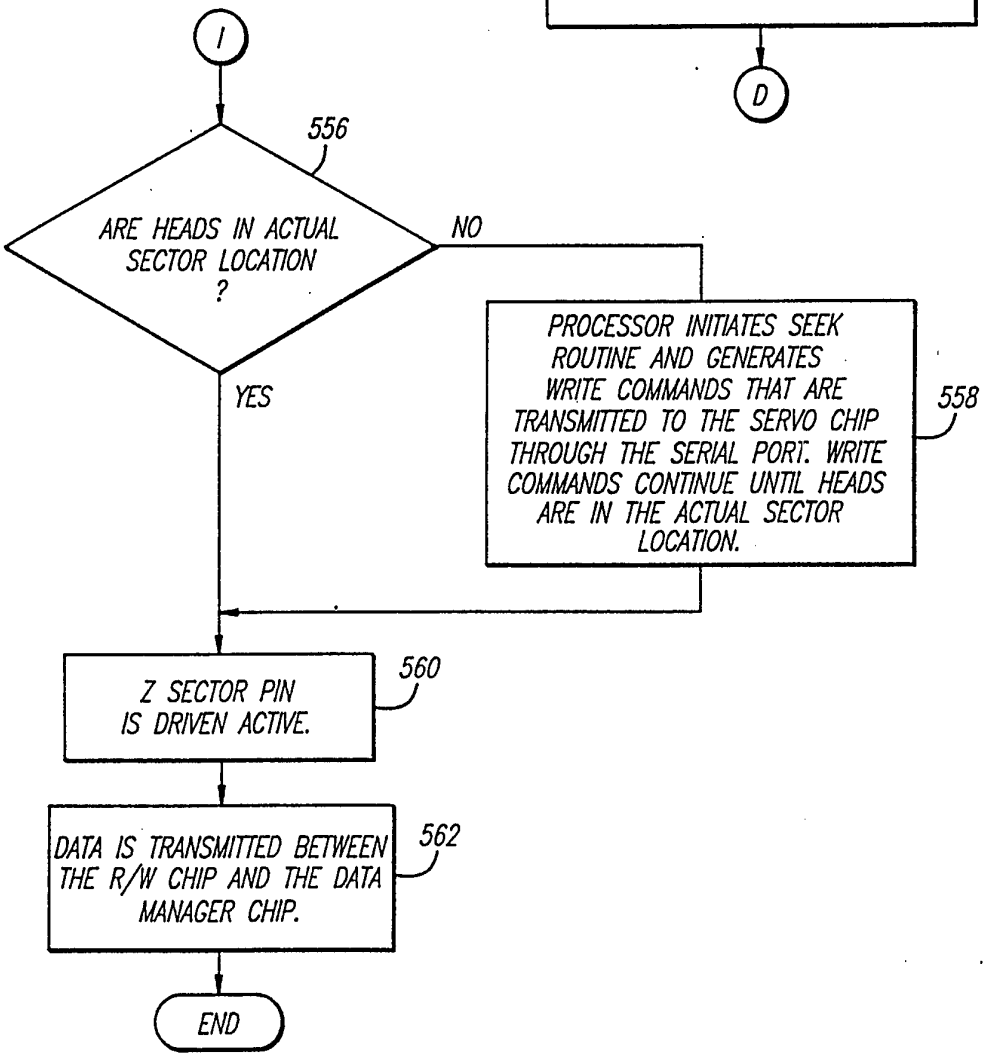
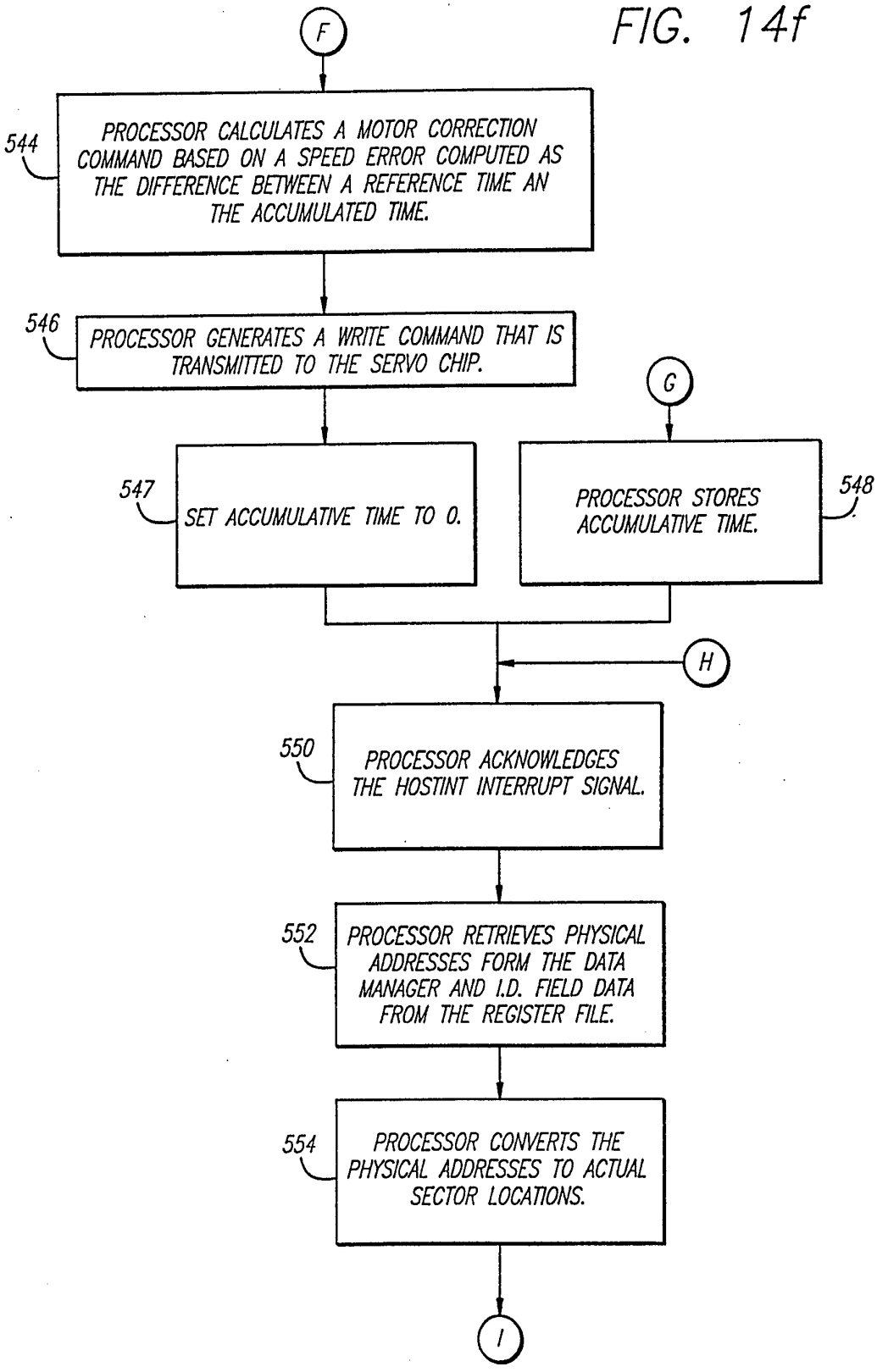


FIG. 14f


F
544
PROCESSOR CALCULATES A MOTOR CORRECTION COMMAND BASED ON A SPEED ERROR COMPUTED AS THE DIFFERENCE BETWEEN A REFERENCE TIME AN THE ACCUMULATED TIME.
546
PROCESSOR GENERATES A WRITE COMMAND THAT IS TRANSMITTED TO THE SERVO CHIP.
G
547
SET ACCUMULATIVE TIME TO 0.
PROCESSOR STORES ACCUMULATIVE TIME.
548
H
550
PROCESSOR ACKNOWLEDGES THE HOSTINT INTERRUPT SIGNAL.
552
PROCESSOR RETRIEVES PHYSICAL ADDRESSES FORM THE DATA MANAGER AND I.D. FIELD DATA FROM THE REGISTER FILE.
554
PROCESSOR CONVERTS THE PHYSICAL ADDRESSES TO ACTUAL SECTOR LOCATIONS.
I

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/07496

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11B21/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO,A,91 02354 (CONNER PERIPHERALS, INC.) 21 February 1991 . see page 10, line 19 - page 34, line 24; figures	14,38 1-3,5-9, 15-20, 25-34, 39-44

P,Y	PATENT ABSTRACTS OF JAPAN vol. 18, no. 57 (P-1684) 28 January 1994 & JP,A,05 274 786 (ALPINE ELECTRON INC.) 22 October 1993 see abstract	1-3,5-9, 15-20, 25-34, 39-44

A	EP,A,0 535 991 (FUJITSU LTD.) 7 April 1993 see page 5, line 28 - page 9, line 32; figures	1,14,25, 38

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 October 1994	21. 10. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Geoghegan, C

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 140 477 (HASHIMOTO) 18 August 1992 see column 3, line 8 - column 5, line 8; figures -----	1,14,25, 38

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US 94/07496

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO-A-9102354	21-02-91	EP-A- 0494869	22-07-92
		JP-T- 5501170	04-03-93
EP-A-0535991	07-04-93	JP-A- 5210924	20-08-93
US-A-5140477	18-08-92	JP-A- 1008564	12-01-89