



- (51) **International Patent Classification:**
H01L 21/203 (2006.01) *H01L 33/00* (2010.01)
- (21) **International Application Number:**
PCT/US2011/064722
- (22) **International Filing Date:**
13 December 2011 (13.12.2011)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
61/424,006 16 December 2010 (16.12.2010) US
13/036,273 28 February 2011 (28.02.2011) US
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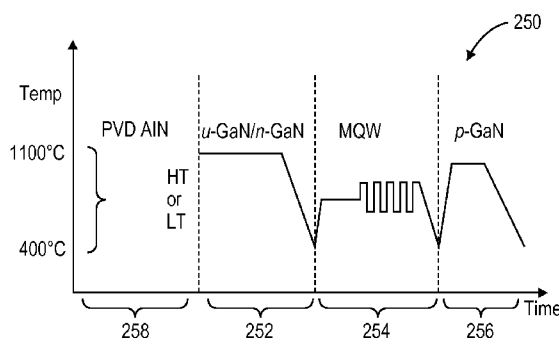
(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) **Title:** GALLIUM NITRIDE-BASED LED FABRICATION WITH PVD-FORMED ALUMINUM NITRIDE BUFFER LAYER

**FIG. 2A**

(57) **Abstract:** Fabrication of gallium nitride-based light emitting diodes (LEDs) with physical vapor deposition (PVD) formed aluminum nitride buffer layers is described. For example, a multi-chamber system includes a physical vapor deposition (PVD) chamber having a target composed of aluminum. A chamber is also included and is adapted to deposit un-doped or n-type gallium nitride, or both. In another example, a method of fabricating a light-emitting diode (LED) structure includes forming an aluminum nitride layer above a substrate in a physical vapor deposition (PVD) chamber of a multi-chamber system. An un-doped or n-type gallium nitride layer is formed on the aluminum nitride layer in a second chamber of the multi-chamber system.



Gallium Nitride-Based LED Fabrication with PVD-Formed Aluminum Nitride Buffer Layer

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Application No. 13/036,273, filed February 28, 2011, which claims the benefit of U.S. Provisional Application No. 61/424,006, filed December 16, 2010, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND

1) FIELD

[0002] Embodiments of the present invention pertain to the field of group III-nitride materials and, in particular, to the fabrication of gallium nitride-based light emitting diodes (LEDs) with physical vapor deposition (PVD) formed aluminum nitride buffer layers.

2) DESCRIPTION OF RELATED ART

[0003] Group III-V materials are playing an ever increasing role in the semiconductor and related, e.g. light-emitting diode (LED), industries. Often, group III-V materials are difficult to grow or deposit on foreign substrates (known as heteroepitaxy) without the formation of defects or cracks. For example, high quality surface preservation of select films, e.g. a gallium nitride film, is not straightforward in many applications using stacks of material layers fabricated sequentially. The inclusion of one or more buffer layers between a substrate and a device layer has been one approach. However, group III-V materials are often sensitive to process conditions and care must be taken to avoid such conditions at particular periods of the fabrication process. Avoiding interaction of a sensitive group III-V film with potential damaging conditions, however, is also not straightforward in many applications.

SUMMARY

[0004] Embodiments of the present invention pertain to the fabrication of gallium nitride-based light emitting diodes (LEDs) with physical vapor deposition (PVD) formed aluminum nitride buffer layers.

[0005] In an embodiment, a multi-chamber system includes a physical vapor deposition (PVD) chamber having a target composed of aluminum. A chamber is also included and is adapted to deposit un-doped or n-type gallium nitride, or both.

[0006] In another embodiment, a multi-chamber system includes a physical vapor deposition (PVD) chamber having a target composed of aluminum. A first metal-organic chemical vapor deposition (MOCVD) chamber is also included and is for depositing un-doped or n-type gallium nitride. A second MOCVD chamber is also included and is for depositing a multiple quantum well (MQW) structure. A third MOCVD chamber is also included and is for depositing p-type aluminum gallium nitride or p-type gallium nitride, or both.

[0007] In another embodiment, a method of fabricating a light-emitting diode (LED) structure includes forming an aluminum nitride layer above a substrate in a physical vapor deposition (PVD) chamber of a multi-chamber system. An un-doped or n-type gallium nitride layer is formed on the aluminum nitride layer in a second chamber of the multi-chamber system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 illustrates a benchmark cluster tool schematic, a benchmark LED structure, and a benchmark time-to-deposition plot, in accordance with one or more embodiments of the present invention.

[0009] Figure 2A illustrates a cluster tool schematic and a corresponding temperature versus time plot for LED structure fabrication, in accordance with an embodiment of the present invention.

[0010] Figure 2B illustrates a light-emitting diode (LED) structure and a corresponding time-to-deposition plot, in accordance with an embodiment of the present invention.

[0011] Figure 3 is a Flowchart representing operations in a method of fabricating a gallium nitride-based light LED with a PVD-formed aluminum nitride buffer layer, in accordance with an embodiment of the present invention.

[0012] Figure 4 is a schematic cross-sectional view of a MOCVD chamber suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0013] Figure 5 is a schematic cross-sectional view of a HVPE chamber suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0014] Figure 6 illustrates a cross-sectional view of a gallium nitride (GaN)-based light-emitting diode (LED) formed on a metalized substrate, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0015] The fabrication of gallium nitride-based light emitting diodes (LEDs) with physical vapor deposition (PVD) formed aluminum nitride buffer layers is described. In the following description, numerous specific details are set forth, such as process chamber configurations and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as specific diode configurations, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. Additionally, other arrangements and configurations may not be explicitly disclosed in embodiments herein, but are still considered to be within the spirit and scope of the invention.

[0016] An LED method of fabrication can include the formation of a buffer layer of gallium nitride between a substrate and a device layer of un-doped and/or doped gallium nitride. In embodiments described herein, an aluminum nitride buffer layer is used in place of such a gallium nitride buffer layer, between the substrate and the device layer of un-doped and doped gallium nitride. The aluminum nitride layer may be formed by sputter deposition in a PVD process. This is in contrast to the fabrication of group III-nitride buffer layers which is typically performed in a metal-organic vapor deposition (MOCVD) chamber or a hydride vapor phase epitaxy (HVPE) chamber. The aluminum nitride layer may be formed by non-reactive sputtering from an aluminum nitride target housed in the PVD chamber or,

alternatively, may be formed by reactive sputtering from an aluminum target housed in the PVD chamber and reacted with a nitrogen-based gas or plasma.

[0017] One or more of the embodiments described herein may enable higher throughput in a multi-chamber fabrication tool used for LED fabrication. Also, by including a PVD-formed aluminum nitride layer instead of a gallium nitride buffer layer, the device layer of un-doped and doped gallium nitride may be thinned overall. In a particular example, the un-doped portion may be thinned or eliminated altogether. Furthermore, preliminary sputter cleaning of a receiving substrate, such as a sapphire substrate, may be performed in the same PVD deposition chamber as is used to deposit the aluminum nitride layer. Additionally, the overall thermal budget of LED fabrication may be reduced since the PVD aluminum nitride layer may be formed at temperatures below 300 degrees Celsius. By contrast, a typical gallium nitride buffer layer is formed between 500-600 degrees Celsius. One or more of the embodiments described herein may enable faster deposition rates, e.g. two times the growth rate, for materials such as un-doped and/or n-type doped gallium nitride. Faster rates may be achieved since, in some embodiments, the un-doped and/or n-type doped gallium nitride layers are formed on an aluminum nitride (AlN) buffer layer which may provide a correct crystal orientation and morphological relationship for growing un-doped and/or n-type doped gallium nitride layers thereon. One or more of the embodiments described herein may enable elimination of oxide removal operations since many of the described operations are performed in-situ in a cluster tool. One or more of the embodiments described herein may enable an improvement of gallium nitride crystalline quality by forming the gallium nitride on a PVD-formed aluminum nitride buffer layer.

[0018] Described in association with one or more embodiments herein are systems for the fabrication of gallium nitride-based LEDs with PVD-formed aluminum nitride buffer layers. In one embodiment, a multi-chamber system includes a PVD chamber having a target composed of a metallic or compound of aluminum. The multi-chamber system also includes chambers adapted to deposit un-doped or n-type gallium nitride, or both, and for other device layers such as multiple quantum well layers and p-type doped gallium nitride layers.

[0019] Also described in association with one or more embodiments herein are methods of fabricating gallium nitride-based LEDs with PVD-formed aluminum nitride buffer layers. In one embodiment, a method of fabricating a LED structure

includes forming an aluminum nitride layer above a substrate in a PVD chamber of a multi-chamber system. The method also includes forming an un-doped or n-type gallium nitride layer on the aluminum nitride layer in a second chamber of the multi-chamber system.

[0020] Embodiments of the present invention may provide improvements over a benchmark system or methodology developed during studies of the presently described systems and methodologies. For example, Figure 1 illustrates a benchmark cluster tool schematic, a benchmark LED structure, and a benchmark time-to-deposition plot, in accordance with one or more embodiments of the present invention.

[0021] Referring to Figure 1, a benchmark cluster tool 100 includes an un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 (MOCVD1: u-GaN/n-GaN), a multiple quantum well (MQW) MOCVD reaction chamber 104 (MOCVD2: MQW), and a p-type gallium nitride MOCVD reaction chamber 106 (MOCVD3: p-GaN). The benchmark cluster tool 100 may also include a load lock 108, a carrier cassette 110, and an optional additional un-doped and/or n-type gallium nitride MOCVD reaction chamber 112 for high volume applications, all of which are depicted in Figure 1.

[0022] A benchmark LED structure 120 includes a stack of various material layers, many of which include III-V materials. For example, the benchmark LED structure 120 includes a silicon or sapphire substrate 122 (Substrate: sapphire, Si), a 20 nanometer thick buffer layer 124 (LT buffer), and an approximately 4 microns thick un-doped/n-type gallium nitride combination layer 126 (u-GaN/n-GaN). The buffer layer 124 may be a gallium nitride layer formed at relatively low processing temperatures. The buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 are formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 of benchmark cluster tool 100. The benchmark LED structure 120 also includes an MQW structure 128 with a thickness in the range of 30 – 500 nanometers. The MQW structure 128 is formed in MQW MOCVD reaction chamber 104 of benchmark cluster tool 100. The benchmark LED structure 120 also includes an approximately 20 nanometers thick p-type gallium aluminum nitride layer 130 (p-AlGaN) and a p-type gallium nitride layer 132 with a thickness in the range of 50 – 200 nanometers (p-GaN). The p-type gallium aluminum nitride layer 130 and the p-

type gallium nitride layer 132 are formed in p-type gallium nitride MOCVD reaction chamber 106 of benchmark cluster tool 100.

[0023] A benchmark time-to-deposition plot 140 represents chamber usage in benchmark cluster tool 100. The formation of the MQW structure 128 in MQW MOCVD reaction chamber 104 has a growth time of approximately 2 hours. And, the formation of the p-type gallium aluminum nitride layer 130 and the p-type gallium nitride layer 132 in p-type gallium nitride MOCVD reaction chamber 106 has a growth time of approximately 1 hour. Meanwhile, the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 has a growth time of approximately 3.5 hours. An additional approximately 1 hour may be required for chamber cleaning of chamber 102. Thus, overall, the cycle time for fabricating benchmark LED structure 120 in benchmark cluster tool 100 is dictated by the cycle time of un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, which is approximately 4.5 hours. It is to be understood that cleaning time may, but need not, include time for shut-down, plus clean time, plus recovery time. It is also to be understood that the above may represent an average since cleaning may not be performed between every chamber usage.

[0024] A benchmark timing sequence for LED material deposition specific to the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, as described in association with Figure 1, is provided below. For example, the growth time of approximately 3.5 hours is broken into a 10 minute high temperature treatment of a sapphire substrate, a 5 minute low temperature formation of a buffer layer, a 10 minute buffer annealing operation, a 30 minute growth recovery operation, a 2 hour un-doped/n-type gallium nitride combination layer formation operation, and a 30 minute temperature ramp and stabilization operation (e.g., temp ramp 2-3°C/s).

[0025] In reference to the benchmark systems and methodologies described in association with Figure 1, the benchmark approach may result in an unbalanced time flow for each functioning layer of the LED. For example, formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 is 3.5 hrs, formation of the MQW structure 128 in MQW MOCVD reaction chamber 104 is 2 hours, and

formation of the p-type gallium aluminum nitride layer 130 and the p-type gallium nitride layer 132 in p-type gallium nitride MOCVD reaction chamber 106 is 1 hour. Furthermore, as mentioned above, an additional approximately 1 hour of chamber cleaning (possibly including pump-down times) may be required between runs in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102. Such additional chamber cleaning may be required to avoid substrate contamination. As such, the progressive growth of the structure 120 with three MOCVD chambers results in significant idle time for the MQW MOCVD reaction chamber 104 and the p-type gallium nitride MOCVD reaction chamber 106, reducing the overall throughput of the system 100.

[0026] In an aspect of the present invention, the throughput of a cluster system for fabricating LED structures may be improved by substituting one of or a portion of one of the above described MOCVD material growth capabilities or operations with a PVD sputtering deposition capability or operation. For example, Figure 2A illustrates a cluster tool schematic and a corresponding temperature versus time plot for LED structure fabrication, in accordance with an embodiment of the present invention. Figure 2B illustrates an LED structure and a corresponding time-to-deposition plot, in accordance with an embodiment of the present invention.

[0027] Referring to Figure 2A, a cluster tool 200 includes a PVD aluminum nitride sputter chamber 202 (PVD AlN), an un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 (MOCVD1: u-GaN/n-GaN), a multiple quantum well (MQW) MOCVD reaction chamber 206 (MOCVD2: MQW), and a p-type gallium nitride MOCVD reaction chamber 208 (MOCVD3: p-GaN). The cluster tool 200 may also include a load lock 210, a carrier cassette 212, and a transfer chamber 214, all of which are depicted in Figure 2A.

[0028] Thus, in accordance with an embodiment of the present invention, a multi-chamber system includes a PVD chamber having a target of metallic or compound aluminum, and a chamber adapted to deposit un-doped and/or n-type gallium nitride, or both. In one embodiment, the target of the PVD chamber is composed of aluminum nitride. In such an embodiment, reactive sputtering need not be used since the target is composed of the same material desired for deposition. However, in an alternative embodiment, a target composed of aluminum is used, and aluminum nitride is reactively sputtered from the aluminum target by or in the presence of a nitrogen source. In one embodiment, the chamber adapted to deposit

un-doped or n-type gallium nitride is a MOCVD chamber, as depicted in Figure 2A. However, in an alternative embodiment, the chamber adapted to deposit un-doped or n-type gallium nitride is a hydride vapor phase epitaxy (HVPE) chamber. In one embodiment, the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in a cluster tool arrangement, as depicted in Figure 2A. However, in an alternative embodiment, the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in an in-line tool arrangement. Deposition processes based on PVD, as described herein, may be performed at temperatures approximating standard room temperature, or may be performed at higher temperatures.

[0029] Referring to Figure 2B, a LED structure 220 includes a stack of various material layers, many of which include III-V materials. For example, the LED structure 220 includes a silicon or sapphire substrate 222 (Substrate: sapphire, Si) and an aluminum nitride layer 224 (AlN) with a thickness approximately in the range of 10 – 200 nanometers. The aluminum nitride layer 224 is formed by sputter deposition in the PVD aluminum nitride sputter chamber 202 of cluster tool 200. The LED structure 220 also includes an approximately 4 microns thick un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 (n-GaN). The un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 is formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 of cluster tool 200. The LED structure 220 also includes an MQW structure 228 with a thickness in the range of 30 – 500 nanometers. The MQW structure 228 is formed in MQW MOCVD reaction chamber 206 of cluster tool 200. In one embodiment, the MQW structure 228 is composed of one or a plurality of field pairs of InGaN well/GaN barrier material layers. The LED structure 220 also includes an approximately 20 nanometers thick p-type gallium aluminum nitride layer 230 (p-AlGaN) and a p-type gallium nitride layer 232 with a thickness in the range of 50 – 200 nanometers (p-GaN). The p-type gallium aluminum nitride layer 230 and the p-type gallium nitride layer 232 are formed in p-type gallium nitride MOCVD reaction chamber 208 of cluster tool 200. It is to be understood that the above thicknesses or thickness ranges are exemplary embodiments, and that other suitable thicknesses or thickness ranges are also considered within the spirit and scope of embodiments of the present invention.

[0030] A time-to-deposition plot 240 represents chamber usage in cluster tool 200. The formation of the MQW structure 228 in MQW MOCVD reaction chamber 206 has a growth time of approximately 2 hours. The formation of the p-type gallium aluminum nitride layer 230 and the p-type gallium nitride layer 232 in p-type gallium nitride MOCVD reaction chamber 208 has a growth time of approximately 1 hour. And, in accordance with an embodiment of the present invention, the formation of the un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 has a growth time of only approximately 2 hours. An additional approximately 1 hour may be required for chamber cleaning of chamber 204. It is to be understood, however, that cleaning time may include time for shut-down, plus clean time, plus recovery time. It is also to be understood that the above may represent an average since cleaning may not be performed between every chamber usage.

[0031] Thus, instead of forming a buffer layer, such as buffer layer 124 of Figure 1, in the MOCVD chamber used to form gallium nitride layer 126, an aluminum nitride buffer layer 224 is instead included and is formed in another chamber, specifically in PVD aluminum nitride sputter chamber 202. Although the AlN growth may be for a duration of approximately 5 minutes, excluding pump time (from approximately 400 torr to approximately 10^{-8} torr), the formation in a chamber separate from MOCVD chamber 1 increases throughput of cluster tool 200. For example, overall, the cycle time for fabricating LED structure 220 in cluster tool 200 is once again dictated by the cycle time of un-doped and/or n-type gallium nitride MOCVD reaction chamber 204, which is reduced to approximately 3 hours versus the benchmark system of 4.5 hours. As such, the progressive growth of the structure 220 with one PVD chamber in addition to three MOCVD chambers results in much less idle time for the MQW MOCVD reaction chamber 206 and the p-type gallium nitride MOCVD reaction chamber 208, improving the overall throughput of the system 200. For example, in one embodiment, tool throughput is improved from approximately 5.3 runs per day to approximately 8 runs per day, demonstrating an approximately 50% throughput improvement.

[0032] Referring again to Figure 2A, a representative temperature versus time plot 250 for LED structure fabrication in cluster tool 200 is provided. Region 252 of plot 250 is specific to the formation of un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 formed in un-doped and/or n-type gallium

nitride MOCVD reaction chamber 204. In this region, only one temperature ramp (ramp down from approximately 1100 degrees Celsius to approximately 400 degrees Celsius) is needed. Such a single ramp event requirement is in stark contrast to the timing sequence for the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, as described above. In that case, the chamber starts at a high temperature for substrate treatment, ramps down in temperature for buffer layer fabrication, ramps back up in temperature for the gallium nitride deposition, and finally down again for stabilization. It is noted that in both cases, however, the region 254 and 256 of plot 250 specific to the formation of the MQW and the p-GaN, will be approximately the same. In an embodiment, referring to region 258 of plot 250, the temperature versus time plot for PVD-formed aluminum nitride could encompass either a high temperature (HT) or low temperature (LT) process, approximately in the range of 20 – 1200 degrees Celsius.

[0033] In addition to the throughput improvement for cluster tool 200, there may be additional benefits to a PVD chamber plus three MOCVD chamber tool arrangement. For example, cost savings may be achieved since less reaction gas may need to be delivered to the first MOCVD chamber. PVD chamber engineering and design may be simpler compared with configuration time and complexity for an MOCVD chamber dedicated to both a buffer layer and a device layer, as is chamber 102 of benchmark cluster tool 100. In the case that the above process enables a reduced thickness for the un-doped gallium nitride portion of device layer 226, simpler down-the-line etch-back processes may be performed. This may also enable the saving of material and operation cost while reducing cycle time. Also, by using an aluminum nitride buffer layer in place of a gallium nitride buffer layer, reduced defectivity in the active layers of a device, such as an LED device, may be achieved.

[0034] Thus, in accordance with an embodiment of the present invention, a multi-chamber system includes a PVD chamber having an aluminum nitride target, and a first MOCVD chamber to deposit un-doped or n-type gallium nitride. The multi-chamber system also includes a second MOCVD chamber to deposit a multiple quantum well (MQW) structure, and a third MOCVD chamber to deposit p-type aluminum gallium nitride or p-type gallium nitride, or both. In one embodiment, the PVD chamber having the aluminum nitride target is for non-reactive sputtering of aluminum nitride. In a specific such embodiment, the PVD chamber is for non-

reactive sputtering of aluminum nitride at a low or slightly elevated temperature approximately in the range of 20 – 200 degrees Celsius. In another specific such embodiment, the PVD chamber is for non-reactive sputtering of aluminum nitride at a high temperature approximately in the range of 200 – 1200 degrees Celsius.

[0035] It may be the case that regardless of deposition temperature, a PVD deposited aluminum nitride layer suitable for inclusion in LED structure 220 may need to be, at some point, exposed to a high temperature approximately in the range of 400 – 1400 degrees Celsius, e.g., about 900 degrees Celsius, in order to achieve requisite material properties (e.g., appropriate defect density, crystal grain size, crystal orientation, etc.). In accordance with an embodiment of the present invention, a rapid thermal processing (RTP) process is performed on the PVD deposited aluminum nitride layer prior to fabrication of additional layers on the aluminum nitride layer. An RTP chamber may, then, in some way be associated with the above described fabrication process for LED structure 220. In one embodiment, a tool, such as a cluster tool or in-line tool including the PVD and three MOCVD chambers also includes a RTP chamber. In an alternative embodiment, however, an RTP process is performed in the PVD chamber. In another alternative embodiment, a laser annealing capability is associated with the above described fabrication process for LED structure 220.

[0036] In another aspect of the present invention, methods of fabricating gallium nitride-based LEDs with PVD-formed aluminum nitride buffer layers are provided. For example, Figure 3 is a Flowchart 300 representing operations in a method of fabricating a gallium nitride-based light LED with a PVD-formed aluminum nitride buffer layer, in accordance with an embodiment of the present invention.

[0037] Referring to operation 302 of Flowchart 300, a method includes forming an aluminum nitride layer above a substrate in a PVD chamber. For example, an aluminum nitride layer may be formed in a chamber such as chamber 202 of cluster tool 200. In one embodiment, forming the aluminum nitride layer includes sputtering from an aluminum nitride target housed in the PVD chamber. In one embodiment, forming the aluminum nitride layer includes performing the forming at a low to slightly elevated substrate temperature approximately in the range of 20 – 200 degrees Celsius. In one embodiment, forming the aluminum nitride layer includes performing

the forming at a high substrate temperature approximately in the range of 200 – 1200 degrees Celsius.

[0038] Referring to operation 304 of Flowchart 300, the method includes forming an un-doped or n-type gallium nitride layer on the aluminum nitride layer. For example, an un-doped or n-type gallium nitride layer may be formed in a chamber such as chamber 204 of cluster tool 200. In one embodiment, forming the un-doped or n-type gallium nitride layer includes performing the forming in a MOCVD chamber. In one embodiment, forming the un-doped or n-type gallium nitride layer includes performing the forming in a HVPE chamber. In one embodiment, the method further includes, prior to forming the un-doped or n-type gallium nitride layer on the aluminum nitride layer, annealing the aluminum nitride layer in a RTP chamber.

[0039] Referring to operation 306 of Flowchart 300, the method also includes forming a MQW structure above the un-doped or n-type gallium nitride layer. For example, a MQW structure may be formed in a chamber such as chamber 206 of cluster tool 200. In one embodiment, the MQW structure is composed of one or a plurality of field pairs of InGaN well/GaN barrier material layers.

[0040] Referring to operation 308 of Flowchart 300, the method further includes forming a p-type aluminum gallium nitride or p-type gallium nitride layer above the MQW structure. For example, the p-type aluminum gallium nitride or p-type gallium nitride layer may be formed in a chamber such as chamber 208 of cluster tool 200.

[0041] Exemplary embodiments of tool platforms suitable for housing a PVD chamber along with three MOCVD chambers include an Opus™ AdvantEdge™ system or a Centura™ system, both commercially available from Applied Materials, Inc. of Santa Clara, CA. Embodiments of the present invention further include an integrated metrology (IM) chamber as a component of the multi-chambered processing platform. The IM chamber may provide control signals to allow adaptive control of integrated deposition process, such as the multiple segmented sputter or epitaxial growth processes described above in association with Figure 3. The IM chamber may include a metrology apparatus suitable to measure various film properties, such as thickness, roughness, composition, and may further be capable of characterizing grating parameters such as critical dimensions (CD), sidewall angle (SWA), feature height (HT) under vacuum in an automated manner. Examples

include, but are not limited to, optical techniques like reflectometry and scatterometry. In particularly advantageous embodiments, in-vacuo optical CD (OCD) techniques are employed where the attributes of a grating formed in a starting material are monitored as the sputter and/or epitaxial growth proceeds. In other embodiments, metrology operations are performed in a process chamber, e.g., in-situ in the process chamber, rather than in a separate IM chamber.

[0042] A multi-chambered processing platform, such as cluster tool 200 may further include an optional substrate aligner chamber, as well as load lock chambers holding cassettes, coupled to a transfer chamber including a robotic handler. In one embodiment of the present invention, adaptive control of the multi-chambered processing platform 200 is provided by a controller. The controller may be one of any form of general-purpose data processing system that can be used in an industrial setting for controlling the various subprocessors and subcontrollers. Generally, the controller includes a central processing unit (CPU) in communication with a memory and an input/output (I/O) circuitry, among other common components. As an example, the controller may perform or otherwise initiate one or more of the operations of any of the methods/processes described herein, including the method described in association with Flowchart 300. Any computer program code that performs and/or initiates such operations may be embodied as a computer program product. Each computer program product described herein may be carried by a medium readable by a computer (e.g., a floppy disc, a compact disc, a DVD, a hard drive, a random access memory, etc.).

[0043] Suitable PVD chambers for the processes and tool configurations contemplated herein may include the Endura PVD system, commercially available from Applied Materials, Inc. of Santa Clara, CA. The Endura PVD system provides superior electromigration resistance and surface morphology as well as low cost of ownership and high system reliability. PVD processes performed therein may be done so at requisite pressures and suitable target-to-wafer distance which creates directional flux of deposited species in the process cavity. Chambers compatible with in-line systems such as the ARISTO chamber, also commercially available from Applied Materials, Inc. of Santa Clara, CA, provides automated loading and unloading capabilities, as well as a magnetic carrier transport system, permitting significantly reduced cycle times. The AKT-PiVot 55KV PVD system, also commercially available from Applied Materials, Inc. of Santa Clara, CA, has a vertical platform for

sputtering deposition. The AKT-PiVot system's module architecture delivers significantly faster cycle time and enables a large variety of configurations to maximize production efficiency. Unlike traditional in-line systems, the AKT-PiVot's parallel processing capability eliminates bottlenecks caused by different process times for each film layer. The system's cluster-like arrangement also allows continuous operation during individual module maintenance. The included rotary cathode technology enables nearly 3x higher target utilization as compared with conventional systems. The PiVot system's deposition modules feature a pre-sputter unit that enables target conditioning using only one substrate, rather than up to 50 substrates that are needed with other systems to achieve the same results.

[0044] An example of an MOCVD deposition chamber which may be suitable for use as one or more of MOCVD chambers 204, 206, or 208, described above, is illustrated and described with respect to Figure 4. Figure 4 is a schematic cross-sectional view of an MOCVD chamber according to an embodiment of the invention. Exemplary systems and chambers that may be adapted to practice the present invention are described in U.S. patent application Ser. No. 11/404,516, filed on Apr. 14, 2006, and Ser. No. 11/429,022, filed on May 5, 2006, both of which are incorporated by reference in their entireties.

[0045] The apparatus 4100 shown in Figure 4 includes a chamber 4102, a gas delivery system 4125, a remote plasma source 4126, and a vacuum system 4112. The chamber 4102 includes a chamber body 4103 that encloses a processing volume 4108. A showerhead assembly 4104 is disposed at one end of the processing volume 4108, and a substrate carrier 4114 is disposed at the other end of the processing volume 4108. A lower dome 4119 is disposed at one end of a lower volume 4110, and the substrate carrier 4114 is disposed at the other end of the lower volume 4110. The substrate carrier 4114 is shown in process position, but may be moved to a lower position where, for example, the substrates 4140 may be loaded or unloaded. An exhaust ring 4120 may be disposed around the periphery of the substrate carrier 4114 to help prevent deposition from occurring in the lower volume 4110 and also help direct exhaust gases from the chamber 4102 to exhaust ports 4109. The lower dome 4119 may be made of transparent material, such as high-purity quartz, to allow light to pass through for radiant heating of the substrates 4140. The radiant heating may be provided by a plurality of inner lamps 4121A and outer lamps 4121B disposed below the lower dome 4119, and reflectors 4166 may be used to help control chamber 4102

exposure to the radiant energy provided by inner and outer lamps 4121A, 4121B. Additional rings of lamps may also be used for finer temperature control of the substrate 4140.

[0046] The substrate carrier 4114 may include one or more recesses 4116 within which one or more substrates 4140 may be disposed during processing. The substrate carrier 4114 may carry six or more substrates 4140. In one embodiment, the substrate carrier 4114 carries eight substrates 4140. It is to be understood that more or less substrates 4140 may be carried on the substrate carrier 4114. Typical substrates 4140 may include sapphire, silicon carbide (SiC), silicon, or gallium nitride (GaN). It is to be understood that other types of substrates 4140, such as glass substrates 4140, may be processed. Substrate 4140 size may range from 50 mm-100 mm in diameter or larger. The substrate carrier 4114 size may range from 200 mm-750 mm. The substrate carrier 4114 may be formed from a variety of materials, including SiC or SiC-coated graphite. It is to be understood that substrates 4140 of other sizes may be processed within the chamber 4102 and according to the processes described herein. The showerhead assembly 4104 may allow for more uniform deposition across a greater number of substrates 4140 and/or larger substrates 4140 than in traditional MOCVD chambers, thereby increasing throughput and reducing processing cost per substrate 4140.

[0047] The substrate carrier 4114 may rotate about an axis during processing. In one embodiment, the substrate carrier 4114 may be rotated at about 2 RPM to about 100 RPM. In another embodiment, the substrate carrier 4114 may be rotated at about 30 RPM. Rotating the substrate carrier 4114 aids in providing uniform heating of the substrates 4140 and uniform exposure of the processing gases to each substrate 4140.

[0048] The plurality of inner and outer lamps 4121A, 4121B may be arranged in concentric circles or zones (not shown), and each lamp zone may be separately powered. In one embodiment, one or more temperature sensors, such as pyrometers (not shown), may be disposed within the showerhead assembly 4104 to measure substrate 4140 and substrate carrier 4114 temperatures, and the temperature data may be sent to a controller (not shown) which can adjust power to separate lamp zones to maintain a predetermined temperature profile across the substrate carrier 4114. In another embodiment, the power to separate lamp zones may be adjusted to compensate for precursor flow or precursor concentration non-uniformity. For example, if the precursor concentration is lower in a substrate carrier 4114 region near

an outer lamp zone, the power to the outer lamp zone may be adjusted to help compensate for the precursor depletion in this region.

[0049] The inner and outer lamps 4121A, 4121B may heat the substrates 4140 to a temperature of about 400 degrees Celsius to about 1200 degrees Celsius. It is to be understood that the invention is not restricted to the use of arrays of inner and outer lamps 4121A, 4121B. Any suitable heating source may be utilized to ensure that the proper temperature is adequately applied to the chamber 4102 and substrates 4140 therein. For example, in another embodiment, the heating source may include resistive heating elements (not shown) which are in thermal contact with the substrate carrier 4114.

[0050] A gas delivery system 4125 may include multiple gas sources, or, depending on the process being run, some of the sources may be liquid sources rather than gases, in which case the gas delivery system may include a liquid injection system or other means (e.g., a bubbler) to vaporize the liquid. The vapor may then be mixed with a carrier gas prior to delivery to the chamber 4102. Different gases, such as precursor gases, carrier gases, purge gases, cleaning/etching gases or others may be supplied from the gas delivery system 4125 to separate supply lines 4131, 4132, and 4133 to the showerhead assembly 4104. The supply lines 4131, 4132, and 4133 may include shut-off valves and mass flow controllers or other types of controllers to monitor and regulate or shut off the flow of gas in each line.

[0051] A conduit 4129 may receive cleaning/etching gases from a remote plasma source 4126. The remote plasma source 4126 may receive gases from the gas delivery system 4125 via supply line 4124, and a valve 4130 may be disposed between the showerhead assembly 4104 and remote plasma source 4126. The valve 4130 may be opened to allow a cleaning and/or etching gas or plasma to flow into the showerhead assembly 4104 via supply line 4133 which may be adapted to function as a conduit for a plasma. In another embodiment, apparatus 4100 may not include remote plasma source 4126 and cleaning/etching gases may be delivered from gas delivery system 4125 for non-plasma cleaning and/or etching using alternate supply line configurations to shower head assembly 4104.

[0052] The remote plasma source 4126 may be a radio frequency or microwave plasma source adapted for chamber 4102 cleaning and/or substrate 4140 etching. Cleaning and/or etching gas may be supplied to the remote plasma source 4126 via supply line 4124 to produce plasma species which may be sent via conduit

4129 and supply line 4133 for dispersion through showerhead assembly 4104 into chamber 4102. Gases for a cleaning application may include fluorine, chlorine or other reactive elements.

[0053] In another embodiment, the gas delivery system 4125 and remote plasma source 4126 may be suitably adapted so that precursor gases may be supplied to the remote plasma source 4126 to produce plasma species which may be sent through showerhead assembly 4104 to deposit CVD layers, such as III-V films, for example, on substrates 4140.

[0054] A purge gas (e.g., nitrogen) may be delivered into the chamber 4102 from the showerhead assembly 4104 and/or from inlet ports or tubes (not shown) disposed below the substrate carrier 4114 and near the bottom of the chamber body 4103. The purge gas enters the lower volume 4110 of the chamber 4102 and flows upwards past the substrate carrier 4114 and exhaust ring 4120 and into multiple exhaust ports 4109 which are disposed around an annular exhaust channel 4105. An exhaust conduit 4106 connects the annular exhaust channel 4105 to a vacuum system 4112 which includes a vacuum pump (not shown). The chamber 4102 pressure may be controlled using a valve system 4107 which controls the rate at which the exhaust gases are drawn from the annular exhaust channel 4105.

[0055] An example of a HVPE deposition chamber which may be suitable for use as the HVPE chamber 204 of alternative embodiments of chamber 204, described above, is illustrated and described with respect to Figure 5. Figure 5 is a schematic cross-sectional view of a HVPE chamber 500 suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0056] The apparatus 500 includes a chamber 502 enclosed by a lid 504. Processing gas from a first gas source 510 is delivered to the chamber 502 through a gas distribution showerhead 506. In one embodiment, the gas source 510 includes a nitrogen containing compound. In another embodiment, the gas source 510 includes ammonia. In one embodiment, an inert gas such as helium or diatomic nitrogen is introduced as well either through the gas distribution showerhead 506 or through the walls 508 of the chamber 502. An energy source 512 may be disposed between the gas source 510 and the gas distribution showerhead 506. In one embodiment, the energy source 512 includes a heater. The energy source 512 may break up the gas from the gas source 510, such as ammonia, so that the nitrogen from the nitrogen containing gas is more reactive.

[0057] To react with the gas from the first source 510, precursor material may be delivered from one or more second sources 518. The precursor may be delivered to the chamber 502 by flowing a reactive gas over and/or through the precursor in the precursor source 518. In one embodiment, the reactive gas includes a chlorine containing gas such as diatomic chlorine. The chlorine containing gas may react with the precursor source to form a chloride. In order to increase the effectiveness of the chlorine containing gas to react with the precursor, the chlorine containing gas may snake through the boat area in the chamber 532 and be heated with the resistive heater 520. By increasing the residence time that the chlorine containing gas is snaked through the chamber 532, the temperature of the chlorine containing gas may be controlled. By increasing the temperature of the chlorine containing gas, the chlorine may react with the precursor faster. In other words, the temperature is a catalyst to the reaction between the chlorine and the precursor.

[0058] In order to increase the reactivity of the precursor, the precursor may be heated by a resistive heater 520 within the second chamber 532 in a boat. The chloride reaction product may then be delivered to the chamber 502. The reactive chloride product first enters a tube 522 where it evenly distributes within the tube 522. The tube 522 is connected to another tube 524. The chloride reaction product enters the second tube 524 after it has been evenly distributed within the first tube 522. The chloride reaction product then enters into the chamber 502 where it mixes with the nitrogen containing gas to form a nitride layer on a substrate 516 that is disposed on a susceptor 514. In one embodiment, the susceptor 514 includes silicon carbide. The nitride layer may include n-type gallium nitride for example. The other reaction products, such as nitrogen and chlorine, are exhausted through an exhaust 526.

[0059] The above described approaches and multi-chamber arrangements are not limited to a single PVD deposition operation or a single PVD deposition chamber. For example, prior to PVD aluminum nitride formation, a PVD tungsten film may be formed to effectively provide a metalized substrate. For example, Figure 6 illustrates a cross-sectional view of a gallium nitride (GaN)-based light-emitting diode (LED) formed on a metalized substrate, in accordance with an embodiment of the present invention.

[0060] Referring to Figure 6, a LED structure 600 includes a stack of various material layers, many of which include III-V materials. For example, the LED structure 600 includes a silicon or sapphire substrate 602 (Substrate: sapphire, Si) and

an approximately 10 – 200 nanometer thick tungsten layer 604 (PVD-W). The LED structure 600 also includes a thin, e.g., less than approximately 25 nanometers, aluminum nitride layer 606 (e.g., PVD AlN). The aluminum nitride layer 224 may be formed by low temperature or high temperature sputter deposition in the PVD aluminum nitride sputter chamber 202 of cluster tool 200. The LED structure 600 also includes an approximately 4 microns thick un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 608 (n-GaN). The un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 608 may be formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 of cluster tool 200. An MQW structure 610 with a thickness in the range of 150 – 300 nanometers is also included. The MQW structure 610 may be formed in MQW MOCVD reaction chamber 206 of cluster tool 200. In one embodiment, the MQW structure 610 is composed of one or a plurality of field pairs of InGaN well/GaN barrier material layers. The LED structure 600 also includes an approximately 20 nanometers thick p-type gallium aluminum nitride layer 612 (p-AlGaN) and a p-type gallium nitride layer 614 with a thickness in the range of 50 – 200 nanometers (p-GaN). The p-type gallium aluminum nitride layer 612 and the p-type gallium nitride layer 614 may be formed in p-type gallium nitride MOCVD reaction chamber 208 of cluster tool 200. It is to be understood that the above thicknesses or thickness ranges are exemplary embodiments, and that other suitable thicknesses or thickness ranges are also considered within the spirit and scope of embodiments of the present invention.

[0061] In an embodiment, the tungsten layer 604 is formed by a PVD process distinct from the PVD process used to form the aluminum nitride layer 606. For example in one embodiment, the method described in association with Flowchart 300 further includes, prior to forming the aluminum nitride layer, forming a tungsten (W) layer above the substrate in a second PVD chamber having a tungsten target. In one embodiment, one or more of the possible systems (in-line or cluster) described in association with multi-chamber system 200 further includes a second PVD chamber having a tungsten (W) target housed therein. In an alternative embodiment, a single PVD chamber houses both an aluminum nitride target and a tungsten target. In one such embodiment, the single PVD chamber is used to deposit, sequentially, both the tungsten layer 604 and the aluminum nitride layer 606.

[0062] By including a metal layer, such as a PVD deposited tungsten layer between a receiving substrate and the PVD aluminum layer, any strain otherwise

existing as a result of the proximity of the aluminum nitride layer and the receiving substrate may be mitigated or eliminated. Also, although silicon substrate embodiments are readily contemplated in the above description, inclusion of such a tungsten intermediate layer may further improve the compatibility of silicon substrates with group III-V material processing thereon. Other benefits may be with respect to processing enablement. For example, the relative easy of wet etching tungsten selective to group III-V material layers and to silicon and sapphire substrates may make patterning and transfer of such stacks more accessible.

[0063] LEDs and related devices may be fabricated from layers of, e.g., group III-V films, especially group III-nitride films. Some embodiments of the present invention relate to forming gallium nitride (GaN) layers in a dedicated chamber of a fabrication tool, such as in a dedicated MOCVD chamber. In some embodiments of the present invention, GaN is a binary GaN film, but in other embodiments, GaN is a ternary film (e.g., InGaN, AlGaN) or is a quaternary film (e.g., InAlGaN). In at least some embodiments, the group III-nitride material layers are formed epitaxially. They may be formed directly on a substrate or on a buffers layer disposed on a substrate. Other contemplated embodiments include p-type doped gallium nitride layers deposited directly on PVD-formed buffer layers, e.g., PVD-formed aluminum nitride.

[0064] It is to be understood that embodiments of the present invention are not limited to formation of layers on the select substrates described above. Other embodiments may include the use of any suitable non-patterned or patterned single crystalline substrate upon which a high quality aluminum nitride layer may be sputter-deposited, e.g., in a non-reactive PVD approach. The substrate may be one such as, but not limited to, a sapphire (Al_2O_3) substrate, a silicon (Si) substrate, a silicon carbide (SiC) substrate, a silicon on diamond (SOD) substrate, a quartz (SiO_2) substrate, a glass substrate, a zinc oxide (ZnO) substrate, a magnesium oxide (MgO) substrate, and a lithium aluminum oxide (LiAlO_2) substrate. Any well know method, such as masking and etching may be utilized to form features, such as posts, from a planar substrate to create a patterned substrate. In a specific embodiment, however, a patterned sapphire substrate (PSS) is used with a (0001) orientation. Patterned sapphire substrates may be ideal for use in the manufacturing of LEDs because they increase the light extraction efficiency which is extremely useful in the fabrication of a new generation of solid state lighting devices. Substrate selection criteria may include

lattice matching to mitigate defect formation and coefficient of thermal expansion (CTE) matching to mitigate thermal stresses.

[0065] As described above, the group III-nitride films can be doped. The group III-nitride films can be p-typed doped using any p-type dopant such as but not limited Mg, Be, Ca, Sr, or any Group I or Group II element have two valence electrons. The group III-nitride films can be p-type doped to a conductivity level of between 1×10^{16} to 1×10^{20} atoms/cm³. The group III-nitride films can be n-typed doped using any n-type dopant such as but not limited silicon or oxygen, or any suitable Group IV or Group VI element. The group III-nitride films can be n-type doped to a conductivity level of between 1×10^{16} to 1×10^{20} atoms/cm³.

[0066] It is to be understood that the above processes may be performed in a dedicated chamber within a cluster tool, or other tool with more than one chamber, e.g. an in-line tool arranged to have a dedicated chamber for fabricating layers of an LED. It is also to be understood that embodiments of the present invention need not be limited to the fabrication of LEDs. For example, in another embodiment, devices other than LED devices may be fabricated by approaches described herein, such as but not limited to field-effect transistor (FET) devices. In such embodiments, there may not be a need for a p-type material on top of a structure of layers. Instead, an n-type or un-doped material may be used in place of the p-type layer. It is also to be understood that multiple operations, such as various combinations of depositing and/or thermal annealing, may be performed in a single process chamber.

[0067] Thus, fabrication of gallium nitride-based LEDs with PVD-formed aluminum nitride buffer layers has been disclosed. In accordance with an embodiment of the present invention, a multi-chamber system includes a PVD chamber having a target composed of a material including aluminum. A chamber adapted to deposit un-doped or n-type gallium nitride, or both, is also included in the multi-chamber system. In one embodiment, the target of the PVD chamber is composed of aluminum nitride. In one embodiment, the chamber adapted to deposit un-doped or n-type gallium nitride is a MOCVD chamber. In one embodiment, the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in a cluster or an in-line tool arrangement.

CLAIMS

What is claimed is:

1. A multi-chamber system, comprising:
 - a physical vapor deposition (PVD) chamber having a target comprising aluminum;
 - and
 - a chamber adapted to deposit un-doped or n-type gallium nitride, or both.
2. The system of claim 1, wherein the target of the PVD chamber comprises aluminum nitride.
3. The system of claim 1, wherein the chamber adapted to deposit un-doped or n-type gallium nitride comprises a metal-organic chemical vapor deposition (MOCVD) chamber.
4. The system of claim 1, wherein the chamber adapted to deposit un-doped or n-type gallium nitride comprises a hydride vapor phase epitaxy (HVPE) chamber.
5. The system of claim 1, wherein the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in a cluster tool arrangement.
6. The system of claim 1, wherein the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in an in-line tool arrangement.
7. The system of claim 1, further comprising:
 - a rapid thermal processing (RTP) chamber or a laser annealing chamber.
8. A method of fabricating a light-emitting diode (LED) structure, the method comprising:
 - forming, in a physical vapor deposition (PVD) chamber of a multi-chamber system, an aluminum nitride layer above a substrate; and
 - forming, in a second chamber of the multi-chamber system, an un-doped or n-type gallium nitride layer on the aluminum nitride layer.

9. The method of claim 8, wherein forming the aluminum nitride layer comprises sputtering from an aluminum nitride target housed in the PVD chamber.
10. The method of claim 8, wherein forming the un-doped or n-type gallium nitride layer in the second chamber comprises forming in a first metal-organic chemical vapor deposition (MOCVD) chamber.
11. The method of claim 10, further comprising:
 - forming, in a second MOCVD chamber of the multi-chamber system, a multiple quantum well (MQW) structure above the un-doped or n-type gallium nitride layer; and
 - forming, in a third MOCVD chamber of the multi-chamber system, a p-type aluminum gallium nitride or p-type gallium nitride layer above the MQW structure.
12. The method of claim 8, wherein forming the aluminum nitride layer comprises forming at a substrate temperature approximately in the range of 20 – 200 degrees Celsius.
13. The method of claim 8, wherein forming the aluminum nitride layer comprises forming at a substrate temperature approximately in the range of 200 – 1200 degrees Celsius.
14. The method of claim 8, further comprising:
 - prior to forming the un-doped or n-type gallium nitride layer on the aluminum nitride layer, annealing the aluminum nitride layer in a rapid thermal processing (RTP) chamber.
15. The method of claim 8, further comprising:
 - prior to forming the aluminum nitride layer, forming a tungsten (W) layer above the substrate in a second PVD chamber having a tungsten target.

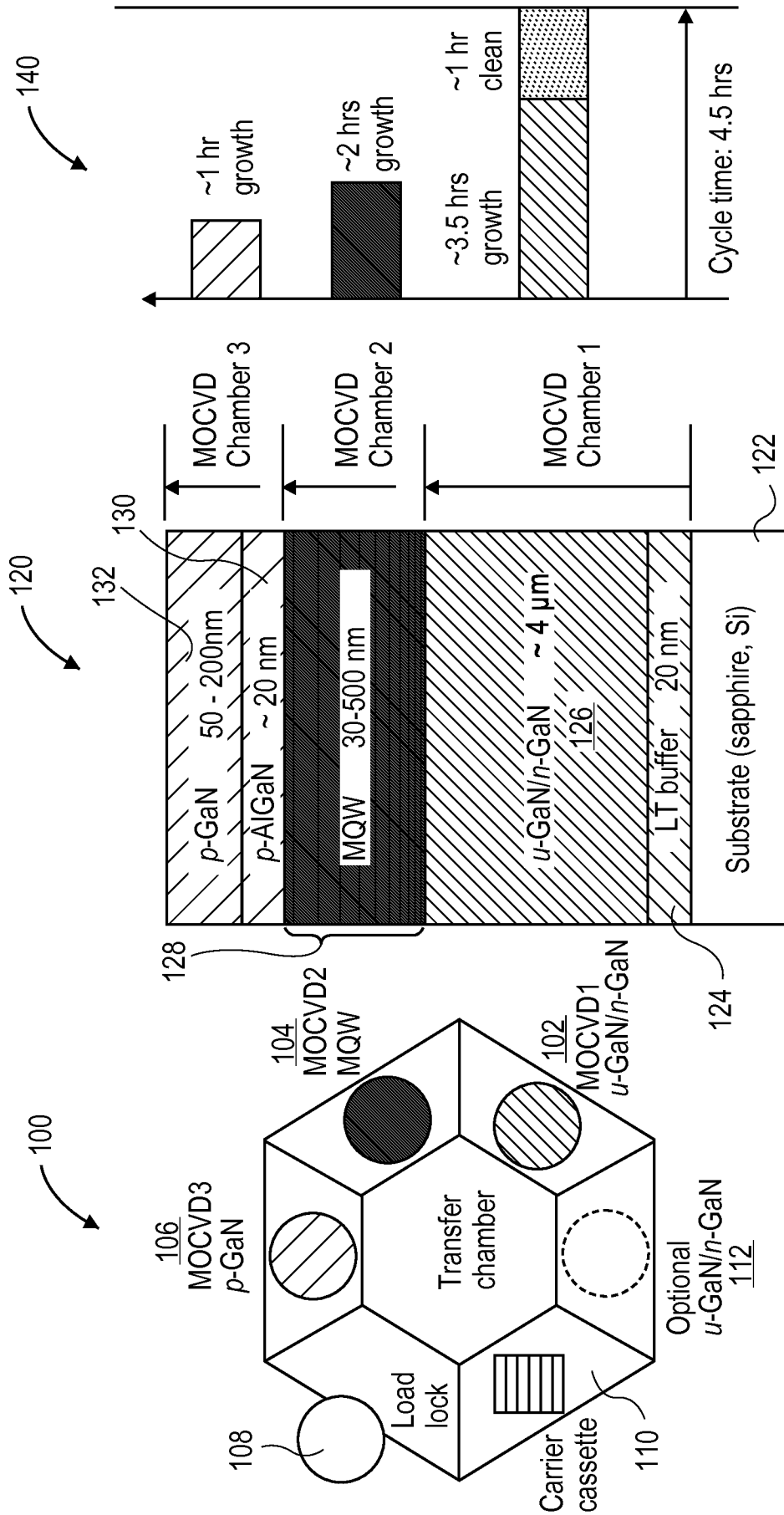
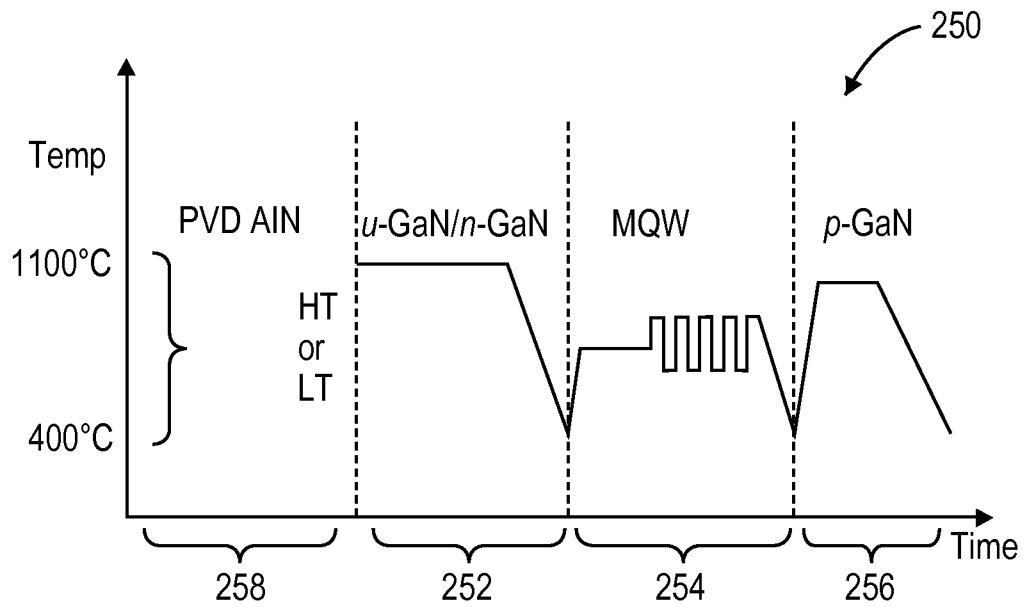
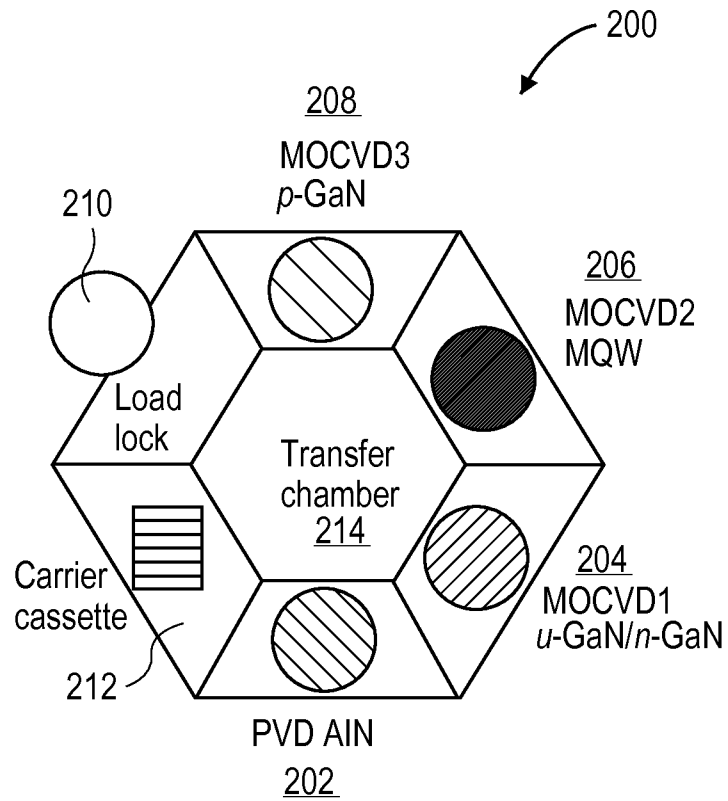


FIG. 1

**FIG. 2A**

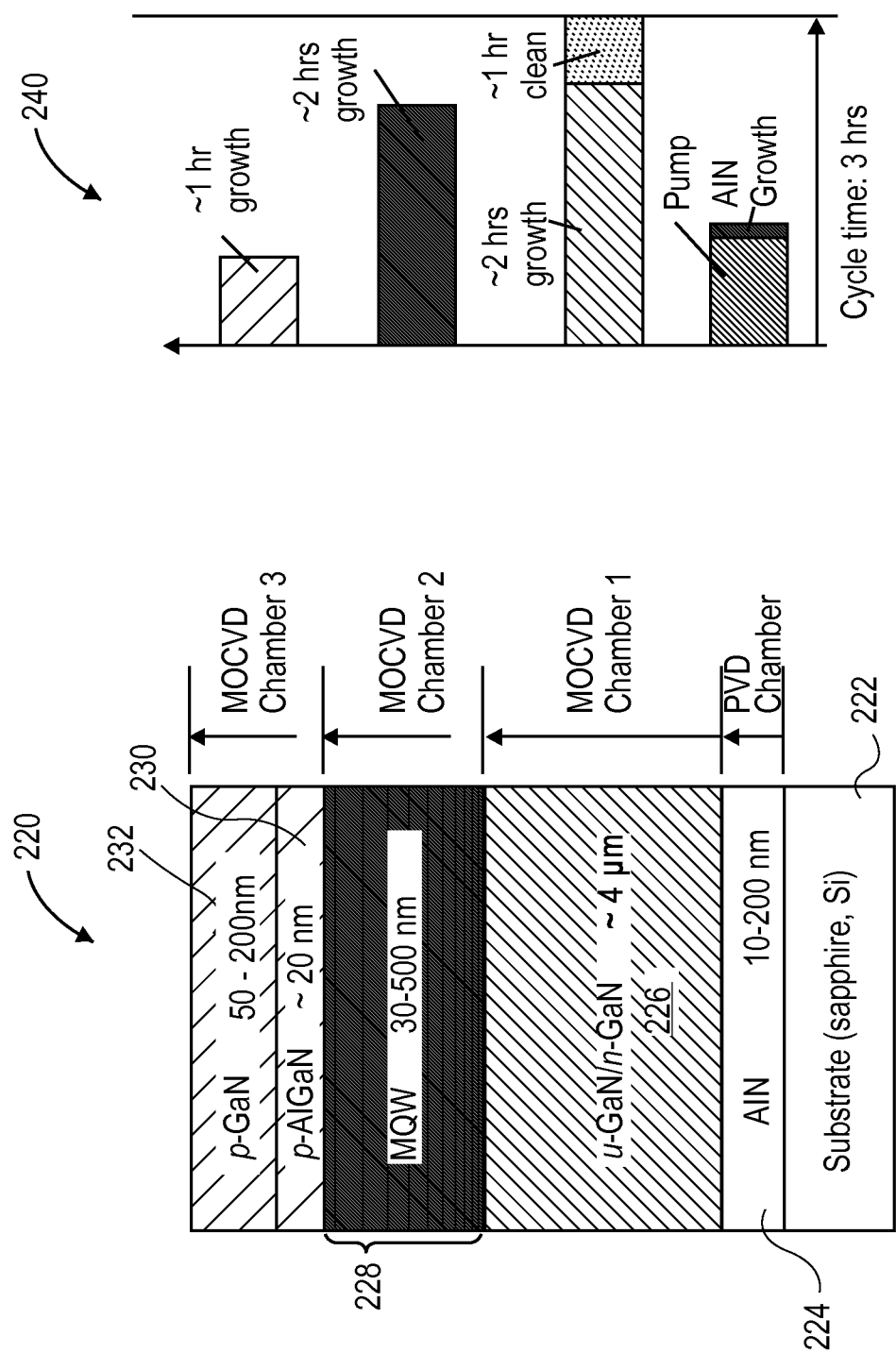
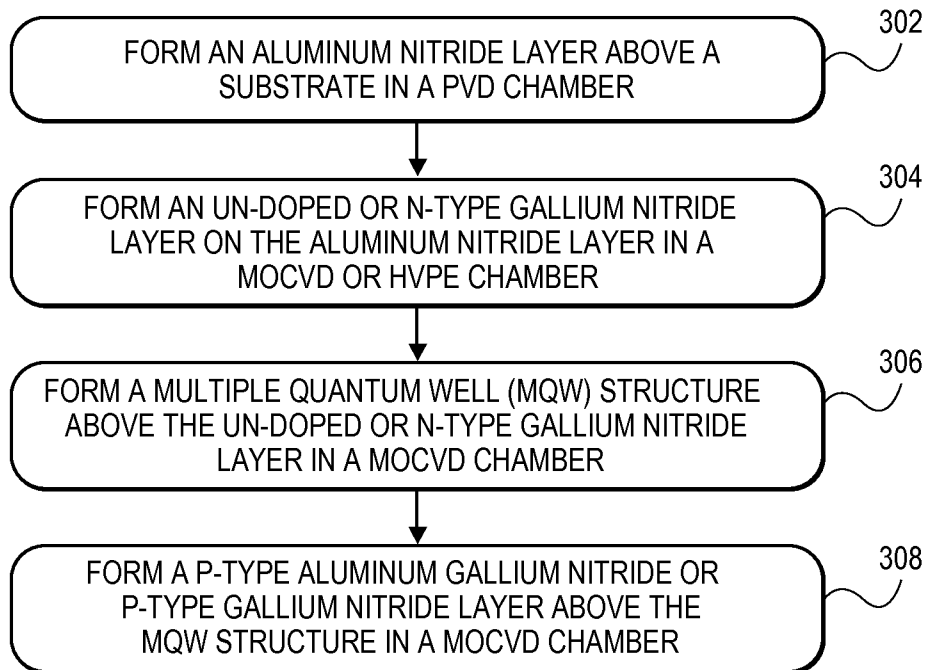


FIG. 2B

FLOWCHART 300

**FIG. 3**

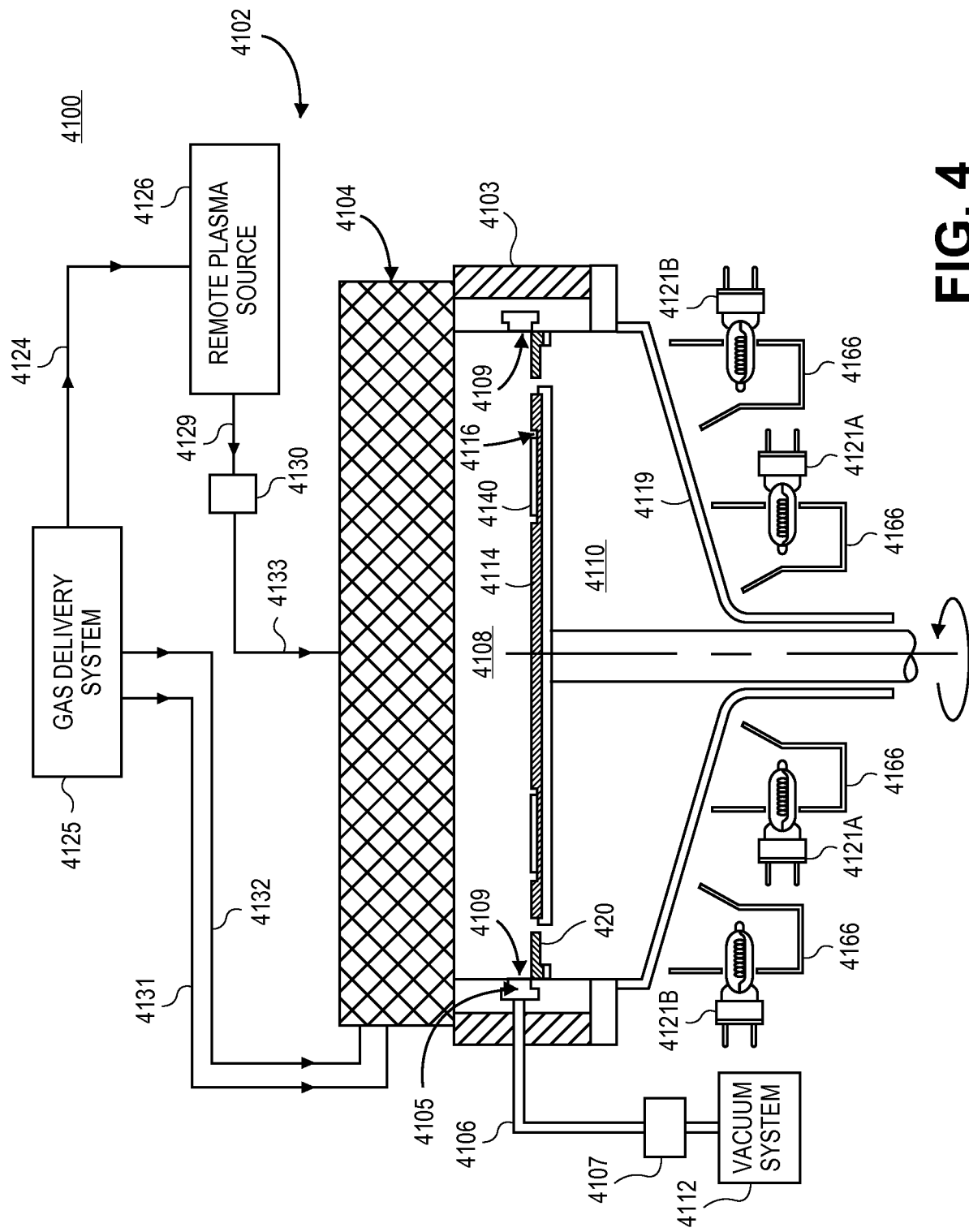


FIG. 4

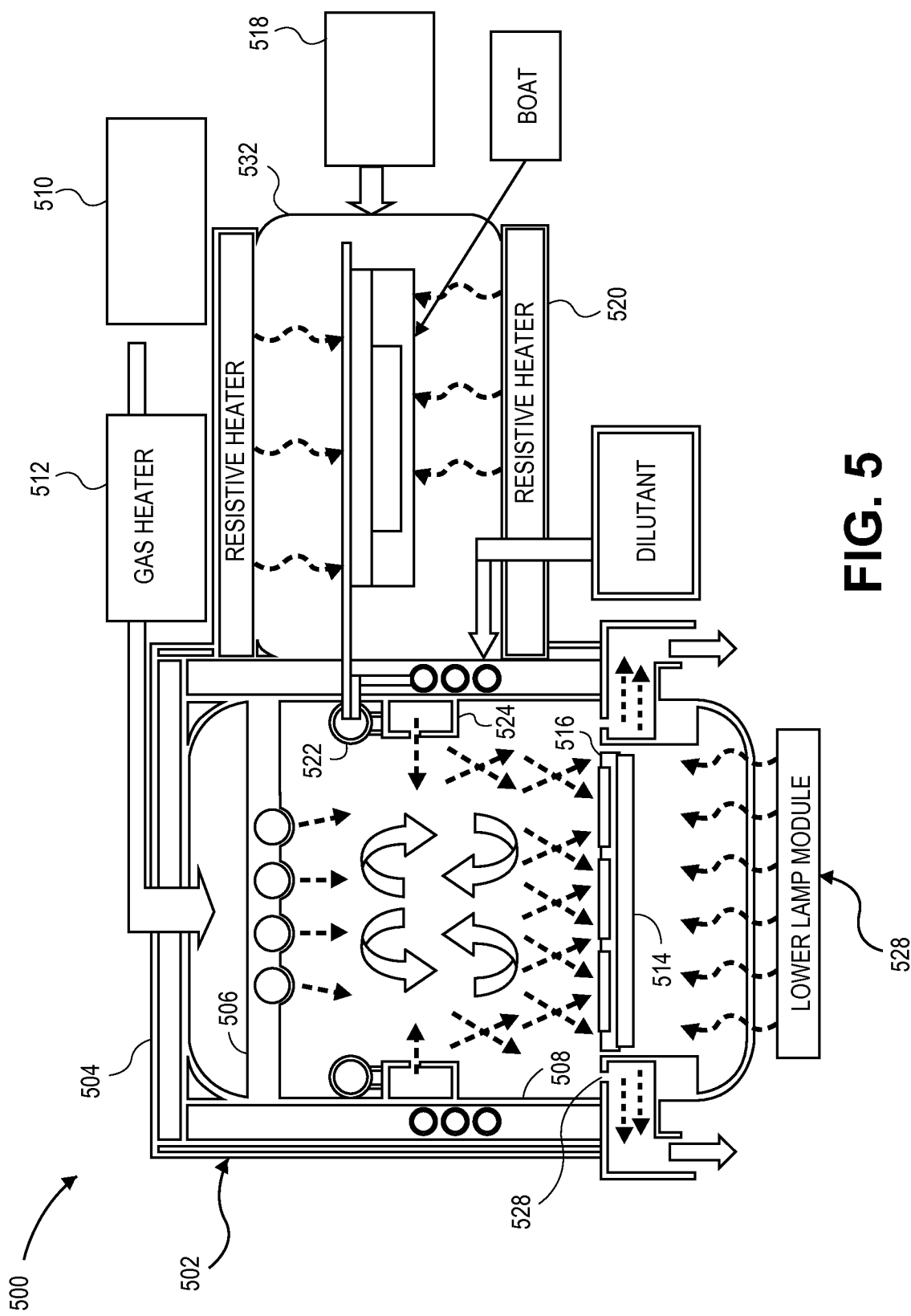
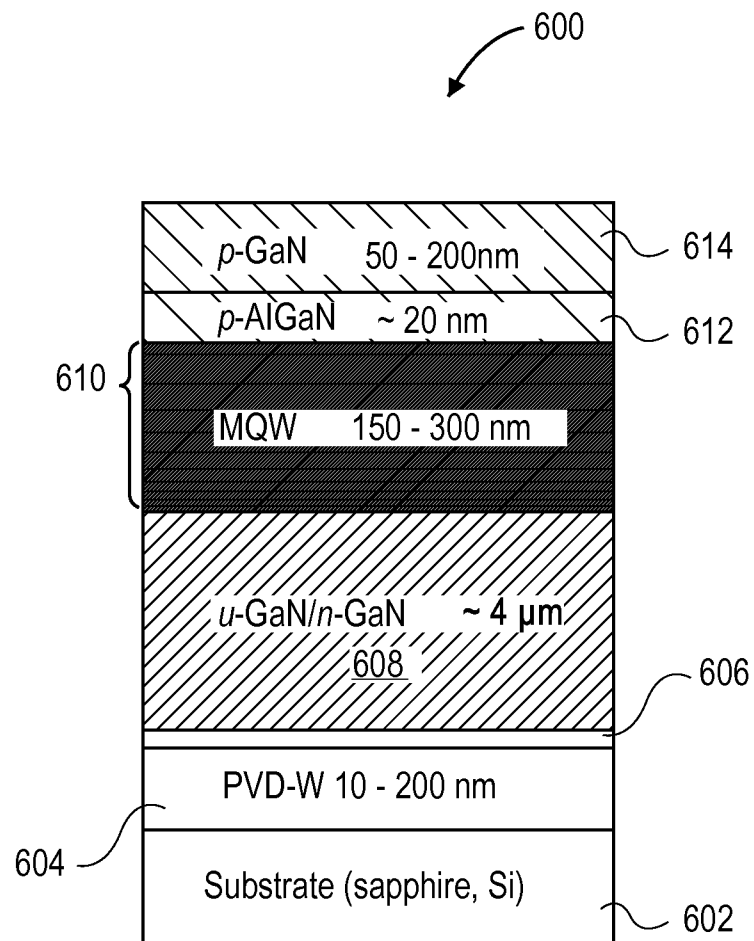


FIG. 5

**FIG. 6**