(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 September 2006 (21.09.2006)

PCT

(10) International Publication Number
WO 2006/099198 A1

(51) International Patent Classification:
H01L 21/8238 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2006/008707

(22) International Filing Date: 8 March 2006 (08.03.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/078,267 11 March 2005 (11.03.2005) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

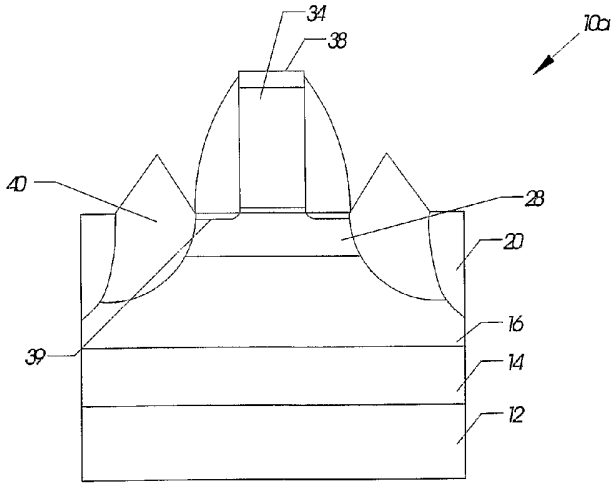
(75) Inventors/Applicants *(for US only)*: **KAVALIEROS, Jack** [US/US]; 14260 Nw Belle Court, Portland, Oregon 97229 (US). **BRASK, Justin** [US/US]; 12748 Nw Bayonne Lane, Portland, Oregon 97229 (US). **DOCZY, Mark** [US/US]; 2922 Nw Norwalk Place, Beaverton, Oregon 97006 (US). **METZ, Matthew** [US/US]; 3136 Ne 13th Ave, Hillsboro, or 97124 (US). **DATTA, Suman** [IN/US]; 16659 Nw Talkingstick Way, Beaverton, Oregon 97006 (US). **DOYLE, Brian** [IE/US]; 11156 Nw Montreux Lane, Portland, Oregon 97229 (US). **CHAU, Robert** [US/US]; 8875 Sw 171st Avenue, Beaverton, Oregon 97007 (US). **WANG, Everett** [US/US]; 1185 Keystone Court, San Jose, California 95132 (US). **MATAGNE, Philippe** [BE/US]; 2515 Sw 171st Place, Beaverton, Oregon 97006 (US). **SHIFREN, Lucian** [ZA/US]; 7123 Ne Rocky Brook St, Hillsboro, Oregon 97124 (US). **JIN, Been** [US/US]; 12872 Sierra Court, Lake Oswego, Oregon 97035 (US). **STETTLER, Mark** [US/US]; 3266 Ne Glencoe Oaks Place, Hillsboro, Oregon 97124 (US). **GILES, Martin** [GB/US]; 12749 Nw Diamond Drive, Portland, Oregon 97229 (US).

(74) Agents: **TROP, Timothy, N.** et al.; TROP, PRUNER & HU, P.C., 1616 S. Voss Rd., Suite 750, Houston, TX 77057-2631 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI,

[Continued on next page]

(54) Title: COMPLEMENTARY METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUIT USING UNIAXIAL COMPRESSIVE STRESS AND BIAXIAL COMPRESSIVE STRESS



(57) Abstract: A transistor may be formed of different layers of silicon germanium, a lowest layer having a graded germanium concentration and upper layers having constant germanium concentrations such that the lowest layer is of the form Si1-xGex. The highest layer may be of the form Si1-yGey on the PMOS side. A source and drain may be formed of epitaxial silicon germanium of the form Si1-zGez on the PMOS side. In some embodiments, x is greater than y and z is greater than x in the PMOS device. Thus, a PMOS device may be formed with both uniaxial compressive stress in the channel direction and in-plane biaxial compressive stress. This combination of stress may result in higher mobility and increased device performance in some cases.

WO 2006/099198 A1

NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUIT USING UNIAXIAL COMPRESSIVE STRESS AND BIAXIAL COMPRESSIVE STRESS

Background

This invention relates generally to the fabrication of integrated circuits.

To increase performance of NMOS and PMOS deep sub-micron transistors in CMOS technology, current state-of-the-art technology uses compressive stress in the channel of the PMOS transistors, and tensile stress in the case of NMOS transistors. This is usually achieved by substrate induced strain which is a very expensive technology option and is also difficult to implement using a single substrate approach.

Brief Description of the Drawings

Figure 1 is an enlarged, cross-sectional view of an NMOS transistor at an early stage of manufacture;

Figure 2 is an enlarged, cross-sectional view of a PMOS transistor at an early stage of manufacture;

Figure 3 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 1 in accordance with one embodiment of the present invention;

Figure 4 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 2 in accordance with one embodiment of the present invention;

Figure 5 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 3 in accordance with one embodiment of the present invention;

Figure 6 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 4 in accordance with one embodiment of the present invention;

Figure 7 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 6 in accordance with one embodiment of the present invention;

Figure 8 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 7 in accordance with one embodiment of the present invention;

Figure 9 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 8 in accordance with one embodiment of the present invention;

Figure 10 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 9 in accordance with one embodiment of the present invention; and

Figure 11 is an enlarged, cross-sectional view at a stage subsequent to the stage shown in Figure 5 in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a silicon substrate 12 may be covered by a graded buffer layer 14. The buffer layer 14 may be formed of silicon germanium of the formula $Si_{1-x}Ge_x$ where x is from .05 to .3. In one embodiment, the buffer layer 14 may be epitaxially grown, while gradually increasing the concentration of germanium. Thus, the germanium concentration is highest at the top of the layer 14, lowest at the bottom, and linearly increases from bottom to top in one embodiment.

Over the layer 14 may be deposited a constant concentration silicon germanium buffer layer 16. In one embodiment of the present invention, this layer 16 may have a thickness of from 2000 to 10,000 Angstroms. The layer 16 may have a constant germanium concentration substantially equal to that of the highest germanium level of the layer 14, in one embodiment.

A tensile strained silicon layer 18 is formed thereover. Shallow trench isolations 20 may be provided as well. In one embodiment of the present invention, the structure 10b, shown in Figure 1, will be utilized to form both NMOS and PMOS transistors of a complementary metal oxide semiconductor integrated circuit technology.

The gradient of germanium in the graded buffer layer 14 can vary depending on the thickness and final germanium concentration. In some embodiments, the concentration of germanium in the graded layer 14 extends from about zero percent at the bottom to about 40 percent at the top. Other percentages may be utilized in different situations. The layer 14 functions to achieve a relaxed silicon germanium layer and to reduce dislocation formation due to mismatch in the lattice constraints between silicon and the silicon germanium. The constant germanium concentration silicon germanium buffer layer 16 further stabilizes the structure.

The tensile strained silicon layer 18 may be grown. The strained nature of the layer 18 is limited by the critical layer thickness associated with the concentration of germanium in the underlying buffer layer 16.

At the same time, the PMOS structure 10a may be fabricated, as shown in Figure 2. The PMOS structure 10a may initially have the same components as the NMOS structure 10b.

Thereafter, as shown in Figure 3, a hard mask 21 may be deposited over the tensile strained silicon layer 18 on the NMOS side 10b and PMOS side 10a.

Then, a hard mask etch and resist removal may be utilized to remove the tensile strained silicon 18 and the hard mask 21 on the PMOS transistor structure 10a as shown in Figure 4. The selective etch may use 5 to 8 percent NH_4OH with a pH between about 10.2 and 10.4 at a temperature between 20°C and 27°C in one embodiment. The resulting structure has the tensile strained silicon removed on the PMOS side 10a. The NMOS side 10b is still covered by the hard mask 21 (Figure 3).

The selective wet etch of the strained silicon layer 18 is such that nucleophillic binding energy of silicon is surpassed and an etch of the silicon layer 18 is effected. However, the nucleophillic binding energy may be only about 0.5 kJ/mol too little to solubilize the germanium to the corresponding aqueous species, so the layer 16 is preserved.

Then, a compressively strained silicon germanium layer 28 is deposited as shown in Figure 6 on the PMOS side 10a. The silicon germanium may be of the formula $Si_{1-y}Ge_y$, where y is greater than x. The higher concentration y means the layer 28 has a larger lattice than the underlying layers, resulting in compressive strain applied upwardly by the layers 14 and 16 to biaxially compress the layer 28.

The layer 28 may be selectively grown on the PMOS side 10a only and not on the NMOS side 10b as indicated in Figure 5 because only the NMOS side 10b was covered by the hard mask 21 at the time the layer 28 was deposited.

The fabrication of the PMOS transistor proceeds as shown in Figures 7-11. On both the NMOS and PMOS sides a silicon dioxide gate oxide 30 may be deposited in one embodiment. The gate oxide 30 may be covered by a gate material 34, such as polysilcon, in turn covered by a hard mask 34 for patterning. Then the gate material 34 and gate oxide 30 are patterned to generate the Figure 7 structure on the PMOS side 10a (and the same structure is created on the NMOS side 10b with the layer 18 replacing the layer 28).

Then, separate tip implants I (Figure 7) and standard lithographic patterning form the lightly doped source drain regions 39 on both NMOS and PMOS sides (Figure 8). A nitride spacer material may be deposited and anisotropically etched on both NMOS and PMOS sides to form the spacers 36.

On the PMOS side 10a only, a trench 24 is formed through the layer 28 and into the layer 16, as shown in Figure 9. The trench 24 may be formed by reactive ion etching

using SF_6 chemistry. The etching is constrained by the isolation 20 on one side and may isotropically undercut the gate structure on the other side. As a result, an isotropic etch profile may be achieved on the inward edges of the trench 24 as shown in Figure 9. During this step the NMOS side 10a may be covered by an oxide mask (not shown).

Then, an epitaxial silicon germanium source drain 40 may be grown which fills the trench 24 and extends thereabove as indicated at Figure 10. The trench 24 may be filled using silicon germanium having 10-40 atomic percent germanium. Source drain doping may be done by insitu doping using a diborane source. The epitaxial source drain 40 only grows in the trench 24 because all other material is masked or covered. The source drain 40 is raised and continues to grow until the facets meet.

The fabrication of the NMOS transistor 10b, shown in Figure 11, proceeds correspondingly. However, a conventionally non-epitaxially grown deeper source drain (not shown) may be created.

The PMOS device 10a may have both uniaxial compressive stress in the channel direction and in-plane biaxial compressive stress. The $Si_{1-y}Ge_y$ layer 28 acts as a channel and is grown on a relaxed $Si_{1-x}Ge_x$ buffer layer 16 with x less than y to produce in-plane biaxial compressive stress. In addition, a silicon germanium epitaxial source drain 40 produces uniaxial compressive stress in the channel <110> crystallographic direction. The source drain 40 has a higher germanium concentration than the layer 14 so the source drain 40 pushes inwardly from the sides compressing layer 28. With this combination of stress, higher mobility and, thus, higher device performance may be achieved compared to using either of the stresses alone in some embodiments.

Once the optimal stress condition is known, the device may be engineered to produce such stress through an epitaxial silicon germanium source drain 40 and a silicon germanium layered structure. Then, a graded silicon germanium buffer layer 14 may be grown on the silicon substrate 12 followed by a relaxed $Si_{1-x}Ge_x$ layer 16 as shown in Figure 10. Then, a thin $Si_{1-y}Ge_y$ layer 28 is grown to form a biaxial compressive strained channel.

The uniaxial stress is produced by the epitaxial source drain process using epitaxial $Si_{1-z}Ge_z$ grown in recessed source drain regions 40. Selecting the germanium fractions so that x is less than y and z is less than x achieves the desired compressive states.

The mobility gain may remain high even as vertical field (gate field) is applied in some embodiments. In addition, more head room may be provided to increase

performance before the device hits the physical stress limit in some embodiments. With the provision of combined stress, holes may stay in their lowest transport effective mass in the <110> channel direction where scattering suppression is also the strongest. Silicon band structure has a minimum at the gamma point. It also has twelve wings in (0, +-1, +-1), (+-1, 0, +-1) and (+-1, +-1, 0) directions. Ideally, almost all of the holes are placed in two wings in the (1, -1, 0) and (-1, 1, 0) direction to achieve the lowest possible transport effective mass in the channel direction. This can be achieved by applying both uniaxial compressive and biaxial compressive stress.

The biaxial compressive stress lowers the energy level of the four in-plane wings and removes holes from the eight off plane wings, placing them in the four in-plane wings. The four in-plane wings not only have smaller effective mass, but also have smaller density states, which leads to a reduction of scattering. The greatest mobility enhancement happens when the uniaxial compressive stress along the channel direction is added to the biaxial compressed device.

According to simulation, when hole-optical phonon and surface roughness scattering occurs, most of the holes stay only in the wings along (1, -1, 0) and (-1, 1, 0), which has the smallest transport effective mass in the channel direction. Since only two wings are occupied, the density of states is also greatly reduced, enhancing scattering suppression. As a result, the combination stressed device may have higher mobility.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A method comprising:

forming a PMOS transistor having both uniaxial compressive stress in the channel direction and in-plane biaxial compressive stress.

2. The method of claim 1 including forming a substrate covered by a first layer having an increasing concentration of germanium extending upwardly through the layer.

3. The method of claim 2 including covering said first layer with a second layer of constant germanium concentration.

4. The method of claim 3 including forming said second layer of $Si_{1-y}Ge_y$ and forming the first layer with $Si_{1-x}Ge_x$ where x is less than y.

5. The method of claim 4 including forming a source and drain of epitaxial silicon germanium of the form
$Si_{1-z}Ge_z$.

6. The method of claim 5 including making z greater than x and x less than y.

7. The method of claim 1 including forming uniaxial compressive stress in the channel direction by forming a silicon germanium epitaxial source drain.

8. The method of claim 1 including forming in-plane biaxial compressive stress by depositing a silicon germanium layer as a channel having the form $Si_{1-y}Ge_y$ and forming an underlying buffer layer of the form $Si_{1-x}Ge_x$ where x is less than y.

9. The method of claim 1 including forming NMOS and PMOS transistors at the same time.

10. The method of claim 9 including forming a graded germanium concentration silicon germanium buffer layer, covering said buffer layer with a layer of

silicon germanium of constant germanium concentration, and covering said constant germanium concentration layer with a tensile strained silicon layer on both the NMOS and PMOS sides.

11. The method of claim 10 including selectively removing the tensile strained biaxial silicon layer on the PMOS side.

12. The method of claim 11 including selectively removing the tensile strained silicon layer using about 5 to 8 percent NH_4OH with a pH between about 10.2 and 10.4 at a temperature between about 20°C and 27°C.

13. The method of claim 11 including removing said tensile strained silicon layer on the PMOS side using an etchant that solubilizes the tensile strained silicon layer but does not solubilize underlying layers having higher germanium concentrations.

14. A semiconductor structure comprising:

a substrate having a raised source drain of $Si_{1-z}Ge_z$;

a gate electrode;

a first layer under said gate electrode of $Si_{1-y}Ge_y$; and

a second layer underneath said first layer, said second layer having $Si_{1-x}Ge_x$.

15. The structure of claim 14 wherein z is greater than x.

16. The structure of claim 15 wherein x is less than y.

17. The structure of claim 14 wherein said second layer has a graded germanium concentration.

18. The structure of claim 17 wherein said graded germanium concentration increases as it extends towards the gate electrode.

19. The structure of claim 14 including a third layer between said first and second layers.

20. The structure of claim 19 wherein said third layer has a relatively constant concentration germanium.

21. The structure of claim 20 wherein said third layer includes a concentration of germanium approximately equal to the maximum concentration of germanium in said second layer.

22. A semiconductor structure comprising:

a substrate;

a gate electrode over said substrate; and

a channel under said gate electrode having uni-axial compressive stress and in-plane biaxial compressive stress.

23. The structure of claim 22 including an epitaxial source drain of $Si_{1-z}Ge_z$.

24. The structure of claim 23 including a first layer under said gate electrode of $Si_{1-y}Ge_y$ and a second layer under said first layer, said second layer having $Si_{1-x}Ge_x$.

25. The structure of claim 24 wherein z is greater than x.

26. The structure of claim 25 wherein x is less than y.

27. The structure of claim 24 wherein said second layer has a graded germanium concentration.

28. The structure of claim 27 wherein said graded germanium concentration increases as it extends towards the gate electrode.

29. The structure of claim 24 including a third layer between said first and second layers.

30. The structure of claim 29 wherein said third layer has a relatively constant concentration germanium.

31. The structure of claim 30 wherein said third layer includes a concentration of germanium approximately equal to the maximum concentration of germanium in said second layer.

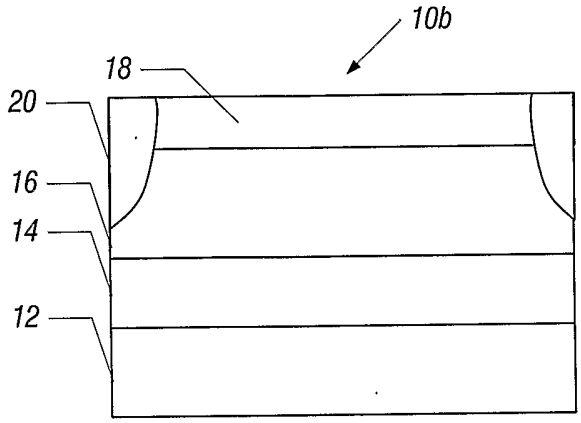


FIG. 1

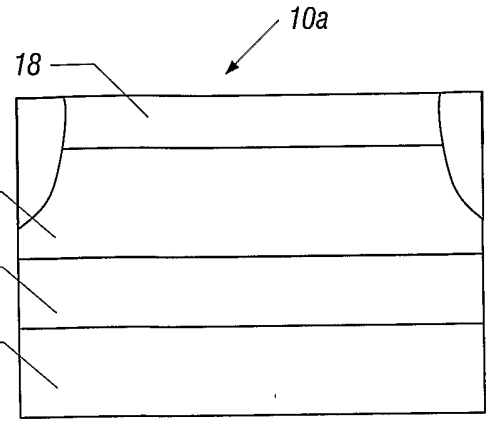


FIG. 2

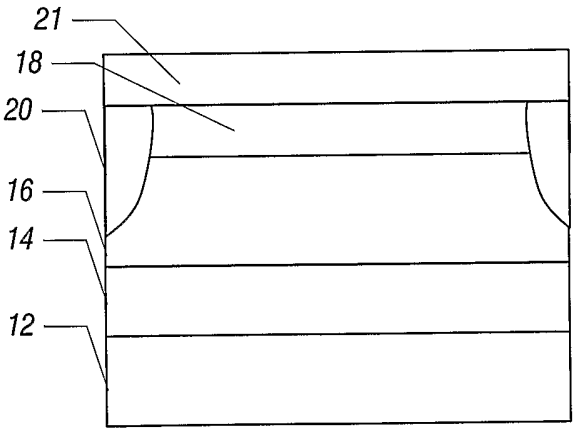


FIG. 3

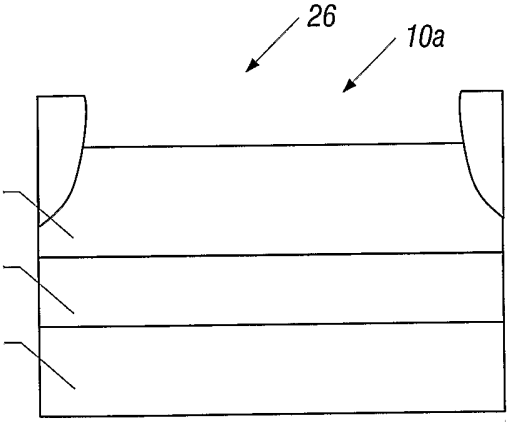


FIG. 4

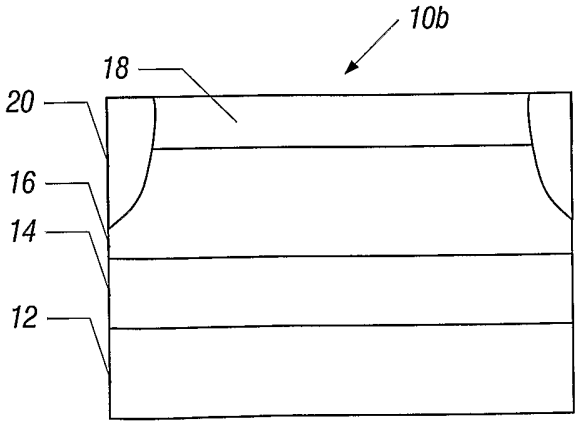


FIG. 5

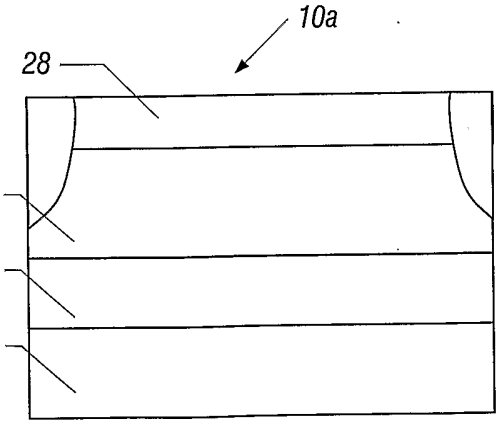


FIG. 6

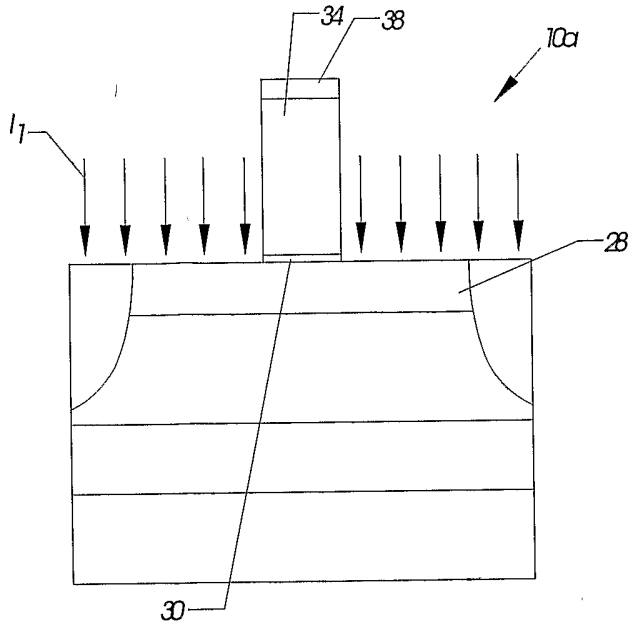


FIG 7

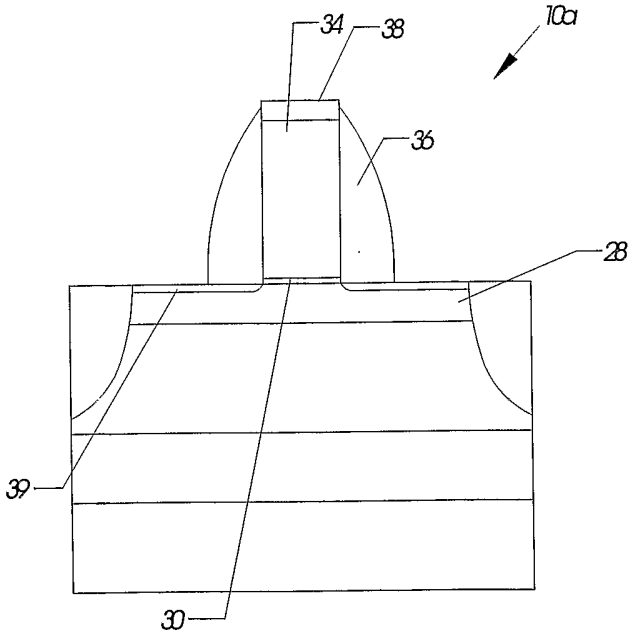


FIG 8

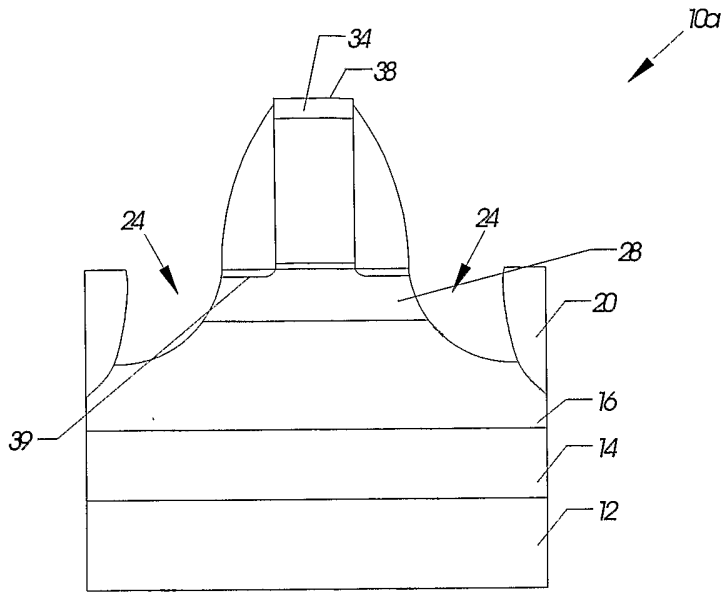


FIG 9

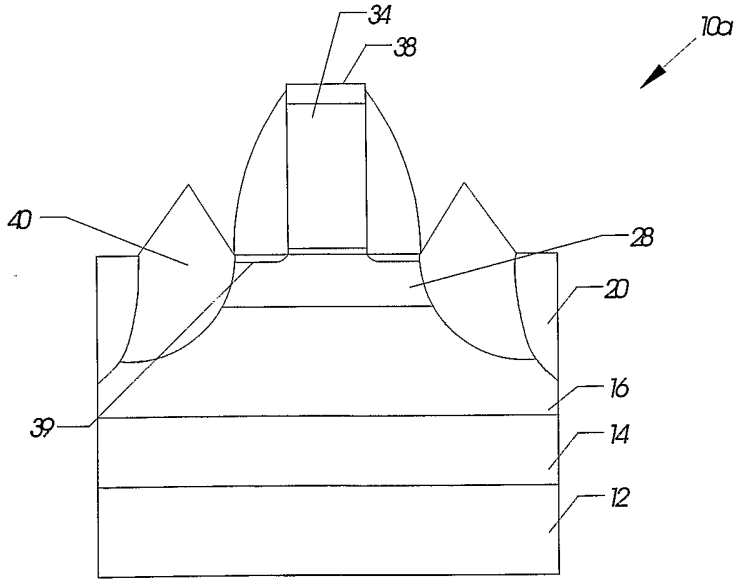


FIG 10

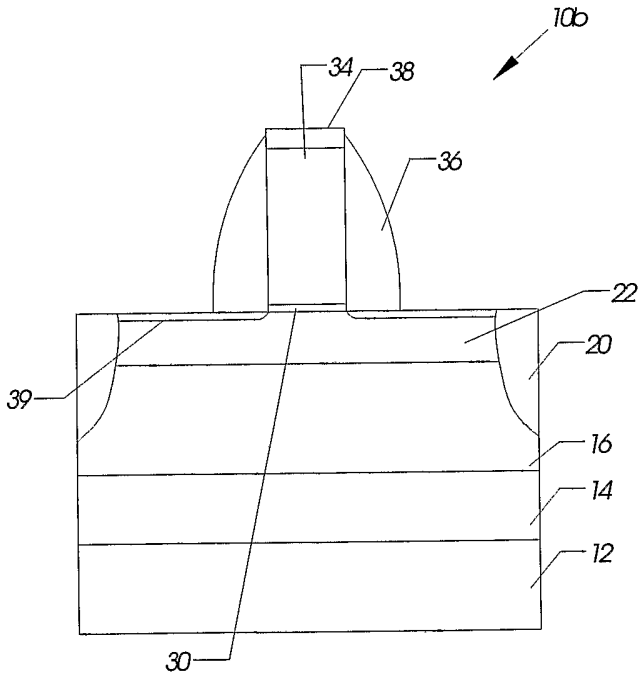


FIG 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/008707

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8238 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 174 928 A (HITACHI, LTD) 23 January 2002 (2002-01-23) paragraphs [0051] - [0056]; figure 11	1-4, 8-10,22
Y		1-31
Y	US 2003/080361 A1 (MURTHY ANAND ET AL) 1 May 2003 (2003-05-01) abstract	1-10, 14-31
Y	US 6 600 170 B1 (XIANG QI) 29 July 2003 (2003-07-29) abstract	11-13
A	US 2004/262683 A1 (BOHR MARK T ET AL) 30 December 2004 (2004-12-30) paragraphs [0022] - [0024], [0027], [0028]; figures 3-7	1,5-7, 14,22

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 August 2006	11/08/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ott, A

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/008707

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/026765 A1 (CURRIE MATTHEW T ET AL) 12 February 2004 (2004-02-12) paragraphs [0043] - [0107]; figures -----	1-31

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/008707

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1174928 A	23-01-2002	AU 3330600 A	23-10-2000
		CN 1349662 A	15-05-2002
		CN 1716570 A	04-01-2006
		WO 0060671 A1	12-10-2000
		JP 2000286418 A	13-10-2000
		TW 557577 B	11-10-2003
US 2003080361 A1	01-05-2003	US 2004084735 A1	06-05-2004
		US 2004070035 A1	15-04-2004
US 6600170 B1	29-07-2003	NONE	
US 2004262683 A1	30-12-2004	AU 2003297139 A1	14-02-2005
		CN 1577890 A	09-02-2005
		EP 1639636 A1	29-03-2006
		WO 2005010982 A1	03-02-2005
US 2004026765 A1	12-02-2004	NONE	