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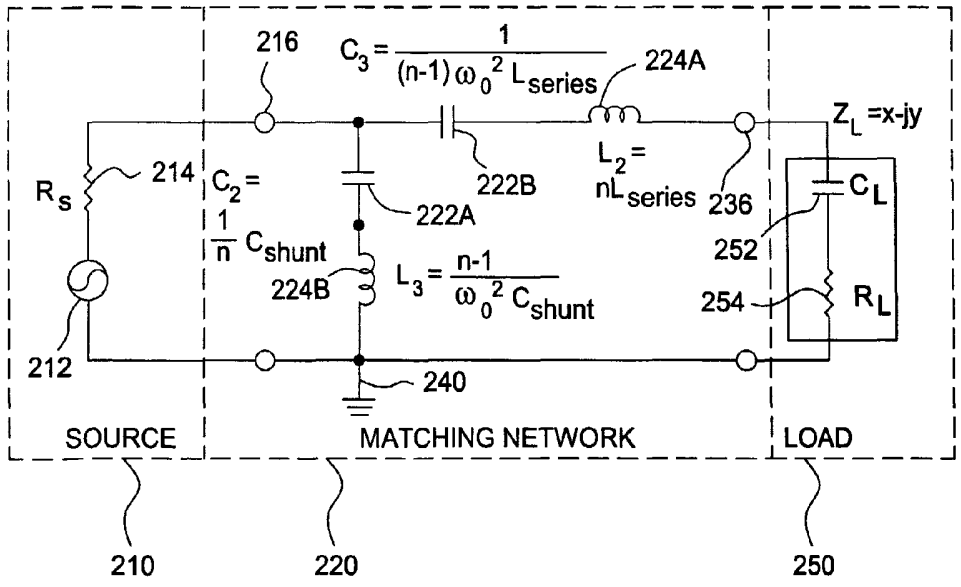
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(54) Title: FIXED MATCHING NETWORK WITH INCREASED MATCH RANGE CAPABILITIES



(57) Abstract: A matching network for performing frequency tuned matching between a source and a load. The matching network includes a first capacitor and first inductor, having fixed values, coupled in series from an input port to an output port. A second capacitor and second inductor, having fixed values, is coupled in series from one of the input port and output port to ground. The input port is adapted to receive a variable frequency RF signal and the output port is adapted to be coupled to a time-variant load impedance. The values of the first inductor and first capacitor are related by a first mathematical relationship, and the values of the second inductor and second capacitor are related by a second mathematical relationship. The substantial impedance range of the matching network enables a match to be maintained over a large fluctuation in load impedance.

WO 2004/015861 A1

FIXED MATCHING NETWORK WITH INCREASED MATCH RANGE CAPABILITIES

FIELD OF THE INVENTION

[0001] The invention relates to an impedance matching network for matching the impedance of a variable frequency radio frequency (RF) signal source to the time-variant impedance of a load and, more particularly, to broadband impedance matching networks.

DESCRIPTION OF THE RELATED ART

[0002] Radio frequency (RF) matching networks are used for coupling RF power (e.g., 13.56 MHz) from an RF source having a substantially resistive impedance (e.g., 50 ohms) to a load having a complex, time-variant impedance. The matching network matches the source impedance to the load impedance to effectively couple RF power from the source to the load. In high power applications, such as, for example, coupling RF power to a plasma within a plasma reaction chamber of a semiconductor wafer processing system, among others, the matching network should be relatively efficient, i.e., the contribution of the matching network to the total loop resistance should be as small as possible.

[0003] During semiconductor wafer fabrication, a plasma is formed in a processing chamber to deposit materials on or etch materials from a workpiece, such as a semiconductor wafer. A gas is provided into the chamber and is ignited by an RF electromagnetic field to form a plasma. The electromagnetic field is formed by providing an RF signal from an RF source to a plasma generating element, such as a coil antenna or an electrode plate. The RF source is coupled to the plasma generating element via the matching network.

[0004] In particular, the reactive impedance of the plasma generating element and the plasma together form a load impedance for the source. However, fluctuations in plasma flux (i.e., the product of plasma density and charge particle velocity) cause the impedance of the load to change substantially during processing. For example, the impedance of the plasma load may illustratively increase by as much as twenty times (20x), depending on the process being performed and the type of chamber used to perform the process. Accordingly, matching the impedance of the RF source to the time-variant load impedance is difficult to maintain during wafer processing. Where

proper impedance matching is not achieved during processing, the transfer of power from the source to the load becomes inefficient due to the power being reflected from the load and back to the source. Such inefficient power coupling impacts wafer processing throughput and may damage wafers and/or the wafer processing system components.

[0005] One type of matching network that is widely used in semiconductor wafer processing systems, is a tunable matching network wherein a series connected frequency-dependent passive element and a shunt connected frequency-dependent passive element are dynamically tuned to achieve an impedance match between the source and the load. One such tunable matching network is disclosed in commonly assigned US patent number 5,952,896 issued September 14, 1999. This matching network comprises a series connected inductor and a shunt connected capacitor. A matching network controller mechanically tunes the capacitor and the inductor to achieve a match between the source and the load. As the load impedance changes, actuators must constantly alter the tunable elements of the inductor and capacitor to maintain the match. In environments where the load impedance is rapidly changing, mechanical tuning can not tune quickly enough to maintain an optimal match.

[0006] An alternative type of matching network that finds use when load impedances are rapidly varying is a fixed matching network with frequency tuning. The fixed matching network uses fixed valued elements, e.g., non-tunable capacitors and inductors. The elements may be tunable to achieve a nominal value, but they are not tuned during match operation to maintain the match as the load impedance changes. As such, the component values are selected to obtain a match from source to load impedance under nominal operating conditions, e.g., a nominal load impedance and a nominal source frequency. As the load impedance varies during wafer processing, the frequency of the RF source is tuned to maintain a match between the source and the load. In effect, the matching process is electronically tuned, and can maintain a match during rapid fluctuations in load impedance.

[0007] The fixed match is usually designed with an inductor or capacitor coupled in series between the power source and the biasing element, and in parallel from the source to ground. As described above, the components of the matching network are constant. When using a dual element matching network, e.g., an inductor in series and

a capacitor in parallel, the range of impedance that the network can operate over is rather narrow. As such, the frequency tuning cannot achieve a match over a wide range of impedance fluctuations.

[0008] For example, in one prior art matching network a single inductor is connected in series between the source and the load, and a single capacitor is connected as a shunt with respect to the source and ground. As illustrated below, the matching range is very narrow, since it is only dependent on the frequency tuning range of the RF power generator. Specifically, the matching range is $\Delta Z / Z_o = 2\Delta\omega / \omega_o < 20\%$, where Z_o is the matching impedance at frequency ω_o, and the RF power generator frequency tuning is from $(\omega_o - \Delta\omega)$ to $(\omega_o + \Delta\omega)$, and where ω_o = the center frequency.

[0009] FIGS. 4A-4H depict schematic diagrams of various embodiments of prior art impedance matching networks 420. Specifically, each exemplary matching network embodiment is illustratively coupled between a RF source 412 to a load 450, such as a capacitive type load or and inductive type load. FIGS. 4A and 4C depict schematic diagrams of fixed matching networks utilizing a series inductor and a shunt capacitor, while FIGS. 4B and 4D depict schematic diagrams of fixed matching networks utilizing a series capacitor and a shunt capacitor. FIGS. 4E and 4G depict schematic diagrams of fixed matching networks utilizing a series inductor and a shunt inductor, while FIGS. 4F and 4H depict schematic diagrams of fixed matching networks utilizing a series capacitor and a shunt inductor.

[0010] Referring to the embodiment of FIG. 4A, a radio frequency (RF) source 412 is first coupled in parallel to a shunt capacitor C_{shunt} to ground 440, and the shunt capacitor C_{shunt} is coupled to a series inductor L_{series}, which is coupled to a capacitive type impedance load Z_L 450, where Z_L= x-jy. Referring to the embodiment of FIG. 4B, an RF source 412 is first coupled in parallel to a shunt capacitor C_{shunt} to ground 440, and the shunt capacitor C_{shunt} is coupled to a series capacitor C_{series}, which is coupled to an inductive type impedance load Z_L 450, where Z_L= x+jy. Referring to the embodiment of FIG. 4C, an RF source 412 is first coupled in series to an inductor L_{series}, which is further coupled to a capacitive type impedance load Z_L 450, where Z_L= x-jy, and a shunt capacitor C_{shunt} is coupled in parallel with the impedance load Z_L 450 to ground 440. Referring to the embodiment of FIG. 4D, an RF source 412 is first

coupled in series to a capacitor C_{series}, which is further coupled to an inductive type impedance load Z_L 450, where Z_L= x+jy, and a shunt capacitor C_{shunt} is coupled in parallel with the impedance load Z_L 450 to ground 440.

[0011] Referring to the embodiment of FIG. 4E, a radio frequency (RF) source 412 is first coupled in parallel to a shunt inductor L_{shunt} to ground 440, and the shunt inductor L_{shunt} is coupled to a series inductor L_{series}, which is coupled to a capacitive type impedance load Z_L 450, where Z_L= x-jy. Referring to the embodiment of FIG. 4F, an RF source 412 is first coupled in parallel to a shunt inductor L_{shunt} to ground 440, and the shunt inductor L_{shunt} is coupled to a series capacitor C_{series}, which is coupled to an inductive type impedance load Z_L 450, where Z_L= x+jy. Referring to the embodiment of FIG. 4G, an RF source 412 is first coupled in series to an inductor L_{series}, which is further coupled to a capacitive type impedance load Z_L 450, where Z_L= x-jy, and a shunt inductor L_{shunt} is coupled in parallel with the impedance load Z_L 450 to ground 440. Referring to the embodiment of FIG. 4H, an RF source 412 is first coupled in series to a capacitor C_{series}, which is further coupled to an inductive type impedance load Z_L 450, where Z_L= x+jy, and a shunt inductor L_{shunt} is coupled in parallel with the impedance load Z_L 450 to ground 440.

[0012] Referring to the prior art embodiment of FIG. 4A, for the series connected inductor L_{series}, the impedance range is $2\Delta\omega L$ when the RF power source is frequency-tuned from (ω_o - $\Delta\omega$) to (ω_o + $\Delta\omega$), where $\omega = 2\pi f$, and L = inductance, as measured in Henry. Using a numerical example, if the frequency is tunable from 1.9 MHz to 2.1 MHz and the inductance L_{series} is 10uH, the range of impedance available is only 12.56 ohms. Similarly, for the parallel connected capacitor C_{shunt}, the impedance range is $\frac{2\Delta\omega}{(\omega_o^2 - \Delta\omega)C_{shunt}}$, when the RF power source is frequency-tuned from (ω_o - $\Delta\omega$) to (ω_o + $\Delta\omega$), where $\omega = 2\pi f$, and C = capacitance, as measured in Farads. Using a numerical example, if the frequency is tunable from 1.9 MHz to 2.1 MHz and the capacitance is 500pf, the range of impedance available is only 15.97 ohms. It is noted that similar numerical examples and analyses are also applicable for the matching network configurations shown in FIGS. 4B through 4H. As such, when such a fixed matching network with frequency tuning is utilized, the match range is very narrow as compared to the wide process window (i.e., wide fluctuations in the load impedance).

[0013] Therefore, there is a need for an improved fixed matching network with frequency tuning that is capable of providing a wide range of impedance matching for time-variant impedance loads.

SUMMARY OF THE INVENTION

[0014] The present invention is a matching network for performing frequency tuned matching between a source and a load. The matching network includes a first capacitor and first inductor, having fixed values, coupled in series from an input port to an output port. A second capacitor and second inductor, having fixed values, is coupled in series from one of the input port and output port to ground. The values of the first inductor and first capacitor are related by a first mathematical relationship, and the values of the second inductor and second capacitor are related by a second mathematical relationship.

[0015] The input port is adapted to receive a variable frequency RF signal and the output port is adapted to be coupled to a time-variant load impedance. The substantial impedance range of the matching network enables a match to be maintained over a large fluctuation in load impedance. One specific application for the matching network is in a plasma enhanced, semiconductor wafer processing system, where the matching network efficiently couples RF energy to a plasma.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] So that the manner in which the above recited features of the invention are attained can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof, which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention, and are therefore, not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0017] FIG. 1 depicts a schematic, cross sectional view of a semiconductor processing system in which the embodiments of the impedance matching networks of the present invention can be utilized;

[0018] FIGS. 2A–2H depict schematic diagrams of various embodiments of impedance matching networks of the present invention;

[0019] FIG. 3 depicts a table comparing the various embodiments of impedance matching networks of the present invention of FIGS. 2A-2H with respect to the various embodiments of prior art impedance matching networks of FIGS. 4A-4H; and

[0020] FIGS. 4A-4H depict schematic diagrams of various embodiments of prior art impedance matching networks.

[0021] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

[0022] The present invention is a wide range, frequency tuned, fixed matching network (referred to herein as a WRFT network) to be used, for example, to couple RF energy to a plasma in a semiconductor wafer processing reactor. The WRFT network provides a wide dynamic range of impedance values for matching a tunable frequency source to a time-variant load impedance. The load impedance is generally defined by a plasma and an associated plasma generating element in a plasma enhanced semiconductor wafer processing reactor. The plasma generating element may be an electrode in a capacitively coupled-type reactor or an antenna in an inductively coupled-type reactor. As shown and discussed in further detail below, the matching range of the present invention is defined by the relationship $\frac{\Delta Z}{Z_o} \approx (2n-1)\left(\frac{2\Delta\omega}{\omega_o}\right)$, where n= a number greater than one (1), and the matching range increases by approximately (2n-1) times.

[0023] Fig. 1 depicts a schematic cross sectional view of a plasma enhanced, semiconductor wafer processing system 100 in which a matching network (WRFT network) of the present invention may be utilized. The illustrative system 100 can be used during integrated circuit fabrication, such as a reactive ion etching process. The inventive WRFT network, such as matching networks 134 and/or 144, finds use in any wafer processing system where the load impedance may change rapidly enough to

make mechanical tuning of the matching network impractical. Such systems may include those that perform plasma enhanced chemical vapor deposition, physical vapor deposition, plasma annealing and the like.

[0024] The system 100 generally comprises a reaction chamber (reactor) 102, a gas source 104, vacuum pump 116, and drive electronics 106. The reactor 102 comprises a chamber body 108 and a lid assembly 110 that defines an evacuable chamber 112 for performing substrate processing. In one embodiment, the reactor 102 may be a Dielectric Etch eMax reactor, available from Applied Materials, Inc. of Santa Clara, California. A detailed description of an eMax system is contained in US Patent Application Serial No.10/146,443, filed May 14, 2002, the contents of which is incorporated by reference herein in its entirety.

[0025] The gas source 104 is coupled to the reactor 102 via one or more gas lines 114 for providing process gases such as etchant gases, purge gases or deposition gases. The vacuum pump 116 is coupled to the reactor 102 via an exhaust port 118 for maintaining a particular pressure in the reactor and exhausting undesirable gases and contaminants.

[0026] The chamber body 108 includes at least one sidewall 120 and a chamber bottom 122. In one embodiment, the at least one sidewall 120 has a polygon shaped (e.g., octagon or substantially rectangular) outside surface and an annular or cylindrical inner surface. Furthermore, the sidewall 120 is generally electrically grounded. The chamber body 108 may be fabricated from a non-magnetic metal, such as anodized aluminum, and the like. The chamber body 108 contains a substrate entry port that is selectively sealed by a slit valve (not shown) disposed in the processing platform.

[0027] The lid assembly 110 is disposed over the sidewalls 120 and defines a processing region 124 within the reactor 102. The lid assembly 110 generally includes a lid 126 and may contain a plasma generating element (e.g., an electrode) 128 mounted to the lid 126. The lid 126 may be fabricated from a dielectric material such as aluminum oxide (Al_2O_3), or a non-magnetic metal such as anodized aluminum. The plasma generating element 128 is fabricated from a conductive material such as aluminum, stainless steel, and the like. The plasma generating element 128 may also function as a showerhead for dispensing gases into the processing region 124.

[0028] The plasma generating element 128 may be coupled to ground 130 (i.e., not used in certain applications). Alternatively, the element 128 may be coupled to a high frequency RF power source 132 via a matching network 134 of the present invention. The high frequency power source (top power source) 132 provides RF power in a range between about 0.5 Watts to 10,000 Watts at a center frequency $\omega_o = 2\pi f_o$, where the center frequency f_o is in a range of about 200 KHz to 150 MHz. The high frequency power source 132 is used to ignite and maintain a plasma from a gas mixture in the chamber 106.

[0029] A substrate support pedestal 136 is disposed within the chamber 112 and is seated on the chamber bottom 122. A substrate (i.e., wafer) 138 undergoing wafer processing is secured on an upper surface 140 of the substrate support pedestal 136. The substrate support 136 may be a susceptor, a heater, ceramic body, or electrostatic chuck on which the substrate is placed during processing. The substrate support pedestal 136 is adapted to receive an RF bias signal, such that the substrate support pedestal serves as a biasing element (e.g., cathode electrode). Specifically, the pedestal 136 contains a component that is either a dedicated electrode or is a conductive component that can be used as an electrode such as a cooling plate.

[0030] Within the drive electronics 106, a bias power source 142 is coupled via a matching network (a WRFT network) 144 of the present invention to the pedestal 136. In one embodiment, the grounded sidewalls 122 and the plasma generating element 128 together define an anode with respect to the biasing element (cathode) in the substrate support pedestal 120. In particular, the bias power source 142 provides RF power in the range of about 0.5 Watts to 10,000 Watts (W) and at a center frequency (f_o) in the range of about 200 KHz to 150 MHz. In one specific embodiment, the bias power source 142 provides RF power in a range of about 10 Watts to 5000 Watts (W), and at a frequency in the range of about 200 KHz to 30 MHz.

[0031] A controller 146 may be utilized to control the bias power source 142 as well as control the high frequency RF power source 132. The controller 146 comprises a central processing unit (CPU) 148, support circuits 150, and a memory 152. The CPU 148 is generally a microprocessor that performs general computer functions in accordance with programming stored in the memory 152. However, the CPU may also be an application specific integrated circuit, a field programmable gate array, and the

like that is capable of controlling the frequency of the RF sources 132 and 142. The support circuits are well-known circuits such as clocks, power supplies, cache, input/output drivers, and the like. The memory 152 may be random access memory, read only memory, floppy disks, hard disks, or any combination thereof. The memory 152 stores frequency control software 154 that is executed by the CPU 148 to control the frequency of the power sources 142 and 132 and maintain a match between the load and the source. The control function is generally closed loop control whereby the controller 146 monitors the reflected power from the load and adjusts the frequency of the source to minimize the reflected power. In one embodiment, the reflected power is monitored using a directional coupler 160.

[0032] FIGS. 2A–2H depict schematic diagrams of various embodiments of impedance matching networks 220 of the present invention. The impedance matching networks 220 are used for coupling RF power from an RF source 210 to a load 250. The circuit 200 illustratively represents a plasma reactor as the load 250 that is used to facilitate semiconductor wafer processing. However, those skilled in the art will recognize that the various embodiments of the matching network may be for other high power applications, such as coupling RF or microwave power to an antenna within a communications system, among others. As discussed below, these illustrative embodiments have a matching range that increases by approximately (2n-1) times over the prior art configurations shown in FIGS. 4A-4H.

[0033] For each of the embodiments shown in FIGS 2A-2H, the RF source 210 is represented by an AC signal source 212 connected to a series resistance R_s 214 (e.g., 50 ohms). Further, the load 250, for example, is a time-variant, complex impedance, such as a plasma within a plasma reaction chamber of a semiconductor wafer processing system of FIG. 1. FIGS. 2A, 2C, 2E, and 2G illustrate embodiments of a capacitively coupled reactor, where the instantaneous load impedance Z_L = x-jy is modeled as a capacitor C_L 252 connected to a series resistance R_L 254. Alternatively, FIGS. 2B, 2D, 2F, and 2H illustrate embodiments of an inductively coupled type reactor, where the instantaneous load impedance Z_L = x+jy is modeled as an inductor L_L 256 connected to a series resistance R_L 254. In either of the capacitively coupled or inductively coupled type reactor embodiments, the matching network 220 of the present invention matches the source impedance to the load impedance, such that fluctuations

in the load impedance during wafer processing will not result in diminished power coupling efficiency.

[0034] Referring to FIG. 2A, the matching network 220 comprises a shunt capacitor C_2 222A, a series inductor L_2 224A, a series capacitor C_3 222B, and a shunt inductor L_3 224B, where the matching network 220 is coupled between a terminal 216 at the source 210 and a terminal 236 at the load 250. Specifically, a first end and a second end of the shunt capacitor C_2 222A are respectively coupled to the terminal 216 and a first end of the shunt inductor L_3 224B. A second end of the shunt inductor L_3 224B is coupled to ground 240, such that the serially coupled shunt capacitor C_2 222A and inductor L_3 224B are parallel to the source 212, which is also coupled to ground 240. Additionally, a first end and a second end of the series capacitor C_3 222B are respectively coupled to the terminal 216 and a first end of the series inductor L_2 224A. A second end of the series inductor L_2 224A is coupled to the load 250 at terminal 236, such that the serially coupled serial capacitor C_3 222B and inductor L_2 224A are serially coupled to the load 250, which is further coupled to ground 240.

[0035] A person skilled in the art for which the invention pertains will appreciate that the network 220 also includes a match (or loop) resistance (not shown), which represents the cumulative resistive losses in all component circuitry within the network 220. However, the match resistance is very low (e.g., 0.01 ohms to 5 ohms) and considered negligible as compared to the overall impedance value of the network 220, and is only mentioned for completeness of understanding the invention.

[0036] The illustrative embodiments shown in FIGS 2A-2D provide load impedance matching by tuning the frequency of the source 210. As discussed in further detail below, FIGS. 2A-2H represent improved matching networks 220 over the respective prior art networks 420 shown in FIGS 4A-4H. Referring to FIG. 2A, the inductor L_2 224A is provided with an inductance value "nL", where "n" is a number greater than one (1). The new inductance value for inductor L_2 224A is "n" times an inductance value "L" of a matching network having just a single series inductor, such as the single series inductor L_{series} 424A of FIG. 4A having the value "L". Further, the capacitor C_3 222B is added in series with the inductor L_2 224A, where the capacitor C_3 222B has an impedance value equal to the original impedance value of the single inductor L_{serial} (FIG. 4A) having a value "L", where $C_{series} = 1/(n-1)\omega_o^2 L_{series}$, and ω_o is a center

frequency of the RF signal provided by the source 210. The combination of the serial coupled capacitor C_3 222B and inductor L_2 224A in the matching network 220 is capable of providing an impedance range that is increased up to approximately (2n-1) times the original range of the impedance range of a single series inductor used in the prior art matching network 420 of FIG. 4A. As such, for a given component value in an existing matching network design, an improved network can be derived by replacing the series inductor L_{series} of a prior art matching network with a combination of a capacitor and an inductor (e.g., C_3 and L_2) each having selective values, as discussed below in further detail. The result is a matching network with an increased impedance range.

[0037] The same principle also applies for a single shunt element (capacitor or inductor) of the matching network 220. The impedance ranges of matching networks 220 can be improved to have an increased impedance range by replacing the single element with a pair of elements having appropriate values. For example, the shunt capacitor C_{shunt} of FIG. 4A is replaced with a shunt capacitor C_2 222A, which is serially coupled to shunt inductor L_3 224B of FIG. 2A. In particular, the capacitor C_2 222A is provided with a new capacitance value $\frac{1}{n}C_{shunt}$, where "n" is a number greater than one (1), as well as the same value as used in the serial leg (elements 222B and 224A) of the network 220. The new capacitance value C_2 is 1/n times the capacitance value "C" of a matching network having just a single series capacitor, such as C_{shunt} 424A of FIG. 4A having the value "C". Further, the inductor L_3 224B is coupled in series with the capacitor C_2 222A, where the inductor L_3 224B has an impedance value equal to the original impedance value of the single capacitor C_{shunt} (FIG. 4A) having a value "C", where $L_3 = n\text{-}1/\omega_o^2 C_{shunt}$, and ω_o is a center frequency of the RF signal provided by the source 210.

[0038] In the prior art matching networks having only a single series coupled inductor "L_{series}" and a single shunt capacitor "C_{shunt}" as shown in FIG. 4A, the single series coupled inductor L_{series} may be defined as having an impedance of Z and an absolute impedance range of $|\Delta Z|$. In particular, for

ω_o, $Z = j\omega_o L$;
$(\omega_o - \Delta\omega)$, $Z = j(\omega_o - \Delta\omega)L$; and
$(\omega_o + \Delta\omega)$, $Z = j(\omega_o + \Delta\omega)L$;

where $\omega_o = 2\pi f_o$ at an initial frequency, $\Delta\omega$ = a change in frequency, and L = inductance as measured in Henries. As such, the impedance range $|\Delta Z| = 2\Delta\omega L$.

[0039] By illustration, a 10μH inductor that is serially coupled between a source 210 and load 250, where the source 210 illustratively provides a 2MHz, +/-100KHz signal, has an impedance of 125.6 ohms and an absolute impedance range of 12.56 ohms. Specifically,

$$j\omega_o L = (2\pi)(2\times10^6)(10\times10^{-6}) = 125.6 \text{ ohms}$$

$$\Delta Z_{@1.9 \text{ MHZ and } 2.1 \text{ MHZ}} = (2\pi)(2\times10^6)(10\times10^{-6})(2.1-1.9) = 12.56 \text{ ohms.}$$

[0040] The exemplary embodiment shown in FIG. 2A increases this absolute impedance range by at least a factor of (2n-1). For example, where the original inductance is increase by a factor of n=2, the absolute impedance range increases by at least a factor of three $((2)(2)-1)=3$. Specifically, the inductance of inductor L_2 224A is "2L" and the capacitor C_3 222A is selected to have the same impedance as the original impedance, illustratively using the single inductor. For

ω_o, $Z = j\omega_o L$;

$(\omega_o - \Delta\omega)$, $Z = (j(\omega_o - \Delta\omega)2L) - j\left(\frac{\omega_o^2 L}{\omega_o - \Delta\omega}\right)$;

$(\omega_o + \Delta\omega)$, $Z = (j(\omega_o + \Delta\omega)2L) - j\left(\frac{\omega_o^2 L}{\omega_o + \Delta\omega}\right)$;

Accordingly, $|\Delta Z| = (4\Delta\omega L) + \left(\frac{2\omega_o^2 \Delta\omega L}{(\omega_o + \Delta\omega)(\omega_o - \Delta\omega)}\right)$.

[0041] Such results provides an increased impedance range of up to three times (3x) the impedance range of the original impedance range provided by a single inductor. By illustration, the inductor L_2 224A is provided with a inductance value of 20uH (i.e., twice the inductance value of the illustrative single inductor L_{series} described above. The value of the capacitor C_3 222A is calculated such that the embodiment absolute impedance is equal to the impedance of the original impedance L_{series} at ω_o. As such, the required capacitance is computed as:

$C = 1/(n-1)\omega_o^2 L_{series} = 1/(2-1)\left((2\pi)(2x10^6)\right)^2(10x10^{-6}) = 634pF$, where L_{series} = the inductance value of the original single series inductor as illustratively shown in FIG. 3A.

[0042] Computing for the impedances at 2MHz +/-100Khz, the result is

$$Z@2MHz = Z_C + Z_L = -\left(\frac{1}{(2\pi)(2x10^6)(634\,x10^{-12})}\right) + \left((2\pi)(2x10^6)(20x10^{-6})\right) = 125.62\Omega$$

Similarly,

$Z@2.1MHz = -119.6 + 263 = 144.16\Omega$

$Z@1.9MHz = -132.19 + 238.64 = 106.45\Omega$

$|\Delta Z| = 144.16 - 106.45 = 37.71\Omega$

[0043] Thus, impedance range has increased by a factor greater than three (>3). In particular, the serial coupled elements (inductor L_2 and capacitor C_3) forming a serial "leg" between terminals 216 and 236 of the matching circuit shown in FIG. 2A has an impedance range of 37.71 ohms, as compared to a single inductor (e.g., L_{series}), which has an impedance range of merely 12.56 ohms.

[0044] A similar analysis may be performed for the matching network circuit 200 where the inductor L_2 224 has an inductance increased three times (i.e., from L to 3L), while the capacitor C_3 has a value selected to provide an impedance value equal to the impedance of the original inductor L_{series} at ω_o. In this instance, the impedance range is increased by a factor of at least three (3) and up to five (5) times the original impedance value. Specifically, $L_2 = nL_{series} = (3)(10x10^{-6}) = 30\mu H$, and C_3 is computed as:

$C = 1/(n-1)\omega_o^2 L_{series} = 1/(3-1)\left((2\pi)(2x10^6)\right)^2(10x10^{-6}) = 316.95pF$

[0045] Further,

ω_o, $Z = j\omega_o L$;

$(\omega_o - \Delta\omega)$, $Z = (j(\omega_o - \Delta\omega)3L) - j\left(\frac{2\omega_o^2 L}{\omega_o - \Delta\omega}\right)$;

$(\omega_o + \Delta\omega)$, $Z = (j(\omega_o + \Delta\omega)3L) - j\left(\frac{2\omega_o^2 L}{\omega_o + \Delta\omega}\right)$;

Accordingly, $|\Delta Z| = (6\Delta\omega L) + \left(\frac{4\omega_o^2 \Delta\omega L}{(\omega_o + \Delta\omega)(\omega_o - \Delta\omega)}\right)$.

[0046] Computing for the impedances at 2MHz +/-100KHz, the result is

$$Z@2MHz = -\left(\frac{1}{(2\pi)(2x10^{6})(316.95x10^{-12})}\right) + ((2\pi)(2x10^{6})(30x10^{-6})) =$$

$$-251.2 + 376.8 = 125.6\Omega$$

$$Z@2.1MHz = -239.2 + 395.83 = 156.63\Omega$$

$$Z@1.9MHz = -264.38 + 357.96 = 93.58\Omega$$

$$|\Delta Z| = 156.63 - 93.58 = 63.05\Omega$$

[0047] The sequence can be carried further to increase the impedance range. The general relationship between the inductance and the capacitance values is mathematically defined. Specifically, the value of the series inductor is nL, where n is a number greater than one (1) that approximately defines the desired impedance range improvement, and L is the inductance value in Henries. The value of the series capacitance is $1/(n-1)j\omega_o^2L$, where ω_o is the nominal frequency of operation for the matching network.

[0048] Additionally, the single shunt coupled capacitor "C" of the matching network 420 as shown in FIG. 4A, may be defined as having an impedance of Z and an absolute impedance range of $|\Delta Z|$. In particular, for

ω_o,	$Z = -j/\omega_o C$;
$(\omega_o - \Delta\omega)$,	$Z = -j/(\omega_o - \Delta\omega)C$; and
$(\omega_o + \Delta\omega)$,	$Z = -j/(\omega_o + \Delta\omega)C$;

where $\omega_o = 2\pi f_o$ at an initial frequency, $\Delta\omega$ = a change in frequency, and L = inductance as measured in Henries. As such, the impedance range $|\Delta Z| = \frac{2\Delta\omega}{(\omega_o + \Delta\omega)(\omega_o - \Delta\omega)C}$.

[0049] By illustration, a 500pf capacitor that is coupled parallel to a source 210 and load 250, where the source 210 illustratively provides a 2MHz, +/-100KHz signal, has an impedance of 159.24 ohms and an absolute impedance range of 15.97 ohms. Specifically,

$1/j\omega_oC = 1/((2\pi)(2x10^6)(500x10^{-12})) = 159.24$ ohms

$\Delta Z_{@1.9\ MHZ\ and\ 2.1\ MHZ} = 1/((2\pi)(2x10^6)(10x10^{-6})(2.1-1.9)) = 15.97$ ohms.

[0050] As discussed above with regard to the series connected elements 222B and 224A of the exemplary embodiment shown in FIG. 2A, the absolute impedance range

increases by at least a factor of (2n-1). For example, where n=2, the original capacitance decreases by a factor of 1/n=2, and the absolute impedance range increases by at least a factor of three $((2)(2)-1)=3$. Specifically, the capacitance of capacitor C_2 222A is "$\frac{1}{2}C$" and the shunt inductor L_3 224B is selected to have the same impedance as the original impedance, illustratively using the single shunt capacitor (422A of FIG. 4A), where $L_3 = \frac{n-1}{\omega_o C_{shunt}}$. For:

ω_o, $Z = \frac{-j}{\omega_o C}$;

$(\omega_o - \Delta\omega)$, $Z = \left(\frac{-j2}{\omega_o - \Delta\omega}\right) - j\left(\frac{\omega_o^2 - \Delta\omega}{\omega_o^2 C}\right)$;

$(\omega_o + \Delta\omega)$, $Z = \left(\frac{-j2}{\omega_o + \Delta\omega}\right) - j\left(\frac{\omega_o^2 + \Delta\omega}{\omega_o^2 C}\right)$;

Accordingly, $|\Delta Z| = \left(\frac{4\Delta\omega}{(\omega_o + \Delta\omega)(\omega_o - \Delta\omega)C}\right) + \left(\frac{2\Delta\omega}{\omega_o^2 C}\right)$.

[0051] Such results provides an increased impedance range of up to three times (3x) the impedance range of the original impedance range provided by a single inductor. By illustration, n is selected as equal to two (n=2), such that the capacitor C_2 222A is provided with a capacitance value of $\frac{1}{n}C_{shunt} = \frac{1}{2}500x10^{-12} = 250\,pf$ (i.e., one-half the original capacitance value (500pf) of the illustrative single shunt capacitor C_{shunt} described above. The value of the inductor L_3 224B is calculated such that its absolute impedance is equal to the impedance of the original impedance, where $L_3 = \frac{n-1}{\omega_o^2 C_{shunt}} = \frac{2-1}{((2\pi)(2x10^6))^2 (500x10^{-12})} = 12.67\mu H$.

[0052] Computing for the impedances at 2MHz +/-100Khz, the result is

$$Z@2MHz = Z_C + Z_L = -\left(\frac{1}{(2\pi)(2x10^6)(250x10^{-12})}\right) + ((2\pi)(2x10^6)(12.67x10^{-6})) =$$

$-318.47 + 159.13 = 159.34\Omega$

Similarly,

$Z@2.1MHz = -303.30 + 167.01 = 136.29\Omega$

$Z@1.9MHz = -335.23 + 151.18 = 184.05\Omega$

$|\Delta Z| = 184.05 - 136.29 = 47.76\Omega$

[0053] Thus, impedance range has increased by a factor greater than three (>3). In particular, the serial coupled elements (forming a parallel "leg") between terminal 216 and ground 240 of the matching circuit shown in FIG. 2A has an impedance range of 47.76 ohms, as compared to a single capacitor, which has an impedance range of merely 15.97 ohms.

[0054] The sequence can be carried further to increase the impedance range. The general relationship between the inductance and the capacitance values is mathematically defined. Specifically, the value of the parallel shunt capacitor is $C_2 = \frac{1}{n}C$ and the shunt inductor $L_3 = \frac{n-1}{\omega_o C_{shumt}}$, where n is a number greater than one (n>1) that approximately defines the desired impedance range improvement, and ω_o is the nominal frequency of operation for the matching network.

[0055] For example, where n is selected to equal three (n=3), the capacitor C_2 222A is $\frac{1}{3}C_{shunt}$ = (1/3)(500pf) = 166.67pf, and the shunt inductor L_3 224B is selected to have the same impedance as the original impedance, illustratively using the single shunt capacitor (422A of FIG. 4A), where $L_3 = \frac{n-1}{\omega_o C_{shumt}} = \frac{3-1}{((2\pi)(2x10^6))^2(500x10^{-12})} = 25.35\mu H$.

[0056] Computing for the impedances at 2MHz +/-100Khz, the result is

$$Z@2MHz = Z_C + Z_L = -\left(\frac{1}{(2\pi)(2x10^6)(166.67x10^{-12})}\right) + ((2\pi)(2x10^6)(25.35x10^{-6})) =$$

$$-477.69 + 318.4 = 159.3\Omega$$

Similarly,

$$Z@2.1MHz = -454.95 + 334.32 = 120.63\Omega$$

$$Z@1.9MHz = -502.83 + 302.47 = 200.36\Omega$$

$$|\Delta Z| = 200.36 - 120.63 = 79.73\Omega$$

[0057] Thus, impedance range has increased by a factor greater than five (>5). In particular, the serial coupled elements (forming a parallel "leg") between terminal 216 and ground 240 of the matching circuit shown in FIG. 2A has an impedance range of 79.73 ohms, as compared to a single capacitor, which has an impedance range of merely 15.97 ohms. Similar computations can be performed for situations where even greater match range capabilities are required to match the load 250 by increasing the multiplier factor "n". For example, when the multiplier factor n is set to 4, the impedance range is increased by a factor greater than seven (i.e., 2n-1 = (2x4)-1= 7). When n=5, the impedance range is increased by a factor greater than nine (i.e., 2n-1 = (2x5)-1= 9), and so forth. In this manner a proper impedance range may be selected for the fixed matching network 230 based on actual or expected fluctuations of the load impedance, such as fluctuations in the impedance of a plasma load during semiconductor wafer processing.

[0058] FIG. 3 depicts a table 300 comparing the various embodiments of impedance matching networks of the present invention of FIGS. 2A-2H with respect to the various embodiments of prior art impedance matching networks of FIGS. 4A-4H. For each of the four types of original matching networks depicted in FIG. 3, each original matching network has a single series element and single shunt element as discussed above. Further, each of the respective wide range matching networks of the present invention comprises dual series elements and dual shunt elements. Moreover, a general relationship between the inductance and the capacitance values is mathematically defined. Specifically, the series inductor and series capacitor are related by a first mathematical relationship, while the shunt inductor and shunt capacitor are related by a second mathematical relationship.

[0059] For example, as discussed above with regard to the prior art embodiment of FIGS. 4A and 4C, the original matching circuit 420 includes a single series inductor $L_{series_original}$ and a single shunt capacitor $C_{shunt_original}$. The table 300 of FIG. 3 shows that each single frequency-dependent passive element is replaced by dual capacitive and inductive elements, as shown in FIGS. 2A and 2C. Specifically, the series inductor $L_{series_original}$ is replaced with an inductor L_{series_new} having a value equal to a multiple value of the original series inductor, where $L_{series_new} = n\ L_{series_original}$, plus a capacitor having a value defined by a relationship $C_{series_new} = 1/(n-1)\omega_o^2 L_{series_original}$. Similarly, the shunt capacitor $C_{shunt_original}$ is replaced with a capacitor C_{shunt_new} having a value $\frac{1}{n}C_{shunt_original}$ plus an inductor having a value $L_{shunt_new} = \frac{n-1}{\omega_o^2 C_{shunt_original}}$.

[0060] Where the original matching circuit 420 includes a single series capacitor $C_{series_original}$ and a single shunt capacitor $C_{shunt_original}$, as shown in the prior art embodiment of FIGS. 4B and 4D, the table 400 of FIG. 3 shows that each single frequency-dependent passive element is replaced by dual capacitive and inductive elements, as shown in FIGS. 2B and 2D. Specifically, the series capacitor $C_{series_original}$ is replaced with an inductor L_{series_new} having a value equal to $L_{series_new} = \frac{n-1}{\omega_o^2 C_{series_original}}$, plus a capacitor having a value defined by a relationship $C_{series_new} = \frac{1}{n}C_{series_original}$. Similarly, the shunt capacitor C_{shunt} is replaced with a capacitor C_{shunt_new} having a value $\frac{1}{n}C_{shunt_original}$, plus an inductor having a value $L_{shunt_new} = \frac{n-1}{\omega_o^2 C_{shunt_original}}$ as discussed above with regard to FIG. 2A.

[0061] Where the original matching circuit 420 includes a single series inductor $L_{series_original}$ and a single shunt inductor $L_{shunt_original}$, as shown in the prior art embodiment of FIGS. 4E and 4G, the table 300 of FIG. 3 shows that each single frequency-dependent passive element is replaced by dual capacitive and inductive elements, as shown in FIGS. 2E and 2G. Specifically, the series inductor $L_{series_original}$ is replaced with an inductor L_{series_new} having a value equal to $L_{series_new} = nL_{series_original}$, plus a capacitor having a value defined by a relationship $C_{series_new} = \frac{1}{(n-1)\omega_o^2 L_{series_original}}$.

Similarly, the shunt capacitor C_{shunt} is replaced with a capacitor C_{shunt_new} having a value $\frac{1}{(n-1)\omega_o^2 L_{shunt_original}}$, plus an inductor having a value $L_{shunt_new} = nL_{shunt_original}$.

[0062] Alternatively, where the original matching circuit 420 includes a single series capacitor $C_{series_original}$ and a single shunt inductor $L_{shunt_original}$, as shown in the prior art embodiment of FIGS. 4F and 4H, the table 300 of FIG. 3 shows that each single frequency-dependent passive element is replaced by dual capacitive and inductive elements, as shown in FIGS. 2F and 2H. Specifically, the series capacitor $C_{series_original}$ is replaced with a capacitor C_{series_new} having a value equal to $\frac{1}{n}C_{series_original}$, plus an inductor having a value defined by a relationship $L_{series_new} = \frac{n-1}{\omega_o^2 C_{series_original}}$. Further, the shunt capacitor C_{shunt} is replaced with a capacitor C_{shunt_new} having a value $\frac{1}{(n-1)\omega_o^2 L_{shunt_original}}$, plus an inductor having a value $L_{shunt_new} = nL_{shunt_original}$.

[0063] Using the inventive WRFT network as a matching network to couple power to a plasma in a semiconductor wafer processing chamber enables the network to maintain a match over a large range of load impedances. The selection of the component value combinations enables the matching network to be designed to operate over large process windows or narrow process windows. As such, the impedance range needed can be matched to the requirements of the reactor.

[0064] Although various embodiments that incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A matching network for performing frequency tuned matching between a source and a load, comprising:

a first capacitor and first inductor, having fixed values, coupled in series from an input port to an output port;

a second capacitor and second inductor, having fixed values, coupled in series from one of said input port and output port to ground; and

where the input port is adapted to receive a variable frequency RF signal and the output port is adapted to be coupled to a time-variant load impedance.

2. The matching network of claim 1, wherein said first capacitor and first inductor values are related by a first mathematic relationship, and said second capacitor and second inductor values are related by a second mathematic relationship.

3. The matching network of claim 2, wherein said first mathematical relationship is the first inductor having a value NL, where N is a number greater than 1 and L is an inductance value in Henries, and the first capacitor having a value $1/(N-1)j\omega_o^2L$, where ω_o is a nominal frequency of operation for the matching network.

4. The matching network of claim 3, wherein said second mathematical relationship is the second capacitor having a value C/N, where C is a capacitance value in Farads, and the second inductor having a value $(N-1)/j\omega_o^2C$.

5. The matching network of claim 3, wherein said second mathematical relationship is the second capacitor having a value $1/(N-1)j\omega_o^2L$, and the second inductor having a value NL.

6. The matching network of claim 2, wherein:

said first mathematical relationship is the first inductor having a value $(N-1)/j\omega_o^2C$, where N is a number greater than 1, ω_o is a nominal frequency of operation for the matching network, and C is a capacitance value in Farads; and

said first capacitor having a value (1/N)C, where C is a capacitance value in Farads.

7. The matching network of claim 6, wherein said second mathematical relationship is the second capacitor having a value C/N, and the second inductor having a value (N-1)/$j\omega_o^2$C.

8. The matching network of claim 6, wherein said second mathematical relationship is the second capacitor having a value 1/(N-1)$j\omega_o^2$L, and the second inductor having a value NL, where L is an inductance value in Henries.

9. Apparatus for processing semiconductor wafers comprising:

a reactor having a pedestal for supporting a wafer and a plasma generating element for coupling RF energy to a gas to form a plasma proximate the wafer;

a variable frequency source, where the variable frequency source is dynamically tuned to maintain an impedance match between the variable frequency source and the plasma generating element; and

a matching network, coupled in series with said reactor and the plasma generating element, said matching network comprising:

a first capacitor and a first inductor, having fixed values, and connected in series between said reactor and the plasma generating element; and

a second capacitor serially connected to a second inductor, having fixed values, where said serially connected second capacitor and second inductor are shunted to ground with respect to one of said reactor and variable frequency source.

10. The apparatus of claim 9, wherein the plasma generating element is an electrode that forms a cathode in the reactor.

11. The apparatus of claim 9, wherein the electrode is a component of the pedestal.

12. The apparatus of claim 9, wherein the electrode is a component of a lid for the reactor.

13. The apparatus of claim 9, wherein the plasma generating element is an antenna positioned proximate the reactor.

14. The apparatus of claim 6 wherein said series connected capacitor and inductor are connected between the variable frequency source and the plasma generating element.

15. The apparatus of claim 11, wherein a value of the first capacitor and a value of the first inductor are related by a first mathematic relationship, and a value of the second capacitor and a value of the second inductor are related by a second mathematic relationship.

16. The apparatus of claim 15, wherein said first mathematical relationship is the first inductor having a value NL, where N is a number greater than 1 and L is an inductance value in Henries, and the first capacitor having a value $1/(N-1)j\omega_o^2L$, where ω_o is a nominal frequency of operation for the matching network.

17. The apparatus of claim 16, wherein said second mathematical relationship is the second capacitor having a value C/N, where C is a capacitance value in Farads, and the second inductor having a value $(N-1)/j\omega_o^2C$.

18. The apparatus of claim 16, wherein said second mathematical relationship is the second capacitor having a value $1/(N-1)j\omega_o^2L$, and the second inductor having a value NL.

19. The apparatus of claim 15, wherein:

said first mathematical relationship is the first inductor having a value $(N-1)/j\omega_o^2C$, where N is a number greater than 1, ω_o is a nominal frequency of operation for the matching network, and C is a capacitance value in Farads; and

said first capacitor having a value (1/N)C, where C is a capacitance value in Farads.

20. The apparatus of claim 19, wherein said second mathematical relationship is the second capacitor having a value C/N, and the second inductor having a value $(N-1)/j\omega_o^2C$.

21. The apparatus of claim 19, wherein said second mathematical relationship is the second capacitor having a value $1/(N-1)j\omega_o^2L$, and the second inductor having a value NL, where L is an inductance value in Henries.

22. A method of increasing the impedance range of a matching network comprising:

replacing each single series component having a component value in an original matching network with a series connected first capacitor and first inductor, where the values of the series connected first capacitor and first inductor are related to the component value by a first mathematical relationship; and

replacing each single shunt component having a component value in an original matching network with a series connected second capacitor and second inductor, where the values of the series connected second capacitor and second inductor are related to the component value by a second mathematical relationship.

23. The method of claim 22, wherein the series connected first capacitor and first inductor are connected from an input port to an output port of the matching network; and the series connected second capacitor and second inductor are shunted to ground with respect to one of said input port and said output port of said matching network.

24. The apparatus of claim 22, wherein said first mathematical relationship is the first inductor having a value NL, where N is a number greater than 1 and L is an inductance value in Henries, and the first capacitor having a value $1/(N-1)j\omega_o^2L$, where ω_o is a nominal frequency of operation for the matching network.

25. The apparatus of claim 24, wherein said second mathematical relationship is the second capacitor having a value C/N, where C is a capacitance value in Farads, and the second inductor having a value $(N-1)/j\omega_o^2C$.

26. The apparatus of claim 25, wherein said second mathematical relationship is the second capacitor having a value $1/(N-1)j\omega_o^2L$, and the second inductor having a value NL.

27. The apparatus of claim 22, wherein:

said first mathematical relationship is the first inductor having a value $(N-1)/j\omega_o^2C$, where N is a number greater than 1, ω_o is a nominal frequency of operation for the matching network, and C is a capacitance value in Farads; and

said first capacitor having a value (1/N)C, where C is a capacitance value in Farads.

28. The apparatus of claim 27, wherein said second mathematical relationship is the second capacitor having a value C/N, and the second inductor having a value $(N-1)/j\omega_o^2C$.

29. The apparatus of claim 27, wherein said second mathematical relationship is the second capacitor having a value $1/(N-1)j\omega_o^2L$, and the second inductor having a value NL, where L is an inductance value in Henries.

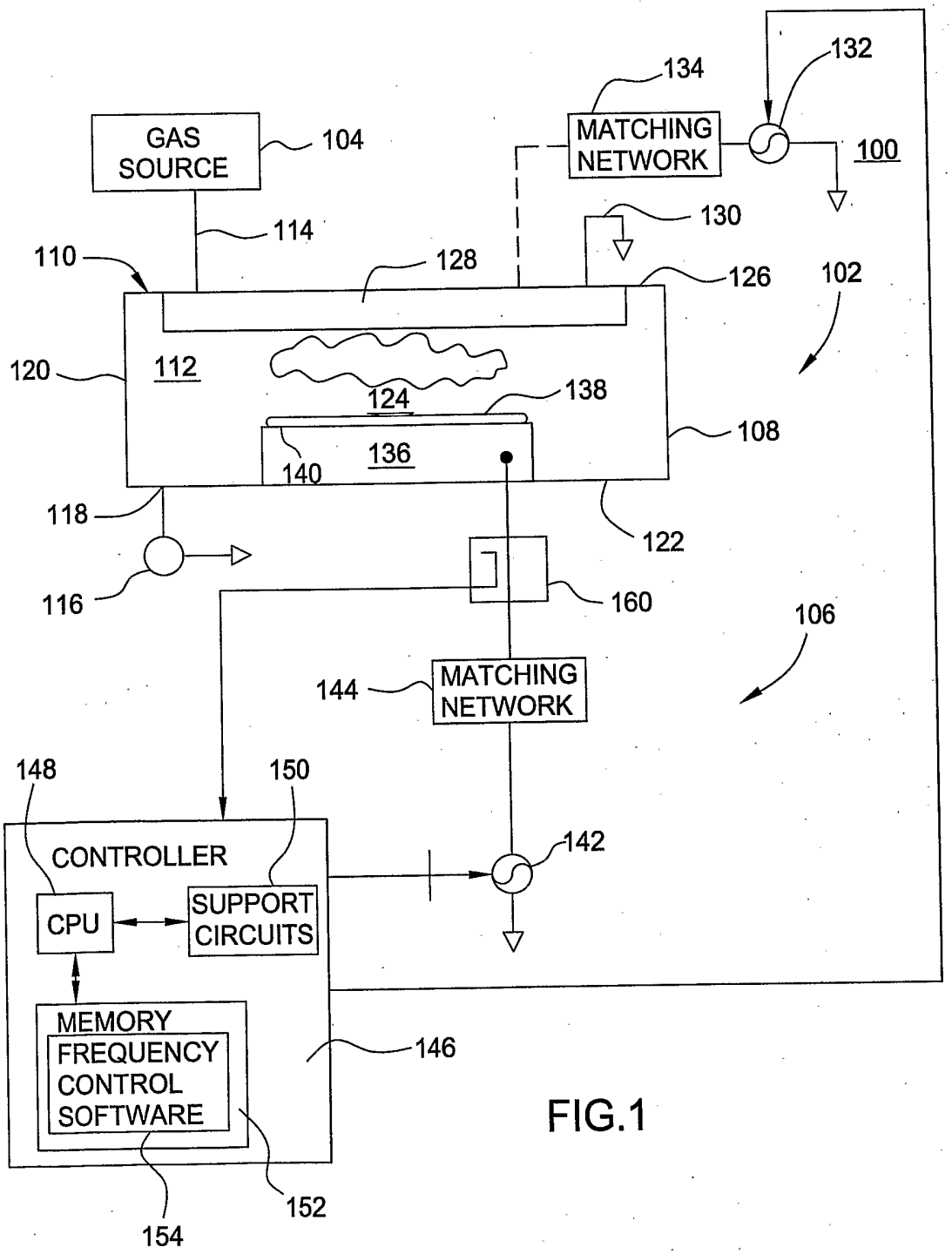

GAS SOURCE
104
MATCHING NETWORK
134
132
100
114
130
110
128
126
102
120
112
124
138
108
136
140
118
122
116
160
106
144
MATCHING NETWORK
148
150
CONTROLLER
142
CPU
SUPPORT CIRCUITS
MEMORY
FREQUENCY CONTROL SOFTWARE
146
152
154

FIG.1

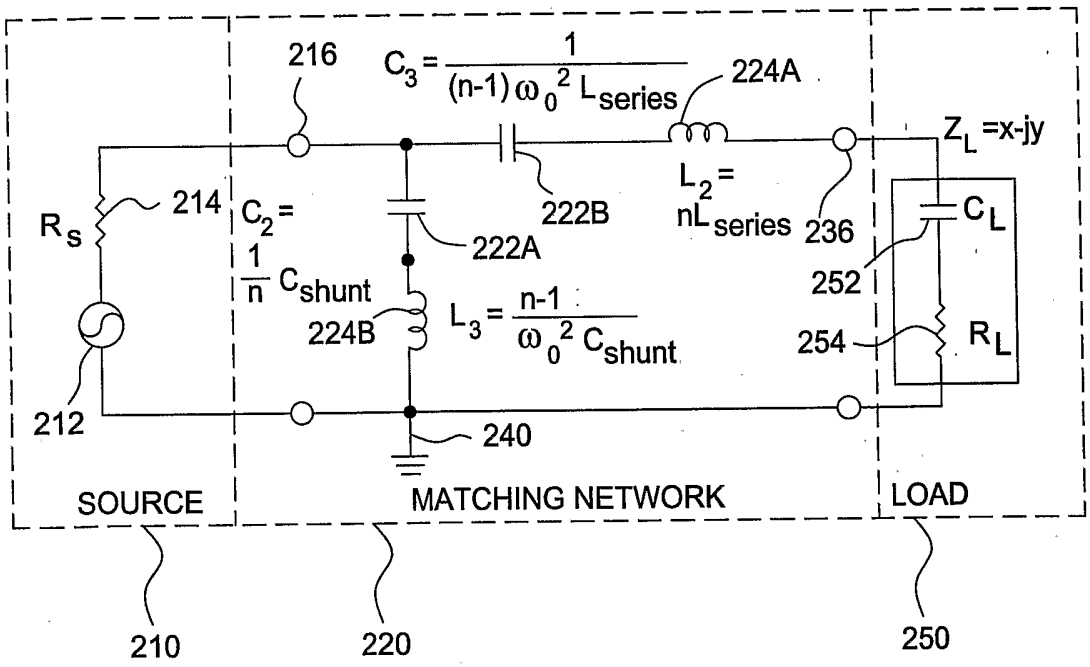

216
$C_3 = \frac{1}{(n-1)\omega_0^2 L_{series}}$
224A
Z_L =x-jy
214
R_S
$C_2 = \frac{1}{n} C_{shunt}$
222B
$L_2 = nL_{series}$
236
C_L
222A
252
224B
$L_3 = \frac{n-1}{\omega_0^2 C_{shunt}}$
254
R_L
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2A

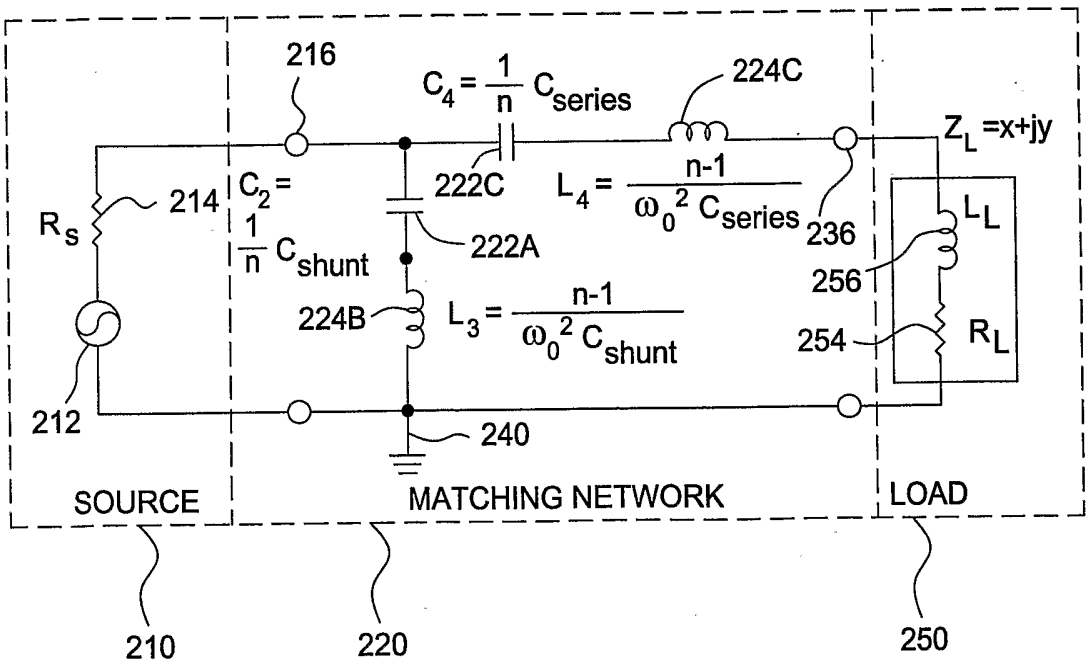

216
$C_4 = \frac{1}{n} C_{series}$
224C
Z_L =x+jy
214
R_S
$C_2 = \frac{1}{n} C_{shunt}$
222C
$L_4 = \frac{n-1}{\omega_0^2 C_{series}}$
236
L_L
222A
256
224B
$L_3 = \frac{n-1}{\omega_0^2 C_{shunt}}$
254
R_L
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2B

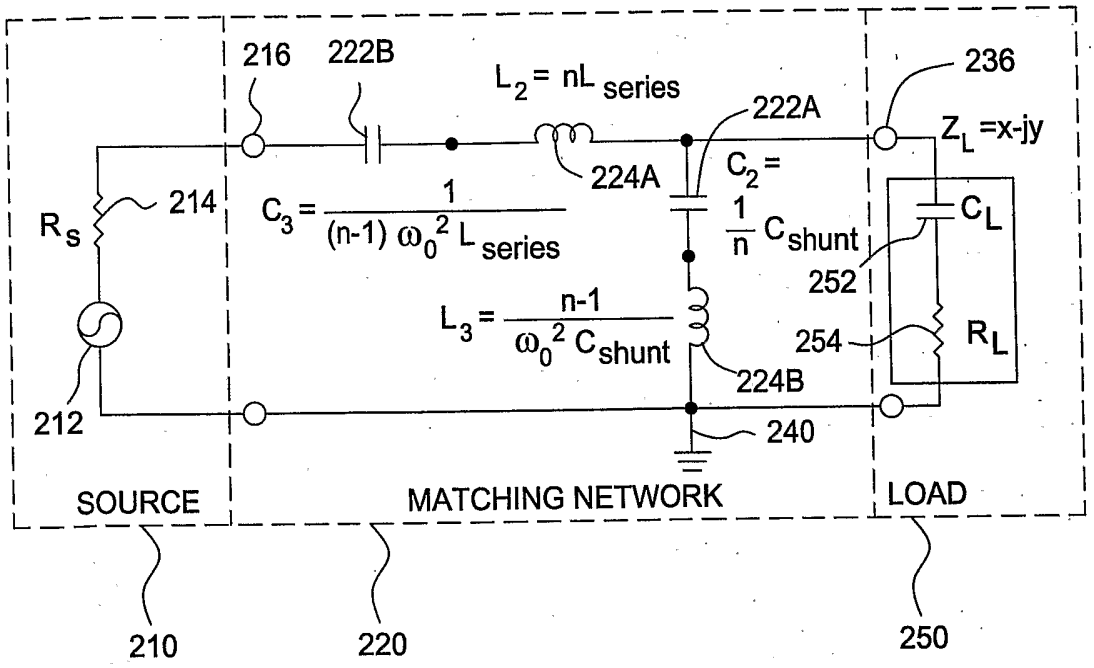

216
222B
$L_2 = nL_{series}$
236
222A
$Z_L = x-jy$
224A
$C_2 = \frac{1}{n} C_{shunt}$
214
R_S
$C_3 = \frac{1}{(n-1)\omega_0^2 L_{series}}$
C_L
252
$L_3 = \frac{n-1}{\omega_0^2 C_{shunt}}$
254
R_L
224B
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2C

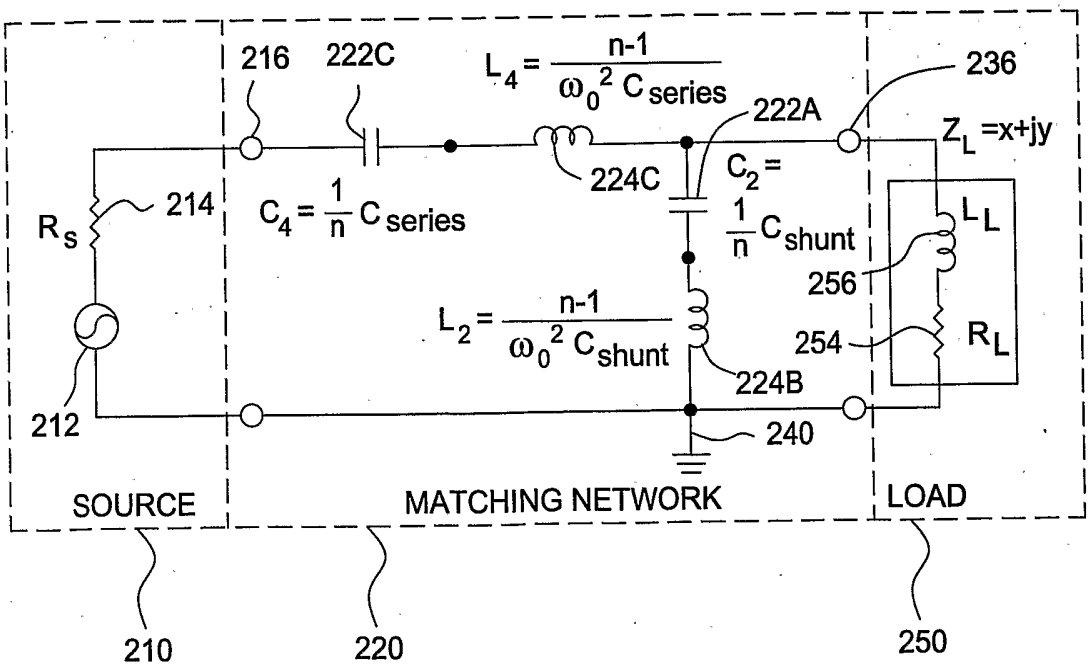

216
222C
$L_4 = \frac{n-1}{\omega_0^2 C_{series}}$
236
222A
$Z_L = x+jy$
224C
$C_2 = \frac{1}{n} C_{shunt}$
214
R_S
$C_4 = \frac{1}{n} C_{series}$
L_L
256
$L_2 = \frac{n-1}{\omega_0^2 C_{shunt}}$
254
R_L
224B
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2D

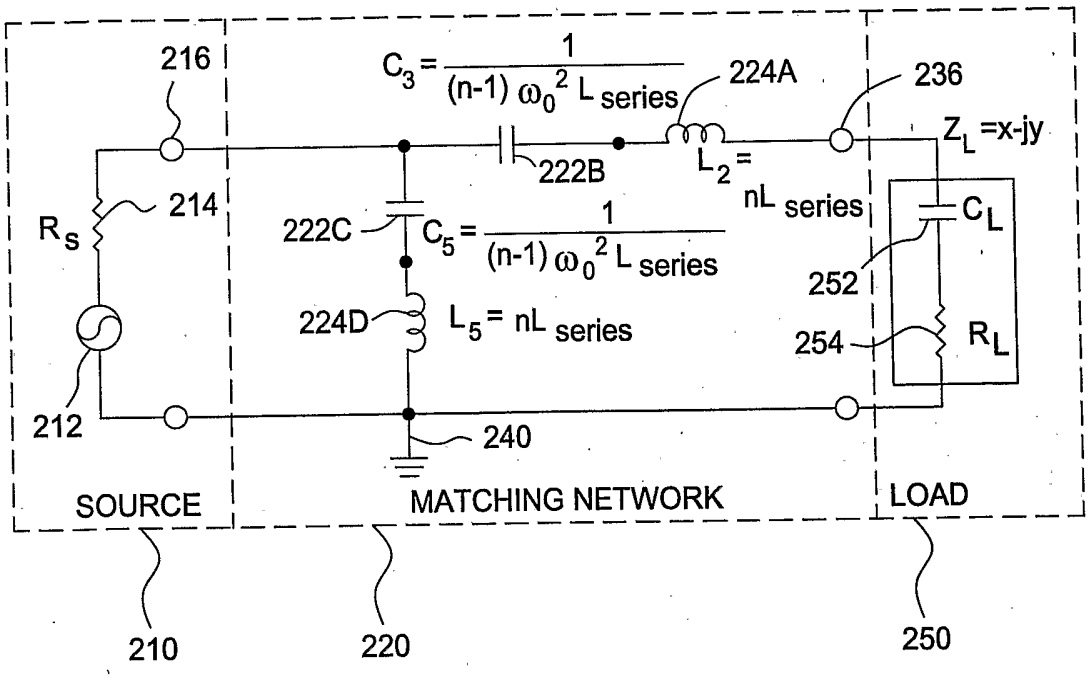

216
$C_3 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
224A
236
Z_L =x-jy
222B
L_2 = nL series
214
R_S
222C
$C_5 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
C_L
252
224D
L_5 = nL series
254
R_L
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2E

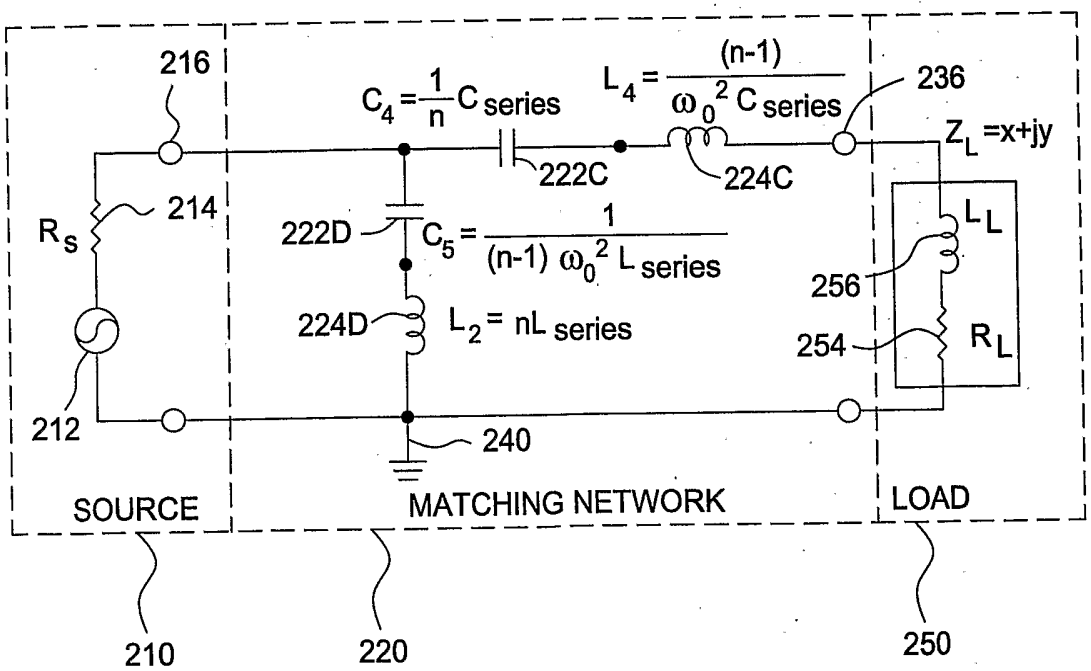

216
$C_4 = \frac{1}{n} C_{series}$
$L_4 = \frac{(n-1)}{\omega_0^2\,C_{series}}$
236
Z_L =x+jy
222C
224C
214
R_S
222D
$C_5 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
L_L
256
224D
L_2 = nL series
254
R_L
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2F

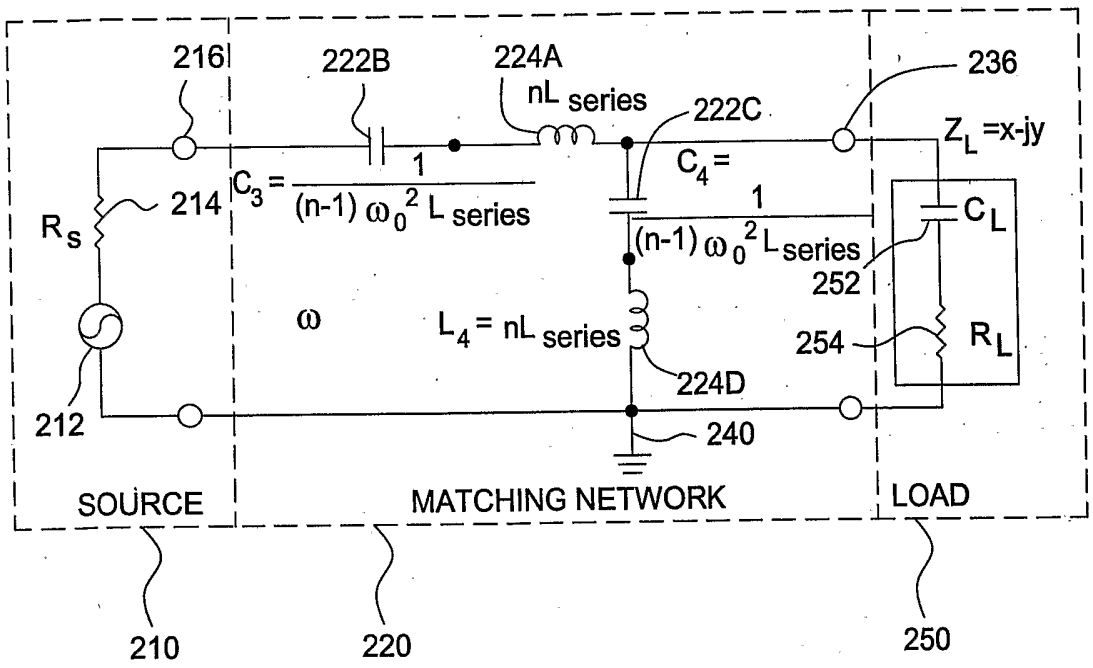

216
222B
224A
nL series
222C
236
Z_L =x-jy
$C_3 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
$C_4 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
214
R_S
C_L
252
ω
L_4 = nL series
254
R_L
224D
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2G

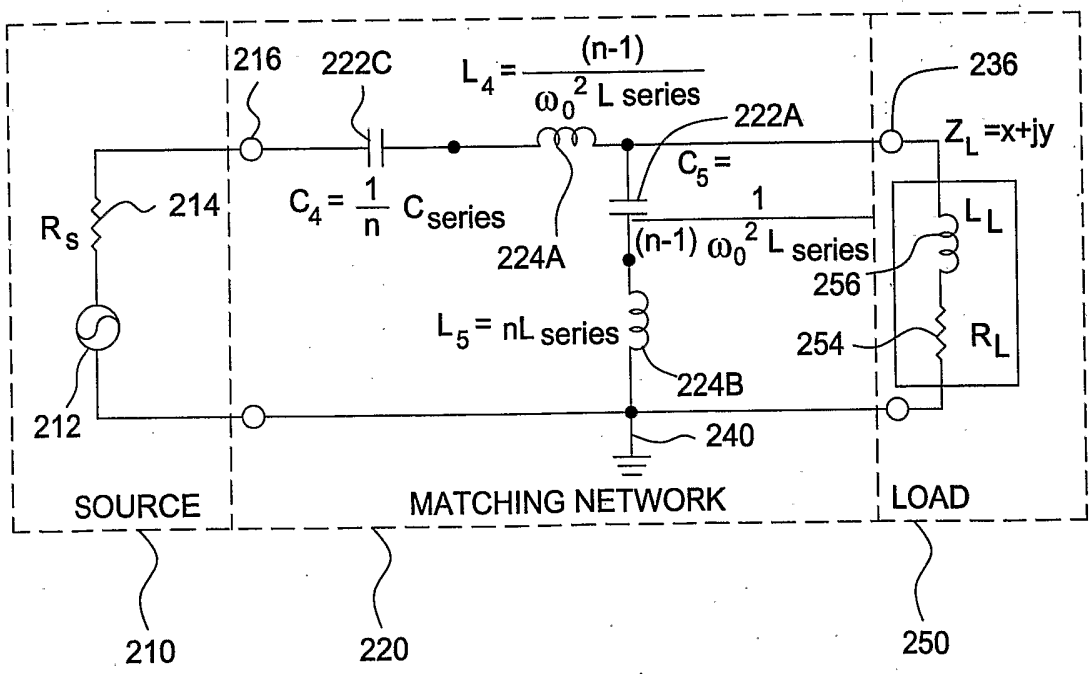

216
222C
$L_4 = \frac{(n-1)}{\omega_0^2\,L_{series}}$
236
222A
Z_L =x+jy
$C_5 = \frac{1}{(n-1)\,\omega_0^2\,L_{series}}$
214
R_S
$C_4 = \frac{1}{n}\,C_{series}$
L_L
224A
256
L_5 = nL series
254
R_L
224B
212
240
SOURCE
MATCHING NETWORK
LOAD
210
220
250

FIG. 2H

TABLE 300

ORIGINAL MATCHING NETWORK	WIRE RANGE MATCHING NETWORK
SERIES INDUCTOR L_{series} SHUNT CAPACITOR C_{shunt} PRIOR ART FIGS 3A AND 3C	$L_{series_new} = nL_{series}$ $C_{series_new} = \frac{1}{(n-1)\omega_0^2 L_{series}}$ $C_{shunt_new} = \frac{1}{n} C_{shunt}$ $L_{shunt_new} = \frac{n-1}{\omega_0^2 C_{shunt}}$ FIGS. 2B AND 2C
SERIES CAPACITOR C_{series} SHUNT CAPACITOR C_{shunt} PRIOR ART FIGS. 3B AND 3C	$L_{series_new} = \frac{n-1}{\omega_0^2 C_{series}}$ $C_{series_new} = \frac{1}{n} C_{series}$ $C_{shunt_new} = \frac{1}{n} C_{shunt}$ $L_{shunt_new} = \frac{n-1}{\omega_0^2 C_{shunt}}$ FIGS. 2B AND 2D
SERIES INDUCTOR L_{series} SHUNT INDUCTOR L_{shunt} PRIOR ART FIG. 3E AND 3G	$L_{series_new} = nL_{series}$ $C_{series_new} = \frac{1}{(n-1)\omega_0^2 L_{series}}$ $C_{shunt_new} = \frac{1}{(n-1)\omega_0^2 L_{series}}$ $L_{shunt_new} = nL_{series}$ FIGS. 2E AND 2G
SERIES CAPACITOR C_{series} SHUNT INDUCTOR L_{shunt} PRIOR ART FIGS. 3F AND 3H	$L_{series_new} = \frac{n-1}{\omega_0^2 C_{series}}$ $C_{series_new} = \frac{1}{n} C_{series}$ $C_{shunt_new} = \frac{1}{(n-1)\omega_0^2 L_{series}}$ $L_{shunt_new} = nL_{series}$ FIGS. 2F AND 2H

FIG. 3

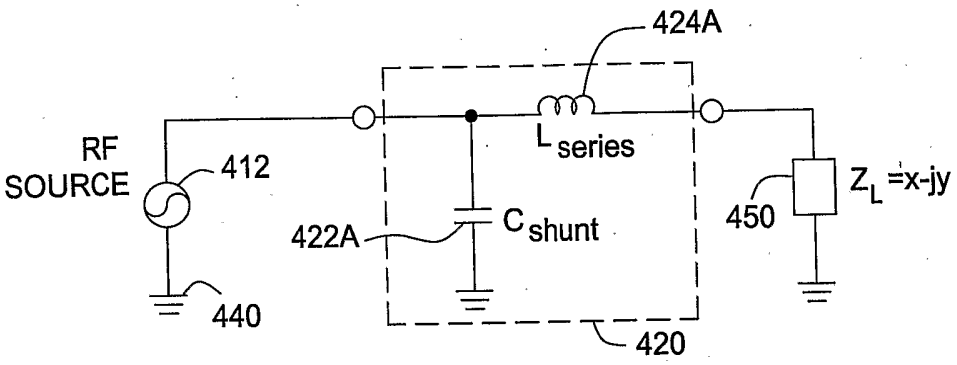


FIG. 4A (PRIOR ART)

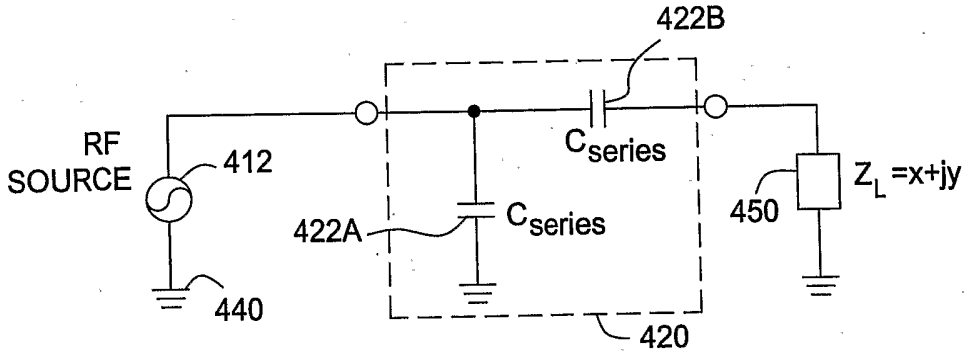


FIG. 4B (PRIOR ART)

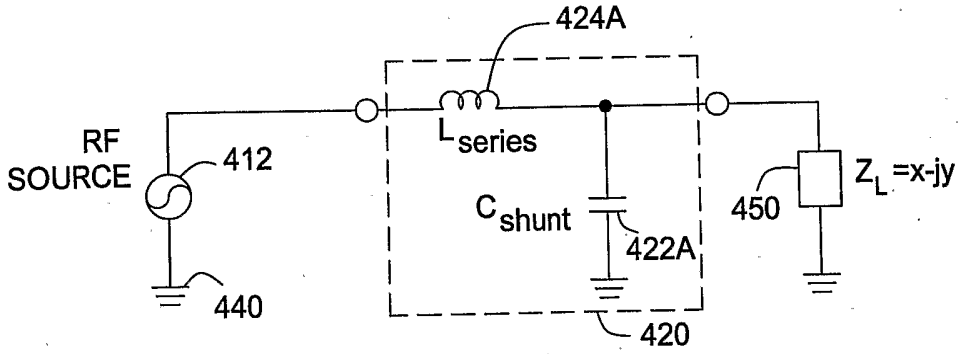


FIG. 4C (PRIOR ART)

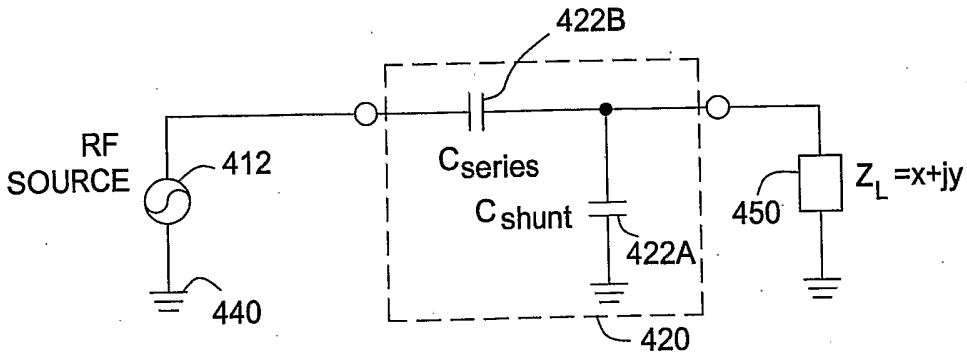


FIG. 4D (PRIOR ART)

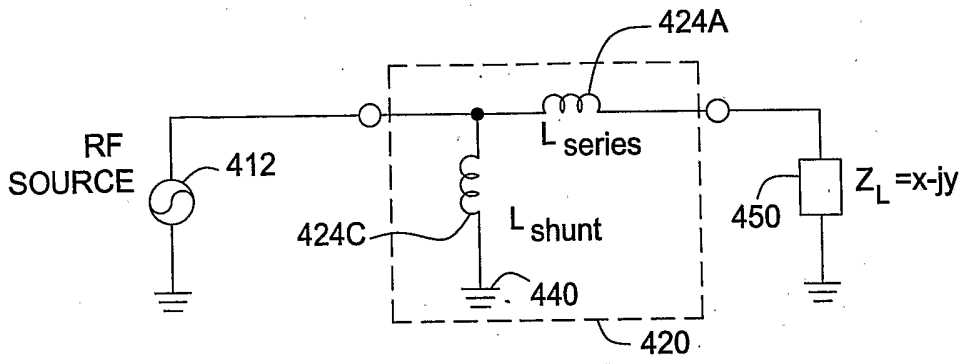


FIG. 4E (PRIOR ART)

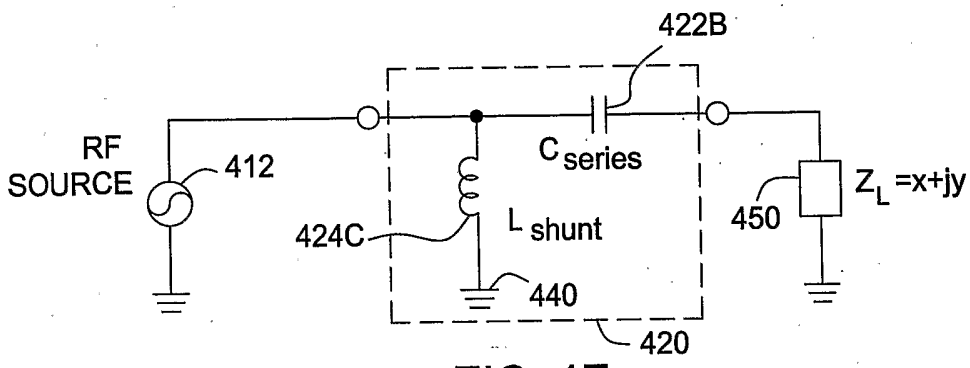


FIG. 4F (PRIOR ART)

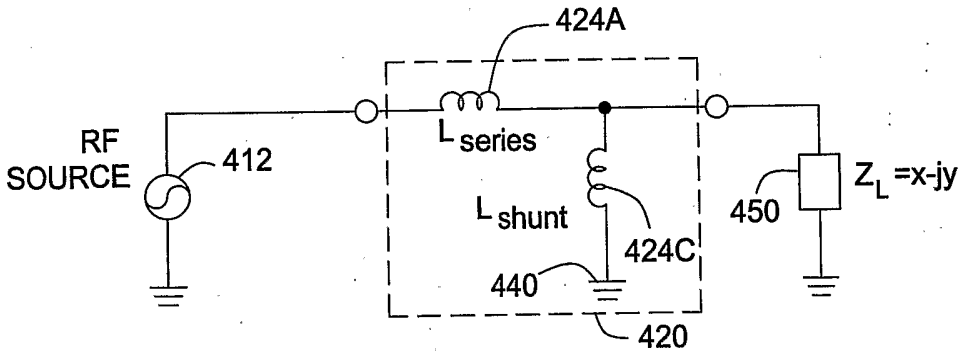


FIG. 4G (PRIOR ART)

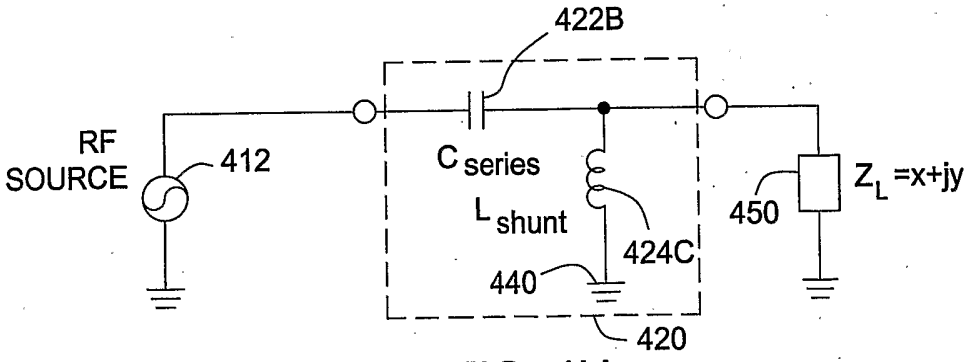


FIG. 4H (PRIOR ART)

INTERNATIONAL SEARCH REPORT

Internation: ılication No
PCT/US 03/24905

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03H7/40 H01J37/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03H H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	EP 0 840 350 A (APPLIED MATERIALS INC) 6 May 1998 (1998-05-06) page 8, column 13, line 39 -page 11, column 19, line 4; figure 6	1,9 2,6, 10-12, 22,23

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
1 December 2003	15/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Coppieters, C

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US 03/24905

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