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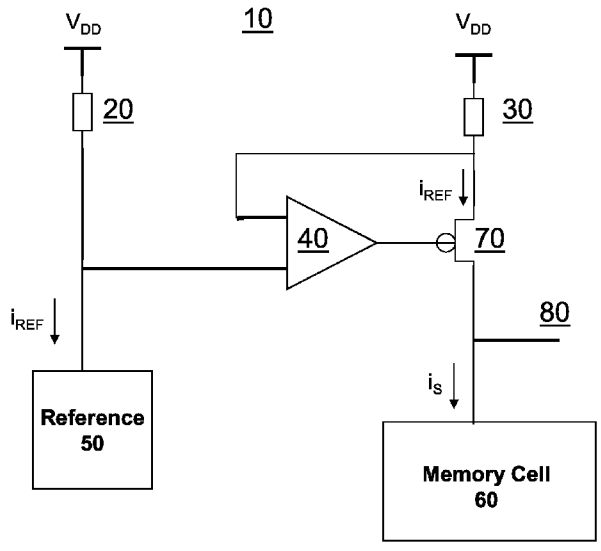
(54) Title: LOW VOLTAGE CURRENT REFERENCE GENERATOR FOR A SENSING AMPLIFIER

FIG. 1



(57) Abstract: A non-volatile memory device with a sensing amplifier (10) that includes a current mirror comprising a pair of resistors (20,30) and an operational amplifier (40) is disclosed.

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LOW VOLTAGE CURRENT REFERENCE GENERATOR FOR A SENSING AMPLIFIER

TECHNICAL FIELD

[0001] A non-volatile memory cell with an improved sensing amplifier is disclosed.

BACKGROUND OF THE INVENTION

[0002] Non-volatile semiconductor memory cells using a floating gate to store charges thereon and memory arrays of such non-volatile memory cells formed in a semiconductor substrate are well known in the art. Typically, such floating gate memory cells have been of the split gate type, or stacked gate type.

[0003] Read operations usually are performed on floating gate memory cells using sensing amplifiers. A sensing amplifier for this purpose is disclosed in U.S. Patent No. 5,386,158 (the "'158 Patent"), which is incorporated herein by reference for all purposes. The '158 Patent discloses using a reference cell that draws a known amount of current. The '158 Patent relies upon a current mirror to mirror the current drawn by the reference cell, and another current mirror to mirror the current drawn by the selected memory cell. The current in each current mirror is then compared, and the value stored in the memory cell (e.g., 0 or 1) can be determined based on which current is greater.

[0004] Another sensing amplifier is disclosed in U.S. Patent No. 5,910,914 (the "'914 Patent"), which is incorporated herein by reference for all purposes. The '914 Patent discloses a sensing circuit for a multi-level floating gate memory cell or MLC, which can store more than one bit of data. It discloses the use of multiple reference cells that are utilized to determine the value stored in the memory cell (e.g., 00, 01, 10, or 11). Current mirrors are utilized in this approach as well.

[0005] The current mirrors of the prior art utilize PMOS transistors. One characteristic of PMOS transistors is that a PMOS transistor can only be turned "on" if the voltage applied to the gate is less than the voltage threshold of the device, typically referred to as V_{TH}. One drawback of using current mirrors that utilize PMOS transistors is that the PMOS transistor causes a V_{TH} drop. This hinders the ability of designers to create sensing amplifiers that operate at lower voltages.

[0006] Another drawback of the prior art design is that PMOS transistors are relatively slow when the gate transitions from high to low (i.e., when the PMOS transistor turns on). This results in delay of the overall sensing amplifier.

[0007] What is needed is an improved sensing circuit that operates using a lower voltage supply than in the prior art.

[0008] What is further needed is an improved sensing circuit where the voltage supply can be turned off when not in use to save power, but where the sensing circuit can become operational without a significant timing penalty once the voltage supply is turned back on.

SUMMARY OF THE INVENTION

[0009] The aforementioned problems and needs are addressed by providing a sensing circuit that utilizes a resistor pair instead of a transistor pair as a current mirror. The use of a resistor pair instead of a transistor pair enables the use of a lower voltage supply with a shorter startup time.

[0010] In one embodiment, a reference cell current is applied to a current mirror. The mirrored current is coupled to the selected memory cell. The mirrored current is compared to the selected memory cell current, and a sense output is generated that indicates the state of the memory cell (e.g., 0 or 1) and that is directly related to the relative size of the current through the selected memory cell compared to the reference current.

[0011] In another embodiment, a mirror pair block is added between the current mirror and the selected memory cell.

[0012] Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 depicts a block diagram of a sensing circuit embodiment that includes a current mirror that comprises a pair of resistors.

[0014] FIG. 2 depicts a block diagram of another sensing circuit embodiment that includes a current mirror that comprises a pair of resistors.

[0015] FIG. 3 depicts an embodiment of a mirror pair block.

[0016] FIG. 4 depicts an embodiment of a reference circuit.

[0017] FIG. 5 depicts another embodiment of a reference circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] An embodiment will now be described with reference to Figure 1. Sensing circuit 10 is shown. A power supply, V_{DD}, is provided to resistor 20 and resistor 30. Resistor 20 is coupled to one positive terminal of operational amplifier 40. Resistor 30 is coupled to another terminal of operational amplifier 40. Operational amplifier 40 acts as a clamp loop. The output of operational amplifier 40 is coupled to the gate of PMOS transistor 70. The gate of PMOS transistor 70 is coupled to resistor 30. The drain of PMOS transistor 70 is coupled to memory cell 60. Resistor 20 is also coupled to reference circuit 50. As can be seen, resistor 20 and resistor 30 each have a first terminal and a second terminal. The source, drain, and gate of PMOS transistor 70 also are terminals.

[0019] Reference circuit 50 will draw a set amount of current, i_{REF}. The current through resistor 20 will be i_{REF}. Because operational amplifier 40 acts as a clamp loop, the voltage drop across resistor 20 and resistor 30 will be the same, and they therefore will form a current mirror, and the current through resistor 30 also will be i_{REF} (or a multiple thereof, if the values of resistor 20 and resistor 30 are not equal).

[0020] In operation, memory cell 60 will draw a level of current, i_S, that depends upon the value stored in the memory cell. For example, memory cell 60 might draw a low amount of current if it is storing a "0" and a high amount of current if it is storing a "1."

[0021] In this example, if $i_{REF} > i_S$, then sense output 80 will have a relatively high voltage. If $i_{REF} < i_S$, then sense output 80 will have a relatively low voltage. Thus, if the value stored in memory cell 60 is "0," then i_S will be relatively low and i_{REF} will be greater than i_S, meaning that sense output 80 will have a high voltage representing a "1." If the value stored in memory cell 60 is "1," then i_S will be relatively high and i_{REF} will be less than i_S, meaning

that sense output 80 will have a low voltage representing a "0." Thus, sense output 80 is the inverse of the value stored in memory cell 60. Optionally, sense output 80 can be coupled to an inverter (not shown), where the inventor would then output a value that directly corresponds to the value stored in memory cell 60.

[0022] In this example, because the current mirror is created using paired resistors instead of paired transistors, V_{DD} can be a lower voltage than in a system using paired transistors. This design allows V_{DD} to be able to operate at a voltage of less than 1.0V. For example, the disclosed embodiments can operate at a minimum voltage of around 0.9V.

[0023] A different embodiment will now be described with reference to Figure 2. Sensing circuit 110 is shown. A power supply, V_{DD}, is provided to resistor 120 and resistor 130. Resistor 120 is coupled to the positive terminal of operational amplifier 140. Resistor 130 is coupled to the negative terminal of operational amplifier 140. Operational amplifier 140 acts as a clamp loop. The output of operational amplifier 140 is coupled to the gate of PMOS transistor 170. The gate of PMOS transistor 170 is coupled to resistor 130. The drain of PMOS transistor 70 is coupled to mirror pair block 190. Mirror pair memory block 190 is coupled to memory cell 160. Sense output 180 is the output of sensing circuit 110 and is a port by which the output can be obtained. As can be seen, resistor 120 and resistor 130 each have a first terminal and a second terminal. The source, drain, and gate of PMOS transistor 170 also are terminals.

[0024] Reference circuit 150 will draw a set amount of current, i_{REF}. The current through resistor 120 will be i_{REF}. Because operational amplifier 140 acts as a clamp loop, the voltage drop across resistor 120 and resistor 130 will be the same, and they therefore will form a current mirror, and the current through resistor 130 also will be i_{REF} (or a multiple thereof, depending upon the values of resistor 120 and resistor 130).

[0025] In operation, memory cell 160 will draw a level of current, i_S, that depends upon the value stored in the memory cell. For example, memory cell 60 might draw a low amount of current if it is storing a "0" and a high amount of current if it is storing a "1."

[0026] Additional detail on mirror pair block 190 will now be described with reference to Figure 3. Here, we again see resistor 130 and PMOS transistor 170 as we did in Figure 2. The drain of PMOS transistor 170 is coupled to the input of mirror pair block 190. The input

will be current i_{REF}. Mirror pair block 190 comprises NMOS transistor 191 and NMOS transistor 192, which are configured as a current mirror. The gates of NMOS transistor 191 and NMOS transistor 192 are coupled together to the gate of NMOS transistor 191, and the drains of NMOS transistor 191 and NMOS transistor 192 are coupled to ground. The voltage drop from gate to drain will be the same for NMOS transistor 191 and NMOS transistor 192, and the current through NMOS transistor 192 therefore also will be i_{REF} (or a multiple thereof, depending on the characteristics of NMOS transistor 191 and NMOS transistor 192).

[0027] Mirror pair block 190 comprises PMOS transistor 193 and PMOS transistor 194. The sources of PMOS transistor 193 and PMOS transistor 194 are connected to V_{DD}. The gates of PMOS transistor 193 and PMOS transistor 194 are connected together and to the drains of PMOS transistor 193, which in turn connects to the source of NMOS transistor 192. The voltage drop from the source-to-gate junction in PMOS transistor 193 and PMOS transistor 194 will be the same. Therefore, PMOS transistor 193 and PMOS transistor 194 will act as a current mirror, and the current through PMOS transistor 194 also will be i_{REF} (or a multiple thereof, depending on the characteristics of PMOS transistor 193 and PMOS transistor 194). The drain of PMOS transistor 194 is coupled to sense output 180, which in turn is connected to memory cell 160.

[0028] The current through sense output 180 will be i_{REF}-i_S. If $i_S > i_{REF}$, then this value will be negative, and sense output 180 will detect a low voltage (i.e., a "0"). If $i_S < i_{REF}$, then this value will be positive, and sense output 180 will detect a high voltage (i.e., a "1"). Thus, sense output 180 is the inverse of the value stored in memory cell 160. Optionally, sense output 180 can be coupled to an inverter (not shown), where the inventor would then output a value that directly corresponds to the value stored in memory cell 160.

[0029] Figure 4 shows an embodiment of a reference circuit, shown as reference circuit 200. Reference circuit 200 can be used for reference circuit 50 or 50, discussed previously. Reference circuit 200 comprises operation amplifier 210. The negative node of operational amplifier 210 is connected to a voltage source (not shown) generating a voltage V_{REF}. V_{REF} can be, for example, 0.8 volts. The output of operational amplifier 210 is connected to the gate of NMOS transistor. The drain of NMOS transistor 220 is the input of the reference circuit 200. The source of NMOS transistor 220 connects to reference memory cell 230.

[0030] Figure 5 shows another embodiment of a reference circuit, shown as reference circuit 300. Reference circuit 300 can be used for reference circuit 50 or 50, discussed previously. Reference circuit 300 comprises inverter 310. The output of inverter 310 is connected to the gate of PMOS transistor 320. The source of PMOS transistor is the input of the reference circuit 200. The drain of PMOS transistor is connected to reference memory cell 330 and is the input to inverter 310.

[0031] Optionally, reference circuit 50 or reference circuit 150 could each comprise a current source circuit. Examples of current source circuits suitable for this purpose are well-known to those of ordinary skill in the art

[0032] References to the present invention herein are not intended to limit the scope of any claim or claim term, but instead merely make reference to one or more features that may be covered by one or more of the claims. Materials, processes and numerical examples described above are exemplary only, and should not be deemed to limit the claims. It should be noted that, as used herein, the terms "over" and "on" both inclusively include "directly on" (no intermediate materials, elements or space disposed there between) and "indirectly on" (intermediate materials, elements or space disposed there between). Likewise, the term "adjacent" includes "directly adjacent" (no intermediate materials, elements or space disposed there between) and "indirectly adjacent" (intermediate materials, elements or space disposed there between). For example, forming an element "over a substrate" can include forming the element directly on the substrate with no intermediate materials/elements there between, as well as forming the element indirectly on the substrate with one or more intermediate materials/elements there between.

What Is Claimed Is:

1. An apparatus for use in a memory device, comprising:

a current mirror comprising a first resistor and a second resistor, the first resistor comprising a first terminal and second terminal and the second resistor comprising a first terminal and a second terminal;

a voltage source coupled to the first terminal of the first resistor and coupled to the first terminal of the second resistor;

a reference circuit coupled to the second terminal of the first resistor;

a transistor comprising a first terminal and a second terminal, wherein the first terminal of the transistor is coupled to the second terminal of the second resistor;

a selected memory cell coupled to the second terminal of the transistor;

wherein the second terminal of the transistor provides a voltage indicative of the value stored in the selected memory cell.

2. The apparatus of claim 1, wherein the voltage source provides a voltage of 1.0 volts or less.

3. The apparatus of claim 1, wherein the selected memory cell is a floating gate memory cell.

4. The apparatus of claim 1, wherein the reference circuit comprises a reference memory cell.

5. The apparatus of claim 4, wherein the reference memory cell is a floating gate memory cell.

6. The apparatus of claim 4, wherein the reference circuit comprises an operational amplifier.

7. The apparatus of claim 4, wherein the reference circuit comprises an inverter.

8. The apparatus of claim 1, wherein the reference circuit comprises a current source.

9. An apparatus for use in a memory device, comprising:

a first resistor, wherein a first terminal of the first resistor is coupled to a voltage source;

a reference circuit coupled to a second terminal of the first resistor;

a second resistor, wherein a first terminal of the second resistor is coupled to the voltage source;

an operational amplifier, wherein a positive input terminal of the operational amplifier is coupled to a second terminal of the first resistor and a negative input terminal of the operational amplifier is coupled to a second terminal of the second resistor;

a PMOS transistor comprising a first terminal, a second terminal, and a third terminal, wherein the first terminal of the PMOS transistor is coupled to a second terminal of the second resistor and the third terminal of the PMOS transistor is coupled to an output of the operational amplifier;

a selected memory cell coupled to the second terminal of the PMOS transistor;

wherein the drain of the PMOS transistor provides a voltage indicative of the value stored in the selected memory cell.

10. The apparatus of claim 9, wherein the voltage source provides a voltage of 1.0 volts or less.

11. The apparatus of claim 9, wherein the selected memory cell is a floating gate memory cell.

12. The apparatus of claim 9, wherein the reference circuit comprises a reference memory cell.

13. The apparatus of claim 12, wherein the reference memory cell is a floating gate memory cell.

14. The apparatus of claim 12, wherein the reference circuit comprises an operational amplifier.

15. The apparatus of claim 12, wherein the reference circuit comprises an inverter.

16. The apparatus of claim 9, wherein the reference circuit comprises a current source.

17. An apparatus for use in a memory device, comprising:

a first resistor, wherein a first terminal of the first resistor is coupled to a voltage source;

a reference circuit coupled to a second terminal of the first resistor;

a second resistor, wherein a first terminal of the second resistor is coupled to the voltage source;

an operational amplifier, wherein a positive input terminal of the operational amplifier is coupled to a second terminal of the first resistor and a negative input terminal of the operational amplifier is coupled to a second terminal of the second resistor;

a PMOS transistor, wherein a first terminal of the PMOS transistor is coupled to a second terminal of the second resistor and a third terminal of the PMOS transistor is coupled to an output of the operational amplifier;

a mirror pair block comprising a first terminal and second terminal, wherein the first terminal of the mirror pair block is coupled to the second terminal of the PMOS transistor and the second terminal of the mirror pair block is coupled to a selected memory cell;

an output port, coupled to the second terminal of the mirror pair block, that provides a voltage indicative of the value stored in the selected memory cell.

18. The apparatus of claim 17, wherein the voltage source provides a voltage of 1.0 volts or less.

19. The apparatus of claim 17, wherein the selected memory cell is a floating gate memory cell.

20. The apparatus of claim 17, wherein the reference circuit comprises a reference memory cell.

21. The apparatus of claim 20, wherein the reference memory cell is a floating gate memory cell.

22. The apparatus of claim 20, wherein the reference circuit comprises an operational amplifier.

23. The apparatus of claim 20, wherein the reference circuit comprises an inverter.

24. The apparatus of claim 17, wherein the reference circuit comprises a current source.

FIG. 1

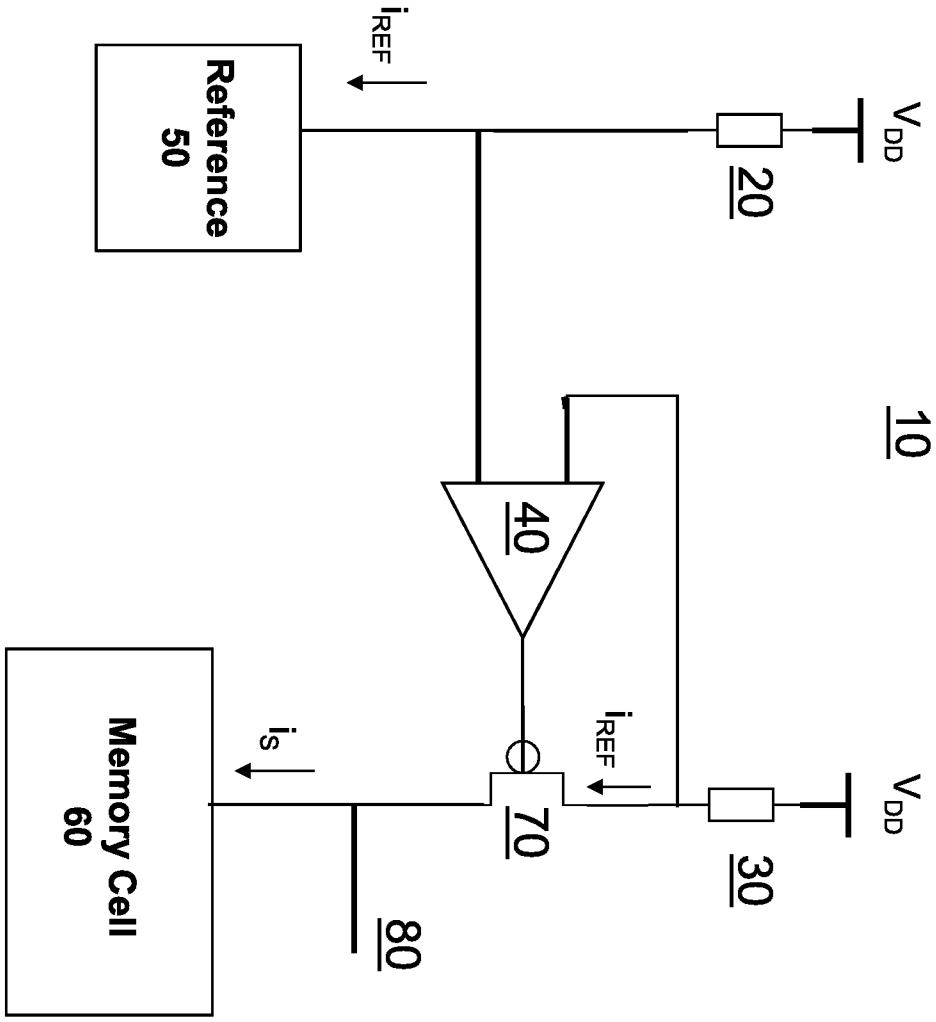

Reference
50
i_{REF}
V_{DD}
20
10
40
Memory Cell
60
i_S
i_{REF}
V_{DD}
70
30
80

FIG. 2

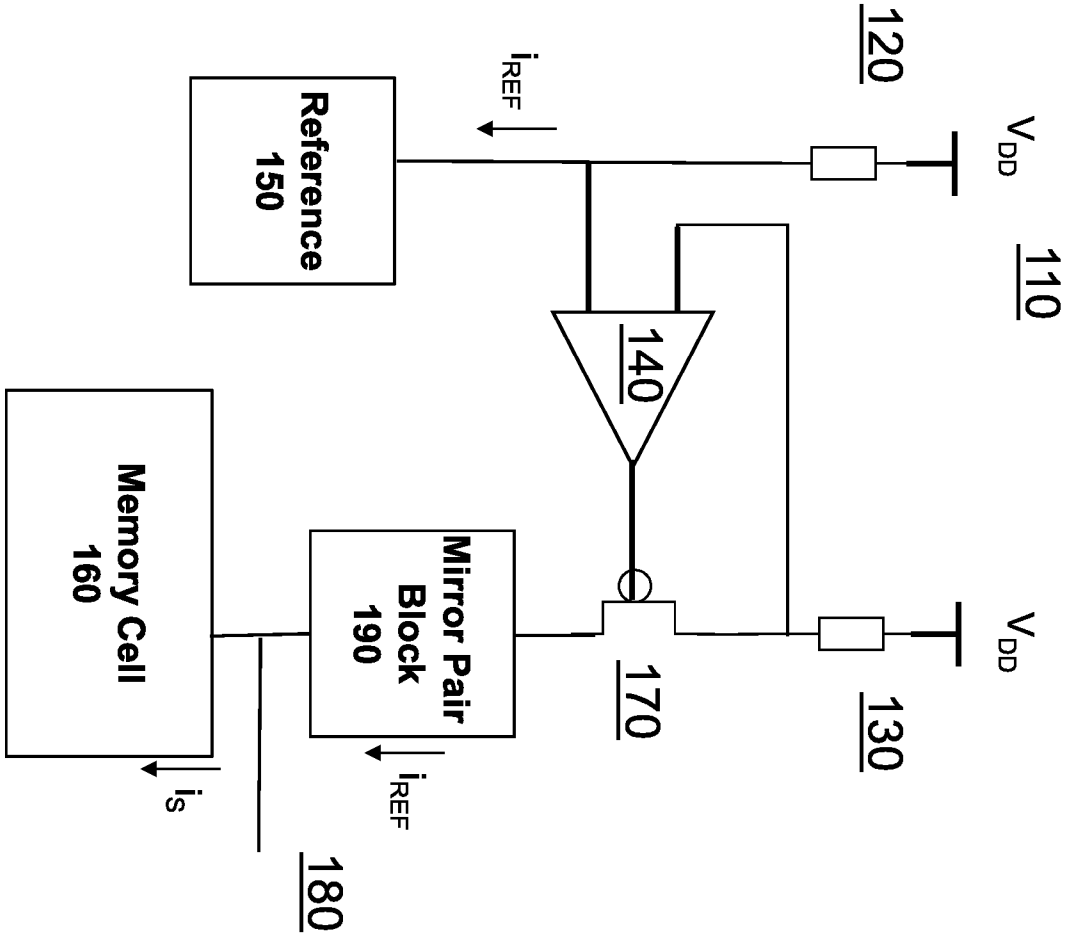
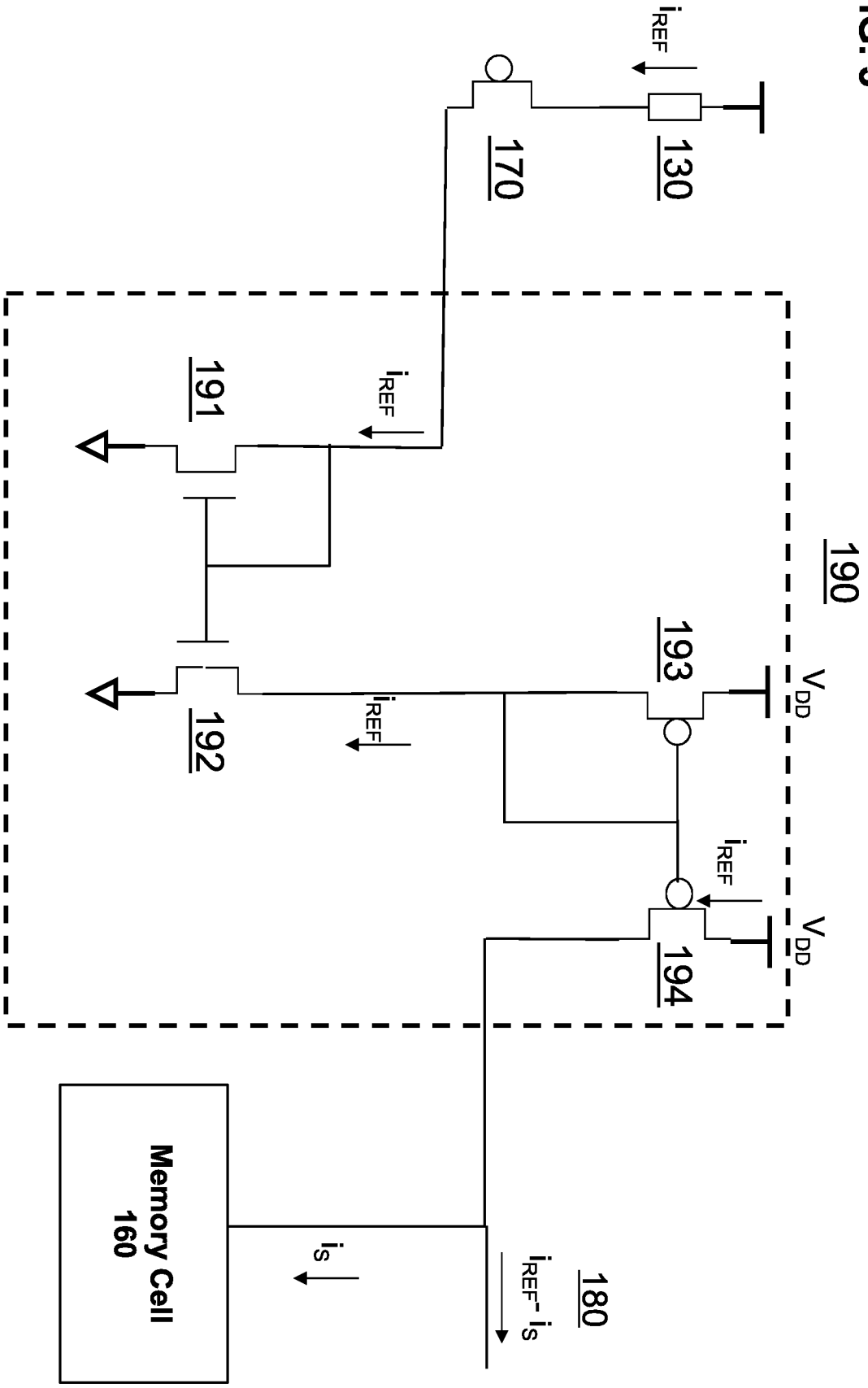

120
V_{DD}
110
i_{REF}
Reference
150
140
Memory Cell
160
Mirror Pair
Block
190
170
V_{DD}
130
i_{REF}
i_S
180

FIG. 3


i_{REF}
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170
190
191
192
193
194
V_{DD}
V_{DD}
i_{REF}
i_{REF}
i_{REF}
180
i_{REF}- i_S
i_S
Memory Cell
160

FIG. 4

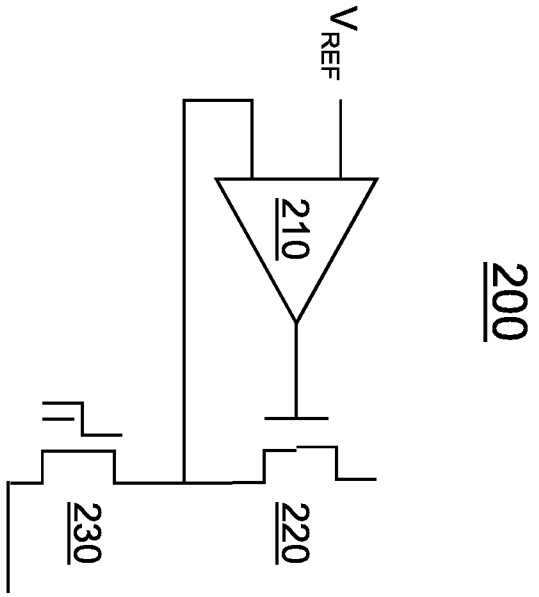
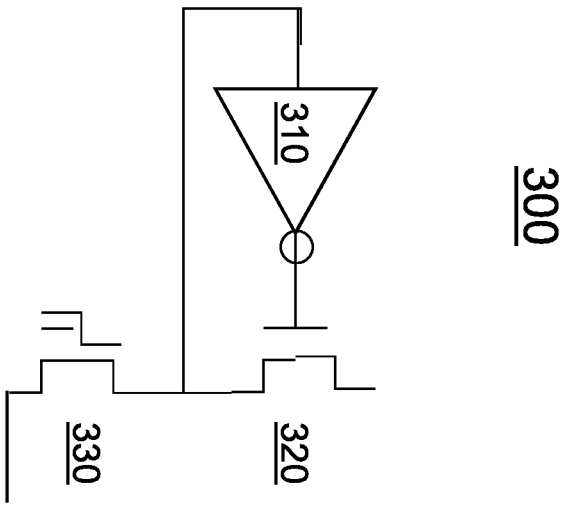


FIG. 5



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/063272

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C7/06 G11C16/28
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 2006/202763 A1 (NIKI YOSHIKI [JP] ET AL) 14 September 2006 (2006-09-14) paragraphs [0048], [0063] - paragraphs [0073], [0087]; claims 8-16; figure 8	1-24
Y	EP 0 936 627 A1 (ST MICROELECTRONICS SRL [IT]) 18 August 1999 (1999-08-18) paragraph [0028] - paragraph [0045]; figure 3 paragraph [0017] - paragraph [0020]; figures 1,2	1-24

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 February 2014	14/02/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Cummings, Anthony

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/063272

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/265783 A1 (KERN THOMAS [DE]) 21 October 2010 (2010-10-21) paragraph [0035] - paragraph [0037]; figure 7	6,14,22
A	US 2004/062116 A1 (TAKANO YOSHINORI [JP] ET AL) 1 April 2004 (2004-04-01) figures 6-13,18-20	1-6, 9-14, 17-22
A	US 2004/228162 A1 (PASOTTI MARCO [IT] ET AL) 18 November 2004 (2004-11-18) paragraph [0032] - paragraph [0046]; figure 2	3-7, 11-15, 19-23
A	US 2007/109157 A1 (LEE POONGYUEB [CA] ET AL LEE POONGYEUB [US] ET AL) 17 May 2007 (2007-05-17) figure	7,15,23
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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