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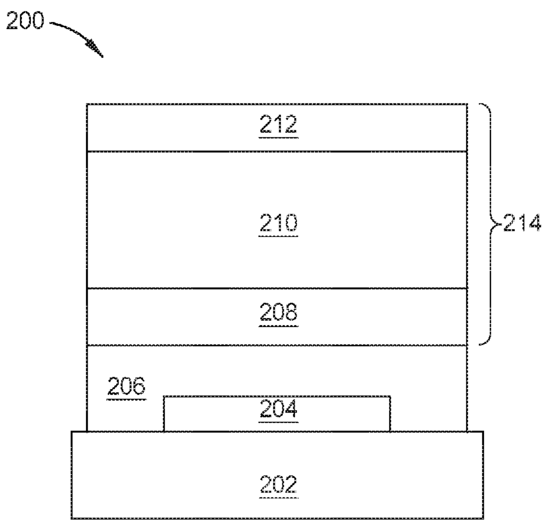

FIG. 2

(57) **Abstract:** Embodiments of the present disclosure generally relate to an organic light emitting diode device, and more particularly, to moisture barrier films utilized in an OLED device. The OLED device comprises a thin film encapsulation structure and/or a thin film transistor. A moisture barrier film is used as a first barrier layer in the thin film encapsulation structure and as a passivation layer and/or a gate insulating layer in the thin film transistor. The moisture barrier film comprises a silicon oxynitride material having a low refractive index of less than about 1.5, a low water vapor transmission rate of less than about 5.0 x 10^{-5} g/m^2/day, and low hydrogen content of less than about 8%.

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MOISTURE BARRIER FILM HAVING LOW REFRACTION INDEX AND LOW WATER VAPOR TRAMISSION RATE

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to an organic light emitting diode (OLED) device, and more particularly, to moisture barrier films utilized in an OLED device.

Description of the Related Art

[0002] An OLED structure is used in the manufacture of television screens, computer monitors, mobile phones, other hand-held devices, etc. for displaying information. OLED displays have gained significant interest recently in display applications due to their faster response time, larger viewing angles, higher contrast, lighter weight, low power, and amenability to flexible substrates, such as compared to liquid crystal displays (LCD).

[0003] OLED structures may have a limited lifetime, characterized by a decrease in electroluminescence efficiency and an increase in drive voltage. A main reason for the degradation of OLED structures is the formation of non-emissive dark spots due to moisture or oxygen ingress. For this reason, OLED structures are typically encapsulated by an organic layer sandwiched between inorganic layers, where the inorganic layers act as moisture barrier layers. However, such an encapsulation structure may cause interference between each of the layers, resulting in an optical loss of about 30% or greater.

[0004] Therefore, there is a need for an improved encapsulation structure for an OLED structure.

SUMMARY

[0005] Embodiments of the present disclosure generally relate to an organic light emitting diode device, and more particularly, to moisture barrier films utilized in an OLED device. The OLED device comprises a thin film encapsulation structure and/or a

thin film transistor. A moisture barrier film is used as a first barrier layer in the thin film encapsulation structure and as a passivation layer and/or a gate insulating layer in the thin film transistor. The moisture barrier film comprises a silicon oxynitride material having a low refractive index of less than about 1.5, a low water vapor transmission rate of less than about 5.0 x 10^{-5} g/m^2/day, and low hydrogen content of less than about 8%.

[0006] In one embodiment, a thin film encapsulation structure comprises a first barrier layer, the first barrier layer comprising a silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0 x 10^{-5} g/m^2/day, and a hydrogen content of less than about 8%. A buffer layer is disposed on the first barrier layer, and a second barrier layer is disposed on the buffer layer.

[0007] In another embodiment, a thin film transistor comprises a gate electrode, a gate insulating layer disposed over the gate electrode, the gate insulating layer comprising a silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0 x 10^{-5} g/m^2/day, and a hydrogen content of less than about 6%. A semiconductor layer is disposed over the gate insulating layer, a drain electrode is disposed over the semiconductor layer, a source electrode is disposed adjacent to the drain electrode, and a passivation layer is disposed over the drain electrode, the source electrode, and the semiconductor layer.

[0008] In yet another embodiment, a display device comprises a light emitting device, a capping layer disposed over the light emitting device, and a thin film encapsulation structure disposed over the capping layer. The thin film encapsulation structure comprises a first barrier layer disposed over the capping layer, the first barrier layer comprising a silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0 x 10^{-5} g/m^2/day, and a hydrogen content of less than about 8%. A buffer layer is disposed on the first barrier layer, and a second barrier layer is disposed on the buffer layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic, cross sectional view of a plasma enhanced chemical vapor deposition apparatus, according to one embodiment.

[0011] Figure 2 is a schematic, cross sectional view of a display device having a thin film encapsulation structure disposed thereon, according to one embodiment.

[0012] Figures 3A-3B illustrate schematic, cross sectional views of thin film transistors utilized in a display device, according to various embodiments.

[0013] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0014] Embodiments of the present disclosure generally relate to an organic light emitting diode device, and more particularly, to moisture barrier films utilized in an OLED device. The OLED device comprises a thin film encapsulation structure and/or a thin film transistor. A moisture barrier film is used as a first barrier layer in the thin film encapsulation structure and as a passivation layer and/or a gate insulating layer in the thin film transistor. The moisture barrier film comprises a silicon oxynitride material having a low refractive index of less than about 1.5, a low water vapor transmission rate of less than about 5.0×10^{-5} g/m^2/day, and low hydrogen content of less than about 8%.

[0015] Figure 1 is a schematic, cross sectional view of a plasma enhanced chemical vapor deposition (PECVD) apparatus 101 that may be used to perform the operations described herein. The PECVD apparatus 101 includes a chamber 100 in which one or more films may be deposited onto a substrate 120. The chamber 100 generally includes walls 102, a bottom 104, and a showerhead 106, which collectively define a process volume. The process volume may be a vacuum environment. A substrate support 118 is disposed within the process volume. The process volume is accessed through a slit valve opening 108 such that the substrate 120 may be transferred in and out of the chamber 100. The substrate support 118 may be coupled to an actuator 116 to raise and lower the substrate support 118. Lift pins 122 are moveably disposed through the substrate support 118 to move the substrate 120 to and from the substrate receiving surface. The substrate support 118 may also include heating and/or cooling elements 124 to maintain the substrate support 118 at a desired temperature. The substrate support 118 may also include RF return straps 126 to provide an RF return path at the periphery of the substrate support 118.

[0016] The showerhead 106 is coupled to a backing plate 112 by a fastening mechanism 150. The showerhead 106 may be coupled to the backing plate 112 by one or more fastening mechanisms 150 to help prevent sag and/or control the straightness/curvature of the showerhead 106.

[0017] A gas source 132 is coupled to the backing plate 112 to provide gas through gas passages in the showerhead 106 to a processing area between the showerhead 106 and the substrate 120. A vacuum pump 110 is coupled to the chamber 100 to maintain the process volume at a desired pressure. An RF source 128 is coupled through a match network 190 to the backing plate 112 and/or to the showerhead 106 to provide an RF current to the showerhead 106. The RF current creates an electric field between the showerhead 106 and the substrate support 118 so that a plasma may be generated from the gases between the showerhead 106 and the substrate support 118.

[0018] A remote plasma source 130, such as an inductively coupled remote plasma source 130, may also be coupled between the gas source 132 and the backing plate

112. Between processing substrates, a cleaning gas may be provided to the remote plasma source 130 so that a remote plasma is generated. The radicals from the remote plasma may be provided to chamber 100 to clean chamber 100 components. The cleaning gas may be further excited by the RF source 128 provided to the showerhead 106.

[0019] The showerhead 106 may additionally be coupled to the backing plate 112 by showerhead suspension 134. In one embodiment, the showerhead suspension 134 is a flexible metal skirt. The showerhead suspension 134 may have a lip 136 upon which the showerhead 106 may rest. The backing plate 112 may rest on an upper surface of a ledge 114 coupled with the chamber walls 102 to seal the chamber 100 to form the vacuum environment.

[0020] Figure 2 is a schematic, cross sectional view of a display device 200 having a thin film encapsulation (TFE) structure 214 disposed thereon, according to one embodiment. The display device 200 comprises a substrate 202. The substrate 202 may be made of a silicon-containing material, glass, polyimide, or plastic, such as polyethyleneterephthalate (PET) or polyethyleneterephthalate (PEN). A light emitting device 204 is disposed on the substrate 202. The light emitting device 204 may be an OLED structure or a quantum-dot structure. A contact layer (not shown) may be disposed between the light emitting device 204 and the substrate 202, and the contact layer is in contact with the substrate 202 and the light emitting device 204.

[0021] A capping layer 206 is disposed over the light emitting device 204 and the substrate 202. The capping layer 206 may have a refractive index of about 1.7 to about 1.8. A thin metal layer (not shown) may be disposed over the capping layer 206. A first barrier layer 208 is disposed on the capping layer 206 or the thin metal layer. A buffer layer 210 is disposed on the first barrier layer 208. A second barrier layer 212 is disposed on the buffer layer 210. The first barrier layer 208, the buffer layer 210, and the second barrier layer 212 comprise the TFE structure 214. The first barrier layer 208 and the second barrier layer 212 are moisture barrier films or layers.

[0022] The TFE structure 214 may have a thickness of about 2 µm to about 10 µm, such as about 4 µm. The buffer layer 210 has a thickness ranging from about 2 µm to about 5 µm. The first barrier layer 208 and the second barrier layer 212 may each have a thickness of about 0.5 µm to about 3 µm. For example, the first barrier layer 208 and the second barrier layer 212 may each have a thickness of about 1 µm, and the buffer layer 210 may have a thickness of about 2 µm. The first barrier layer 208 and the second barrier layer 212 may comprise the same material, or first barrier layer 208 and the second barrier layer 212 may comprise different materials. Additionally, the first barrier layer 208 and the second barrier layer 212 may have the same thickness, or the first barrier layer 208 and the second barrier layer 212 may have different thicknesses.

[0023] The buffer layer 210 may comprise an organic material having a refractive index of about 1.5. The buffer layer 210 may comprise organosilicon compounds, such as plasma-polymerized hexamethyldisiloxane (pp-HMDSO), fluorinated plasma-polymerized hexamethyldisiloxane (pp-HMDSO:F), and hexamethyldisilazane (HMDSN). Alternatively, the buffer layer 210 may be a polymer material composed by hydrocarbon compounds. The polymer material may have a formula $C_xH_yO_z$, wherein x, y and z are integers. In one embodiment, the buffer layer 210 may be selected from a group consisting of polyacrylate, parylene, polyimides, polytetrafluoroethylene, copolymer of fluorinated ethylene propylene, perfluoroalkoxy copolymer resin, copolymer of ethylene and tetrafluoroethylene, parylene. In one specific example, the buffer layer 210 is polyacrylate or parylene.

[0024] The first barrier layer 208 is comprised of a material comprising silicon oxynitride (SiON). The SiON material of the first barrier layer 108 has a refractive index at 632 nm of less than about 1.5, such as about 1.46 to about 1.48, and a water vapor transmission rate (WVTR) of less than about 5.0×10^{-5} g/m^2/day at 40 degrees Celsius and a relative humidity of 100%. The SiON material of the first buffer layer 108 has a composition by x-ray photoelectron spectroscopy (XPS) of about 1.70 to about 2.15 of O/Si and about 0.01 to about 0.05 of N/Si. The SiON material of the first barrier layer 208 further has a density by XPS of about 2.15 g/cm^3 to about 2.20 g/cm^3, such as about 2.18 g/cm^3. The SiON material of the first barrier layer 208 has a composition by hydrogen forward scattering (HFS) of hydrogen (H_2) of about less than 8%. The SiON material of the first barrier layer 208 has a Si-O-Si peak position of about 1050 cm^{-1} to about 1080 cm^{-1} when measured by Fourier-transform infrared spectroscopy (FTIR). Additionally, the SiON material of the first barrier layer 208 has a thickness change percentage of about 104% to about 106% at 85 degrees Celsius and a relative humidity of 85% (i.e., saturated). In some embodiments, the second barrier layer 212 may comprise the same material as the first barrier layer 208 (i.e., the SiON film having the above described properties and composition).

[0025] Each layer of the TFE structure 214 may be deposited using a PECVD process and apparatus, such as the PECVD apparatus 101 of Figure 1. In some embodiments, each layer of the TFE structure 214 may be deposited using a chemical vapor deposition (CVD) process and apparatus, or an atomic layer deposition (ALD) process and apparatus. Each layer of the TFE structure 214 may be deposited in a single PECVD chamber, such as the chamber 100 of Figure 1. Purging of the PECVD chamber may be performed between cycles to minimize the risk of contamination. The single chamber process is advantageous in reducing cycle times as well as reducing the number of chambers (and equipment costs) of using a multiple chamber process.

[0026] In one embodiment, the TFE structure 214 is formed by placing the substrate 202 including the light emitting device 204 into the chamber, such as the chamber 100 of Figure 1. The capping layer 206 may be deposited on the light emitting device 204 in the PECVD chamber, or the capping layer 206 may already be deposited on the light emitting device when placed into the chamber. The first barrier layer 208 is deposited on the capping layer 206 in the chamber by a PECVD process. The PECVD process for depositing the first barrier layer 208 may include introducing a silicon-containing precursor and a nitrogen containing precursor into the PECVD chamber at a temperature of less than about 100 degrees Celsius.

[0027] In one embodiment, the first barrier layer 208 is SiON, and SiH_4, N_2O, NH_3, N_2, and H_2 gases are introduced into the chamber for depositing the SiON first barrier layer 208. The flow rate ratio of the NH_3 gas to the SiH_4 gas ranges from about 0.9 to

1.1, the flow rate ratio of the N_2O gas to the SiH_4 gas ranges from about 15.5 to 16.5, the flow rate ratio of the N_2 gas to the SiH_4 gas ranges from about 8.4 to 8.5, the flow rate ratio of the H_2 gas to the total flow ratio ranges from about 0.13 to 0.16, and the flow rate ratio of the N_2O gas to the total flow ratio ranges from about 0.23 to 0.36. The chamber pressure ranges from about 0.13 Torr to about 0.14 Torr, and a power density ranges from about 4.5 mW/mm^2 to about 6.5 mW/mm^2.

[0028] The buffer layer 210 is deposited over the first barrier layer 208 in the chamber by a PECVD process. A purge step is performed after depositing the first barrier layer 208 prior to depositing the buffer layer 210, because different precursors are being used for the deposition processes. After the buffer layer 210 is deposited, another purge step is performed. The second barrier layer 212 is deposited over the buffer layer 210, and the second barrier layer 212 may be deposited under the same process conditions as the first barrier layer 208.

[0029] Utilizing the TFE 214 having the first barrier layer 208 comprising SiON having a low refractive index of less than about 1.5, a low WVTR of less than about 5.0 x 10^{-5} $g/m^2/day$, and low H_2 content of less than about 8% enables the first barrier layer 208 to be a reliable barrier layer in transparent or flexible display devices that are moisture sensitive, H bond sensitive, and/or OH bond sensitive devices. Additionally, the first barrier layer 208 having the above mentioned properties reduces the optical loss by about 10% as compared to silicon nitride films and helps prevent moisture and/or hydrogen diffusion from occurring within the display devices, further preventing the TFE 214 from failing.

[0030] Figures 3A-3B are a schematic, cross sectional view of thin film transistors (TFT) 300, 350, respectively, utilized in a display device, according to various embodiments. The TFT 300 of Figure 3A and the TFT 350 of Figure 3B are the same; however the gate insulating layer 306 of the TFT 300 of Figure 3A is a single layer while the gate insulating layer 306 of the TFT 350 of Figure 3B is a dual layer, and the passivation layer 310 of the TFT 300 of Figure 3A is a single layer while the passivation layer 310 of the TFT 350 of Figure 3B is a dual layer. The TFT 300 of Figure 3A and the TFT 350 of Figure 3B each comprise a substrate 302. The substrate 302 may be made of a silicon-containing material, glass, polyimide, or plastic, such as PET or PEN. A gate electrode 304 is disposed on the substrate 302. The gate electrode 304 may comprise copper, tungsten, tantalum, aluminum, among others. A gate insulating layer 306 is disposed over the gate electrode 304 and the substrate 302.

[0031] A semiconductor layer 308 is disposed over the gate insulating layer 306. The semiconductor layer 308 may comprise a metal oxide semiconductor material, a metal oxynitride semiconductor material, such as indium gallium zinc oxide (IGZO), or silicon, such as amorphous silicon, crystalline silicon, and polysilicon, among others. A drain electrode 312 and a source electrode 314 are disposed on the semiconductor layer 308. The drain electrode 312 is spaced from and adjacent to the source electrode 314. The drain electrode 312 and the source electrode 314 may each comprise copper, tungsten, tantalum, aluminum, among others. A passivation layer 310 is disposed over the semiconductor layer 308, the drain electrode 312, and the source electrode 314. The passivation layer 310 and the gate insulating layer 306 are moisture barrier films or layers.

[0032] The passivation layer 310 and the gate insulating layer 306 may each individually comprise the same material as the first barrier layer 208 of Figure 2. The passivation layer 310 and/or the gate insulating layer 306 are at least partially comprised of a material comprising silicon oxynitride (SiON). The SiON material of the passivation layer 310 and/or the gate insulating layer 306 has a refractive index at 632 nm of less than about 1.5, such as about 1.46 to about 1.48, and a WVTR of less than about 5.0×10^{-5} g/m^2/day at 40 degrees Celsius and a relative humidity of 100%. The SiON material of the passivation layer 310 and/or the gate insulating layer 306 has a composition by XPS of about 1.70 to about 2.15 of O/Si and about 0.01 to about 0.05 of N/Si. The SiON material of the passivation layer 310 and/or the gate insulating layer 306 further has a density by XPS of about 2.15 g/cm^3 to about 2.20 g/cm^3. The SiON material of the passivation layer 310 and/or the gate insulating layer 306 has a Si-O-Si peak position of about 1050 cm^{-1} to about 1080 cm^{-1} when measured by FTIR. Additionally, the SiON material of the passivation layer 310 and/or the gate insulating layer 306 has a thickness change percentage of about 104% to about 106% at 85 degrees Celsius and a relative humidity of 85% (i.e., saturated).

[0033] The SiON material of the passivation layer 310 and/or the gate insulating layer 306 has a composition by HFS of hydrogen of about less than 8%. In one embodiment, the SiON material of the passivation layer 310 has a composition by HFS of hydrogen of about less than 6%, and the SiON material of the gate insulating layer 306 has a composition by HFS of hydrogen of about less than 5%. The passivation layer 310 and the gate insulating layer 306 may each comprise the SiON material having the above described properties and composition, or only one of the passivation layer 310 or the gate insulating layer 306 may comprise the SiON material having the above described properties and composition.

[0034] Figure 3A illustrates a single layer gate insulating layer 306 and a single layer passivation layer 310. The single layer gate insulating layer 306 and the single layer passivation layer 310 may each individually comprise SiON. Figure 3B illustrates a dual layer gate insulating layer 306 and a dual layer passivation layer 310. In the TFT 350 of Figure 3B, the gate insulating layer 306 comprises a layer comprising SiON 306A and a layer comprising silicon oxide (SiOx) 306B. The layer comprising SiON 306A of the gate insulating layer 306 is disposed on and in contact with the substrate 302 and the gate electrode 304. The layer comprising SiOx 306B of the gate insulating layer 306 is disposed between and in contact with the dielectric layer 308 and the layer comprising SiON 306A. The passivation layer 310 of the TFT 350 of Figure 3B comprises a layer comprising SiOx 310A and a layer comprising SiON 310B. The layer comprising SiOx 310A of the passivation layer 310 is disposed on the dielectric layer 308, the drain electrode 312, and the source electrode 314. The layer comprising SiON 310B of the passivation layer 310 is disposed on the layer comprising SiOx 310A.

[0035] The passivation layer 310 and the gate insulating layer 306 may be formed by the same PECVD process as the first barrier layer 208 of Figure 2. In some embodiments, the passivation layer 310 and the gate insulating layer 306 may be formed by a CVD or ALD process. The PECVD process for depositing the passivation layer 310 and/or the gate insulating layer 306 may include introducing a silicon-containing precursor and a nitrogen containing precursor into a PECVD chamber, such as the chamber 100 of Figure 1. In some embodiments, the passivation layer 310 is deposited at a temperature of less than about 300 degrees Celsius and the gate insulating layer 306 is deposited at a temperature of less than about 100 degrees Celsius. In one embodiment, the passivation layer 310 and the gate insulating layer 306 are each SiON, and SiH_4, N_2O, NH_3, N_2, and H_2 gases are introduced into the chamber for depositing the SiON passivation layer 310 and the SiON gate insulating layer 306. The gate insulating layer 306 is deposited first, followed by the semiconductor layer 308, followed by the passivation layer 310. The chamber may be purged between each layer deposition.

[0036] For both the passivation layer 310 and the gate insulating layer 306, the flow rate ratio of the NH_3 gas to the SiH_4 gas ranges from about 0.9 to 1.1, the flow rate ratio of the N_2O gas to the SiH_4 gas ranges from about 15.5 to 16.5, the flow rate ratio of the N_2 gas to the SiH_4 gas ranges from about 8.4 to 8.5, the flow rate ratio of the H_2 gas to the total flow ratio ranges from about 0.13 to 0.16, and the flow rate ratio of the N_2O gas to the total flow ratio ranges from about 0.23 to 0.36. The chamber pressure ranges from about 0.13 Torr to about 0.14 Torr, and a power density ranges from about 4.5 mW/mm^2 to about 6.5 mW/mm^2.

[0037] Utilizing the TFTs 300, 350 having the passivation layer 310 and/or the gate insulating layer 306 comprising SiON having a low refractive index of less than about 1.5, a low WVTR of less than about 5.0×10^{-5} $g/m^2/day$, and low H_2 content of less than about 8% enables the passivation layer 310 and/or the gate insulating layer 306 to be reliable barrier layers in transparent or flexible display devices that are moisture sensitive, H bond sensitive, and/or OH bond sensitive devices. The passivation layer 310 and/or the gate insulating layer 306 having the above mentioned properties reduce the optical loss by about 10% as compared to silicon nitride films and help prevent moisture and/or hydrogen diffusion from occurring within the display devices, further preventing the characteristics of the TFTs 300, 350 from shifting undesirably.

[0038] Moreover, utilizing the passivation layer 310 and/or the gate insulating layer 306 having a low refractive index of less than about 1.5, a low WVTR of less than about 5.0 x 10^{-5} g/m^2/day, and low H_2 content of less than about 8% results in less change in positive bias temperature stress, negative bias temperature stress, and negative bias temperature illumination stress. As such, the passivation layer 310 and/or the gate insulating layer 306 having the above mentioned properties enable better bias stability and lower turn-on voltages when integrated into the TFTs 300, 350.

[0039] Therefore, utilizing a moisture barrier film as a first barrier layer in a TFE or as a passivation layer and/or a gate insulating layer in a TFT comprising SiON having a low refractive index of less than about 1.5, a low WVTR of less than about 5.0 x 10^{-5} g/m^2/day, and low H_2 content of less than about 8% enables the layers to be reliable barrier layers in transparent or flexible display devices that are moisture sensitive, H bond sensitive, and/or OH bond sensitive devices. Additionally, the moisture barrier layers each having the above mentioned properties reduce the optical loss by about 10% as compared to silicon nitride films and help prevent moisture and/or hydrogen diffusion from occurring within the display devices, further preventing TFEs from failing and preventing the characteristics of TFTs from shifting undesirably.

[0040] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A thin film encapsulation structure, comprising:

a first barrier layer, the first barrier layer comprising a silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0×10^{-5} $g/m^2/day$, and a hydrogen content of less than about 8%;

a buffer layer disposed on the first barrier layer; and

a second barrier layer disposed on the buffer layer.

2. The thin film encapsulation structure of claim 1, wherein the second barrier layer comprises the same material as the first barrier layer.

3. The thin film encapsulation structure of claim 1, wherein the second barrier layer comprises a different material than the first barrier layer.

4. The thin film encapsulation structure of claim 1, wherein the first barrier layer has a thickness of about 0.5 micrometers to about 3 micrometers.

5. The thin film encapsulation structure of claim 1, wherein

the silicon oxynitride material has a thickness change percentage of about 104% to about 106% at 85 degrees Celsius and a relative humidity of 85%.

6. A thin film transistor, comprising:

a gate electrode;

a gate insulating layer disposed over the gate electrode, the gate insulating layer comprising a silicon oxynitride material having a refractive index of less than about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0×10^{-5} $g/m^2/day$, and a hydrogen content of less than about 6%;

a semiconductor layer disposed over the gate insulating layer;

a drain electrode disposed over the semiconductor layer;

a source electrode disposed adjacent to the drain electrode; and

a passivation layer disposed over the drain electrode, the source electrode, and the semiconductor layer.

7. The thin film transistor of claim 6, wherein the passivation layer comprises the silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0×10^{-5} g/m^2/day, and a hydrogen content of less than about 6%.

8. The thin film transistor of claim 7, wherein

the passivation layer is deposited by a plasma enhanced chemical vapor deposition process at temperature of less than about 300 degrees Celsius, or

the silicon oxynitride material has a thickness change percentage of about 104% to about 106% at 85 degrees Celsius and a relative humidity of 85%.

9. The thin film transistor of claim 7, wherein the silicon oxynitride material of the gate insulating layer is combined with a layer comprising silicon oxide to form a dual layer.

10. The thin film transistor of claim 9, wherein the silicon oxynitride material of the dual layer is disposed adjacent to the gate electrode and the layer comprising silicon oxide is disposed adjacent to the semiconductor layer, the drain electrode, and the source electrode.

11. The thin film transistor of claim 7, wherein the silicon oxynitride material of the passivation layer is combined with a layer comprising silicon oxide to form a dual layer.

12. The thin film transistor of claim 11, wherein the layer comprising silicon oxide of the dual layer is disposed adjacent to the semiconductor layer, the drain electrode, and the source electrode, and the silicon oxynitride material is disposed on the layer comprising silicon oxide.

13. A display device, comprising:

a light emitting device;

a capping layer disposed over the light emitting device; and

a thin film encapsulation structure disposed over the capping layer, the thin film encapsulation structure comprising:

a first barrier layer disposed over the capping layer, the first barrier layer comprising a silicon oxynitride material having a refractive index of about 1.46 to about 1.48, a water vapor transmission rate of less than about 5.0 x 10^{-5} $g/m^2/day$, and a hydrogen content of less than about 8%;

a buffer layer disposed on the first barrier layer; and

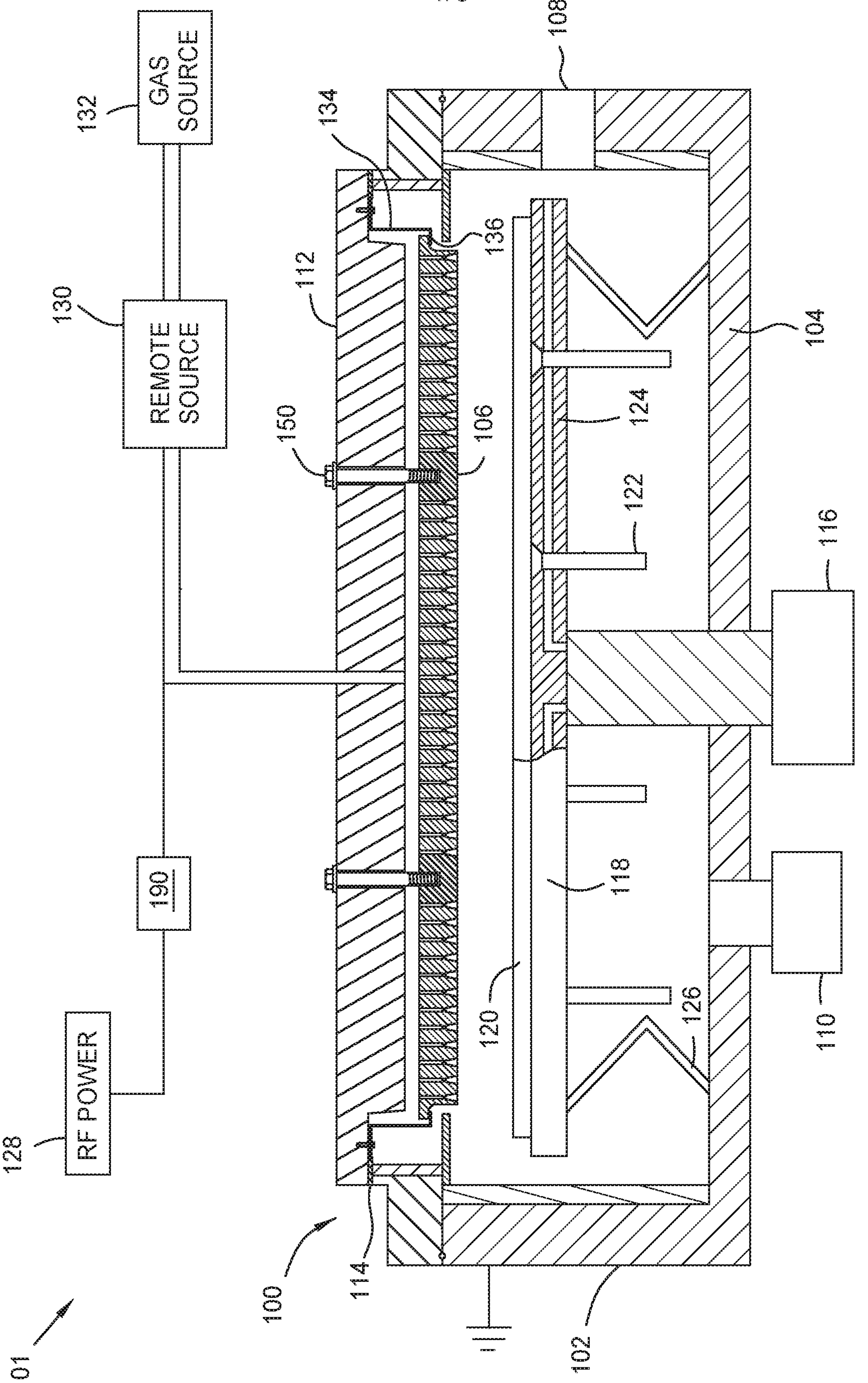
a second barrier layer disposed on the buffer layer.

14. The display device of claim 13, wherein

the light emitting device is an organic light emitting diode device, or

the second barrier layer comprises the same material as the first barrier layer.

15. The display device of claim 13, wherein the silicon oxynitride material has a thickness change percentage of about 104% to about 106% at 85 degrees Celsius and a relative humidity of 85%.



GAS SOURCE
132
REMOTE SOURCE
130
RF POWER
128
190
101
100
102
104
106
108
110
112
114
116
118
120
122
124
126
134
136
150

FIG. 1

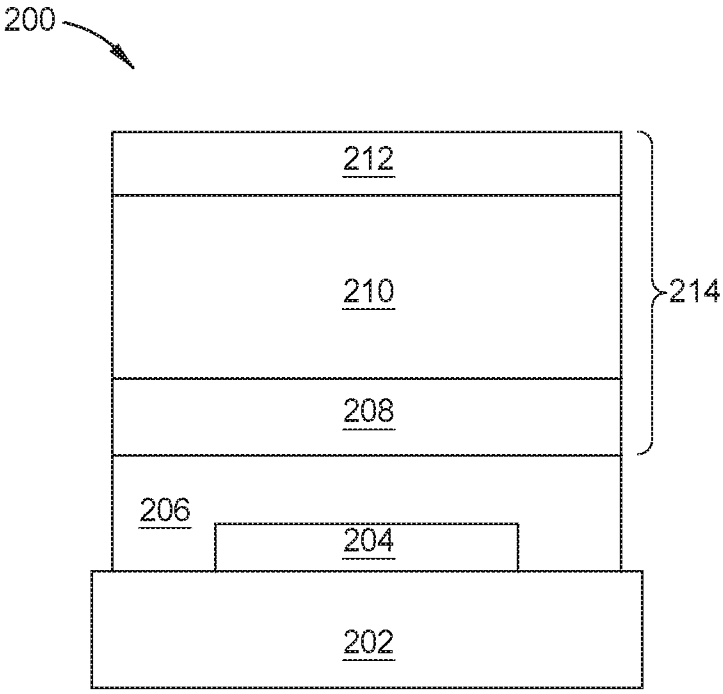


FIG. 2

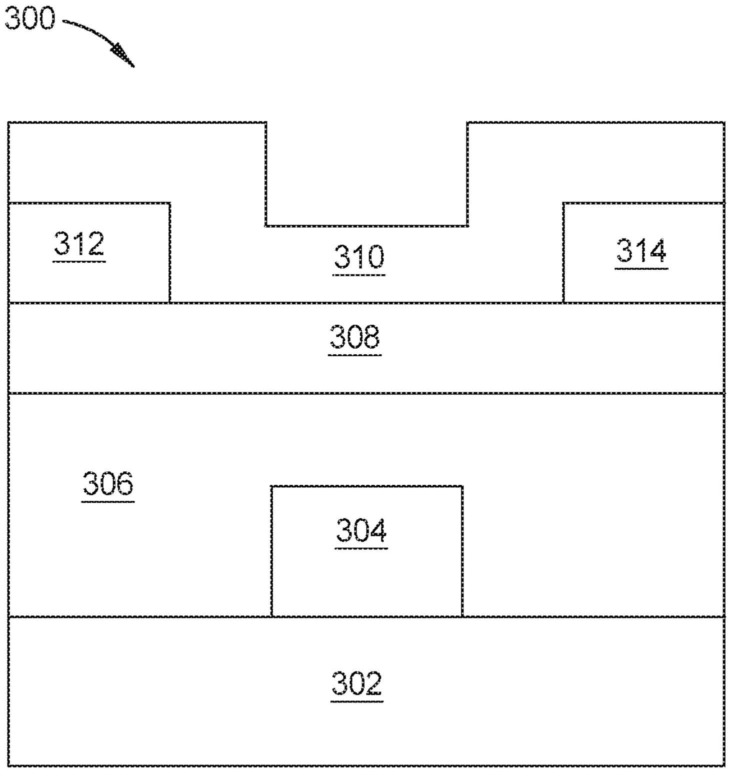


FIG. 3A

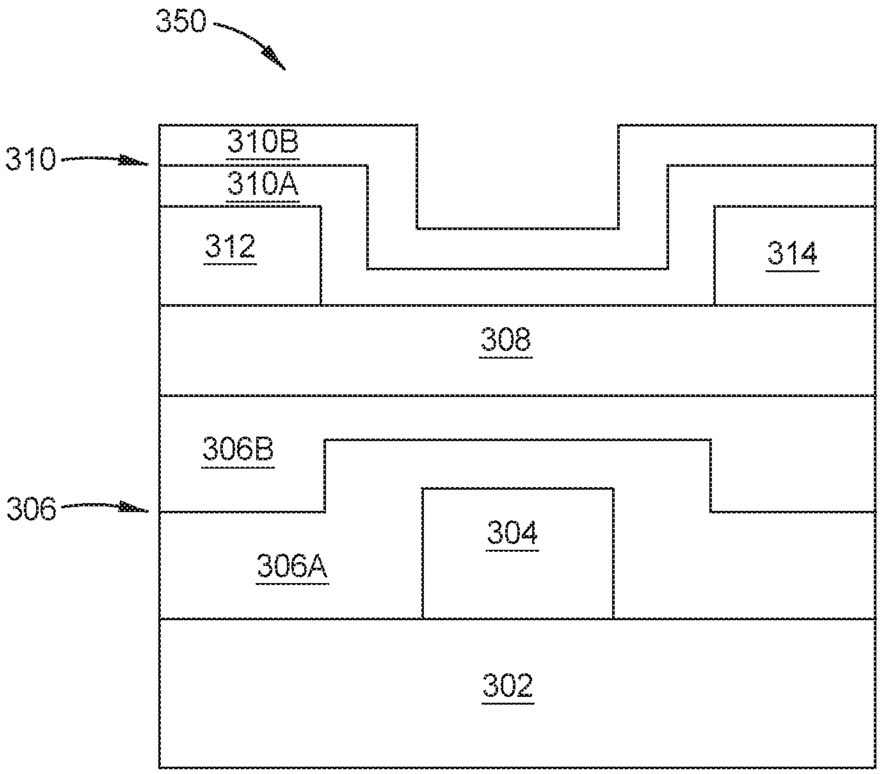


FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/041163

A. CLASSIFICATION OF SUBJECT MATTER

H01L 51/52(2006.01)i, H01L 51/56(2006.01)i, H01L 27/32(2006.01)i, H01L 29/786(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 51/52; B32B 15/08; B32B 15/082; H01L 21/02; H01L 31/0203; H01L 33/36; H01L 33/56; H01L 51/00; H01L 51/56; H01L 27/32; H01L 29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: moisture, barrier, thin film, buffer, WVTR (water vapor transmission rate)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2018-130288 A1 (APPLIED MATERIALS, INC. et al.) 19 July 2018 See paragraphs [0022]-[0038]; and figure 1 .	1-5,13-15
A		6-12
Y	KR 10-2018-0003287 A (LG DISPLAY CO., LTD.) 09 January 2018 See paragraphs [0035], [0070], [0106], [0110]; and figures 1-3.	1-15
Y	US 2016-0190511 A1 (SAMSUNG DISPLAY CO., LTD.) 30 June 2016 See paragraphs [0067]-[0081]; and figure 1.	6-12
A	US 2013-0334511 A1 (PLASMASI, INC.) 19 December 2013 See paragraphs [0058]-[0104]; and figures 1(a)-4.	1-15
A	KR 10-1942042 B1 (MAVEN OPTRONICS CO., LTD.) 25 January 2019 See paragraphs [0028]-[0060]; and figures 1a-1f.	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 January 2020 (21.01.2020)	**22 January 2020 (22.01.2020)**

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2019/041163

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