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(54) Title: DISTRIBUTED RC TERMINATION

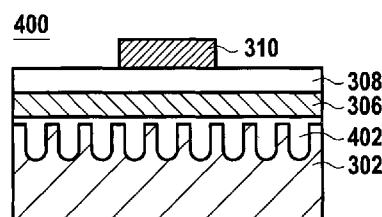
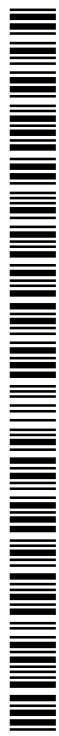


FIG.4

(57) Abstract: An integrated resistor-capacitor (RC) structure (400) is disclosed. The integrated RC structure includes a vertical capacitor (302, 402, 306) and a resistive element (308, 310) disposed above the capacitor. The integrated RC structure uses a low ohmic substrate (302) to ensure a good ground return path for the capacitor. Further, a resistivity of the substrate is configured such that a top plate (306) of the capacitor provides a reference ground above a predefined frequency. The impedance of the resistive element (308, 310) is matched, relative to the reference ground, to a predetermined resistance. As such, the resistance of the resistive element (308, 310) can be controlled to provide an impedance controlled RC structure over a range of operating frequencies.



Distributed RC Termination

Field of the invention

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The present invention relates to integrated structures including resistive and capacitive elements.

Background

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In various applications, for example in radio-frequency (RF) applications such as optical transceivers or RF power amplifiers, passive elements such as resistors and capacitors are often required. As the operating bandwidth continues to increase for these applications, reaching up to several
15 GHz in some cases, it is desirable to control the behaviour of the passive elements. Specifically, it is desirable to manage bandwidth limitations due to the passive elements to ensure a substantially constant frequency response of the passive elements over the entire operating bandwidth.

For example, a decoupling capacitor and a damping resistor are often
20 used to provide signal termination in RF applications. Conventionally, these two components are implemented as separate devices on separate substrates due to antagonistic requirements for substrate properties. To ensure a wide bandwidth resistor, for example a resistor having a stable impedance value from D.C. up into the gigahertz range, a high-ohmic substrate is typically
25 needed to reduce parasitic impedance forming through the substrate. In contrast, a low-ohmic substrate is needed to facilitate a good ground return path for the decoupling capacitor.

While providing separate substrates for the capacitor and the resistor can ensure stable performance for each component, the implementation
30 requires more circuit area, a large number of interconnections, and a prolonged fabrication process.

Summary

The present invention provides a semiconductor device that integrates a capacitor and a resistive element in the same die. In an embodiment, the capacitor provides a decoupling capacitor and the resistive element provides a broadband damping resistor. Despite using a low resistivity substrate (which accommodates design considerations of the capacitor but not the resistive element), a substantially constant resistance for the resistive element can be maintained over a wide bandwidth. The low resistivity substrate ensures a good ground return path for the capacitor. With the semiconductor device configured to have a substantially constant impedance over a wide bandwidth, the device can be highly suited for use in impedance controlled circuits, such as termination circuits, for example.

More specifically, a first aspect of the present invention provides a semiconductor device, comprising:

- a substrate;
- a first dielectric layer disposed above the substrate;
- a conductive layer disposed above the first dielectric layer;
- a second dielectric layer disposed above the conductive layer; and
- a resistive layer disposed above the second dielectric layer,

wherein the substrate, the first dielectric layer and the conductive layer form a vertical capacitor,

wherein the second dielectric layer and the resistive layer form a resistive element,

wherein a resistivity of the substrate is configured such that the conductive layer provides a reference ground above a predefined frequency, and

wherein the second dielectric layer and the resistive layer are configured such that the resistive element is impedance matched, relative to the reference ground, to a predetermined resistance.

Typically, the substrate is configured to have low resistivity. In an embodiment, the resistivity of the substrate is lower than or equal to 1

mOhms.cm. In an implementation, the substrate is implemented to contain doped material. In another embodiment, a thickness of the substrate is lower than or equal to 100 micrometers. The low resistivity of the substrate allows the capacitor to have a good ground return path making the capacitor highly suited as a decoupling capacitor. In another embodiment, the capacitor is further configured to have very low parasitic components (i.e., very low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL)), thereby also having low impedance at low and high frequency.

In some embodiments, the first dielectric layer is planar or deposited into a trench etched into the substrate. The trench implementation allows to augment a surface area of the vertical capacitor, thereby increasing its capacitance. In an embodiment, the vertical capacitor is formed using Passive Integrated Common Substrate (PICS®) technology. In a particular embodiment, the capacitance per unit area of the vertical capacitor is preferably higher than 6 nF/mm².

In some embodiments, a thickness of the second dielectric layer is between 0.2 and 0.3 micrometers.

In some embodiments, a sheet resistance of the resistive layer is between 10 mOhms per square to 20 Ohms per square. In one embodiment, the resistive layer corresponds to a metallization layer made of alumina. This embodiment is suited for applications requiring a resistance of the resistive element of approximately 0.5 Ohms over 1 GHz. In another embodiment, the targeted resistance of the resistive element is approximately 50 Ohms, in which case the resistive layer may be made of tantalum nitride.

According to some embodiments, the second dielectric layer and the resistive layer (i.e., the resistive element) form a transmission line. The second dielectric layer and the resistive layer can be configured to provide a microstrip transmission line, wherein the resistive layer is disposed on top of the second dielectric layer. In another embodiment, material forming a first auxiliary ground plane is disposed to surround one or more sides of the resistive layer, thereby the second dielectric layer, the first auxiliary ground

plane and the resistive layer form a grounded coplanar transmission line. In a further embodiment, material forming a first auxiliary ground plane is disposed to surround one or more sides of the resistive layer and material forming a second auxiliary ground plane is disposed over a top surface of the resistive layer, thereby the second dielectric layer, the material forming the first and second auxiliary ground planes, and the resistive layer form a stripline transmission line.

In some embodiments, the impedance of the transmission line is configured to remain substantially constant over a predetermined frequency band. This configuration may involve configuring several properties of the transmission line, including the transmission line configuration (microstrip, coplanar, or stripline), the materials used for the second dielectric layer and the resistive layer, the shape and thickness of the resistive layer and/or the second dielectric layer, etc.

Correlatively, according to a second aspect the present invention provides a method for fabricating a semiconductor device, comprising:

- providing a substrate;
- forming a first dielectric layer above the substrate;
- forming a conductive layer above the first dielectric layer;
- forming a second dielectric layer above the conductive layer; and
- forming a resistive layer above the second dielectric layer,

wherein the second dielectric layer and the resistive layer form a resistive element,

wherein providing the substrate comprises configuring a resistivity of the substrate such that the conductive layer provides a reference ground above a predefined frequency, and

wherein forming the second dielectric layer and the resistive layer comprises configuring the second dielectric layer and the resistive layer such that the resistive element is impedance matched, relative to the reference ground, to a predetermined resistance.

Brief description of the drawings

The accompanying drawings illustrate certain embodiments of the present invention and, together with the description, serve to inform a person skilled in the art regarding how to put the invention into effect.

Figure 1 illustrates a simplified circuit diagram of a radio-frequency (RF) transmission system.

Figure 2 illustrates a simplified circuit diagram of an RF transmission system according to an embodiment.

Figure 3 illustrates a cross-section of a resistor-capacitor (RC) structure according to an embodiment.

Figure 4 illustrates a cross-section of another RC structure according to an embodiment.

Figure 5 is a three-dimensional view of a portion of the RC structure illustrated in Figure 3 or Figure 4.

Figure 6 illustrates a cross-section of a portion of another RC structure according to an embodiment.

Figure 7 is a three-dimensional view of the RC structure portion illustrated in Figure 6.

Figure 8 illustrates a cross-section of a portion of another RC structure according to an embodiment.

Figure 9 is a three-dimensional view of the RC structure portion illustrated in Figure 8.

Figure 10 illustrates the frequency response performance of a resistive element of an RC structure according to an embodiment.

The present disclosure will be described with reference to the accompanying drawings. Generally, the drawing in which an element first appears is typically indicated by the leftmost digit(s) in the corresponding reference number.

Description of the embodiments

Figure 1 illustrates a simplified circuit diagram of a radio-frequency (RF) transmission system 100. RF transmission system 100 may be a RF power transmitter or power amplifier for example. Alternatively, RF transmission system 100 may be an input stage of an optical transceiver. As shown in FIG. 1, RF transmission system 100 has a source resistance 102, a transmission line 104 having a characteristic impedance Z_c , and a resistor-capacitor (RC) circuit 106. RC circuit 106 includes a resistor 108 and a capacitor 110.

In an embodiment, where RF transmission system 100 is an RF power transmitter using envelope injection, RC circuit 106 provides an envelope termination circuit with capacitor 110 acting as a decoupling capacitor and resistor 108 acting as a damping resistor. In this case, RC circuit 106 may provide low resistive termination (below 1 Ohms) to eliminate LC-induced spikes and oscillation. In another embodiment, where RF transmission system 100 is used in an optical transceiver, RC circuit 106 may provide adapted termination (around 50 Ohms) to match a 50 Ohms transmission line.

In one embodiment, RF transmission system 100 is treated like a matched impedance line with a source impedance, a characteristic impedance, and a load impedance. RC circuit 106 is treated as the load of the matched impedance line. Impedance matching is performed by ensuring that the source impedance, the characteristic impedance of the transmission line, and the load impedance are equal. This ensures both maximum power transfer from the source to the load and reduces power reflection from the load.

In an embodiment, to ensure a high decoupling performance of capacitor 110, capacitor 110 is designed to have very low parasitic components (i.e., very low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL)) at both low and high frequency thereby ensuring that capacitor 110 has a low impedance across the operating frequency band. Furthermore, to ensure a good ground return path for capacitor 110, a low ohmic substrate is used.

As noted above, the low ohmic substrate used for capacitor performance is typically incompatible with the wideband performance requirement for resistor 108. This is because a low ohmic substrate typically increases the parasitic impedance through the substrate, resulting in a frequency variable effective resistance for resistor 108. In an embodiment, to realize a substantially constant effective resistance over a wide frequency range, resistor parasitics are controlled. In the integration, resistor 108 is laid directly on top of capacitor 110. In addition, resistor 108 is designed like a transmission line that is tuned based on a reference ground provided by the top plate of capacitor 110. This is because, with the above described capacitor design choices, capacitor 110 behaves as a wideband shunt to ground at higher frequencies.

In an embodiment, parasitics due to resistor 108 (inductive and capacitive parasitics) are distributed over the top plate capacitor so that the AC impedance of resistor 108 equals its DC resistance.

The concept of treating the resistor as a transmission line is further illustrated in Figure 2, which shows a simplified circuit diagram of an RF transmission system 200 according to an embodiment. RF transmission system 200 has a source resistance 202, a transmission line 204 having a characteristic impedance Z_c equal to a DC resistance Z_0 , and an RC circuit 206. RC circuit 206 includes a resistor 208 having a DC resistance equal to Z_0 and a capacitor 210. As shown, because capacitor 210 is designed to behave as a wideband shunt to ground, RC circuit 206 can be represented as a transmission line 212 having a DC resistance Z_0 coupled to a reference ground provided by capacitor 210.

Example implementations of embodiments are now described. These implementations are provided for the purpose of illustration only and are not limiting.

Figure 3 illustrates a cross-section of an RC structure 300 according to an embodiment. In an embodiment, RC structure 300 forms an envelope termination circuit used in an RF power transmitter utilizing envelope

injection. In an embodiment, RC structure 300 provides a decoupling capacitor and a broadband damping resistor.

As shown in FIG. 3, RC structure 300 includes a substrate 302, a first dielectric layer 304 disposed above substrate 302; a conductive layer 306
5 disposed above first dielectric layer 304; a second dielectric layer 308 disposed above conductive layer 306; and a resistive layer 310 disposed above second dielectric layer 308.

Substrate 302, first dielectric layer 304, and conductive layer 306 form a vertical capacitor, with conductive layer 306 providing the top capacitor
10 plate and substrate 302 providing the bottom capacitor plate.

In one embodiment, the vertical capacitor is configured to have very low parasitics (i.e., low ESR and ESL) and high capacitance. In a particular embodiment, the capacitance per unit area of the vertical capacitor is preferably higher than 6 nF/mm². In one implementation, the vertical
15 capacitor may be formed using Passive Integrated Common Substrate (PICS®) technology.

To ensure a good ground return path for the vertical capacitor, substrate 302 is configured to be a low ohmic substrate. In embodiments, the resistivity of substrate 302 is configured such that conductive layer 306
20 provides a reference ground above a predefined frequency. In certain embodiments, the resistivity of substrate 302 is lower than or equal to 1 mOhms.cm. To achieve the low resistivity, in some embodiments, substrate 302 contains doped material. Alternatively or additionally, substrate 302 may have a thickness that is lower than or equal to 100 micrometers. In
25 embodiments, substrate 302 can be made of a silicon material, N type or P type doped, with gallium, gallium arsenide, gallium nitride, etc.

First dielectric layer 304 can be made of silicon oxide, but other materials may be used such as, for example, nitride, alumina nitride, etc. In an embodiment, first dielectric layer 304 includes a combination of layers
30 made from one or more of the described materials. First dielectric layer 304 can be planar as shown in FIG. 3. Alternatively, as shown in FIG. 4, first

dielectric layer 304 can be deposited into one or more three dimensional trenches etched into substrate 302. The trench implementation allows to augment a surface area of the vertical capacitor, thereby further increasing its capacitance.

5 Conductive layer 306 can be made of alumina, but other materials may be used such as, for example, alumina alloy, titanium, platinum, copper, etc. As noted above, conductive layer 306 provides the top plate of the vertical capacitor. Above a predefined frequency, conductive layer 306 provides a reference ground that is used to tune the resistive element as
10 described below.

 Second dielectric layer 308 and resistive layer 310 form a resistive element. Second dielectric layer 308 can be made of Silicon oxide, nitride, polyimide, etc. In some embodiments, for example in embodiments where the target resistance of the resistive element over the operating frequency
15 range is 0.5 Ohms, a thickness of second dielectric layer 308 may be between 0.2 and 0.3 micrometers

 In an embodiment, second dielectric layer 308 and resistive layer 310 are configured such that the resistive element is impedance matched, relative to the reference ground provided by conductive layer 306, to a
20 predetermined resistance. In an embodiment, the predetermined resistance corresponds to the load resistance targeted by the application (e.g., 0.5 Ohms, 50 Ohms, etc.).

 In embodiments, a sheet resistance of resistive layer 310 is between 10 mOhms per square to 20 Ohms per square. In one embodiment, suited for
25 applications requiring a resistance of the resistive element of approximately 0.5 Ohms over 1 GHz, resistive layer 310 is provided in the form of a metallization layer made of alumina but other materials may be used such as, for example, titanium, platinum, copper, etc. In another embodiment, resistive layer 310 is made of tantalum, though other materials may also be
30 used such as, for example, tantalum nitride, tungsten, or a combination of

both. This embodiment is suitable for applications targeting a resistance of approximately 50 Ohms for the resistive element.

As noted above, according to embodiments, second dielectric layer 308 and resistive layer 310 form a transmission line. Depending on the application, different transmission line configurations can be used. For example, second dielectric layer 308 and resistive layer 310 can be configured, as shown in FIGs. 3, 4, and 5 to provide a microstrip transmission line. In this configuration, resistive layer 310 is entirely disposed above second dielectric layer 308. This configuration presents the advantage that it is easy to implement. However, because second dielectric layer 308 is in direct contact with the air, it may be sensitive to external electromagnetic perturbation.

In another embodiment, shown in a cross-sectional view and a three-dimensional view in FIGs. 6 and 7 respectively, material forming a first auxiliary ground plane 602 is disposed to surround one or more sides of resistive layer 310. Vias 604 are formed through second dielectric layer 308 to connect first auxiliary ground plane 602 to conductive layer 306. A grounded coplanar transmission line is thus formed. A coplanar transmission line configuration may be useful in embodiments requiring a lower impedance (e.g., in the range of 0.5 Ohms) as, generally, the impedance can be reduced further using this configuration than using a microstrip configuration, for example. The material forming the first auxiliary ground plane may be made of alumina or copper.

In a further embodiment, shown in a cross-sectional view and a three-dimensional view in FIGs. 8 and 9 respectively, material forming a second auxiliary ground plane 802 is disposed above resistive layer 310, in addition to the material 602 forming the first auxiliary ground plane. Specifically, an oxide layer 804 is disposed on top of first auxiliary ground plane 602 and resistive layer 310, and second auxiliary ground plane 802 is disposed on top of oxide layer 804. Vias 806 are formed through oxide layer 804 to connect second auxiliary ground plane 802 to first auxiliary ground plane 602. First

auxiliary ground plane 602, as in the coplanar transmission line configuration, is connected to conductive layer 306 using vias 604. A stripline transmission line is thus formed. One advantage of this configuration is that resistive layer 310 can be better protected from external electromagnetic perturbation. The material forming the second auxiliary ground plane may be made of alumina or copper.

In embodiments, the impedance of the transmission line is configured to remain substantially constant over a predetermined frequency band. This configuration may be performed by appropriately setting one or more properties of the transmission line, for example: the transmission line configuration (microstrip, coplanar, or stripline), the materials used for second dielectric layer 308 and resistive layer 310, the shape and thickness of resistive layer 310 and/or second dielectric layer 308, etc.

For instance, resistive and inductive components of the transmission line may be controlled by appropriate setting of the dimensions and electrical properties of resistive layer 310 and second dielectric layer 308 as well as the positioning of resistive layer 310 relative to the reference ground/auxiliary ground planes. For example, in an embodiment, the thickness of second dielectric layer 308 may be selected, and the dimensions, resistivity, and permittivity of resistive layer 310 may be set based on the thickness of second dielectric layer 308. In an embodiment, the thicker second dielectric layer 308 is, the more appropriate it is to narrow the width of resistive layer 310 to maintain the impedance of the transmission line constant and equal to the DC resistance value thereof.

As an example, in order to obtain an impedance which remains substantially equal to 0.5 Ohms over a range of operating frequencies from D.C. up into the gigahertz range, the following example configuration (in a microstrip configuration) may be used. The low frequency part of the impedance (e.g., DC resistance) is driven by the resistivity of resistive layer 310. Assuming a square resistance (R_{square}) of 30 mOhms and a track width

(w) of 75 micrometers, a track length (L) of 1250 micrometers provides a resistive termination of 0.5 Ohms using the equation (1) below.

$$R = R_{\text{square}} * \frac{L}{w} \quad (1)$$

For the higher frequency or AC part of the impedance, microstrip transmission line design formulas (See e.g., *Transmission Line Design Handbook* by Brian C. Wadell, Artech House 1991) can be used to calculate the required transmission line parameters. In this example, with the parameters above for resistive layer 310 (i.e., square resistance, track length L, and track width w), a permittivity of about 3.9 and a thickness of about 0.2 micrometers for second dielectric layer 308 can be determined to result in a resistance termination of 0.5 Ohms in the Ghz range.

In another embodiment, to achieve a target resistance of 50 Ohms over a range of operating frequencies from D.C. up into the gigahertz range, a configuration may be obtained using the same approach described above. An example configuration may include a resistivity of 10 Ohms / square, a track length (L) of 5.5 micrometers, and a track width (w) of 0.5um for resistive layer 310 and a permittivity of about 3.9 and a thickness of 3 micrometers for second dielectric layer 308.

The skilled person will readily recognize that, in the above examples, the target value of DC resistance (0.5Ω or 50Ω, respectively) may be obtained using a resistive layer 310 having values of square resistance, track width (w) and track length (L) that are different from those used in the above examples but which still respect equation (1). In a case where the resistive layer 310 has different values of square resistance, track width (w) and track length (L) from the values given in the examples, the parameters of the transmission line (and, in particular, the properties of the second dielectric layer 308) may be adjusted, as required, using microstrip transmission line design formulas, to achieve the desired 0.5Ω or 50Ω impedance up to the Gigahertz range.

Figure 10 illustrates the frequency response performance of the resistive element of an example RC structure according to an embodiment.

The example RC structure provided a 5nF vertical capacitor and targeted a resistance of 0.5 Ohms for the resistive element over the frequency band extending from DC to 5 GHz. A microstrip transmission line configuration was used for the resistive element.

5 As shown by curve 1002 in FIG. 10, the resistive element according to the embodiment has a substantially constant resistance of about 0.5 Ohms over the entire target frequency range. Uniform performance for the device can thus be achieved over the operating frequency range.

10 In contrast, curve 1004 shows the performance of a resistor with uncontrolled impedance. The resistor with uncontrolled impedance is laid on top of a high ohmic substrate and is not dimensioned as a transmission line. As shown, the uncontrolled impedance starts to increase dramatically at around 10^8 Hz (100 MHz) and almost doubles in value at about 10^9 Hz (1 GHz). This results in uneven performance over the operating frequency range
15 for the device.

20 The foregoing description of the embodiments will so fully reveal the general nature of the disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt the embodiments for various applications, without undue experimentation, without departing from the general concept of the present disclosure. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

25 The breadth and scope of embodiments of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims.

CLAIMS:

1. A semiconductor device (300, 400), comprising:
a substrate (302);
5 a first dielectric layer (304, 402) disposed above the substrate (302);
a conductive layer (306) disposed above the first dielectric layer (304, 402);
a second dielectric layer (308) disposed above the conductive layer (306); and
10 a resistive layer (310) disposed above the second dielectric layer (308),
wherein the substrate (302), the first dielectric layer (304, 402) and the conductive layer (306) form a vertical capacitor,
wherein the second dielectric layer (308) and the resistive layer (310)
15 form a resistive element,
wherein a resistivity of the substrate (302) is configured such that the conductive layer (306) provides a reference ground above a predefined frequency, and
wherein the second dielectric layer (308) and the resistive layer (310)
20 are configured such that the resistive element is impedance matched, relative to the reference ground, to a predetermined resistance.
2. The semiconductor device (300, 400) of claim 1, wherein the resistivity of the substrate (302) is lower than or equal to 1 mOhms.cm.
25
3. The semiconductor device (300, 400) of any of claims 1 and 2, wherein the substrate (302) contains doped material.
4. The semiconductor device (300, 400) of any of claims 1 to 3,
30 wherein a thickness of the substrate (302) is lower or equal to 100 micrometers.

5. The semiconductor device (300, 400) of any of claims 1 to 4, wherein the first dielectric layer (304, 402) is planar or deposited into a trench etched into the substrate (302).

5 6. The semiconductor device (300, 400) of any of claims 1 to 5, wherein a thickness of the second dielectric layer (308) is between 0.2 and 0.3 micrometers.

7. The semiconductor device (300, 400) of any of claims 1 to 6,
10 wherein a sheet resistance of the resistive layer (310) is between 10 mOhms per square to 20 Ohms per square.

8. The semiconductor device (300, 400) of any of claims 1 to 7,
15 wherein the resistive layer (310) corresponds to a metallization layer made of alumina.

9. The semiconductor device (300, 400) of any of claims 1 to 7, wherein the resistive layer (310) is made of tantalum nitride.

20 10. The semiconductor device (300, 400) of any of claims 1-9, wherein the second dielectric layer (308) and the resistive layer (310) form a microstrip transmission line.

11. The semiconductor device (300, 400) of any of claims 1-9, and
25 comprising a first auxiliary ground plane (602) disposed to surround one or more sides of the resistive layer (310), thereby the second dielectric layer (308), first auxiliary ground plane and the resistive layer (310) form a coplanar transmission line.

30 12. The semiconductor device (300, 400) of any of claims 1-9, and further comprising a first auxiliary ground plane (802) disposed to surround

one or more sides of the resistive layer (310), and a second auxiliary ground plane (802) disposed above the resistive layer (310), thereby the second dielectric layer, (308), the first and second auxiliary ground planes (602,802) and the resistive layer (310) form a stripline transmission line.

5

13. The semiconductor device (300, 400) of any of claims 1-12, wherein the vertical capacitor provides a decoupling capacitor and the resistive element provides a broadband damping resistor.

10

14. The semiconductor device (300, 400) of any of claims 1-13, wherein the semiconductor device (300, 400) forms an envelope termination circuit of a radio frequency (RF) power transmitter.

15

15. A method for fabricating a semiconductor device, comprising:
providing a substrate (302);
forming a first dielectric layer (304, 402) above the substrate (302);
forming a conductive layer (306) above the first dielectric layer (304, 402);
forming a second dielectric layer (308) above the conductive layer (306); and
forming a resistive layer (310) above the second dielectric layer (308),
wherein the second dielectric layer (308) and the resistive layer (310) form a resistive element,

20

wherein providing the substrate (302) comprises configuring a resistivity of the substrate (302) such that the conductive layer (306) provides a reference ground above a predefined frequency, and

25

wherein forming the second dielectric layer (308) and the resistive layer (310) comprises configuring the second dielectric layer (308) and the resistive layer (310) such that the resistive element is impedance matched, relative to the reference ground, to a predetermined resistance.

30

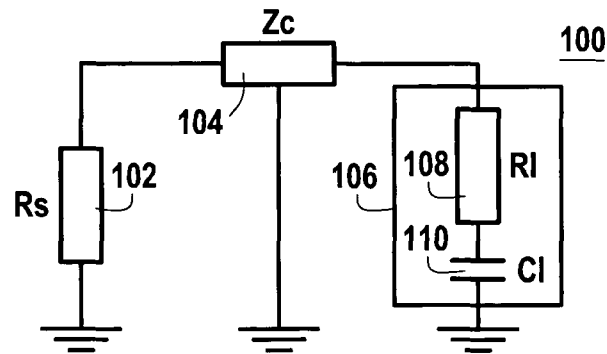


FIG.1

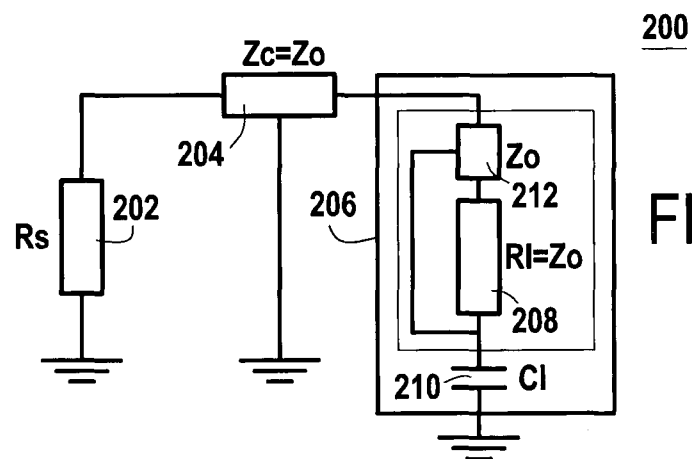


FIG.2

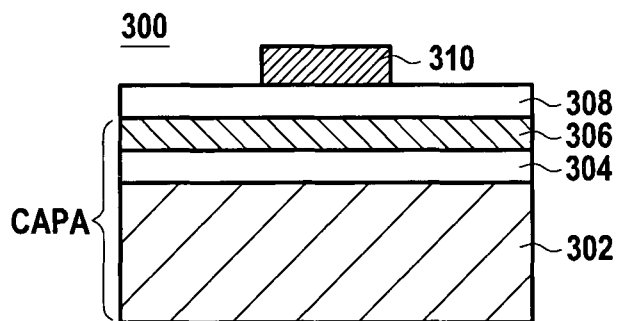


FIG.3

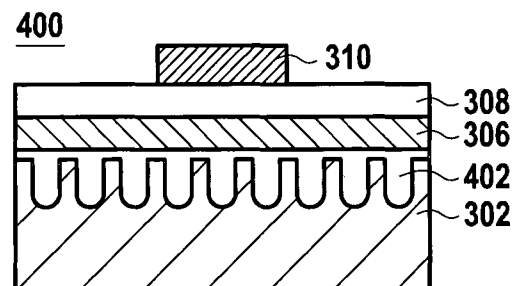


FIG.4

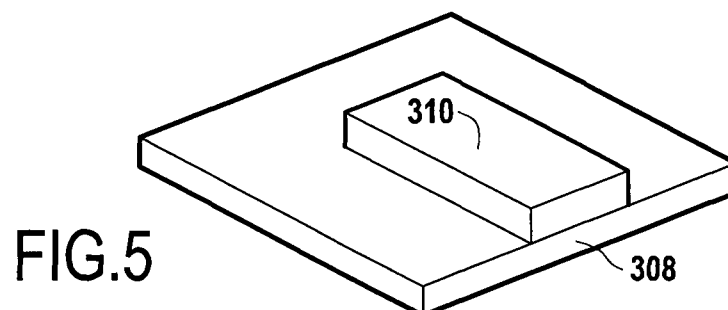


FIG.5

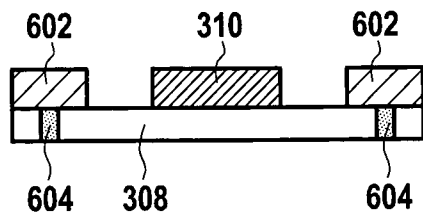


FIG. 6

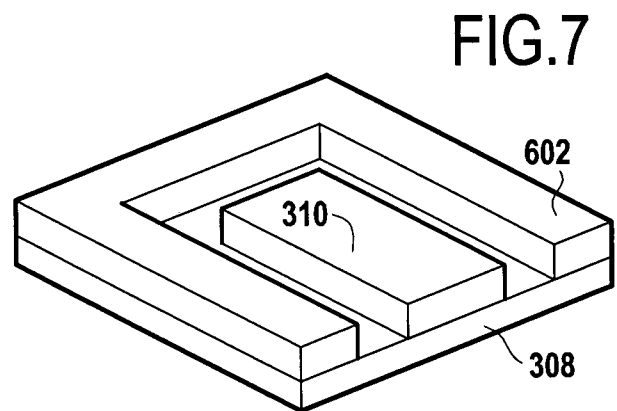


FIG. 7

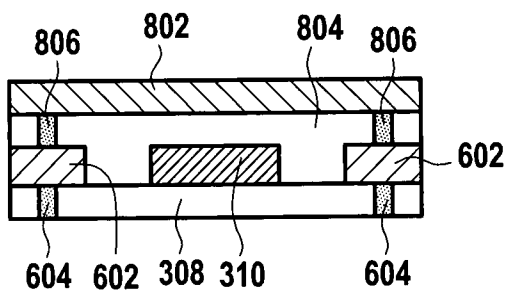


FIG. 8

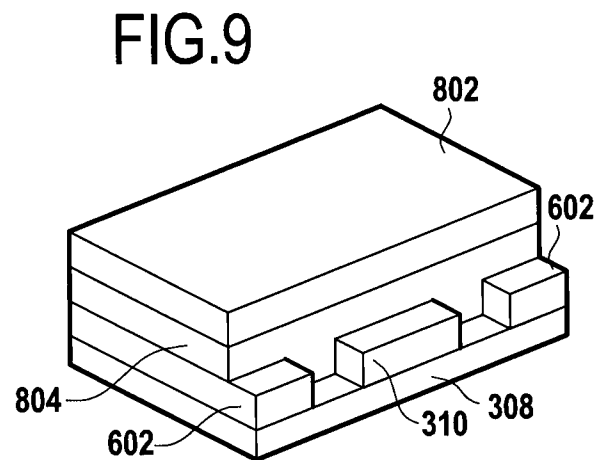


FIG. 9

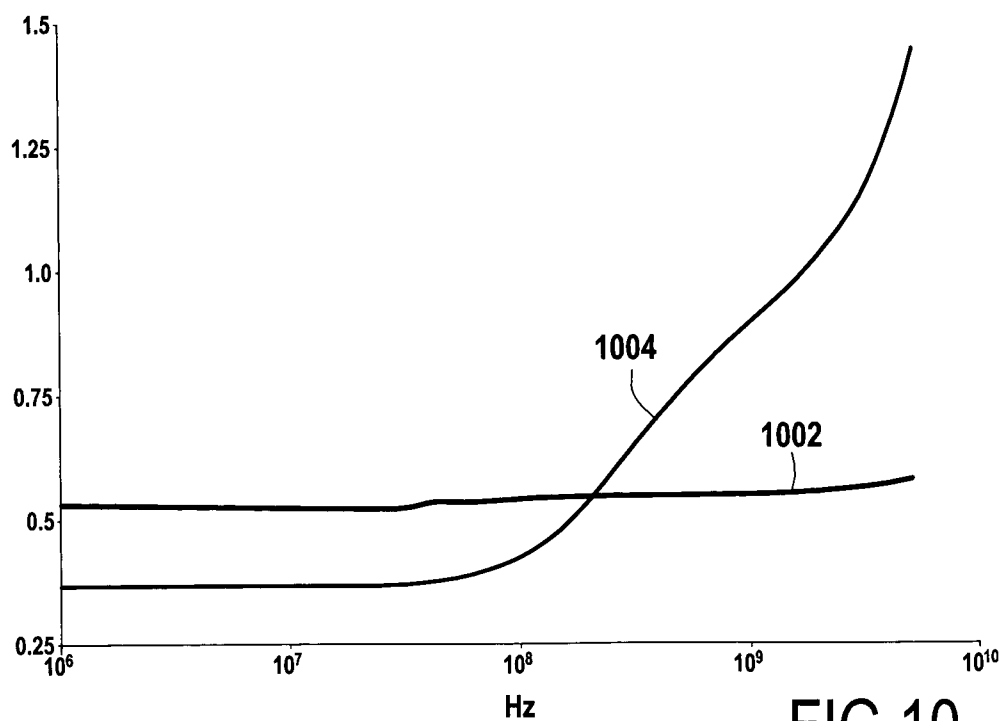


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2018/000742

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L29/66 H01L27/06 H01L27/07 H01L29/94 H01L49/02 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/197518 A1 (MAIORANA VITTORIO GIUSEPPE [IT] ET AL) 17 July 2014 (2014-07-17) paragraphs [0003] - [0005], [0013] - [0017]; figures 1,2 -----	1-15
X	EP 0 700 091 A2 (IBM CORP) 6 March 1996 (1996-03-06) abstract; figure 1 column 2, line 29 - column 3, line 53 -----	1-15
A	US 2002/020879 A1 (SHI IKI MIKA [JP] ET AL) 21 February 2002 (2002-02-21) figure 2 -----	6-9
T	US 4 821 007 A (FIELDS WALTER D [US] ET AL) 11 April 1989 (1989-04-11) column 6, line 1 - line 23; figure 1 -----	10-12
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 11 October 2018		Date of mailing of the international search report 17/10/2018
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Mosig, Karsten

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2018/000742

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014197518	A1	17-07-2014	NONE
EP 0700091	A2	06-03-1996	DE 69523525 D1 06-12-2001 EP 0700091 A2 06-03-1996 JP H08107186 A 23-04-1996 US 5541442 A 30-07-1996
US 2002020879	A1	21-02-2002	CN 1337745 A 27-02-2002 JP 2002124639 A 26-04-2002 KR 20020013451 A 20-02-2002 TW 516046 B 01-01-2003 US 2002020879 A1 21-02-2002
US 4821007	A	11-04-1989	NONE