PATENT SPECIFICATION (11) 1 598 146

(54) A METHOD AND AN APPARTUS FOR PLASMA TREATMENT OF SEMICONDUCTOR MATERIALS

(71) We, FUJITSU LIMITED, a Company organized and existing under the laws of Japan of 1015, Kamikodanaka, Naka-hara-ku, Kawasaki, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an apparatus for the plasma treatment of substrate materials such as semiconductor substrates or wafers. The plasma treatment includes chemical vapor deposition by means of plasma, for example, the deposition of insulating substances or semiconductor substances on the surfaces of the semiconductor materials, and plasma etching, for example, the etching of semiconductor materials or of the coatings formed on the semiconductor materials.

A proposal was made in the U.S. Patent No. 3837856, in which a first chamber containing semiconductor wafers is located at a predetermined distance from a second chamber which produces a plasma discharge, which second chamber being communicated with the first chamber through a connection path at an end of the second chamber. Reaction substances in the plasma produced by electrodeless radio frequency excitation in the second chamber are transmitted to the first chamber through the connection path. Semiconductor materials are treated by such reaction substances in the first chamber. However, according to this U.S. Patent, a uniform distribution of the plasma treatment cannot be realized either with regard to the surface of a semiconductor wafer or with regard to a series of semiconductor wafers, the speed of the plasma treatment cannot be increased because of the decrease in the effectiveness of the reaction substances and because of the loss of the reaction substances due to their being deposited on the walls of the first and the second chambers, and the speed of mass-producing the treated semiconductor materials is relatively low because of the limited number of semiconductor wafers which are treated simultaneously in the first chamber. Besides, if this U.S. Patent is used for carrying out chemical vapor deposition of semiconductor materials, vapor decomposition tends to take place, and the impurities produced by such decomposition are included in the deposit, which forms the coating on the semiconductor material, so that the quality of the coating becomes poor.

Another plasma treatment was proposed in U.S. Patent No. 3615956, in which semiconductor wafers are received into a number of parallel slots extending longitudinally in a boat arranged in a reaction tube. A pair of elongate semicircular plates is provided on the outer surface of the reaction tube. The surfaces of the semiconductor wafers are all arranged in parallel with the axis of the reaction tube. However, according to this U.S. Patent, the effects of the plasma treatment are not uniform with regard to the position of the semiconductor wafer in the reaction tube, the speed of the plasma treatment cannot be easily increased and the diameter of the cross-section of the reaction tube tends to become too large if the number of the rows of semiconductor wafers is increased.

Another proposed plasma treatment method is known to manufacturers of semiconductor devices in which a batch of semiconductor wafers is treated on a plate arranged in a bell-jar type treatment vessel, instead of being arranged in tubular treatment vessels which have horizontal axes, as disclosed in the above-mentioned U.S. patents. A group of semiconductor wafers (i.e., the first batch) is placed flat on the plate in the treatment vessel during the plasma treatment, then these wafers are replaced by another group of semiconductor wafers (i.e.

the next batch). However, the speed of mass-producing the treated semiconductor wafers cannot be easily increased because of the limited number of semiconductor wafers which can be included in a batch.

The present invention originated from attempts to solve the above-mentioned problems in the prior arts.

It is an object of the present invention to provide an improved plasma treatment apparatus.

According to the present invention, there is provided an apparatus for the plasma treatment of substrates in the manufacture of semiconductor components, comprising a reaction tube into which an ionisable reaction gas can be introduced, and into which a row of semiconductor substrates can be successively introduced, and two electrodes between which an electrical field can be produced by supplying to the electrodes direct current or high-frequency or low-frequency electric power, characterised in that the electrodes are disposed in the interior of the reaction tube, the electrodes comprising two electrode holders which support a row of electrode plates a plurality of which are arranged in series along the longitudinal axis of the reaction tube, the planes defined by the electrode plates being perpendicular to the said longitudinal axis of the reaction tube, and the electrode plates being electrically connected to the electrode holders such that for each pair of adjacent electrode plates one plate is connected to one electrode holder and the other plate is connected to the other electrode holder.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a plasma treatment apparatus for explaining the fundamental structure of the present invention,

Fig. 2 is a cross-sectional view taken along the line II–II of Fig. 1,

Figs. 3, 4, and 5 illustrate in detail the parts of the apparatus shown in Fig. 1, wherein Fig. 4 is a cross-sectional view taken along the line IV–IV of Fig. 3,

Fig. 6 shows the electrical circuitry for the apparatus shown in Fig. 1,

Figs. 7 and 8 show modified examples of the electrode plates for the apparatus shown in Fig. 1, which are used for carrying out the plasma etching, wherein Fig. 8 is a cross-sectional view taken along the line VIII–VIII of Fig. 7,

Figs. 9 and 10 show a modified structure of the connection between the electrode plate and the conductor rod shown in Fig. 1,

Fig. 11 shows the arrangement of electrode plates and semiconductor materials in the reaction tube for the embodiments of the present invention,

Figs. 12 to 15 show results of an embodiment for the chemical vapor deposition, and Figs. 16 to 19 show results of another embodiment for the plasma etching, according to the present invention.

Figs. 1 and 2 respectively show the fundamental structure of an apparatus used for plasma treatment of substrate materials, for example, semiconductor materials, according to the present invention. In a reaction tube 1 made of quartz glass, Pyrex (Registered Trade Mark) glass or the like, a number of electrode plates 2 are arranged in series along the axis of the reaction tube 1. The planes of the electrode plates 2 are parallel to each other and perpendicular to the axis of the reaction tube 1. Each of the electrode plates 2 is fixed on a pair of electrode supports 3, 4 arranged in the reaction tube 1. The reaction tube 1 has a circular cross-section. Each electrode plate has portions 2a, 2b located in the lower part thereof where the thickness of the electrode plate is increased, thus forming a V-shaped slot 2c (Fig. 4) which serves as a holder of the edge of a semiconductor material such as a silicon substrate or wafer.

Each of the electrode plates 2 is connected to either of the two terminals of a power source 6 through one of the supports 3 and 4. Thus, the series of electrode plates 2 shown in Fig. 1 function as the electrically connected parallel capacitors shown in Fig. 6.

In operation, the reaction tube 1 is evacuated and a reaction gas is introduced therein. By applying a DC (Direct Current) low-frequency or high-frequency electric power to the electrode plates 2, an electric field is created between adjacent electrode plates 2. Due to the effect of the established electric field, the reaction gas is thereby ionized and thus produces a plasma between the adjacent electrode plates 2.

Because the electric field is established uniformly between adjacent parallel electrode plates, the plasma is produced uniformly in the spaces between the electrode plates. Accordingly, the plasma treatment is effected uniformly on the semiconductor materials, such as on a silicon substrate or on wafers which are mounted on the electrode plates.

Prior to voltage application to the electrode plates, the reaction tube is evacuated and the reaction gas is introduced therein at a pressure of approximately 0.1 to 2 Torr. For the purpose of carrying out chemical vapor deposition, the reaction gas can consist of, for example, ammonia (NH_3), monosilane (SiH_4), nitrogen (N_2) or oxygen (O_2); while for the purpose of etching, the reaction gas can consist of, for example, carbon tetrafluoride (CF_4) or oxygen (O_2). If a high-frequency electric power is chosen as the type of electric power used for producing plasma, a considerably high frequency such as approx-

imately 13.56 MHz is usually selected. If heating of semiconductor materials is required during the plasma treatment, such heating is conducted by means of a heater 7 which surrounds the reaction tube 1 and is connected to the power source 8.

Figs. 3, 4 and Fig. 5 illustrate the electrode plate and the electrode supports in detail. An electrode plate 2 has V-shaped slots 2c at the edges of the portions 2a, 2b which securely hold the edge of a semiconductor material to be mounted on the electrode plate. The semiconductor materials 5 can be mounted on both surfaces of the electrode plate 2, because the slots 2c are formed on both surfaces of the electrode plate 2. The location of the portions 2a, 2b and the depth of the slots are selected so that the center of the mounted semiconductor material 5 can coincide with the center of the electrode plate 2. The electrode supports 3, 4 consist of insulating sheaths 3b, 4b made of, for example, quartz, and electrically conductive rods 3a, 4a which penetrate the sheaths 3b, 4b. The electrode plate has a pair of semicircular recesses, a large diameter recess 2e and a small diameter recess 2d. The electrode plate 2 and rods 3a, 4a are made of, for example, aluminum. In the electrode plates 2(A) and 2(C) shown in Fig. 5, the rod 3a fits into the recess 2d at a location where the rod 3a is not covered by the insulation sheath 3b, and the rod 4a fits into the recess 2e at a location where the rod 4a is covered by the insulation sheath 4b. The electrode plate 2 may be welded to the rod 3a at the location of the recess 2d. Thus, the electrode plates 2(A) and 2(C) are electrically connected to the rod 3a and mechanically supported by the rod 3a and the insulated support 4 having the insulation sheath 4b. In the adjacent electrode plate 2(B) shown in Fig. 5, the large recess 2e and the small recess 2d are reversely located compared with the electrode plates 2(A) and 2(C). Thus, the adjacent electrode plate 2(B) is electrically connected to the rod 4a and mechanically supported by the rod 4a and the insulated support 3 having the insulation sheath 3b.

As illustrated in Fig. 6, each of the electrode plates 2 is electrically connected to a power source 6 through either of the rods 3a and 4a, in such a manner that each of the adjacent electrode plates 2 is connected to the opposite terminals of the power source 6. The diameter and the level of the supports 3, 4 are selected so that the center of the electrode plates 2 supported by the supports 3, 4 can be positioned to coincide with the axis of the reaction tube 1.

Figs. 7 and 8 show a modified structure of the electrode plates which are used for carrying out the plasma etching according to the present invention. A porous or mesh electrode 11 is arranged on both sides of each of the electrode plates 2 at a predetermined distance from the surface of the electrode plate 2. The polarity and the potential of the electrode 11 are kept the same as those of the corresponding electrode plate 2 situated between a pair of the porous or mesh electrodes 11. The porous or mesh electrode 11 is made of, for example, aluminum. A plasma producing discharge is formed between adjacent porous or mesh electrodes 11 having opposite polarities. Since the active substances in the produced plasma react with the surfaces of the semiconductor material 5 mounted on the electrode plates 2 through the porosity or mesh 15 of the electrodes 11, undesirable sputtering of ions is suppressed and good results of plasma etching are obtained. In addition, the value of the applied plasma-producing voltage can be reduced because of the substantially reduced distance between the adjacent plasma-producing electrodes of opposite polarities due to the presence of the porous or mesh electrodes. The density of the reaction gas can be increased, and the uniformity of the plasma treatment can be enhanced.

Figs. 9 and 10 respectively show two examples of a modified structure for connecting electrode plates to electrode supports.

In Fig. 9, a projection of a member 3aa fixed to the rod 3a is fitted into a recess 2f formed on the edge of the electrode plate 2. Thus, the electrode plate 2 is electrically connected to the conductor rod 3a and mechanically supported by the conductor rod 3a and the insulated support 4 having the insulation sheath 4b.

In Fig. 10, a projection 2g is formed on a predetermined portion of the edge of the electrode plate 2. The projection 2g penetrates through a window 9 on the insulation sheath 3b and is electrically connected to the rod 3a. At another predetermined portion of the edge of the electrode plate 2, the electrode plate 2 is mechanically supported by a projection 4bb of the insulation sheath 4b.

In the structures for supporting electrode plates shown in Figs. 3, 8, 9 and 10, the insulation sheaths 3b and 4b have extended portions in the direction perpendicular to the axes of the rods 3a, 4a at the ends of the sheaths 3b and 4b, and the extended portions are jointed to each other to form a combined support structure (not shown in detail in these figures). By using the support structure, the following process of plasma treatment is performed. That is, at the outside of the reaction tube, electrode plates are fixed to the support structure; semiconductor materials to be plasma-treated are mounted on the electrode plates; and then the support structure carrying the electrode plates and semiconductor materials is inserted into a reaction tube to undergo plasma treatment.

Further, it is also possible to form addi-

tional extended portions of the insulation sheaths 3b, 4b in the downward direction to serve as legs of the electrode supports. According to this structure, the optimum horizontal position of the electrode plates relative to the reaction tube and hence the optimum horizontal position of the semiconductor materials to be treated relative to the reaction tube can be selected by varying the length of the legs.

Fig. 11 shows the arrangement of silicon semiconductor substrates 5–1 through 5–22 mounted on the electrode plates 2–1 through 2–12 in the reaction tube 1 used in the embodiments of the present invention. The reaction tube 1 is made of quartz glass and has an inner diameter of 115 mm. The electrode plate 2 is made of aluminum and has a diameter of 95 mm and a thickness of 3 mm, the thickness of the semiconductor material supporting portion being 5 mm. The silicon semiconductor material 5 has a diameter of 75 mm. The center of the silicon semiconductor material 5 is positioned to coincide with the axis of the reaction tube 1. The semiconductor material to be treated is mounted on the supporting portion of at least one side of the electrode plates. The electrode plates are supported by the electrode supports while the planes of the electrode plates are kept perpendicular to the axis of the electrode supports. The electrode supports carrying the electrode plates are inserted into and placed at a predetermined position in the reaction tube. In order to position the center of the electrode plate and the center of the semiconductor material so as to coincide with the axis of the reaction tube, the configuration of the supporting portion of the electrode plate and the level of the electrode support are predetermined. A high-frequency power source is connected to the conductive rods in the electrode supports.

In the apparatus shown in Fig. 11, twelve electrode plates are arranged in the reaction tube. The electrode plates 2–1 and 2–12 situated at both ends of a sequence of electrode plates carry the semiconductor materials to be treated only on the inside plane thereof, while the electrode plates 2–2 through 2–11 carry the materials on both planes thereof.

Five silicon semiconductor materials 5–3, 5–7, 5–11, 5–15 and 5–19 situated on the gas-exit side plane of the second, fourth, sixth, eighth and tenth electrode plates, respectively, are used as samples for measuring the effects of the plasma treatment.

An embodiment for obtaining a chemical vapor deposition will hereinafter be described with reference to Figs. 12 through 15. In this embodiment, the silicon nitride (Si₃N₄) coating is formed on the surface of the silicon semiconductor material. In order to verify the uniformity of the formed coating, the inventor of the present invention carried out a measurement of the thickness distribution of the formed coating in the cases of:

(a) varying the component ratio of the reaction gas;

(b) varying the pressure of the reaction gas;

(c) varying the high-frequency electrical power applied to the semiconductor material to be treated, and;

(d) varying the spacing of the adjacent semiconductor materials to be treated, respectively.

Figs. 12, 13 and 14 are graphs obtained from the results of the experiments for an embodiment of the present invention in the case where the present invention is used for carrying out chemical vapor deposition on semiconductor materials. In these figures, the abscissa represents the position of the treated semiconductor material in the reaction tube and the ordinate represents the growth rate expressed in Å/min of the silicon nitride (Si_3N_4) coating on the surface of the treated semiconductor material. The thickness of the coating at the center of the semiconductor material is plotted by a dot mark, while the thickness of the coating at the circumference of the circle which has a radius of 5 mm less than the radius of the semiconductor material is plotted by a cross mark. According to the arrangement in which the center of the electrode plate and the center of the semiconductor material are positioned to coincide with the axis of the reaction tube, the thickness of the formed coating is uniform along the circumference of the circle. In these experiments, the temperature of the semiconductor materials is kept around 350°C.

In Fig. 12, the parameter R represents the component (pressure) ratio between ammonia and monosilane $(R=NH_3/SiH_4)$. The value of R is selected as 25, 50 or 100, respectively. The pressure of the reaction gas is maintained at 1.3 Torr, the spacing between the adjacent semiconductor materials is 17 mm, and the high-frequency electrical power fed to each semiconductor material is 1 W.

As for the chemical vapor deposition performed according to the present invention, as shown in Fig. 12, the variance of the thickness of the formed coatings on the samples of the semiconductor materials which belong to the same lot is too small to be detected and the difference between the thickness of the coating formed at the middle portion and the thickness of the coating formed at the peripheral portions is less than 5%, which is considered substantially negligible.

During the experiment for Fig. 12, it was found that the refractive index (n) of the formed silicon nitride coating is 2.0 when the

component ratio (R) is selected from the range of 30 through 50. This value 2.0 is also the value of the refractive index of pure silicon nitride. Accordingly, the quality of the silicon nitride coating can be measured by using the refractive index.

In Fig. 13, the parameter P represents the pressure Torr of the reaction gas. The value of P is selected as 0.8, 1.3 or 1.8 Torr, respectively. The value of R is selected as 50, the spacing between the adjacent semiconductor materials is 17 mm, and the high-frequency electrical power fed to each semiconductor material is 1 W.

As shown in Fig. 13, the variance of the thicknesses of the formed coatings on the samples of the semiconductor materials which belong to the same lot is too small to be detected, and the difference between the thickness of the coating formed at the middle portion and the thickness of the coating formed at the peripheral portions is less than 5%.

In Fig. 14, the parameter E represents the high-frequency electrical power fed to semiconductor materials. The value of E is selected as 0.6, 1, 2, 3 or 4 W/wafer, respectively. The value of R is selected as 50, the spacing between the adjacent semiconductor materials is 17 mm, and the pressure of the reaction gas is 1.3 Torr.

As shown in Fig. 14, the variance of the thicknesses of the formed coatings on the samples of the semiconductor materials which belong to the same lot is undetectable when the range of the high-frequency electrical power is between 0.6 W/wafer and 2 W/wafer, and the difference between the thickness of the coating formed at the middle portion and the thickness of the coating formed at the peripheral portions is less than 5%. However, both the variance and the difference of the thicknesses tend to increase in the case where the value of the high-frequency electrical power reaches approximately 3 or 4 W/wafer and the rate of deposition of the coating on the semiconductor material becomes too low for practical use.

Fig. 15 illustrates the products of the experiments for testing the effects of using the apparatus of the present invention in the case where a chemical vapor deposition on semiconductor materials is carried out. In this experiment the spacing of the semiconductor materials to be treated is varied. The spacing must be 10 mm, 15 mm, 20 mm and 30 mm in order to obtain the products (a), (b), (c) and (d), respectively. The value of R is selected as 50, the pressure of the reaction gas is 1.3 Torr, and the high-frequency electrical power fed to each of the semiconductor materials of silicon is 1 W. The deposited coating 51 is silicon nitride. The five samples described hereinbefore with reference to Fig. 11 are used for obtaining the data of each of the products (a) through (d). In Fig. 15, the following features can be observed. With regard to the product (a), the formed silicon nitride coating 51 is thin at the middle portion of the product as the result of a low deposition rate, and thick at the peripheral portions of the product as the result of a high deposition rate. With regard to the product (b), the thickness of the formed silicon nitride coating is uniform on the entire surface of the semiconductor material. With regard to the product (c), the formed silicon nitride coating is thick at the middle portion of the product and thin at the peripheral portions of the product. With regard to the product (d), the formed silicon nitride coating is thicker at the middle portion of the product and thinner at peripheral portions of the product than in the case of the product (C).

In the foregoing experiments, the temperature of the semiconductor materials is kept around 350°C by means of heating. Such heating improves the quality of the formed coating, which quality can be measured in terms of the strength, uniformity and other characteristics of the formed coating. A temperature below 500°C does not produce any harmful effect on the uniformity of the thickness of the coating formed on the semiconductor material.

Relating to the foregoing description of the experiments, the inventor of the present invention has confirmed that the chemical vapor depositions of silicon dioxide, polycrystalline silicon, phosphosilicate glass, borosilicate glass, and the like can be carried out by selecting the reaction gas. According to an experiment conducted by the inventor of the present invention, a silicon dioxide coating of a uniform thickness can be obtained at a deposition rate which is similar to that of silicon nitride, by using the reaction gas of oxygen (O_2) and monosilane (SiH_4) and by selecting the component ratio of the reaction gas, the pressure of the reaction gas, the high-frequency electrical power and the spacing between the adjacent semiconductor materials in a way similar to that of the case of silicon nitride. According to another experiment conducted by the inventor of the present invention, good results were obtained in forming a polycrystalline silicon coating by the vapor decomposition of monosilane SiH_4), and in forming a phosphosilicate glass glass coating by vapor reaction of phosphine (PH_3), oxygen (O_2), and monosilane (SiH_4). Hence, it is expected that a good result can be obtained in forming borosilicate glass by the vapor reaction of diborane (B_2H_6), oxygen (O_2), and monosilane (SiH_4).

It is also expected that, instead of the insulation material coating, a metal coating can be obtained by using the reaction gas of

hydrides or halides, for example, $(C_2H_5)_3Al$ for obtaining the aluminum coating, MoF_6 for obtaining the molybdenum coating, and WF_6 for obtaining the tungsten coating. During formation of the metal coatings, the structure of Fig. 10 can be modified in order to prevent the influence of plasma on the supports 3 and 4 by, for example, increasing the length of the projection 2g of the electrode plate 2 and the length of the projection 4bb of the insulation sheath 4b.

Figs. 16 and 17 are graphs obtained from the results of the experiments for another embodiment of the present invention in the case where the present invention is used for carrying out the etching of silicon semiconductor substrates. In these figures, the abscissa represents the position of treated semiconductor material in the reaction tube and the ordinate represents the etching rate (Å/min) of silicon semiconductor material. The etched depth at the center of the seminconductor materials is plotted by dot marks, while the etched depth at 5 mm inside from the periphery of the semiconductor materials is plotted by cross marks. In this experiment, the etching gas consists of carbon tetrafluoride containing 5% (volume) oxygen, and the semiconductor materials are maintained at a temperature of 20°C during the treatment.

In Fig. 16, the parameter P represents the pressure of the reaction gas. The value of P is selected as 0.3, 0.6 or 0.9 Torr, respectively.

As shown in Fig. 16, the variance of the etched depths on the samples of the semiconductor materials which belong to the same lot is too small to be detected in the case where the pressure of the reaction gas is selected to be, for example, 0.6 Torr. Also, the difference between the etched depths on the samples of the semiconductor material at the middle portion and the etched depths at the peripheral portions is less than 3%, which differences is considered substantially negligible. In the case wherein the pressure of the reaction gas is selected to be 0.9 Torr, the variance is 10% and the difference is less than 3%. Thus, the percentage of the variance is larger than in the case wherein the pressure of the gas is selected to be 0.6 Torr. However, the plasma etching can be carried out for a practical use at a high etching rate in the case wherein the pressure of the reaction gas is selected to be 0.9 Torr.

In Fig. 17, the parameter E represents the high-frequency electrical power applied to semiconductor materials. The value of E is selected as 2.5, 5.0 and 7.5 W/wafer, respectively.

As shown in Fig. 17, the variance of the etched depths on the samples of the semiconductor materials which belong to the same lot is too small to be detected in the case where the high-frequency electrical power is selected within the range of from 2.5 W/wafer through 5 W/wafer. Also, the difference between the etched depths on the samples of the semiconductor material at the middle portion and at the peripheral portions is less than 3%. However, in the case in which the high-frequency electrical power is raised to 7.5 W/wafer, the variance of the etched depths among the samples tends to increase. In the case wherein the high-frequency electrical power is reduced below 2.5 W/wafer, the etching rate becomes too low for practical use.

Fig. 18 illustrates the products of the experiments used for testing the effects of the present invention in the case where apparatus of the present invention is used for carrying out the etching of the semiconductor materials. In this experiment, the spacing of the treated semiconductor materials is varied. To obtain the products (a), (b), (c), and (d), the spacings are 10 mm, 15 mm, 20 mm and 30 mm, respectively. The five samples described as hereinbefore with reference to Fig. 11 are used for obtaining data of each of the products (a) through (d). In these experiments, the pressure of the reaction gas is 0.6 Torr, and the high-frequency electrical power fed to each of the semiconductor materials is 5 W.

In Fig. 18, the following features can be observed. With regard to the product (a), the etched semiconductor material is thick at the middle portion, thus showing a small amount of etching and thin at the peripheral portions showing a large amount of etching. With regard to the product (b), the etched semiconductor material has a uniform thickness throughout the entire surface thereof. With regard to the product (c), the etched semiconductor material is thin at the middle portion and thick at the peripheral portions. With regard to the product (d), the etched semiconductor material is thinner at the middle portion and thicker at the peripheral portions, than in the case of the product (c).

The inventor of the present invention has confirmed by experiments that the etchings of the insulation coatings, for example, silicon dioxide coating, silicon nitride coating, polycrystalline coating, phosphosilicate glass, borosilicate glass, or photoresist material, and the etchings of metal coatings, for example, aluminum coating can be obtained according to the present invention. For the etchings of aluminum coatings, a reaction gas such as carbon tetrachloride can be used.

Fig. 19 is a graph obtained from the results of the experiment for testing the effects of the present invention in the case where the present invention is used for carrying out the etching of the semiconductor materials having no coatings or having a coating of silicon nitride or silicon dioxide. In Fig. 19, the abscissa represents the high-frequency elec-

trical power fed to the electrode plates W/wafer and the ordinate represents the etching rate Å/min of the semiconductor materials. In this experiment, the etching gas consists of carbon tetrafluoride containing 5% (volume) oxygen, the pressure of the gas is 0.6 Torr, and the spacing between adjacent semiconductor materials to be treated is 17 mm. In Fig. 19, the curves (a), (b) and (c) represent the etching rates of silicon dioxide coating, silicon nitride coating, and silicon semiconductor substrate, respectively. It was found during this experiment that the variance of the etched depths on the silicon nitride or silicon dioxide coating of the semiconductor materials which belong to the same lot was too small to be detected, and that the difference between the etched depths of the silicon nitride or silicon dioxide coating at the middle portion of the semiconductor material and the etched depths at the peripheral portions thereof was also too small to be detected.

WHAT WE CLAIM IS:—

1. An apparatus for the plasma treatment of substrates in the manufacture of semiconductor components, comprising a reaction tube into which an ionisable reaction gas can be introduced, and into which a row of semiconductor substrates can be successively introduced, and two electrodes between which an electrical field can be produced by supplying to the electrodes direct current or high-frequency or low-frequency electric power, characterised in that the electrodes are disposed in the interior of the reaction tube, the electrodes comprising two electrode holders which support a row of electrode plates a plurality of which are arranged in series along the longitudinal axis of the reaction tube, the planes defined by the electrode plates being perpendicular to the said longitudinal axis of the reaction tube, and the electrode plates being electrically connected to the electrode holders such that for each pair of adjacent electrode plates one plate is connected to one electrode holder and the other plate is connected to the other electrode holder.

2. An apparatus according to claim 1, characterised in that a respective porous or mesh auxiliary electrode is provide on each side of each of the electrode plates, the electrical potential of the auxiliary electrodes corresponding to the potential of the respective electrode plate.

3. An apparatus according to claim 1 or 2, characterised in that each electrode plate has openings at its periphery and each electrode holder comprises an insulating casing and a conductor bar which extends through the casing, either the casing or the conductor bar fitting into the opening at the periphery of the electrode plate and the conductor bar being electrically connected to the electrode plate.

4. An apparatus according to claim 1 or 2, characterised in that each electrode plate has an opening at its periphery and a portion of an element which extends from a conductor bar of the respective electrode holder fits into said opening.

5. An apparatus according to claim 1 or 2, characterised in that each electrode plate has a projection at its periphery, which projection extends through an opening in an insulating casing covering a conductor bar of the respective electrode holder and is electrically connected to the said conductor bar.

6. An apparatus according to claim 5, characterised in that at another position on its periphery each electrode plate has an opening into which fits a projection which projects from an insulating casing of the other electrode holder.

7. An apparatus for the plasma treatment of substrates in the manufacture of semiconductor substrates substantially as hereinbefore described with reference to the accompanying drawings.

MARKS & CLERK.

Fig. I

Fig. 2
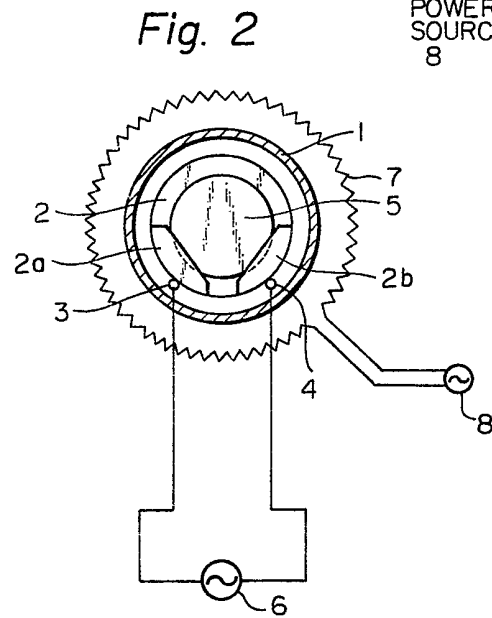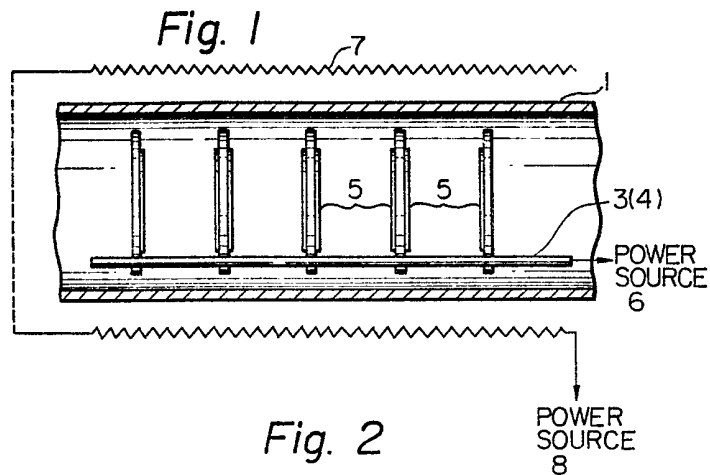
Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7
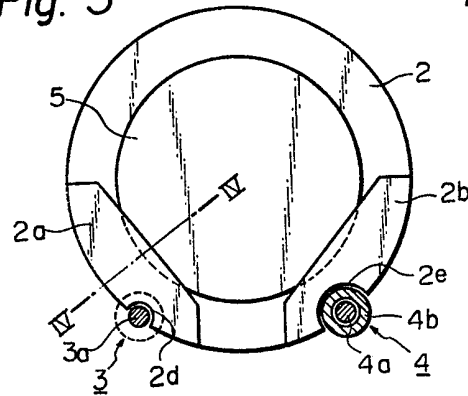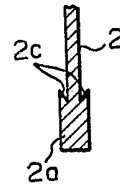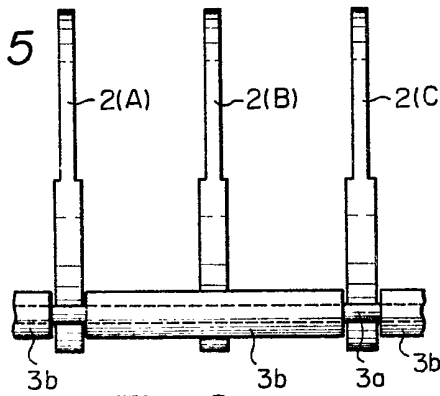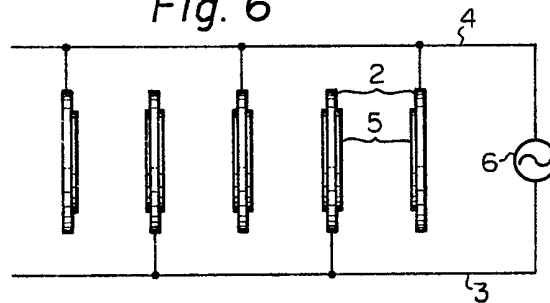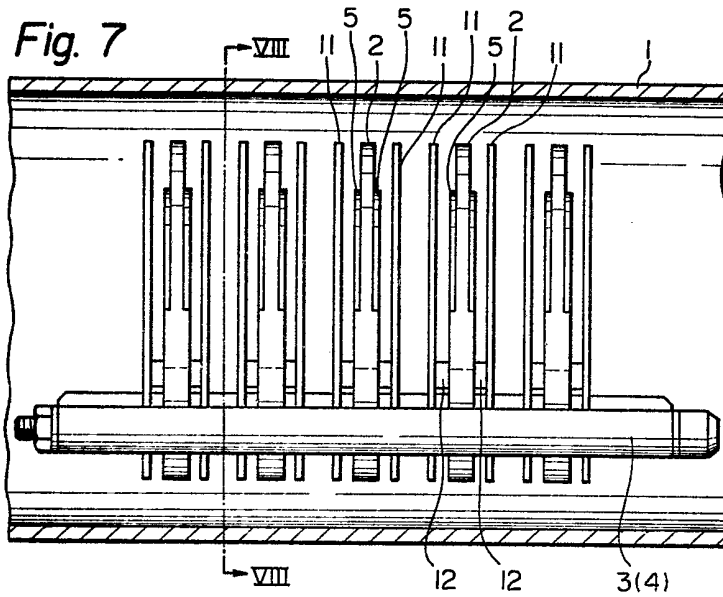
Fig. 8

Fig. 9

Fig. 10

Fig. 11

Fig. 12

$P=1.3$ (Torr)
$E=1$ (W/wafer)
$D=17$ (mm)

Fig. 13

Fig. 14

R=50
P=1.3 [Torr]
D=17 [mm]

E = 4 [W/wafer]
E = 3 [W/wafer]
E = 2 [W/wafer]
E = 1 [W/wafer]
E=0.6 [W/wafer]

GROWTH RATE [Å/min]

400
300
200
100

5-3   5-7   5-11   5-15   5-19

WAFER POSITION

Fig. 15

R=50
P=1.3 [Torr]
E=1 [W/wafer]

(a)   (b)   (c)   (d)

Fig. 16

E = 5 [W/wafer]
D=17 [mm]

P=0.9 [Torr]
P=0.6 [Torr]
P=0.3 [Torr]

ETCHING RATE [Å/min]

WAFER POSITION

5-3   5-7   5-11   5-15   5-19
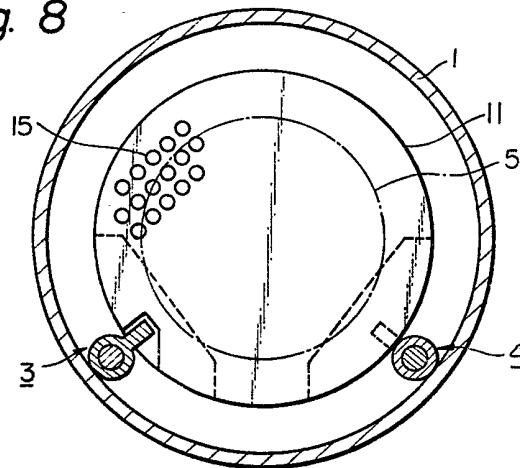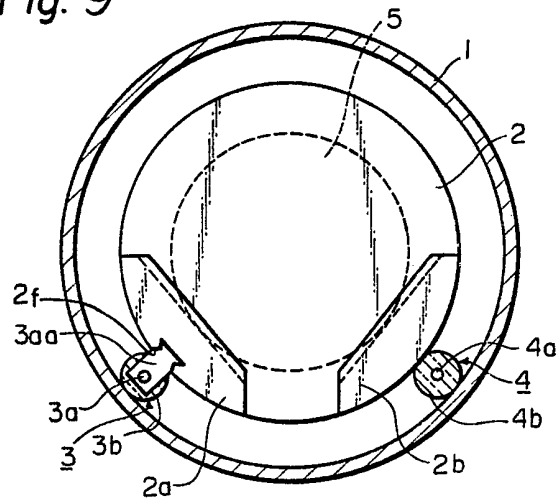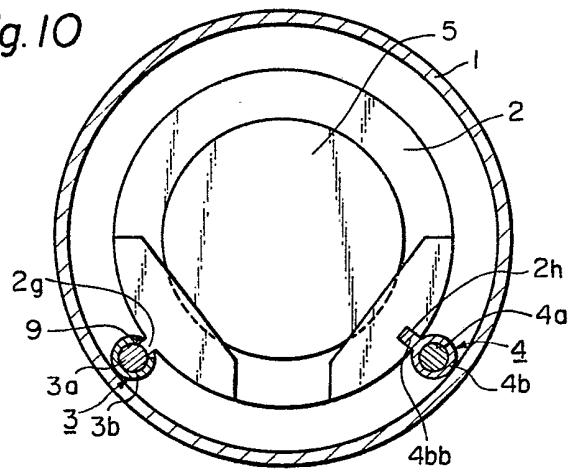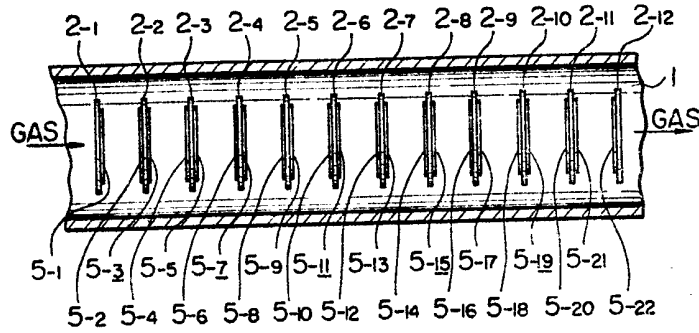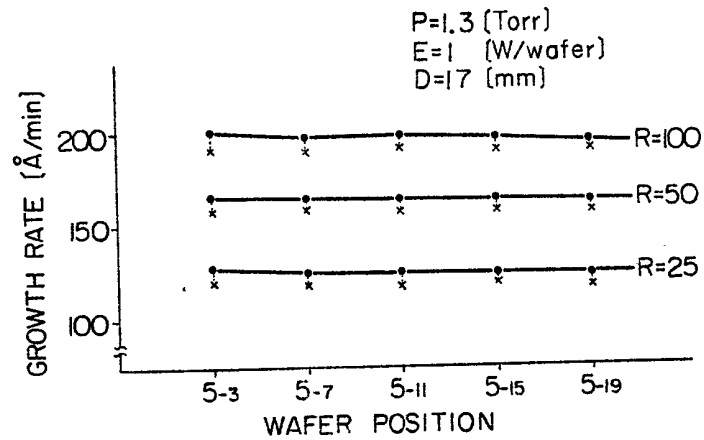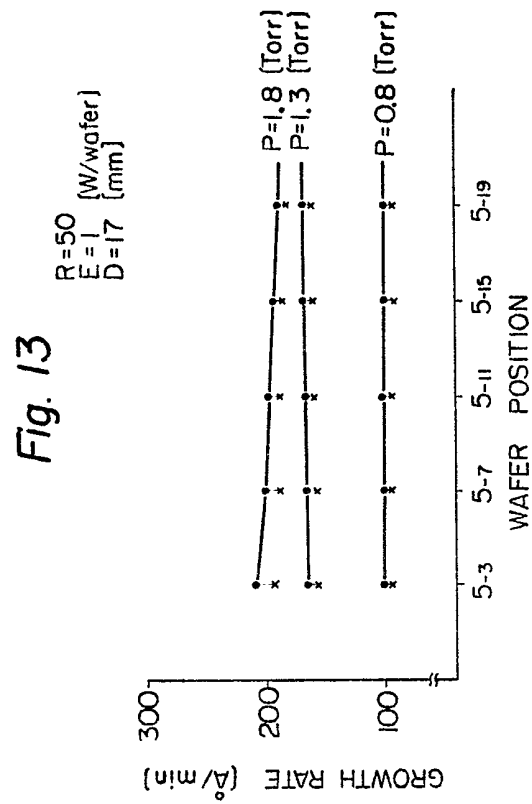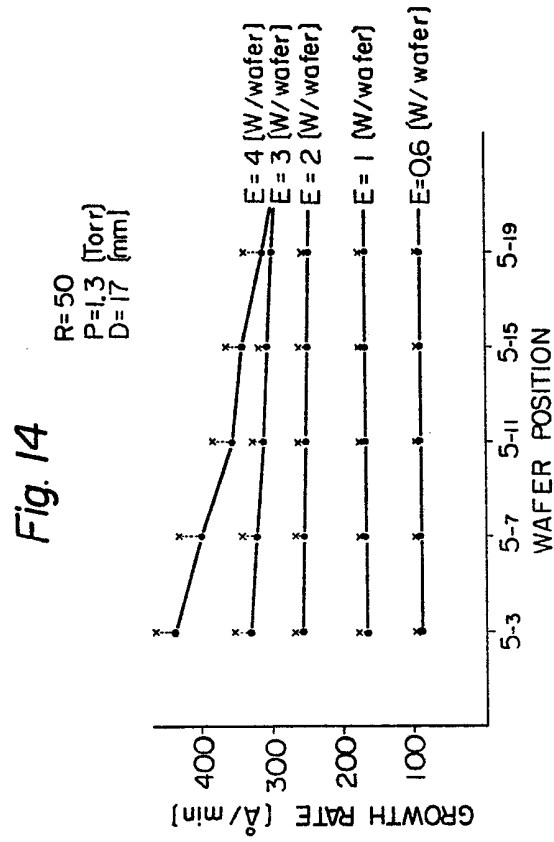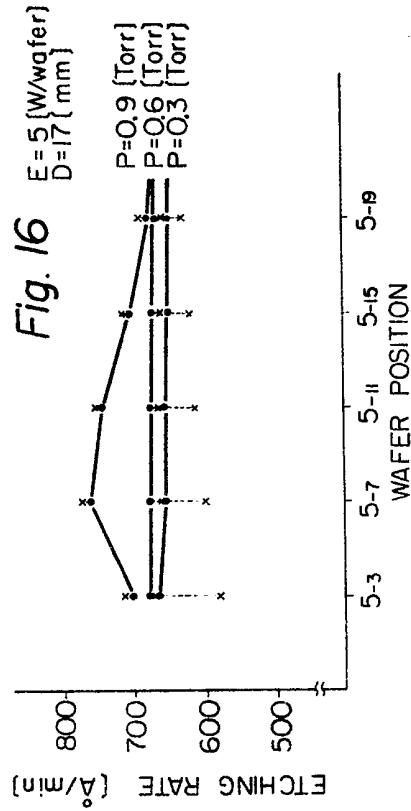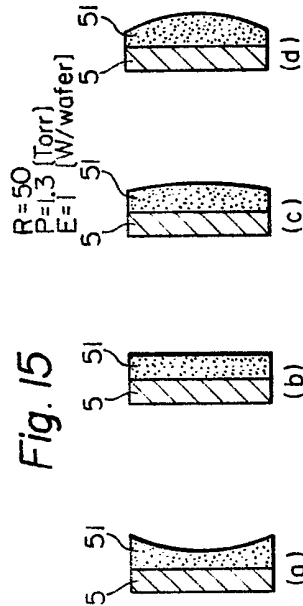
Fig. 17
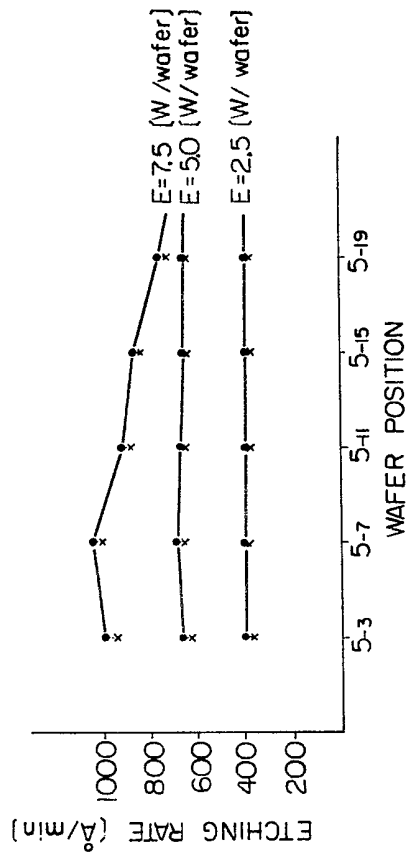
P = 0.6 [Torr]
D = 17 [mm]

Fig. 18   P=0.6 [Torr]
E= 5   [W/wafer]

(a)   (b)   (c)   (d)
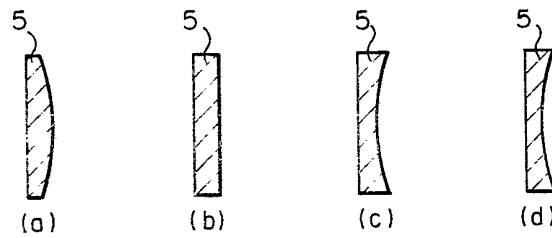
Fig. 19   P=0.6 [Torr]
D= 17 [mm]

(c)

(b)

(a)

HIGH FREQUENCY POWER [W/wafer]