(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 September 2001 (27.09.2001)

PCT

(10) International Publication Number
WO 01/71927 A2

(51) International Patent Classification[7]: H04B

(21) International Application Number: PCT/US01/09157

(22) International Filing Date: 21 March 2001 (21.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/190,803 21 March 2000 (21.03.2000) US

(71) Applicant: TELCORDIA TECHNOLOGIES, INC. [US/US]; 445 South Street, Morristown, NJ 07960-6438 (US).

(72) Inventors: LIBERTI, Joseph; 11 Spruce Hollow Drive, Howell, NJ 07731 (US). MOSHAVI, Shimon; Apartment G-4F, 550 Grand Street, New York, NY 10002 (US). ZABLOCKY, Paul, G.; 4 Buttonwood Drive, Shrewsbury, NJ 07702 (US).

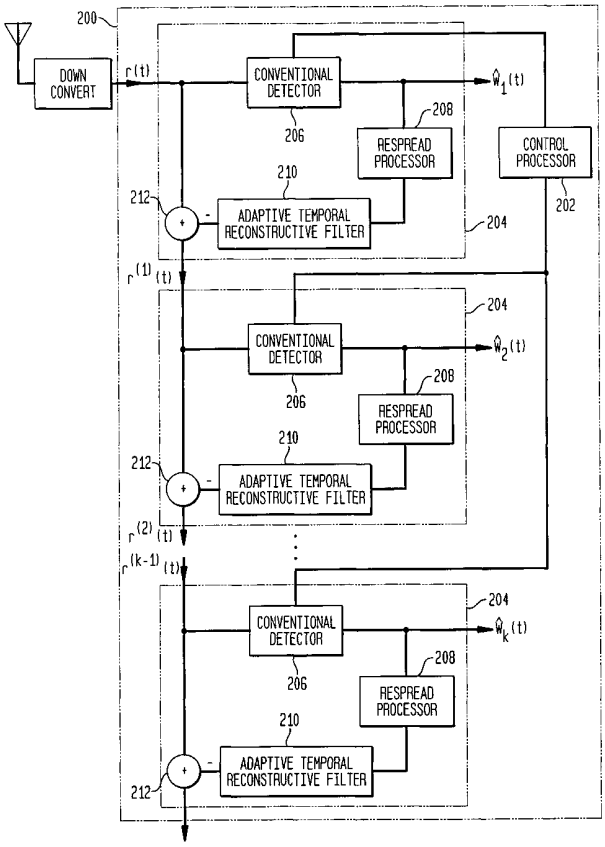
(74) Agents: HEY, David et al.; c/o International Coordinator, Telcordia Technologies, Inc., Room 1G112R, 445 South Street, Morristown, NJ 07960-6438 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,

[Continued on next page]

(54) Title: COMBINED ADAPTIVE SPATIO-TEMPORAL PROCESSING AND MULTI-USER DETECTION FOR CDMA WIRELESS SYSTEMS



(57) Abstract: Methods and systems in a wireless receiver for enabling the reception of input signals at varied power levels in the presence of co-channel interference utilizing combinations of space-time adaptive processing (STAP), interference cancellation multi-user detection (MUD), and combined STAP/MUD techniques. In MUD, code, timing, and possibly channel information of multiple users are jointly used to better detect each individual user. The novel combination of adaptive signal reconstruction techniques with interference cancellation MUD techniques provides accurate temporal cancellation of interference with minimal interference residuals. Additional methods and systems extend adaptive signal reconstruction techniques to take Doppler spread into account. STAP techniques permit a wireless receiver to exploit multiple antenna elements to form beams in the direction of the desired signal and nulls in the direction of the interfering signals. The combined STAP-MUD methods and systems increase the probability of successful user detection by taking advantage of the benefits of each reception method. An additional method and system utilizes STAP techniques in the case where no pilot signal is available. This method compares the outputs of various hypothesized STAP solutions.

WO 01/71927 A2

IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations*

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

COMBINED ADAPTIVE SPATIO-TEMPORAL PROCESSING AND MULTI-USER DETECTION FOR CDMA WIRELESS SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/190,803 filed March 21, 2000.

FIELD OF THE INVENTION

This invention relates to wireless communication networks and more specifically to CDMA wireless systems subject to co-channel interference.

BACKGROUND OF THE INVENTION

Code Division Multiple Access (CDMA) networks are widely deployed throughout the world. The current implementations of CDMA typically follow the IS-95 industry standards and are referred to as IS-95 wireless systems. With the advent of enhancements to CDMA technology such as third generation CDMA, CDMA2000 and W-CDMA, the deployment of CDMA is expected to increase dramatically.

A typical CDMA system 100 is shown in Figure 1. It is divided into a plurality of cells 121. Each cell contains a fixed base station 103. Each base station 103 is connected to a centralized switch or mobile switching center 109 that provides switching capabilities and acts as a gateway to wired networks such as the public switched telephone network (PSTN), the Internet, and other public and private data communications networks. As is known, the base station 103 includes a transmitter 105 and a receiver 107 for communicating with the mobile customers or users.

On the customer side, users connect to the wireless network through wireless mobile nodes 101 that can act as transmitters and receivers. The mobile nodes 101 communicate with the base stations 103 over wireless communications links. The link from a base station transmitter 105 to a mobile node receiver is the forward link 115 (or downlink). The link from the mobile node transmitter to a base station receiver 107 is referred to as the reverse link 113 (or uplink).

One advantage of CDMA over other wireless access systems is that all users share the same spectrum at the same time. However, the fact that multiple users occupy the same bandwidth limits performance and capacity. Because the conventional matched filter receiver 107 does an imperfect job of removing signals from these users, each user in a CDMA system degrades the performance of every other user; this effect is called multiple access interference or MAI. An increase in interference between users can lower the ability of a wireless provider to reuse frequencies, resulting in a reduction of system capacity. Because of the tremendous demand for wireless voice and data services and increased competition between service providers, CDMA network providers cannot afford such a reduction in system capacity. Therefore, wireless providers are continually striving to maximize system capacity, which in turn, requires limiting interference.

In CDMA wireless systems, power control is used to control the level of MAI at the base station. By adjusting every user's power so that all user transmissions arrive at the base station at approximately the same level, the base station receiver for each user sees the same amount of MAI, and the link quality is roughly the same for each user. If power control was not implemented, then a single user close to the base station could prevent the conventional CDMA receiver for other users from receiving a usable signal, resulting in the so-called near-far problem.

Power control works reasonably well for currently deployed CDMA wireless systems although limitations in the speed of power control are a constant engineering concern and limit capacity and link quality. However, there are frequently situations where it is desirable to deploy auxiliary receivers that are not the target of mobile station power control. Auxiliary receivers can be used to monitor the health of a CDMA wireless system or assist in geolocation. These auxiliary receivers may even be used by law enforcement and military operators for non-cooperative monitoring of a CDMA system for drug-interdiction, counter-terrorism and international intelligence gathering. In these cases, the auxiliary receiver must contend with a wide range of received power levels. Often the auxiliary receiver may need to receive a signal from a mobile station whose received power level is far below (30dB or more) below the strongest arriving signal.

A need therefore exists for enabling a user in a CDMA system to receive user signals in the presence of interference from other users when the power level of all co-channel signals is not adjusted to be substantially the same.

SUMMARY OF THE INVENTION

In accordance with an aspect of our invention, we combine concepts from space-time adaptive processing (STAP), interference cancellation, and multi-user detection (MUD) in multiple embodiments that are able to extract low-level CDMA signals in dense multi-user environments. The performance of these embodiments depends on the accuracy of the signal reconstruction and cancellation. This is particularly crucial if there is a wide range in received power (e.g., from lack of power control). For example, if there is an interfering signal that is 30 dB stronger than the signal we wish to receive and this signal is cancelled with 90% accuracy (meaning that 90% of the interfering signal power is canceled), then the residual portion is still 20 dB above the desired signal. Thus, in addition to symbol detection accuracy, channel estimation accuracy becomes very important in reducing the cancellation residuals.

Our invention utilizes adaptive temporal reconstruction filter (ATRF) techniques for reconstructing the signal interference. This novel approach permits very accurate channel estimation and signal cancellation. Through our novel use of ATRF, individual multipath components do not need to be tracked and separately estimated. The ATRF recreates the multipath channel structure with accurate amplitude and phase estimates for each component. The use of cost estimation techniques within the ATRF further minimizes cancellation residuals. In addition, cancellation timing errors are mitigated because the filter weights do not need to be exactly centered around the main multipath peak in order to solve for them accurately.

There has been extensive work on combined successive interference cancellation and multi-user detection systems. Much of this work is focused on simple channel estimation techniques, such as averaging the outputs of the conventional detector's correlators in order to estimate the amplitude and phase of signals to cancel. The reasons for this are that this approach is simple to describe, simulate and implement and the focus is most often on applications where power control is available to the receiver. Thus, small inaccuracies in cancellation do not significantly affect the performance. Also, there are only a limited number of multipath components which are strong enough to be worth tracking and canceling.

There has also been some work on channel estimation for MUD with the more theoretical motivation of determining the limits of estimation accuracy. These works

have often focused on complex maximum likelihood approaches. Because our invention applies successive interference cancellation to complex, non-discrete multipath channels encountered in the real world, our invention takes transmit filtering into account and compensates for timing errors. Our approach minimizes residuals and estimates all multipath components without the need to track them individually.

Through the addition of STAP, the receiver is able to spatially separate the signals using array (smart antenna) receiver technology. This allows the STAP receiver to place spatial beam pattern nulls on strong interferers. In addition, the STAP receiver combines multipath energy, including both the resolvable multipath that is captured by the rake receiver, as well as unresolved multipath that the rake receiver cannot effectively exploit. We combine these techniques with MUD approaches, where the receiver jointly operates on the received waveform to extract signals for all users simultaneously. By carefully estimating higher level signals and canceling them from the array data for the STAP receivers for lower-level signals, the combined STAP-MUD approach is much more effective than either approach implemented individually.

In multi-user detection (MUD), code, timing and possibly channel information associated with multiple users are jointly used to better detect each individual user. Thus, at the outputs of a conventional MUD detector, each user sees less multiple access interference and enjoys improved performance. One form of multi-user detection known as interference cancellation estimates, reconstructs and subtracts interfering signals out of the received signal. Unlike the traditional CDMA detectors, interference cancellation MUD utilizes information about other users when detecting a single user. One aspect of our invention is the novel combination of these interference cancellation MUD techniques and adaptive minimum cost channel estimation in the reconstruction of signals. This combination improves performance of signal reconstruction including symbol detection accuracy and channel estimation fidelity.

Using this combination, we have demonstrated that the STAP-MUD receiver can operate independently of power control, extracting waveforms that are over 35 dB below the strongest arriving CDMA signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a network diagram illustrating a typical wireless CDMA network.

Fig. 2 is a network diagram of an illustrative embodiment of a SIC-MCCE combination system in accordance with our invention.

Fig. 3 depicts an illustrative conventional detector for the combination of Fig. 2.

Fig. 4 depicts an illustrative respread processor for the combination of Fig. 2.

Fig. 5 depicts an illustrative adaptive temporal filter (ATRF) for the combination of Fig. 2.

Fig. 6 is a flow diagram illustrating a method of operation for the SIC-MCCE combination system of Fig. 2.

Fig. 7 is a network diagram of an illustrative embodiment of a SIC-JMCCE combination system in accordance with our invention.

Fig. 8 is a network diagram of an illustrative embodiment of a SIC-MF-MCCE combination system in accordance with our invention.

Fig. 8a is a flow diagram illustrating a method of operation for the SIC-MF-MCCE combination system of Fig. 8.

Fig. 9 is a network diagram of an illustrative embodiment of a PIC-MCCE combination system in accordance with our invention.

Fig. 10 is a flow diagram illustrating a method of operation for the PIC-MCCE combination of Fig. 9.

Fig. 11a is a partial network diagram of an illustrative embodiment of a PIC-JMCCE combination system comprising an ATRF in each parallel processor in accordance with our invention.

Fig. 11b is a partial network diagram of an illustrative embodiment of a PIC-JMCCE combination system comprising a single ATRF processor in accordance with our invention.

Fig. 12 is a network diagram of an illustrative embodiment of a STAP receiver in accordance with our invention.

Fig. 13 is a network diagram of an illustrative embodiment of a stage in a STAP/VSIC-MCCE combination system in accordance with our invention.

Fig. 14 is a network diagram of an illustrative embodiment of a J-STAPSIC combination system in accordance with our invention.

Fig. 15 depicts an illustrative J-STAPSIC stage for the combination of Fig. 14.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

I. Interference Cancellation MUD Combined with Adaptive Temporal Channel Estimation

Interference cancellation can take the form of either successive interference cancellation or parallel interference cancellation. Figure 2 depicts one illustrative embodiment of our invention comprising a system 200 combining successive interference cancellation (SIC) and adaptive minimum cost channel estimation (MCCE) for enabling a CDMA receiver to receive signals at different power levels in the presence of interference from other users. We shall refer to this combination as the SIC-MCCE system. The SIC-MCCE system 200 can be implemented as a component within an auxiliary CDMA receiver or within a CDMA base station receiver system.

The illustrative system of Figure 2 comprises a control processor 202 and a plurality of processors 204 combining successive interference cancellation (SIC) multi-user detection and adaptive temporal reconstruction filters (ATRF). The plurality of SIC-ATRF processors 204 are arranged in successive stages. At each stage, the next user is decisioned, respread, temporally reconstructed, and subtracted out by the SIC-ATRF processor associated with that stage. The output of the SIC-ATRF processor in the first stage, a cleaned received signal, is used as the input to the SIC-ATRF processor in the second stage and the output of the processor in the second stage is used as input to the processor in the next stage. This arrangement is continued for each stage. The number of stages used by the SIC-MCCE system is determined based on the total number of users for the system.

Each SIC-ATRF processor 204 includes a conventional detector 206, a respread processor 208, an adaptive temporal reconstruction filter (ATRF) 210, and a complex mathematical processor 212. The conventional detector 210 is connected to the respread processor 208 and the mathematical operations processor 212 of the SIC-ATRF processor in the previous stage. For the SIC-ATRF processor 204 in the first stage, the conventional detector 210 is connected to an external entity providing a processed version of the received signal r(t) and to the respread processor 208. The respread processor 208 is in turn connected to the ATRF 210, which is connected to the mathematical operations processor 212. The output of the mathematical operations processor 212 is connected to the conventional detector 208 of the SIC-ATRF processor of the next stage and the

mathematical operations processor 212 of the next stage. For the SIC-ATRF processor 204 in the first stage, the mathematical operations processor 212 is connected to the external entity providing a processed version of the received signal r(t) instead of the mathematical operations processor 212 of a previous stage.

The exact format of the conventional detector and respread processor will differ based on the modulation, coding, and spreading schemes of the particular CDMA system utilized in the wireless receiver system. Although the conventional detector and respread processor can be designed based on third generation CDMA, CDMA2000, or W-CDMA technology, figures 3 and 4 are block diagrams of the conventional detector 206 and respread processor 208 of the embodiment of Figure 2 according to an illustrative IS-95 implementation. In this implementation, the conventional detector can be an IS-95 conventional detector or an IS-95 rake conventional detector.

The IS-95 conventional detector 206, shown in Figure 3, is a fundamental component of standard IS-95 receivers. The IS-95 conventional detector 206 comprises three parts: a short code despreader 31, a long code despreader 32, and a 64-ary matched filter bank 33. The short code despreader 31 separately multiplies the received signal by the real and imaginary components of the IS-95 short code, denoted by $p_i(t)$ and $p_q(t)$. The delays of these components are adjusted to match the offset in time of the intended received signal. Next, the resulting despread signals are recombined, using time delays as illustrated in figure 3, and multiplied by a local copy of the long code, $p_l(t)$ corresponding to the desired user in the long code despreader 32. The long code is also offset according to the expected delay of the arriving signal. The resulting signal is used as input to a 64-ary matched filter bank 33. The 64-ary matched filter bank 33 contains copies of each of the 64 possible Walsh symbols that could be transmitted during a symbol period. The 64 outputs of the matched filter bank contain the squares of the absolute values of the inner products between the signal at the matched filter bank input and each of these 64 potential symbols. This process may be equally accomplished using a Walsh-Hadamard transform. When the IS-95 conventional detector is used alone, the matched filter bank output with the largest value determines the receiver's estimate of the transmitted symbol during a particular symbol period.

The IS-95 conventional rake detector, a standard technique employed in practice, embodies several instantiations of the IS-95 conventional detector. Each

detector uses the same long and short code, however a different delay is applied to each constituent IS-95 conventional detection. The delays correspond to different multipath components, so that a different IS-95 conventional detector tracks each significant multipath component. The outputs from the 64-ary matched filter banks of each of the IS-95 conventional detectors are combined in the IS-95 rake conventional detector using a non-coherent combining technique. Several non-coherent combining techniques are available; however, a simple example is the equal –gain combiner, in which the power from the corresponding ports from each of the 64 matched filter bank outputs in the constituent IS-95 conventional detectors are added, resulting in 64 new variables. These variables are compared, and the one with the largest power is selected as the receiver's estimate of the transmitted symbol from a 64-ary alphabet.

The respread processor 208, shown in Figure 4, is used as a fundamental component of IS-95 receivers employing interference cancellation. The respread processor 208 uses as inputs the symbol decisions obtained from either the IS-95 conventional detector, the IS-95 conventional rake detector, or the IS-95 STAP detector, or other similar sources. The respread processor creates a symbol from the 64-ary alphabet corresponding to the selected symbol. Next the symbol is spread using the IS-95 long code, $p_l(t)$, then the result is spread using the complex short code using the offset quadrature method specified in the IS-95 standard. The respread processor then matches the resulting signal to the signal received from the antenna using minimum mean square error techniques.

Figure 5 is a block diagram of the ATRF 210 of the embodiment of Figure 2. The ATRF 210 comprises tap weights 62, a tap delay line 61, and a mathematical summing circuit 63. In addition, the ATRF has an MCCE weight update processor 64. This processor may be located within the ATRF or as a separate entity between the mathematical operations processor 212 and the ATRF 210 as shown in Figure 6. The tap weights contain the amplitude, phase, and multipath structure of the received signal for the *k*th user. The length of the ATRF should be at least as long as the transmit filter (e.g., for IS-95 the transmit filter is 12 chips in duration), and ideally should be long enough to accommodate the delay spread of the signal (to recreate all multipath components).

Figure 6 shows a flow diagram of the operation of the system 200 of our invention. After initial processing such as downconversion to baseband is performed on the received signal by an external entity, the control processor 202

orders the user signals according to a pre-defined methodology (step 605). The user signals are then assigned to a stage based on the ordering. For example, the signal for user A is assigned to the first stage; the signal for user B is assigned to the second stage; and the signal for user k is assigned to the k^{th} stage.

An illustrative methodology ranks signals in descending order of received powers. An advantage of this methodology is that by canceling the strongest users first, the remaining users receive the largest benefit from MAI reduction. In alternative methodology, the control processor identifies signals above a certain threshold without performing a hard ranking of each signal.

Based on the ordering, the control processor 202 communicates a separate user code to the conventional detector 206 in each stage of the system (step 610). For example, the first stage receives the user code associated with user A. In the first stage of the system 200, the conventional detector 206 despreads the received signal and estimates the symbol transmitted for the identified user, $\hat{W}_1(t)$ (step 620). The technique used in the IS-95 conventional detector and IS-95 rake conventional detector is discussed above.

In step 630, the symbol estimate generated by the conventional detector 206 is mixed with the user codes in the respread processor 208 to generate a scaled estimate of the transmitted signal for the user. Using the scaled estimate as input, the ATRF 210 estimates the channel for the user, (i.e., the multipath components and their associated amplitudes and phases) and reconstructs the signal interference associated with the user signal (step 640). The reconstructed signal for the user is then cancelled from the total received signal r(t) in the mathematical operations processor 212 (step 650). The output of the mathematical operations processor 212 is then input to the SIC-ATRF processor 203 in the next stage of SIC-MCCE system 200. The output is also fed back to the MCCE weight update processor 64. Steps 620 through 650 are successively repeated for each of the k stages.

A more detailed description of the basic SIC-MCCE channel estimation and reconstruction performed in the ATRF 210 is described below. In a preferred embodiment, the adaptive technique used for channel estimation is based on minimum cost estimation techniques.

In basic SIC-MCCE channel estimation (step 640 in Figure 6), the MCCE weight update processor 64 determines the adaptive filter tap weights 62 that minimize a pre-determined cost function between the received signal and the output of the

adaptive filter. In an illustrative mode of operation, the MCCE weight update processor functions as follows. The output of the jth stage is given by:

$$r^{(j)}(lT_s) = r(lT_s) - \sum_{k=0}^{j-1}\sum_{n=0}^{N-1} w_{k,n}\hat{s}_k((l-n)T_s)$$

this is expressed in vector form as:

$$\mathbf{r}_l^{(j)} = \mathbf{r}_l - \mathbf{w}^H\mathbf{B}_l^H$$

where $\mathbf{r}_l$ is the vector of received signals at time index l, and samples of the reconstructed waveform are contained in the vector:

$$\hat{\mathbf{s}}_{k,n} = [\hat{s}_k(nT_s) \quad \hat{s}_k((n+1)T_s) \quad \ldots \quad \hat{s}_k((n+Q-1)T_s)]$$

$$\hat{\mathbf{S}}_{k,l} = \begin{bmatrix} \hat{\mathbf{s}}_{k,l} \\ \hat{\mathbf{s}}_{k,l-1} \\ \vdots \\ \hat{\mathbf{s}}_{k,l-N+1} \end{bmatrix} \qquad \mathbf{B}_l^H = \begin{bmatrix} \hat{\mathbf{S}}_{0,l} \\ \vdots \\ \hat{\mathbf{S}}_{j-1,l} \end{bmatrix}$$

Different weight vectors can be obtained by using minimizing different cost functions, each of which represents the quality of the performance of the SIC stage in some manner. One implementation of the minimum cost channel estimate solution is the minimum mean square error solution. The minimum mean square error solution for the weight vector w is the solution that minimizes the following cost function:

$$J(\mathbf{w}) = \left|\mathbf{r}_l^{(j)}\right|^2 = \left|\mathbf{r}_l - \mathbf{w}^H\mathbf{B}_l^H\right|^2$$

which simultaneously minimizes both the residual at the output of the j^{th} stage of the SIC receiver and the difference between the ATRF filter output and the received data r_l. The solution to this problem is obtained using standard techniques, where we obtain:

$$\mathbf{w} = \left(\mathbf{B}_l^H\mathbf{B}_l\right)\mathbf{B}_l^H\mathbf{r}_l^H$$

Since this solution minimizes the mean square error between the ATRF filter output and the received data at this input to the stage, this is called the minimum mean square error (MMSE) solution. In an alternate illustrative embodiment of our invention, the channel is estimated jointly over multiple users. We will refer to this combination of a jointly optimized ATRF and SIC multi-user detection as the SIC-JMCCE system. An illustrative multi-stage SIC-JMCCE system is shown in Figure 7. The SIC-JMCCE system 700 comprises a similar structure as the SIC-MCCE

system. However, in the SIC-JMCCE system 700, the outputs of the respread processors 208 for all previous stages are communicated as inputs to the ATRF filter 710 of the current stage. For example, the SIC-ATRF processor in the third stage of a SIC-JMCCE system uses the output of the first stage respread processor and the second stage respread processor as inputs to the third stage ATRF.

The mode of operation in accordance with the SIC-JMCCE system is as described above for the SIC-MCCE system, Figure 6. However, the channel estimation step 640 is modified to estimate the channel over multiple users. During channel estimation, the tap weights 62 of the current stage ATRF 710 are determined by jointly minimizing the cost function between the received signal and the sum of the outputs of the ATRFs 710 of previously completed stages. The ATRF 710 for each stage jointly estimates and reconstructs all of the currently detected signals including those detected in previous stages of SIC-JMCCE. Thus, the symbols of a single user are detected in each stage (step 620), but the temporal signal structures of all previous detected users are re-estimated and cancelled at each stage. At step 650, the output of the current stage ATRF 710 consisting of all the currently detected signals is subtracted from the received signal in the mathematical operations processor 212.

The above approaches to channel estimation in accordance with our invention reconstruct the temporal structure of the signals. However, these approaches do not take into account the frequency content of the signals. In another illustrative embodiment, the ATRF is extended to take into account Doppler spread. We refer to this combination of SIC multi-user detection and multiple frequency adaptive reconstruction as a SIC-MF-MCCE system. The MF-MCCE ATRF can be implemented either in an independent or joint arrangement. An independent MF-MCCE ATRF is shown in Figure 8. In this arrangement, a frequency shift processor 814 is connected between the respread processor 208 and the ATRF 810 in each stage of the system.

The mode of operation in accordance with the independent SIC-MF-MCCE system is shown in Figure 8a. In this mode, steps 605 through 630 are identical to those described for the SIC-MCCE and SIC-JMCCE systems. However, an additional step (step 835) is added to shift the frequency of the signal output from the respread processor to take into account Doppler spread and un-compensated frequency tracking errors. The output of the frequency shift processor 814 is then used as input to the MCCE weight update processor 64. At step 840, the ATRF

810 estimates the channel using either the basic or joint technique previously discussed. The following is a more detailed description of the operation of the MF-MCCE ATRF in accordance with a preferred embodiment of our invention. $\hat{s}_{k,p,n}$ represents a row vector containing Q samples of the reconstructed signal for user k, from time nT_s to $(n+Q-1)T_s$, and frequency shifted by $(p-P/2)/(QT_s)$ Hz:

$$\hat{s}_{k,p,n} = \left[\hat{s}_k(nT_s)e^{j2\pi\left(p-\frac{P}{2}\right)(n)/Q} \hat{s}((n+1)T_s)e^{j2\pi\left(p-\frac{P}{2}\right)(n+1)/Q} \ldots \hat{s}((n+Q-1)T_s)e^{j2\pi\left(p-\frac{P}{2}\right)(n+Q-1)/Q} \right]$$

$\mathbf{r}_l$ represents a row vector containing the Q samples of the received signal, $r(nT_s)$ through $r((n+Q-1)T_s)$. Then at stage j, the cleaned signal is:

$$\mathbf{r}_l^{(j)} = \mathbf{r}_l - \mathbf{w}^H \mathbf{B}_l$$

where

$$\mathbf{B}_l = \begin{bmatrix} \mathbf{A}_{0,l} \\ \vdots \\ \mathbf{A}_{j-1,l} \end{bmatrix}, \mathbf{A}_{k,l} = \begin{bmatrix} \hat{\mathbf{S}}_{k,0,l} \\ \vdots \\ \hat{\mathbf{S}}_{k,P-1,l} \end{bmatrix}, \hat{\mathbf{S}}_{k,p,l} = \begin{bmatrix} \hat{\mathbf{s}}_{k,p,l+N/2} \\ \hat{\mathbf{s}}_{k,p,l+N/2-1} \\ \vdots \\ \hat{\mathbf{s}}_{k,p,l+N/2}+1 \end{bmatrix}$$

Using these equations, the MF-MCCE ATRF 810 determines the filter tap weight vector that minimizes the cost function set for the ATRF. For example, where a minimum mean square error cost function is used, the ATRF 810 determines the weight vector according to the following equations.

$$J(\mathbf{w}) = \left\| \mathbf{r}_l - \mathbf{w}^H \mathbf{B}_l \right\|^2$$

which gives:

$$\mathbf{w} = (\mathbf{B}_l \mathbf{B}_l^H)^{-1} \mathbf{B}_l \mathbf{r}_l^H$$

The MF-MCCE ATRF 810 applies this weight vector to the delayed and frequency shifted version of the signal received from the previous stage (or the antenna input if this is the first stage).

The SIC detection approach is particularly attractive where there is a wide range in received powers (e.g., due to lack of power control). The SIC approach exploits the power distribution by canceling based on signal strength ordering. For applications where signals are received at about the same power (e.g., through power control), the PIC approach is often preferable.

The combination of interference cancellation and ATRF channel estimation can also be extended to parallel interference cancellation techniques. Figure 9 depicts one stage of a system 900 combining parallel interference cancellation (PIC) and adaptive minimum cost channel estimation (MCCE) according to a further specific illustrative embodiment of our invention. We shall refer to this system as a PIC-

MCCE system. In the PIC-MCCE system 900, rather than detecting one additional user at each stage of the detector as in the SIC-MCCE system 200, every user is detected anew at each stage.

The PIC-MCCE system 900 includes a plurality of parallel processors 905. The number of processors can vary but is typically determined by the number of users associated with the system. Each processor is comprised of a conventional detector 206, a respread processor 208 and an ATRF 910. The conventional detector 206 in each parallel processor 905 is connected to a respread processor 208 and to a single external entity that communicates the received signal r(t) as input to the conventional detector. The ATRF 910 in each parallel processor 905 is connected between a respread processor 208 and a series 913 of mathematical operations processors 212. Alternatively, a partial summer circuit could be substituted for the series of mathematical operations processors. The series of mathematical operations processors 913 (or alternatively the partial summer circuit) is connected to the ATRF 210 in every parallel processor 905 and to the external entity providing the received signal.

The conventional detector 206 and the respread processor 208 are identical to the conventional detector 206 and respread processor 208 used in the SIC-MCCE embodiment. In addition, a control processor 902 could optionally be included to provide ordering of the signals prior to processing by the PIC-MCCE system.

Figure 10 shows a flow diagram of the operation of each processor 905 of the embodiment of Figure 9. After initial processing such as downconversion to baseband is performed on the received signal by an external entity, the received signal is sent in parallel to each of the processors 905 in the first stage of the PIC-MCCE system. The conventional detector 206 in each processor 905 determines the initial symbol decision estimate for the user assigned to that processor (step 1010). In each processor 905, the initial symbol estimate is communicated to the respread processor 208. The respread processor 208 generates a scaled estimate of the transmitted signal waveform for the user (step 1020). After respreading, each user is temporally reconstructed in the ATRF 910 (step 1030).

The outputs from the ATRF 910 in each processor are sent in parallel to the series of mathematical operations processors 913 (or alternatively to the partial summer). The mathematical operations processors 212 sum up all signals but one for each output, thus, forming an estimate of the interference for each user (step 1040). This interference estimate is then subtracted out of the received signal (step

1050). This process can be repeated for multiple PIC stages until the signal converges. At each stage, different numbers of users are successfully detected. Typically, as the number of stages increases, the number of users successfully detected increases, although oscillatory conditions can also occur. We define convergence as occurring at the stage after which no substantial increase is obtained in the number of successfully detected stages. The number of repetitions can be fixed or under dynamic control. Due to the computational complexity of repeating the PIC-MCCE stages, a preferred implementation defines the optimal number of repetitions.

A first approach to channel estimation in the PIC structure is the same as described above for basic SIC-MCCE channel estimation. A joint MCCE channel estimation approach, described above for the SIC-JMCCE system, can also be applied to the parallel structure. We refer to this system as PIC-JMCCE.

A partial PIC-JMCCE system is shown in Figure 11A according to an illustrative embodiment of our invention. In this embodiment, each processor 905 of the PIC-JMCCE system has an individual ATRF 911. In a system with k users, each ATRF 911 receives k input signals, one from each of the respread processors 208 in the other parallel processors 905. Each ATRF 911 processes the signals as described above for step 544 of SIC-JMCCE processing.

An alternative embodiment of the PIC-JMCCE system is shown in Figure 11B, having a single ATRF 912. In this embodiment, each processor 905 has a conventional detector 206 and a respread processor 208. The output of the respread processor 208 in every parallel processor 905 is communicated as input to the single ATRF 912. In the PIC-JMCCE receiver, since the channels are estimated simultaneously for all successfully detected signals, only a single ATRF module is needed at each state, however, this ATRF module produces channel estimates for all signals. After reconstruction, the ATRF outputs the signal interference associated with each user to the series of mathematical operations processors 913.

A third approach to channel estimation, PIC-MF-MCCE, extends the ATRF to account for Doppler spread. This approach is identical to the approach described above for SIC-MF-MCCE. In the PIC-MF-MCCE arrangement, a frequency shift processor 814 is connected between the respread processor 208 and the ATRF 810 in each parallel processor 905 of the system.

The above embodiment assumes that all signals are used in the PIC-MCCE

system at each stage. This condition can be relaxed to include groups of signals at each stage. For example, a control processor could be used to order the received signals in groups of similar power and successively detect groups of users in parallel. Similarly, the PIC-JMCCE system need not include all previously detected signals at each stage, but possibly, some subset of them.

II. Application of STAP to Systems Without a Pilot Reference Signal

Through the use of space time adaptive processing (STAP), a receiver is able to spatially separate user signals using array (smart antenna) receiver technology. This feature allows a STAP receiver to place spatial beam pattern nulls on strong interferers. In addition, the STAP receiver combines multipath energy, including both the resolvable multipath that is captured by a rake receiver, as well as unresolved multipath that the rake receiver cannot effectively exploit.

A single user space time adaptive processing (STAP) receiver is depicted in Figure 12 in accordance with an illustrative embodiment of our invention. The STAP receiver 1200 includes a plurality of filters 1250, one per antenna, in a parallel arrangement, a mathematical summation processor 1270 for combining the outputs of all the filters prior to detection, a conventional detector 206, a respread processor 208, mathematical operations processor 212, and an MCCE weight update processor 64. The receiver in Figure 12 also can include implementations with a one time tap per antenna (spatial adaptive signal processing) or with a single antenna element and multiple time taps (single element adaptive rake receiver). Each filter 1250 contains a tap delay line 1252, a series of STAP weights 1254, and a summation processor 1256. In a traditional STAP receiver, the STAP weights in the filter 1250 can be trained using a known pilot signal. However, a key complication in applying STAP to the IS-95 reverse link is that there is no pilot present in the received signal. Our invention provides innovative processes for blind adaptation where no pilot signal exists to train the filter weight.

An illustrative embodiment of our invention comprises a space time adaptive processing (STAP) processor, means for hypothesizing possible symbols transmitted during a symbol period, a respread processor, means for weight computation wherein the hypothesized symbol and the vector input symbol are used to form a set of STAP weights which filter the input data spatially and temporally, a matched filter bank, means for determining a metric to measure the quality of the matched filter bank, and means for comparing generated metrics. The STAP processor includes a plurality of filters, each comprising a set of STAP

weights, and a plurality of mathematical summation circuits. In addition, each filter may also include a tapped delay line. In a preferred IS-95 implementation, the matched filter bank is a bank of 64 matched filters that correspond to the 64 possible Walsh symbols.

When a user signal is received by the antenna array, the user signal from each antenna in the array is first downconverted to baseband in a processor (not shown) and sampled. Downconversion and sampling are performed by an external processor. After the resulting signal $r_1(t)$, $r_2(t)$, ... $r_M(t)$ is received, a metric is determined associated with a hypothesized symbol value. The metric used may also be referred to as the sharpness factor. The step of determining a metric is repeated for each of the possible 64 Walsh symbols. The resulting 64 metrics are compared in the comparison means to determine the best estimate for the transmitted signal. This estimate is the output of the blind adaptive STAP detector.

A more detailed description of the metric determination step is described below. After the input signal vector is received, the hypothesizing means hypothesizes which symbol was transmitted. The hypothesized symbol is communicated to the respread processor and spread to create a replica of the transmitted waveform. The replica of the transmitted waveform and the input signal vector are input to the weight computation means. The weight computation means uses these inputs to determine the appropriate STAP weights for the STAP filters. After the determination is made, these STAP weights are communicated to the filters and applied to each signal vector component, $r_1(t)$, $r_2(t)$, ... $r_M(t)$. Before application of the STAP weights, a tapped delay line may be applied to each component of the input signal vector. After application of the STAP weights, the weighted signals from every antenna are combined in a mathematical summation circuit. The output of the summation circuit is despread and input into the matched filter bank. The matched filter bank generates a metric associated with the hypothesized symbol.

In an alternate embodiment, the STAP processor may despread the delayed signals from each antenna element and then apply the STAP weights. After the STAP weights are applied, the results are summed and used as input to the matched filter bank.

For example in IS-95, the sharpness factor is computed by taking the ratio of the peak output (i.e., for the most likely transmitted symbol) to the sum of the outputs for all the other 63 hypothesized Walsh symbols. The sharpness factor can also be based on the distance between the peak output and the average of all other

outputs. In either case the STAP solution with the largest sharpness factor is chosen to determine the correctly hypothesized symbol. This embodiment can be extended across multiple symbols where we hypothesize all combinations of multiple symbols.

In an alternative embodiment, the STAP filter weights are determined based on a combination of "known" symbols and hypothesized symbols. The known symbols may be obtained by feeding back previously detected symbols, or from a priori known pilot reference symbols. Utilizing the known symbols allows extension of the length of the training sequence without requiring additional hypothesized symbols. It also anchors the hypothesized STAP solutions to a partially known training sequence, which makes it more likely that the correctly hypothesized solution will stand out. The above embodiments can be repeated for each symbol. These procedures can also be utilized to detect initial symbol(s), and then utilize an update procedure to compute the STAP weights for the remaining symbols. In other words, the STAP weights of the previous symbol can be used to detect the current symbol which can then in turn be used to update the STAP tap weights for the next symbol.

III. Combined STAP and MUD

The STAP receiver shown in Figure 12 is limited in several ways. First, it can only effectively null M-1 high level signals (including temporally resolvable multipath components) where M is the number of antennas used. Therefore, it is only effective at extracting the M strongest signal components. Another embodiment of our invention combines MUD and temporal interference cancellation techniques and thus, removes much of the interfering signals before applying the STAP receiver. This approach frees up STAP degrees of freedom to operate on the remaining interference more effectively.

Figure 13 depicts a single stage of a system 1300 combining STAP, interference cancellation MUD, and minimum cost channel estimation (MCCE) according to a specific illustrative embodiment of our invention. The illustrative embodiment of our invention shown in Figure 13 applies SIC (e.g., SIC-MCCE or SIC-JMCCE) to each antenna element separately. We shall refer to this system as the STAP/VSIC system where the V refers to the vector nature of the cancellation process. The multi-stage STAP/VSIC receivers resemble the multi-stage SIC receivers of figure 2, 4, and 5, except that the received signal and cleaned received

signals are now vectors of size M.

A single stage of the STAP/VSIC system includes a STAP processor 1200, a plurality of ATRFs 1210, and a plurality of mathematical operations processors 212. The STAP processor can be a standard STAP processor or a blind adaptive STAP processor. In an illustrative embodiment of our invention, the STAP processor includes a plurality of filters 1250, a mathematical operations processor, and a conventional detector. In an alternate embodiment, the STAP processor may include a respread processor and may also include a MCCE weight update processor.

When a user signal is received by the antenna array, the user signal from each antenna in the array is first downconverted to baseband in a processor (not shown) and sampled. For each antenna, the resulting signal, $r_1(t)$, $r_2(t)$, ... $r_M(t)$, is communicated to the STAP processor 1200. After processing by the STAP filters, conventional detector, and respread processor as described in the embodiments above, the output of the respread processor, a vector estimate of the transmitted signal for the user, is communicated to the ATRFs 1210, one per antenna. Each ATRF 1210 then estimates the channel associated with the signal and reconstructs the signal interference. The methods used for channel estimation in the STAP/VSIC system can be either basic MCCE, JMCCE, or MF-MCCE techniques. Each reconstructed signal is then cancelled from the total received input for that antenna in a mathematical processor 212. The output of the plurality of mathematical processors, one per antenna, is then used as the vector input to the next STAP/VSIC stage.

The STAP/VSIC system approach can also be extended to vectorized parallel interference cancellation. We shall refer to this system as the STAP/VPIC system. In these embodiments, the system would take the form of the PIC detector shown in Figure 9 with the conventional detector replaced by the one of the above described embodiments of a STAP processor.

Another embodiment of our invention combines STAP with interference cancellation techniques. In this embodiment, the system jointly solves for the ATRF tap weights and STAP tap weights. For example, the system minimizes the error associated with the cost function between the transmitted symbol replica and the sum of the STAP filter outputs and ATRF filter outputs. Figure 14 depicts one illustrative embodiment of our invention. We shall refer to this system as the J-STAPSIC system.

The illustrative system of Figure 14 comprises a plurality of J-STAPSIC processors arranged in successive stages 1404. The input to the J-STAPSIC system 1400 is a vector of size M where M is equivalent to one received signal stream for each antenna element). Each stage utilizes the symbols of all previously detected users, and detects one additional user's symbols. The number of stages, K, is equivalent to the total number of users associated with the system.

An illustrative embodiment of a k^{th} J-STAPSIC stage 1404 is shown in Figure 15. Each J-STAPSIC stage comprises a plurality of STAP filters 1252, one per antenna, in a parallel arrangement, a plurality of respread processors, one per previous stage, in a parallel arrangement for receiving the symbol estimates from the previous J-STAPSIC stages, a plurality of ATRF filters 1410, one per previous stage, a mathematical summation circuit 1414 for summing the outputs of the plurality of STAP filters, a mathematical summation circuit 1414 for summing the outputs of the plurality of ATRF filters, a mathematical operations processor 212 for adding the outputs of the mathematical summation circuits 1414, a conventional detector 206, and a respread processor 208.

In the k^{th} stage, the plurality of STAP filters 1252 receive a cleaned vector received signal, $r_1(t)$, $r_2(t)$, ... $r_M(t)$ from the previous stage and the plurality of parallel respread processors receive a vector comprising symbol estimates determined in the previous stage. In each parallel respread processor, the symbol estimates are spread. The mathematical summation circuit 1414 sums the outputs from the plurality of the STAP filters and another mathematical summation circuit sums the outputs from the plurality of ATRF filters. The outputs of these summation circuits are then combined in a mathematical operations circuit 212. Using the output of the mathematical operations circuit 212, the conventional detector despreads the input and estimates the symbol transmitted. The symbol estimate is then spread by the respread processor. The output of the respread processor is combined with the output of the conventional detector and is used as input to an MCCE weight update processor. The MCCE weight update processor then updates in parallel the tap weights of the plurality of STAP and ATRF filters.

Although the invention has been shown and described with respect to exemplary embodiments thereof, it should be understood by those skilled in the art that various changes, omissions and additions may be therein and thereto, without departing from the spirit and the scope of the invention.

WHAT IS CLAIMED IS:

1. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a control processor comprising a means for ordering user signals; and

a plurality of SIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection and adaptive temporal reconstruction filtering in a successive arrangement wherein the output of one of the said processors is the input to the next successive processor, each of said SIC-ATRF processors comprising:

a conventional detector;

a respread processor;

an adaptive temporal filter (ATRF); and

a complex mathematical operation processor for canceling the reconstructed signal for the user from the total received signal.

2. The combination of claim 1 wherein each conventional detector is an IS-95 conventional detector comprising a short code despreader, a long code despreader, and a 64-ary matched filter bank.

3. The combination of claim 1 wherein each conventional detector is an IS-95 rake conventional detector.

4. The combination of claim 1 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

5. The combination of claim 4 wherein each SIC-ATRF processor further comprises a minimum cost channel estimate (MCCE) weight update processor.

6. The combination of claim 4 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

7. The combination of claim 4 wherein each ATRF is a minimum mean square error filter.

8. The combination of claim 1 wherein the output of each respread processor is the input for the ATRF.

9. The combination of claim 8 wherein the input to each ATRF further comprises the outputs of the respread processors in all the previous SIC-ATRF processors.

10. The combination of claim 1 wherein each SIC-ATRF processor further comprises a frequency shift processor connected between the respread processor and the adaptive temporal filter.

11. The combination of claim 10 wherein each frequency shift processor comprises means to shift the frequency of the signal output from the respread processor to take into account Doppler spread.

12. A method in a combination system for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering user signals according to a pre-defined methodology and assigning each user signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, an adaptive temporal filter; and a complex mathematical operation processor for canceling the reconstructed signal for the user from the total received signal;

communicating a separate user code associated with the user signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

estimating a channel for the user associated with the SIC-ATRF processor and reconstructing the signal interference associated with the user signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the user associated with the SIC-ATRF processor from the total received signal.

if a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to the next successive SIC-ATRF processor.

13. The method of claim 12 wherein the step of ordering user signals according to a pre-defined methodology comprises ranking signals in descending order of received powers.

14. The method of claim 12 wherein the step of ordering user signals according to a pre-defined methodology comprises identifying signals above a certain threshold.

15. The method of claim 12 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

16. The method of claim 15 wherein the pre-determined cost function is a minimum mean square error function.

17. The method of claim 12 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of previous SIC-ATRF processors; and

updating, in the ATRF, the filter tap weights.

18. The method of claim 17 wherein the pre-determined cost function is a minimum mean square error function.

19. A method in a combination system for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a control processor and a plurality of SIC-ATRF processors in a successive arrangement, said method comprising:

ordering user signals according to a pre-defined methodology and assigning each user signal to one of the SIC-ATRF processors wherein each SIC-ATRF processor comprises a conventional detector, a respread processor, a frequency shift processor, an adaptive temporal filter; and a complex mathematical operation processor for canceling the reconstructed signal for the user from the total received signal.;

communicating a separate user code associated with the user signal to each SIC-ATRF processor according to the ordering;

in each successive SIC-ATRF processor, performing the steps of:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

shifting, in the frequency shift processor, the symbol estimate generated by the respread processor for the user associated with the SIC-ATRF processor;

estimating a channel for the user associated with the SIC-ATRF processor and reconstructing the signal interference associated with the user signal; and

canceling, in a mathematical operations processor, the reconstructed signal for the user associated with the SIC-ATRF processor from the total received signal.

If a plurality of SIC-ATRF processors remain, inputting the output of the current SIC-ATRF processor to the next successive SIC-ATRF processor.

20. The method of claim 19 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

21. The method of claim 19 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received frequency shift estimate and the sum of the outputs of the frequency shift processors of previous SIC-ATRF processors; and

updating, in the ATRF, the filter tap weights.

22. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every processor is a received signal, each of said parallel processors comprising:

a conventional detector;

a respread processor; and

an adaptive temporal filter (ATRF); and

means for summing signals to form an interference estimate and subtracting the estimate from the received signal.

23. The combination of claim 22 further comprising a control processor including a means for ordering user signals.

24. The combination of claim 22 wherein the summation and subtraction means is a series of mathematical operations processors.

25. The system of claim 22 wherein the summation and subtraction means is a partial summer circuit.

26. The combination of claim 22 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

27. The combination of claim 26 wherein each parallel processor further comprises an MCCE weight update processor.

28. The combination of claim 26 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

29. The combination of claim 22 wherein, in each parallel processor, the output of the respread processor is the input for the ATRF.

30. The combination of claim 22 wherein, in each parallel processor, the input to the ATRF comprises the outputs of the respread processors in all the other parallel processors.

31. The combination of claim 22 wherein each parallel processor further comprises a frequency shift processor connected between the respread processor and the ATRF.

32. The combination of claim 31 wherein each frequency shift processor comprises means to shift the frequency of the signal output from the respread processor to take into account doppler spread.

33. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every processor is a received signal, each of said parallel processors comprising:

a conventional detector; and

a respread processor;

an adaptive temporal filter (ATRF); and

means for summing signals to form an interference estimate and subtracting the estimate from the received signal.

34. The combination of claim 33 wherein the input to each ATRF comprises the outputs of the respread processors in all the parallel processors.

35. The combination of claim 33 wherein the ATRF further comprises a MCCE weight update processor.

36. The combination of claim 35 wherein each parallel processor further comprises a frequency shift processor connected between the respread processor in the parallel processor and the ATRF.

37. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors and means for summing signals to form an interference estimate and subtracting the estimate from the received signal:

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector, a respread processor, and an adaptive temporal filter (ATRF);

generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate; and

estimating a channel for the signal associated with the parallel processor and reconstructing the signal interference;

communicating the output of each parallel processor to a means for mathematically summing signals and subtracting signal estimates from the received signal;

generating, in the mathematical means, an interference estimate for each user; and

subtracting, in the mathematical means, the interference estimate from the received signal.

38. The method of claim 37 further comprising the steps of:

ordering user signals according to a pre-defined methodology; and

communicating a separate user code to a conventional detector in each parallel processor.

39. The method of claim 37 wherein the step of channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

40. The method of claim 37 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

41. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors, an adaptive temporal filter (ATRF), and means for summing signals to form an interference estimate and subtracting the estimate from the received signal, the method comprising the steps of:

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector and a respread processor;

generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor; and

spreading, in the respread processor, the symbol estimate;

estimating a channel for the signal associated with each parallel processor and reconstructing the signal interference;

communicating the output of the ATRF to a means for mathematically summing signals and subtracting signal estimates from the received signal;

generating, in the mathematical means, an interference estimate for each user; and

subtracting, in the mathematical means, the interference estimate from the received signal.

42. The method of claim 41 wherein the step of channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

43. The method of claim 41 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

44. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said combination comprises a plurality of parallel processors and means for summing signals to form an interference estimate and subtracting the estimate from the received signal, the method comprising the steps of:

communicating a received signal to the plurality of parallel processors wherein each of the processors comprises a conventional detector, a respread processor, a frequency shift processor and an adaptive temporal filter (ATRF);

generating a reconstructed signal in each of the parallel processors for a user associated with the parallel processor; said generation step further comprising:

despreading, in the conventional detector, the received signal and estimating a symbol transmitted for the desired user signal;

communicating the symbol estimate to the respread processor;

spreading, in the respread processor, the symbol estimate;

shifting, in the frequency shift processor, the symbol estimate generated by the respread processor for the user association with the parallel processor; and

estimating a channel for the signal associated with the parallel processor and reconstructing the signal interference;

communicating the output of each parallel processor to a means for mathematically summing signals and subtracting signal estimates from the received signal;

generating, in the mathematical means, an interference estimate for each user; and

subtracting, in the mathematical means, the interference estimate from the received signal.

45. The method of claim 44 wherein the step of channel estimation step further comprises:

determining the adaptive filter tap weights that minimize a pre-determined cost function between the received signal and an output of the adaptive filter; and

updating, in the ATRF, the filter tap weights.

46. The method of claim 44 wherein the channel estimation step further comprises:

determining the adaptive filter tap weights by jointly minimizing the cost function between the received signal and the sum of the outputs of the respread processors of all the other parallel processors; and

updating, in the ATRF, the filter tap weights.

47. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver, said combination comprising:

a space-time adaptive processing (STAP) processor;

means for hypothesizing possible symbols transmitted during a symbol period;

a respread processor;

means for weight computation wherein the hypothesized symbol and the vector input symbol are used to form a set of STAP weights which filter the input data spatially and temporally;

a matched filter bank;

means for determining a metric to measure the quality of the matched filter bank; and

means for comparing generated metrics.

48. The combination of claim 47 wherein the STAP processor comprises a plurality of tapped delay lines, one per antenna element.

49. The combination of claim 47 wherein the possible symbols transmitted are the 64 Walsh symbols for an IS-95 reverse link transmitter.

50. The combination of claim 49 wherein the matched filter bank is a bank of 64 matched filters corresponding to the 64 Walsh symbols.

51. The combination of claim 47 wherein the means for weight computation further comprises a means for using previously detected or known symbols.

52. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said

input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver; the method comprising the steps of:

receiving the input signal vector;

determining a metric, said determining step comprising:

hypothesizing which symbol was transmitted;

respreading the hypothesized symbol;

determining STAP weight update based on respread hypothesized symbol and input signal vector;

applying a tap delay line to each signal vector component;

applying STAP weights to each signal vector component, one per antenna;

summing the weighted results in a mathematical summation circuit;

despreading the output of the summation circuit and inputting the despread signal to a matched filter bank; and

generating a metric associated with the hypothesized signal;

repeating the metric determining step for each of the possible 64 Walsh symbols;

comparing each of the 64 metrics; and

determining, based on the comparison, the transmitted symbol.

53. A method in a combination system for enabling a receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver; the method comprising the steps of:

receiving the input signal vector;

determining a metric, said determining step comprising:

hypothesizing which symbol was transmitted;

respreading the hypothesized symbol;

determining STAP weight update based on respread hypothesized symbol and input signal vector;

despreading the delayed signal vector components, one per antenna;

applying the STAP weights to each of the despread signal vector components;

summing the weighted results in a mathematical summation circuit; and

generating a metric associated with the hypothesized signal;

repeating the metric determining step for each of the possible 64 Walsh symbols;

comparing each of the 64 metrics; and

determining, based on the comparison, the transmitted symbol.

54. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference wherein said input signal is a vector comprised of one signal from each antenna in an antenna array of the receiver, said combination comprising:

a control processor comprising a means for ordering user signals; and

a plurality of STAP/VSIC-ATRF processors combining successive interface cancellation (SIC) multi-user detection, space-time adaptive processing and adaptive temporal reconstruction filtering in a successive arrangement wherein the output of one of the said processors is the vector input to the next successive processor, each of said STAP/VSIC-ATRF processors comprising:

a space-time adaptive processing (STAP) processor;

a plurality of adaptive temporal filters (ATRFs), one per antenna; and

a plurality of complex mathematical operation processors, one per ATRF, for canceling the reconstructed signal for the user from the total received signal.

55. The combination of claim 54 wherein each STAP processor comprises:

a plurality of filters, one per antenna;

a mathematical summation processor for combining the outputs of all the filters;

a conventional detector; and

a minimum cost channel weight update processor.

56. The combination of claim 55 wherein the STAP processor is a blind adaptive STAP processor.

57. The combination of claim 55 wherein each STAP/VSIC-ATRF processor further comprises a plurality of respread processors.

58. The combination of claim 55 wherein each STAP processor further comprises a respread processor.

59. The combination of claim 54 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

60. The combination of claim 59 wherein each ATRF further comprises a minimum cost channel estimate weight update processor.

61. The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, the output of the respread processor is the input for the plurality of ATRFs.

62. The combination of claim 57 wherein, in each STAP/VSIC-ATRF processor, the input to the plurality of ATRFs further comprises the outputs of the respread processors in all the previous STAP/VSIC-ATRF processors.

63. The combination of claim 57 wherein each STAP/VSIC-ATRF processor further comprises a plurality of frequency shift processors connected between the respread processor and the plurality of ATRFs.

64. In a wireless receiver for a CDMA system, a combination for enabling the receiver to receive input signals at varied power levels in the presence of interference, said combination comprising:

a plurality of processors in a parallel arrangement wherein the input to every processor is a received signal, each of said parallel processors comprising:

a space-time adaptive processing (STAP) processor; and

a plurality of adaptive temporal filters (ATRFs); and

means for summing signals to form an interference estimate and subtracting the estimate from the received signal.

65. The combination of claim 64 wherein each STAP processor comprises:

a plurality of filters, one per antenna;

a mathematical summation processor for combining the outputs of all the filters; and

a conventional detector.

66. The combination of claim 64 wherein each parallel processor further comprises an MCCE weight update processor.

67. The combination of claim 65 wherein each STAP processor further comprises an MCCE weight update processor.

68. The combination of claim 64 wherein each parallel processor further comprises a of respread processor.

69. The combination of claim 65 wherein each STAP processor further comprises a respread processor.

70. The combination of claim 64 wherein the summation and subtraction means is a series of mathematical operations processors.

71. The combination of claim 64 wherein the summation and subtraction means is a series of mathematical operations processors.

72.The combination of claim 64 wherein each ATRF comprises:

tap weights;

a tap delay line; and

a mathematical summing circuit.

73.The combination of claim 68 wherein, in each parallel processor, the output of the respread processor is the input for the plurality of ATRFs.

74. The combination of claim 68 wherein, in each parallel processor, the input to the plurality of ATRFs further comprises the outputs of the respread processors in all the other parallel processors.

75. The combination of claim 68 wherein each parallel processor further comprises a plurality of frequency shift processors connected between the respread processor and the plurality of ATRFs.

FIG. 1

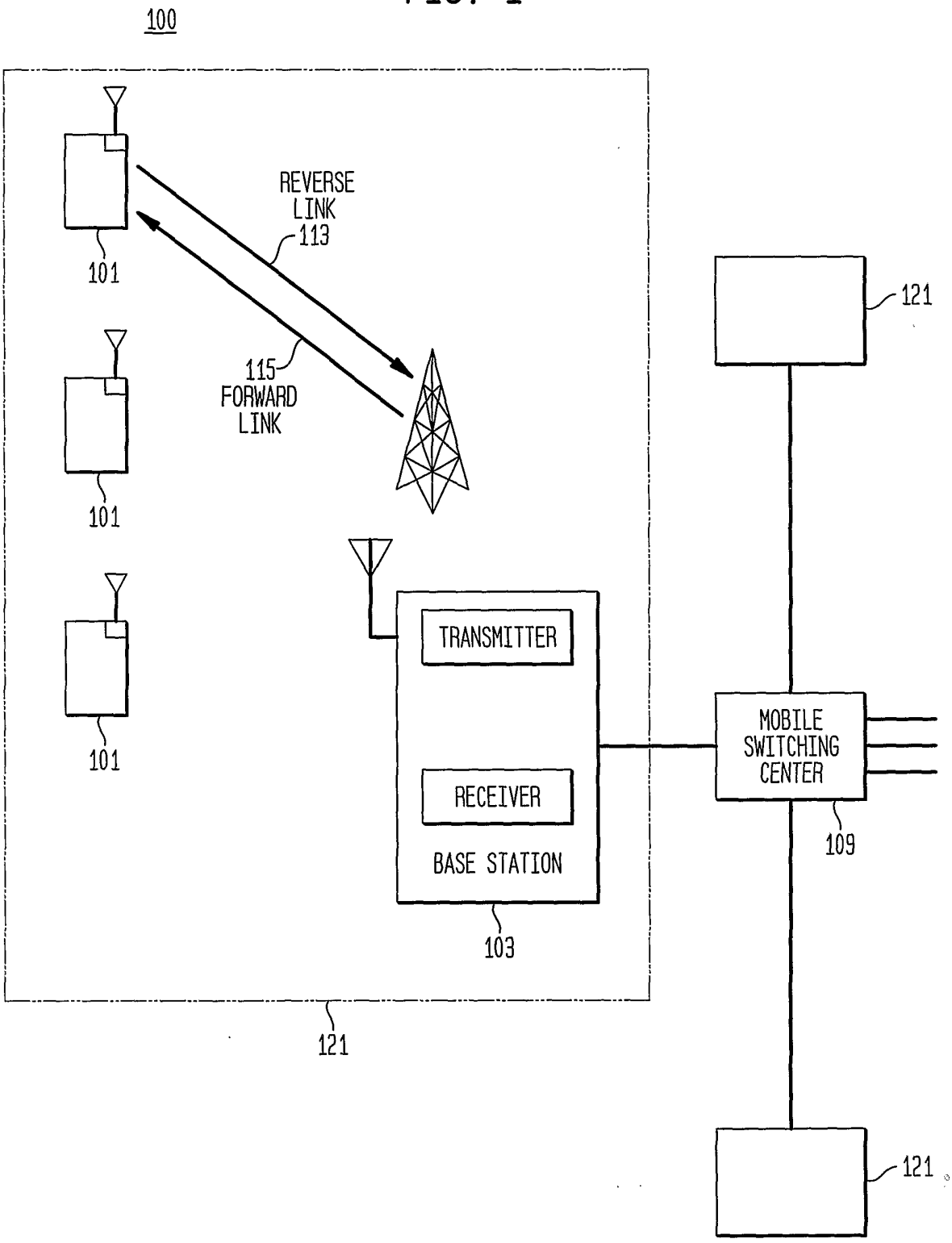

100
REVERSE LINK
113
115
FORWARD LINK
101
101
101
TRANSMITTER
RECEIVER
BASE STATION
103
121
121
121
MOBILE SWITCHING CENTER
109

FIG. 2

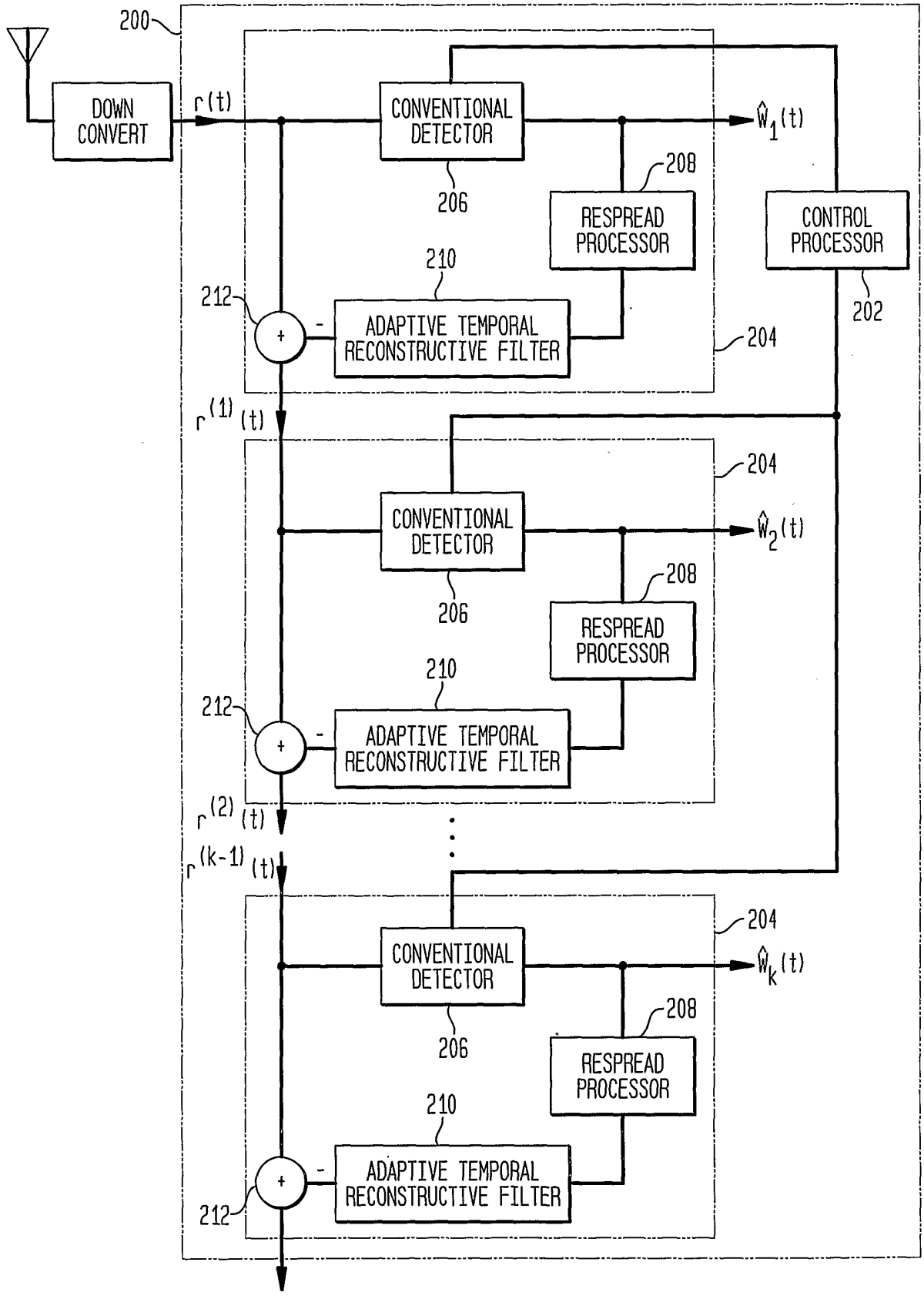

200
DOWN CONVERT
r(t)
CONVENTIONAL DETECTOR
206
208
RESPREAD PROCESSOR
CONTROL PROCESSOR
202
210
212
ADAPTIVE TEMPORAL RECONSTRUCTIVE FILTER
204
$\hat{W}_1(t)$
$r^{(1)}(t)$
$\hat{W}_2(t)$
$r^{(2)}(t)$
$r^{(k-1)}(t)$
$\hat{W}_k(t)$

FIG. 3

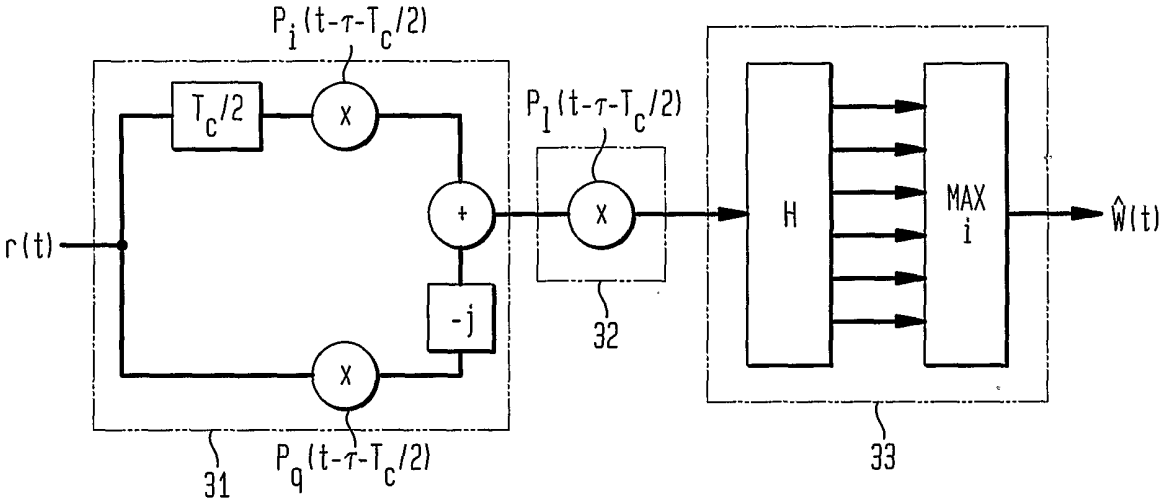

$P_i(t-\tau-T_c/2)$
$T_c/2$
X
+
-j
X
r(t)
$P_q(t-\tau-T_c/2)$
31
$P_l(t-\tau-T_c/2)$
X
32
H
MAX
i
$\hat{W}(t)$
33

FIG. 4

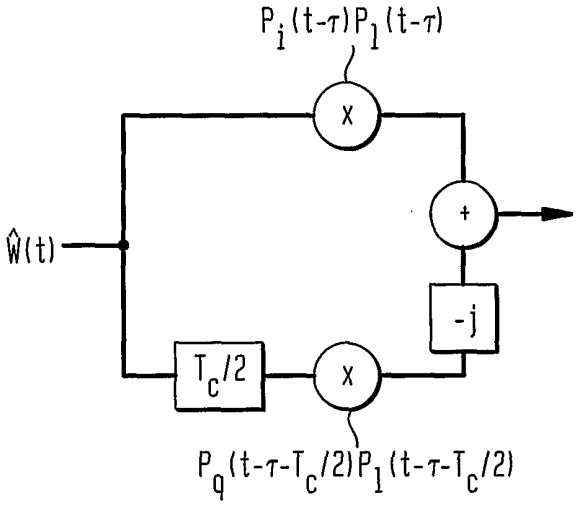

$P_i(t-\tau)P_l(t-\tau)$
X
+
$\hat{W}(t)$
-j
$T_c/2$
X
$P_q(t-\tau-T_c/2)P_l(t-\tau-T_c/2)$

FIG. 5

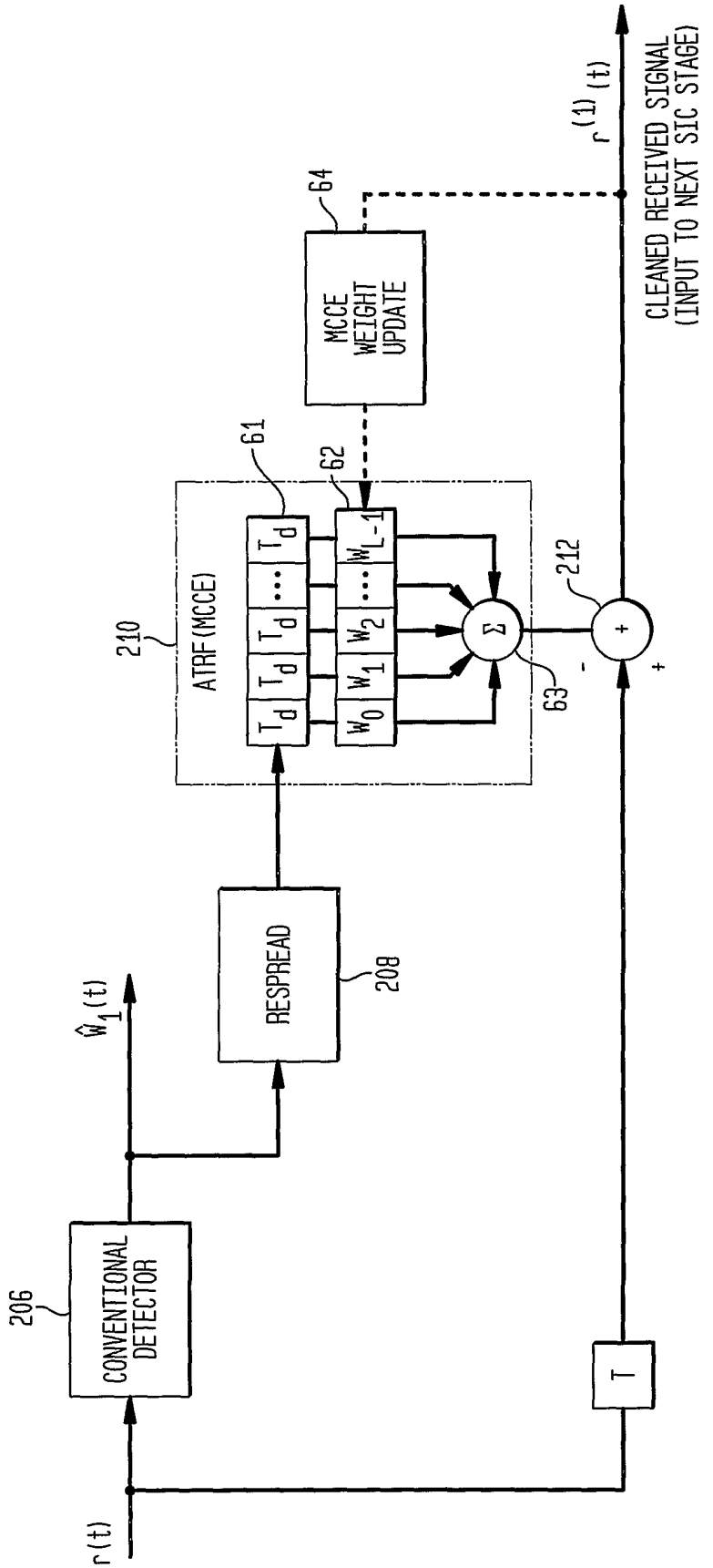

r(t)
CONVENTIONAL DETECTOR
206
$\hat{w}_1(t)$
RESPREAD
208
ATRF (MCCE)
210
61
62
T_d
w_0
w_1
w_2
w_{L-1}
Σ
63
212
+
-
MCCE WEIGHT UPDATE
64
T
$r^{(1)}(t)$
CLEANED RECEIVED SIGNAL (INPUT TO NEXT SIC STAGE)

FIG. 6

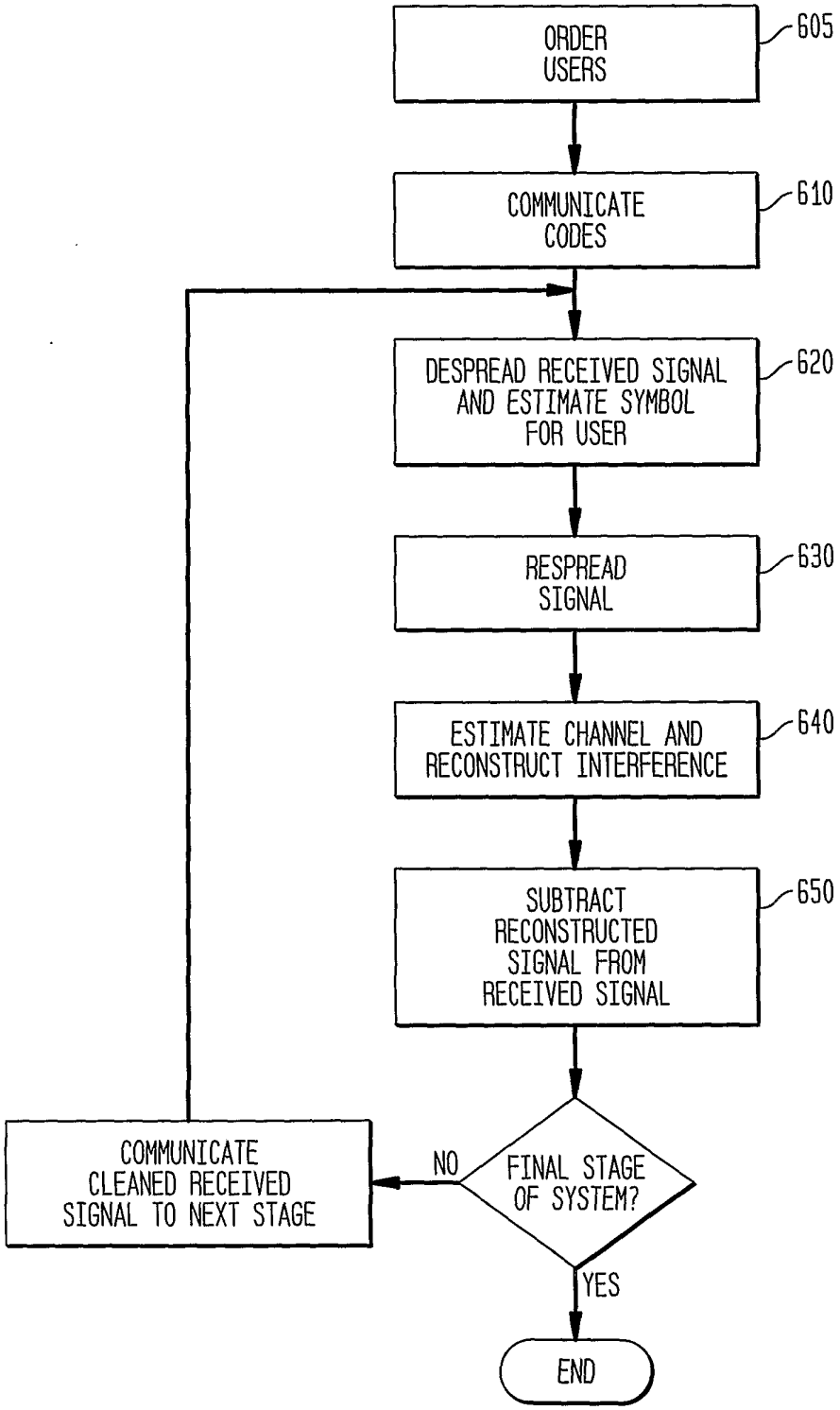
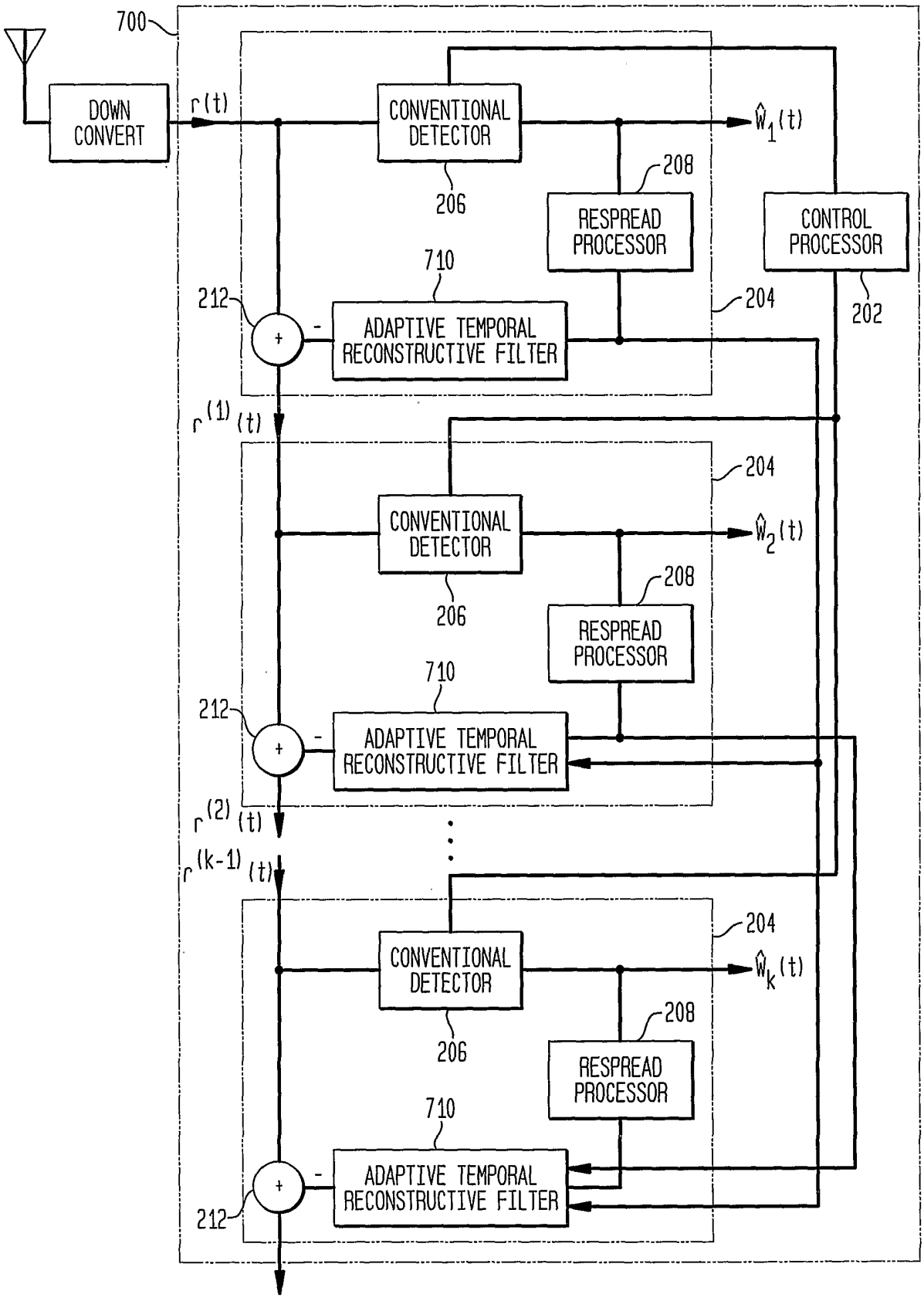

ORDER USERS
605
COMMUNICATE CODES
610
DESPREAD RECEIVED SIGNAL AND ESTIMATE SYMBOL FOR USER
620
RESPREAD SIGNAL
630
ESTIMATE CHANNEL AND RECONSTRUCT INTERFERENCE
640
SUBTRACT RECONSTRUCTED SIGNAL FROM RECEIVED SIGNAL
650
FINAL STAGE OF SYSTEM?
NO
YES
COMMUNICATE CLEANED RECEIVED SIGNAL TO NEXT STAGE
END

FIG. 7


700
DOWN CONVERT
r(t)
CONVENTIONAL DETECTOR
206
208
RESPREAD PROCESSOR
CONTROL PROCESSOR
202
204
710
212
ADAPTIVE TEMPORAL RECONSTRUCTIVE FILTER
$\hat{W}_1(t)$
$r^{(1)}(t)$
$\hat{W}_2(t)$
$r^{(2)}(t)$
$r^{(k-1)}(t)$
$\hat{W}_k(t)$

7/15

FIG. 8

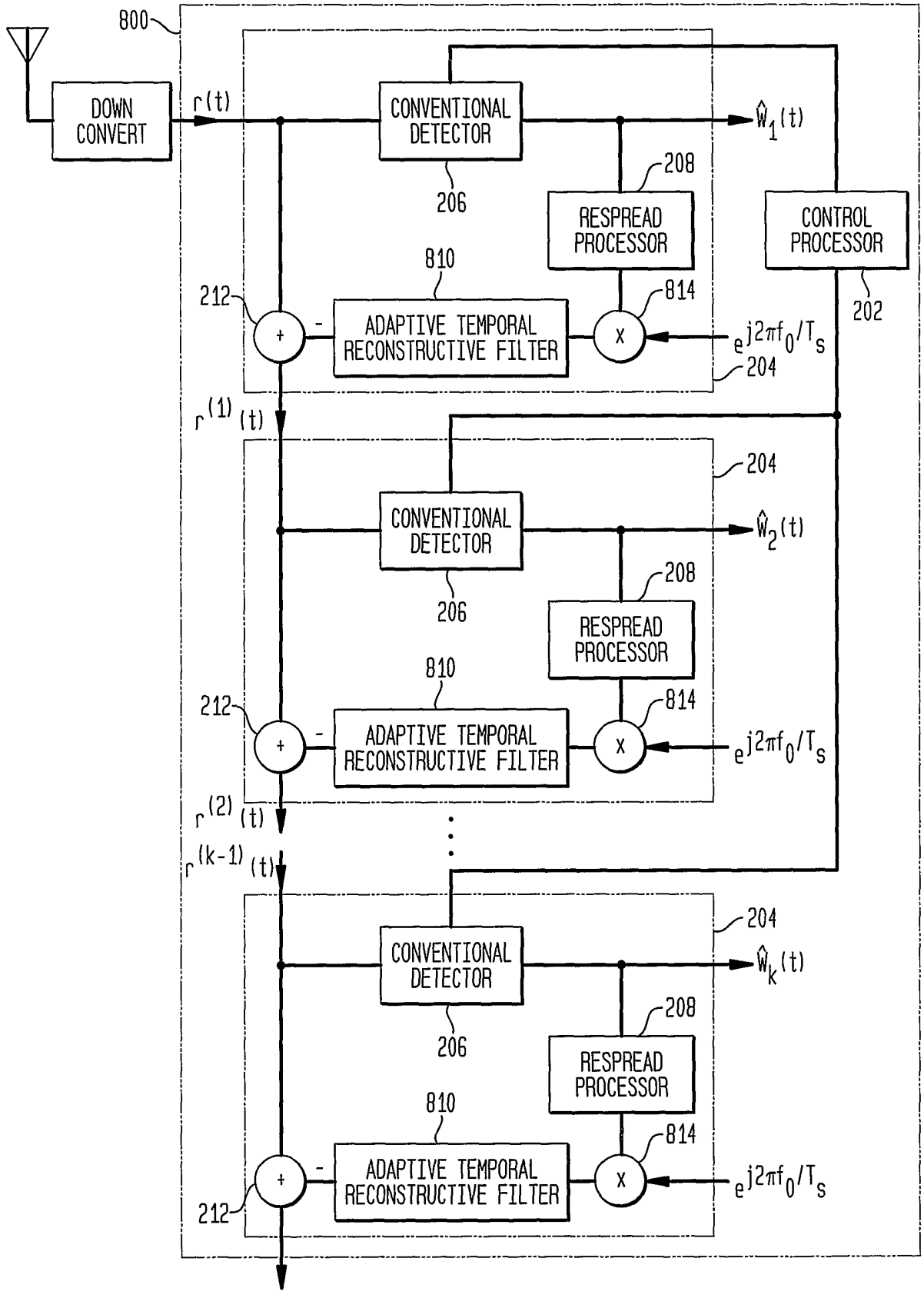

800
DOWN CONVERT
r(t)
CONVENTIONAL DETECTOR
206
208
RESPREAD PROCESSOR
CONTROL PROCESSOR
202
$\hat{W}_1(t)$
810
212
+
-
ADAPTIVE TEMPORAL RECONSTRUCTIVE FILTER
814
X
$e^{j2\pi f_0/T_s}$
204
$r^{(1)}(t)$
$\hat{W}_2(t)$
$r^{(2)}(t)$
$r^{(k-1)}(t)$
$\hat{W}_k(t)$

FIG. 8A

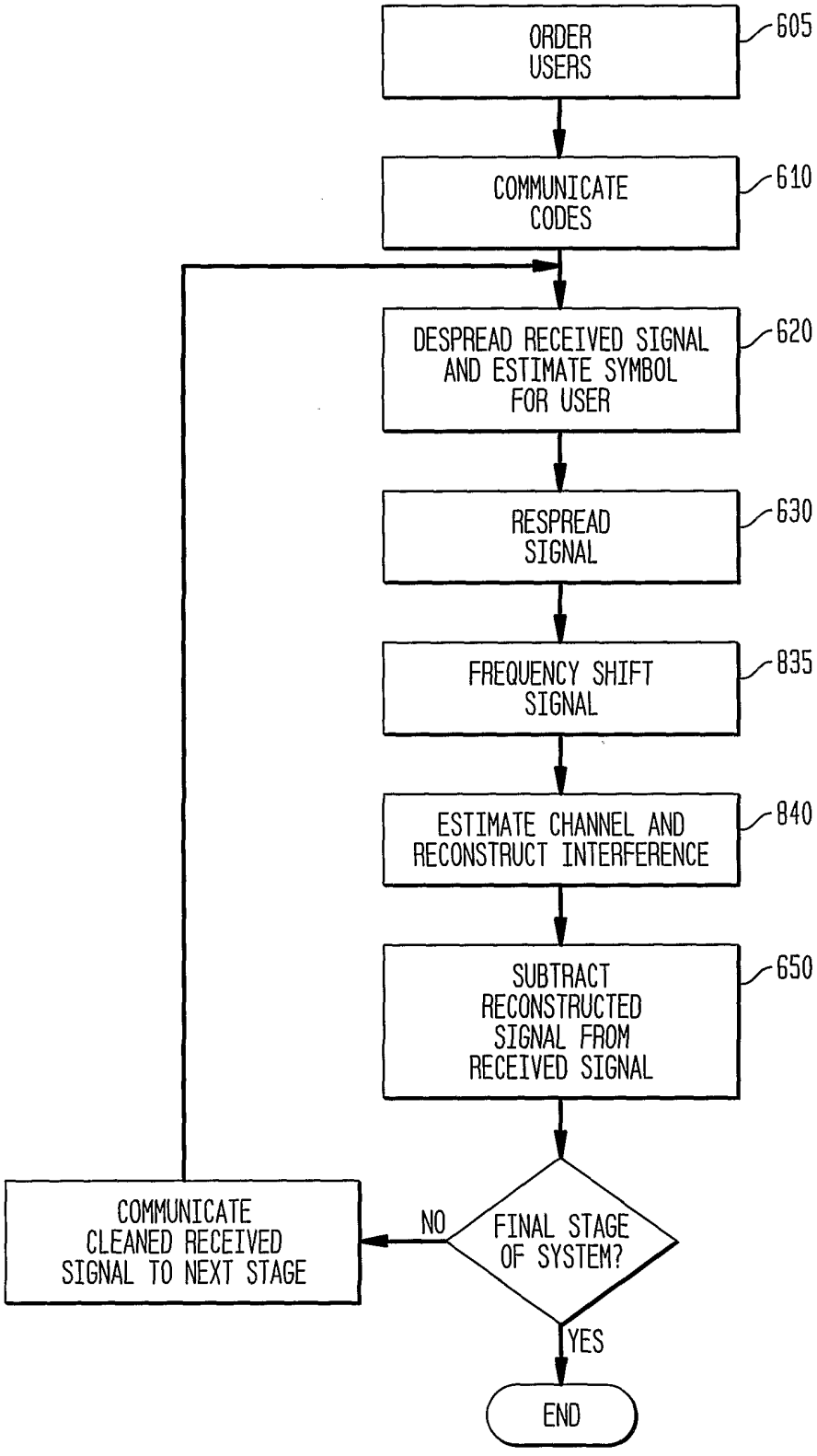

ORDER USERS
605
COMMUNICATE CODES
610
DESPREAD RECEIVED SIGNAL AND ESTIMATE SYMBOL FOR USER
620
RESPREAD SIGNAL
630
FREQUENCY SHIFT SIGNAL
835
ESTIMATE CHANNEL AND RECONSTRUCT INTERFERENCE
840
SUBTRACT RECONSTRUCTED SIGNAL FROM RECEIVED SIGNAL
650
FINAL STAGE OF SYSTEM?
NO
COMMUNICATE CLEANED RECEIVED SIGNAL TO NEXT STAGE
YES
END

FIG. 9

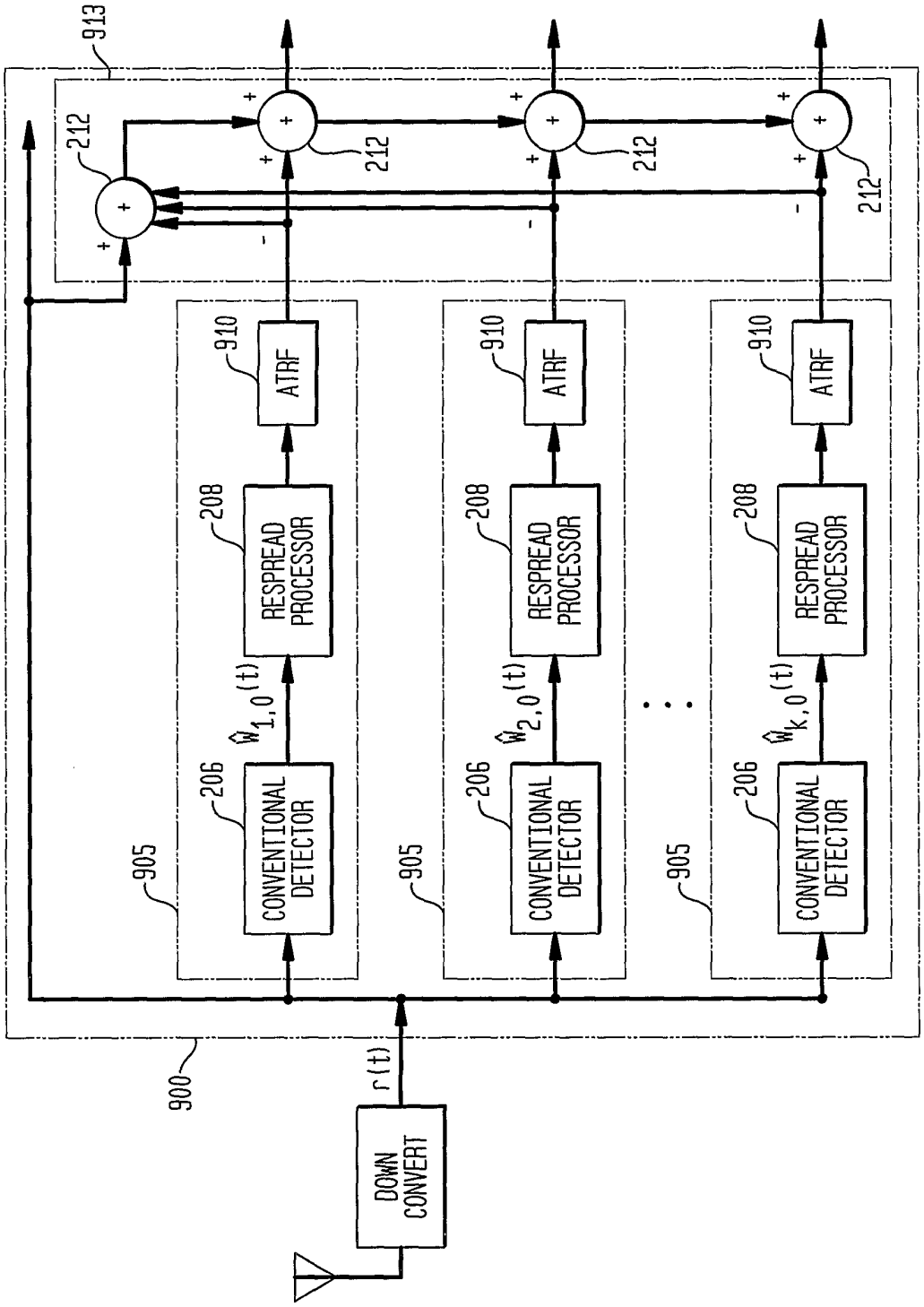

913
212
212
212
212
910
910
910
ATRF
ATRF
ATRF
208
208
208
RESPREAD PROCESSOR
RESPREAD PROCESSOR
RESPREAD PROCESSOR
$\hat{w}_{1,0}(t)$
$\hat{w}_{2,0}(t)$
$\hat{w}_{k,0}(t)$
206
206
206
CONVENTIONAL DETECTOR
CONVENTIONAL DETECTOR
CONVENTIONAL DETECTOR
905
905
905
900
r(t)
DOWN CONVERT

FIG. 10

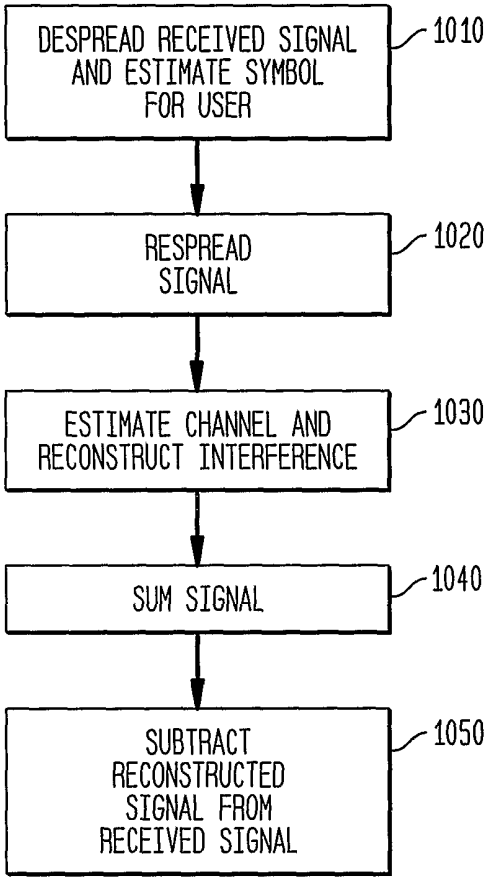

DESPREAD RECEIVED SIGNAL AND ESTIMATE SYMBOL FOR USER
1010
RESPREAD SIGNAL
1020
ESTIMATE CHANNEL AND RECONSTRUCT INTERFERENCE
1030
SUM SIGNAL
1040
SUBTRACT RECONSTRUCTED SIGNAL FROM RECEIVED SIGNAL
1050

FIG. 11A

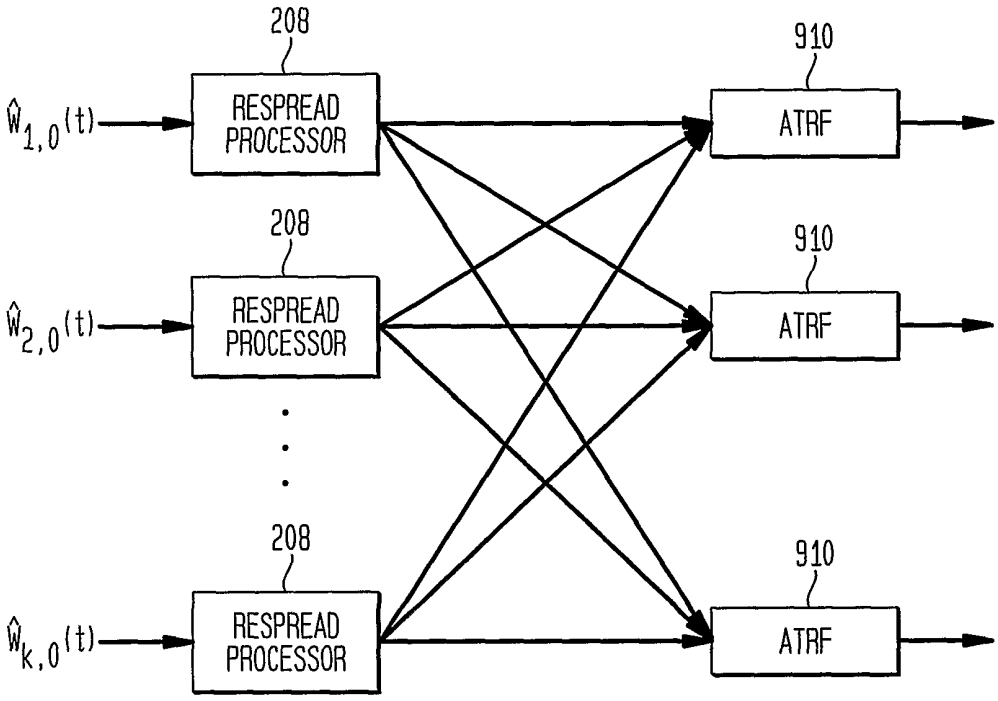


FIG. 11B

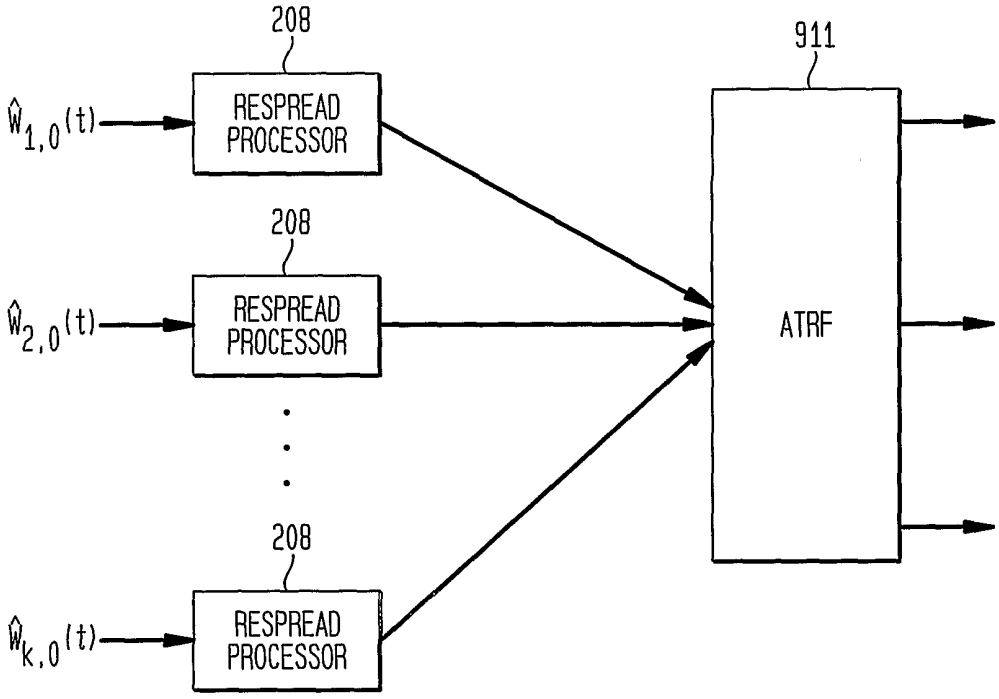


FIG. 12

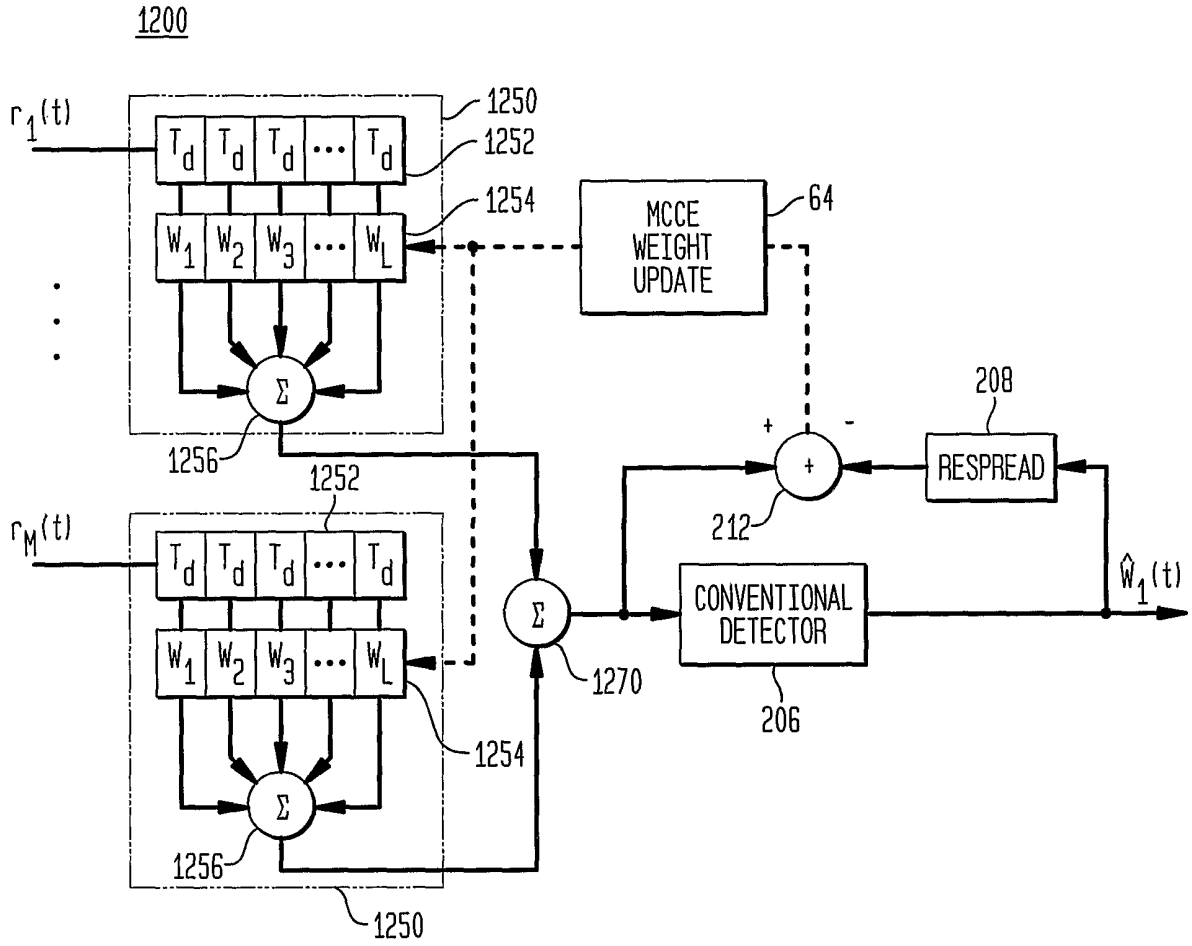

1200
$r_1(t)$
$r_M(t)$
T_d
W_1 W_2 W_3 ... W_L
Σ
1250
1252
1254
1256
MCCE WEIGHT UPDATE
64
208
RESPREAD
212
CONVENTIONAL DETECTOR
206
1270
$\hat{W}_1(t)$

FIG. 13

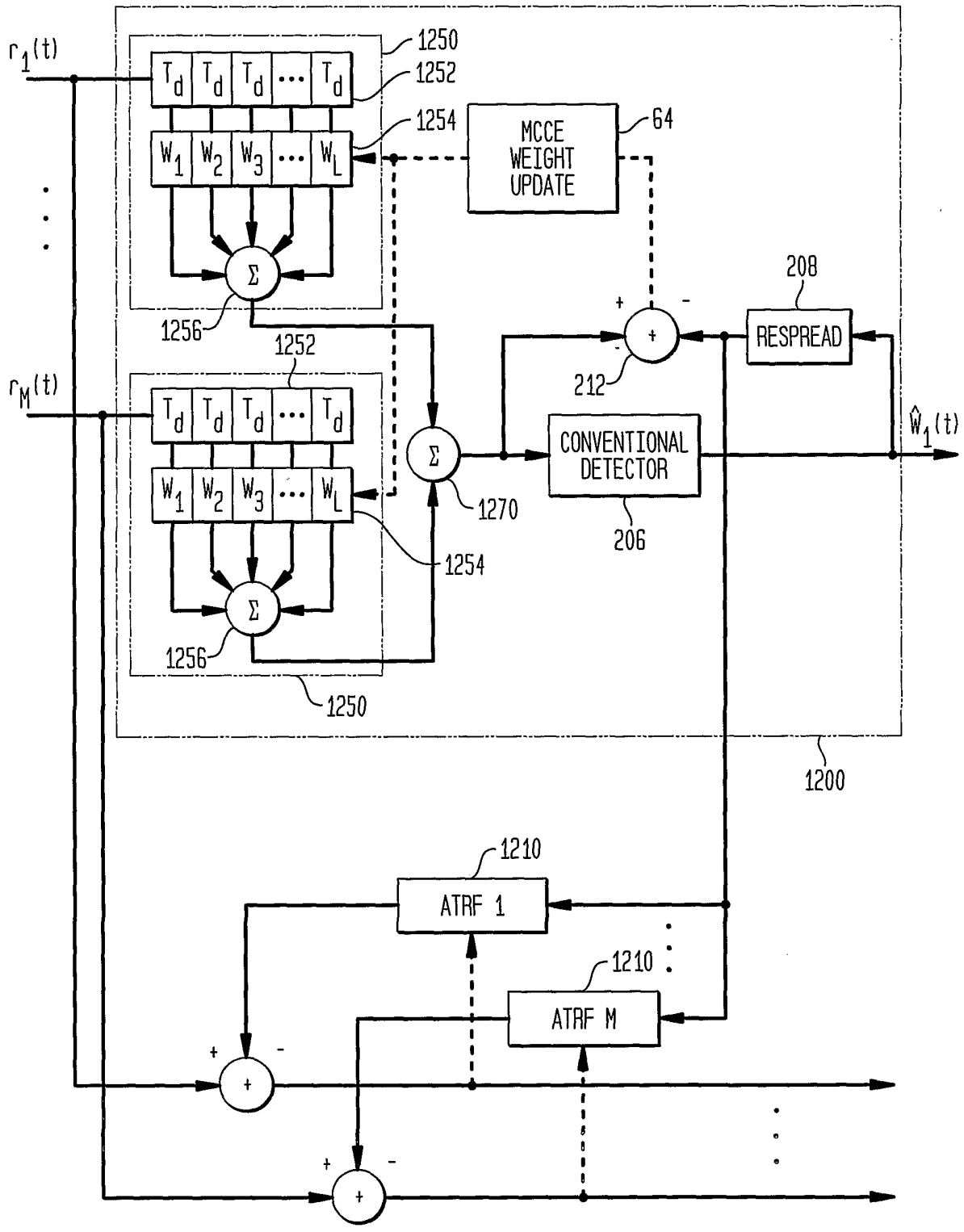

$r_1(t)$
$r_M(t)$
T_d
W_1 W_2 W_3 ... W_L
Σ
1250
1252
1254
1256
MCCE WEIGHT UPDATE
64
208
RESPREAD
212
CONVENTIONAL DETECTOR
206
1270
$\hat{W}_1(t)$
1200
1210
ATRF 1
ATRF M
+
-

FIG. 14

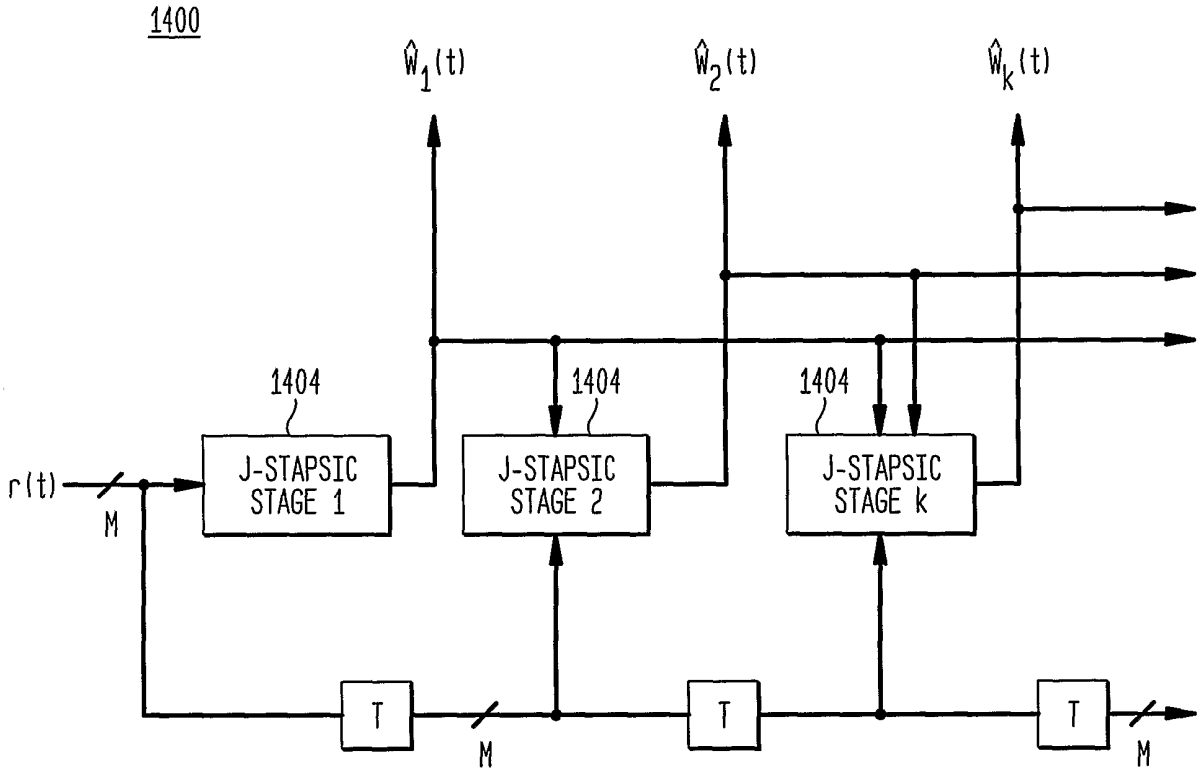
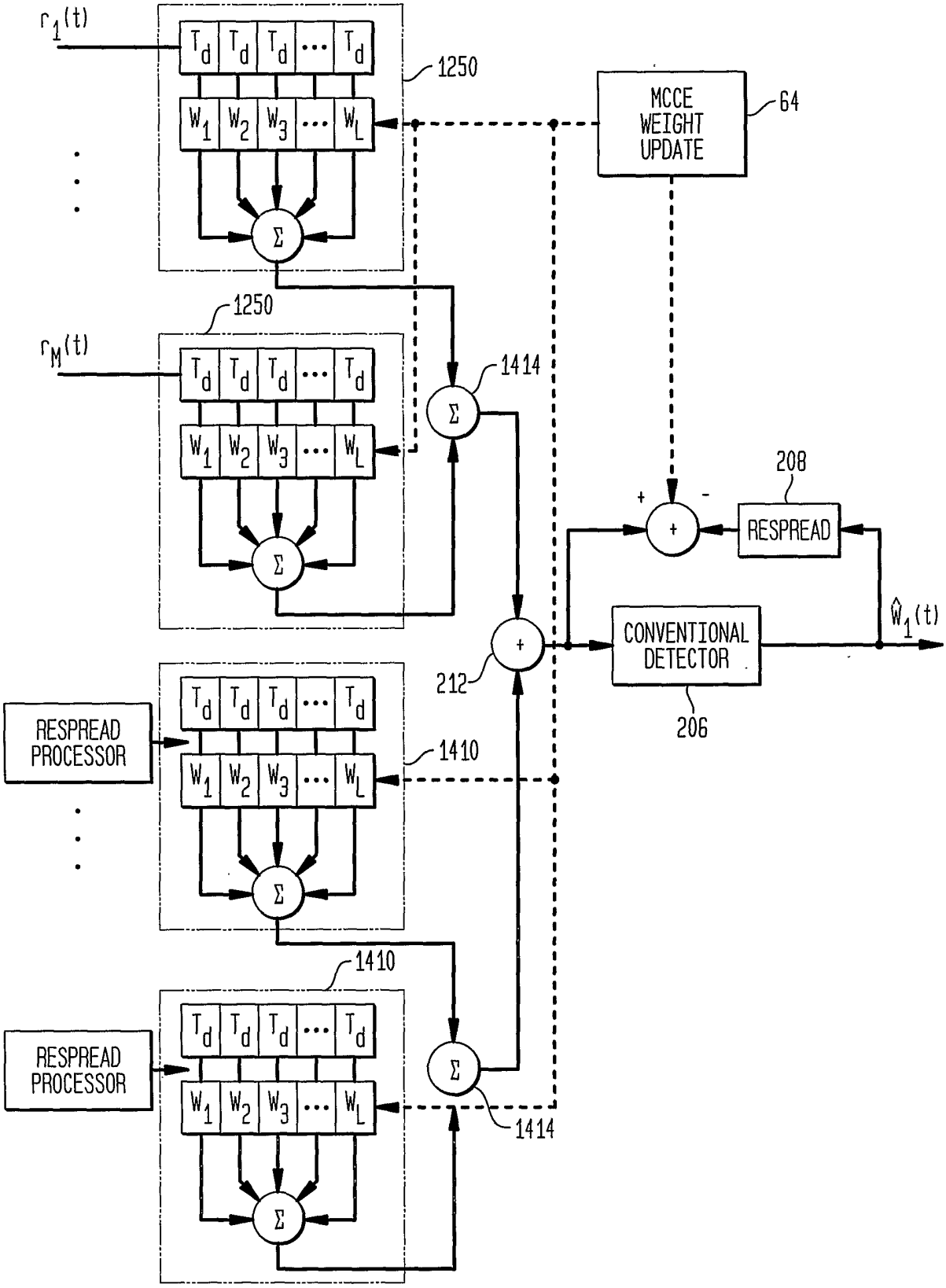

1400
$\hat{W}_1(t)$
$\hat{W}_2(t)$
$\hat{W}_k(t)$
1404
1404
1404
J-STAPSIC STAGE 1
J-STAPSIC STAGE 2
J-STAPSIC STAGE k
r(t)
M
T
T
T
M
M

FIG. 15


$r_1(t)$
$r_M(t)$
T_d
W_1 W_2 W_3 ... W_L
Σ
1250
1414
1410
MCCE WEIGHT UPDATE
64
208
RESPREAD
CONVENTIONAL DETECTOR
206
212
$\hat{W}_1(t)$
RESPREAD PROCESSOR
RESPREAD PROCESSOR