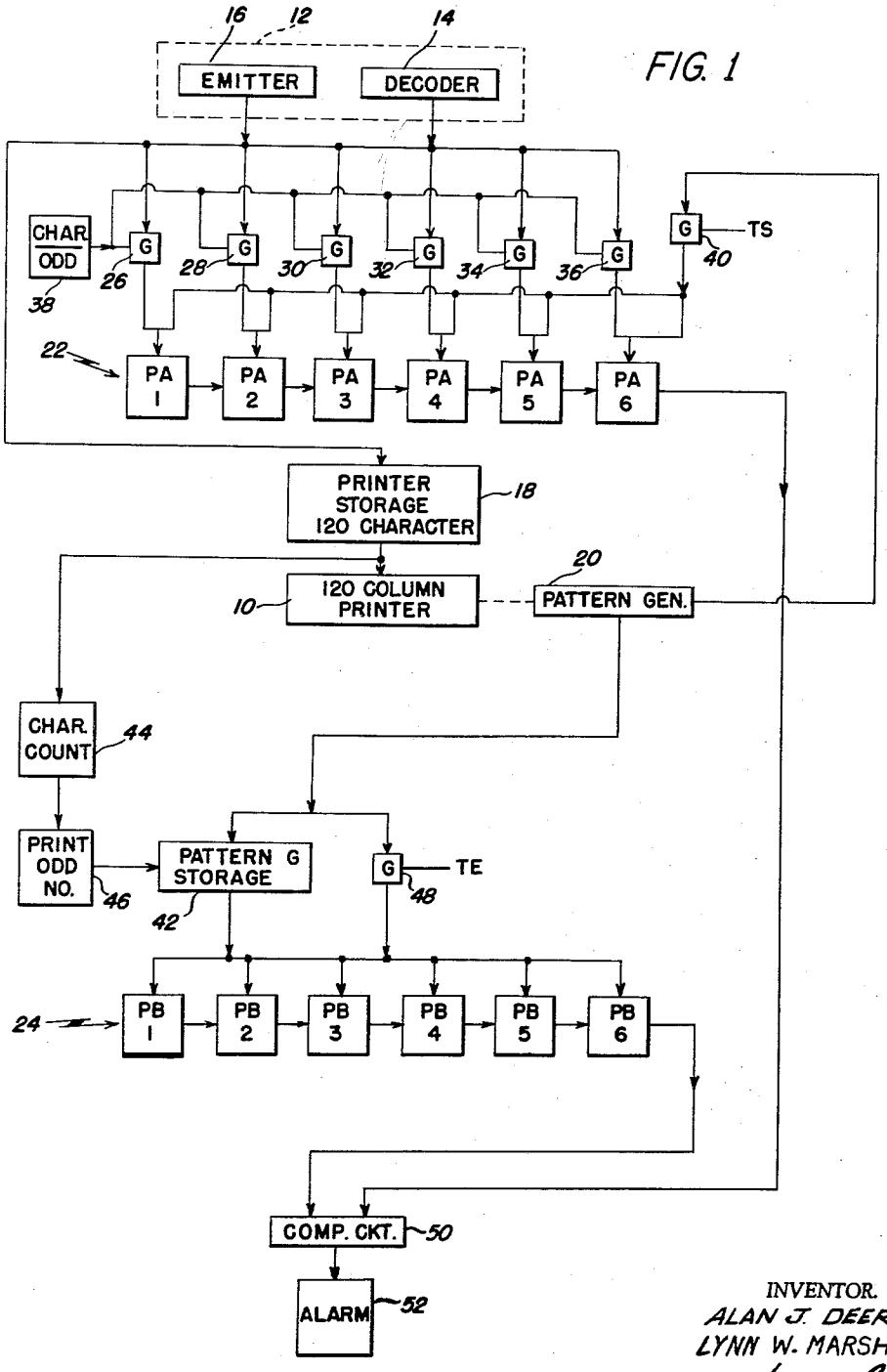
Dec. 27, 1960 A. J. DEERFIELD ET AL 2,966,113

INFORMATION HANDLING APPARATUS

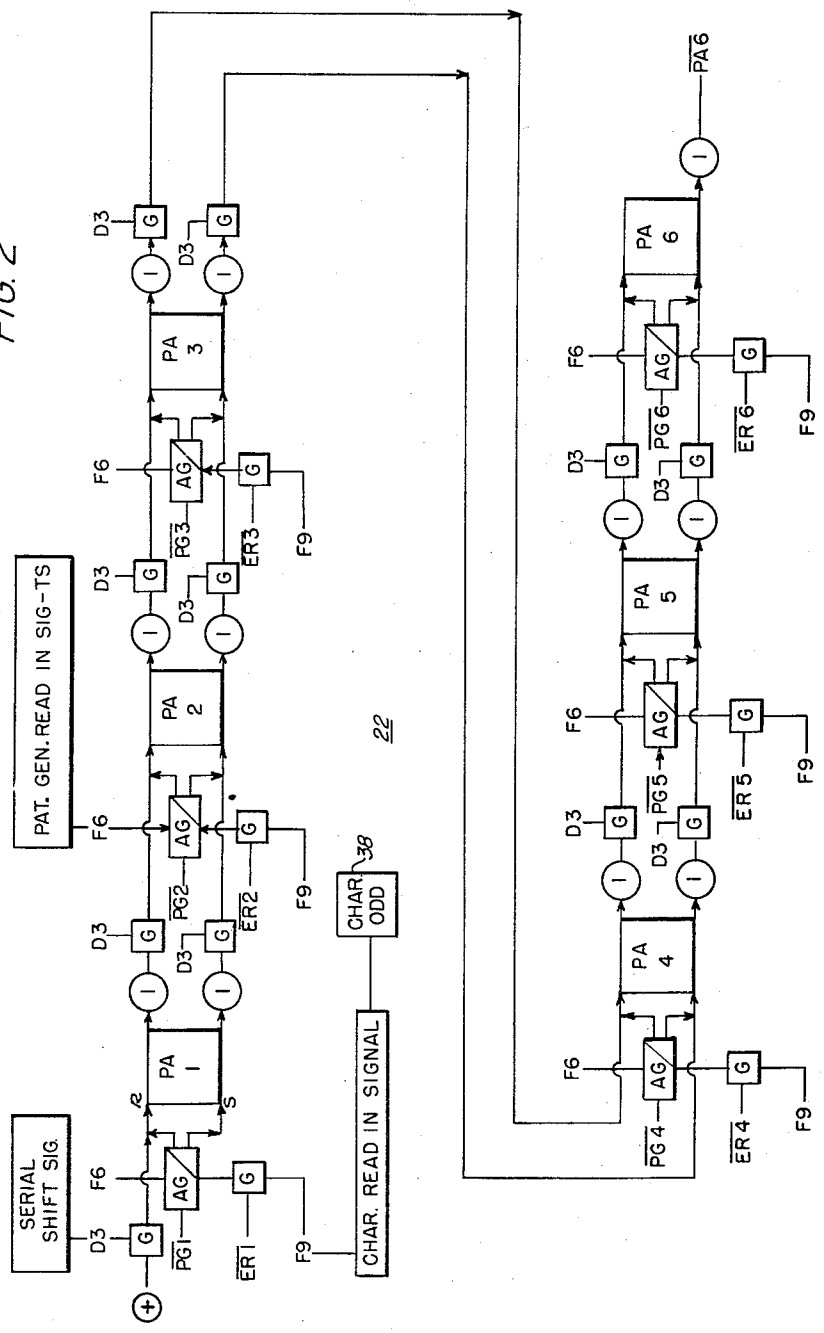
Filed Nov. 5, 1958 4 Sheets-Sheet 1

FIG. 1



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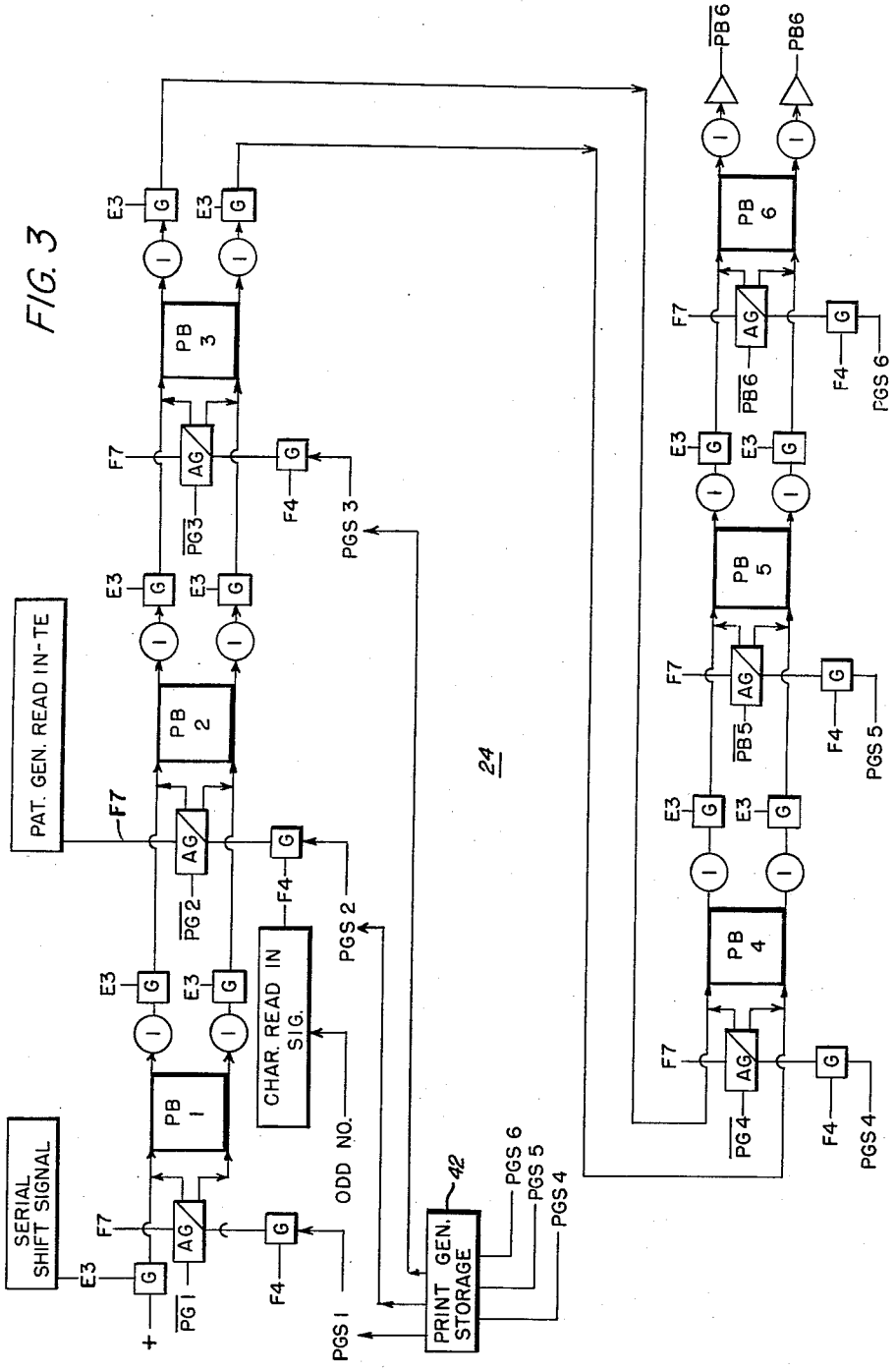
FIG. 2


SERIAL SHIFT SIG.
PAT. GEN. READ IN SIG-TS
CHAR. READ IN SIGNAL
CHAR ODD
22
38
PA 1
PA 2
PA 3
PA 4
PA 5
PA 6
AG
G
I
D3
F6
F9
PG1
PG2
PG3
PG4
PG5
PG6
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ER2
ER3
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ER5
ER6
PA6

INFORMATION HANDLING APPARATUS

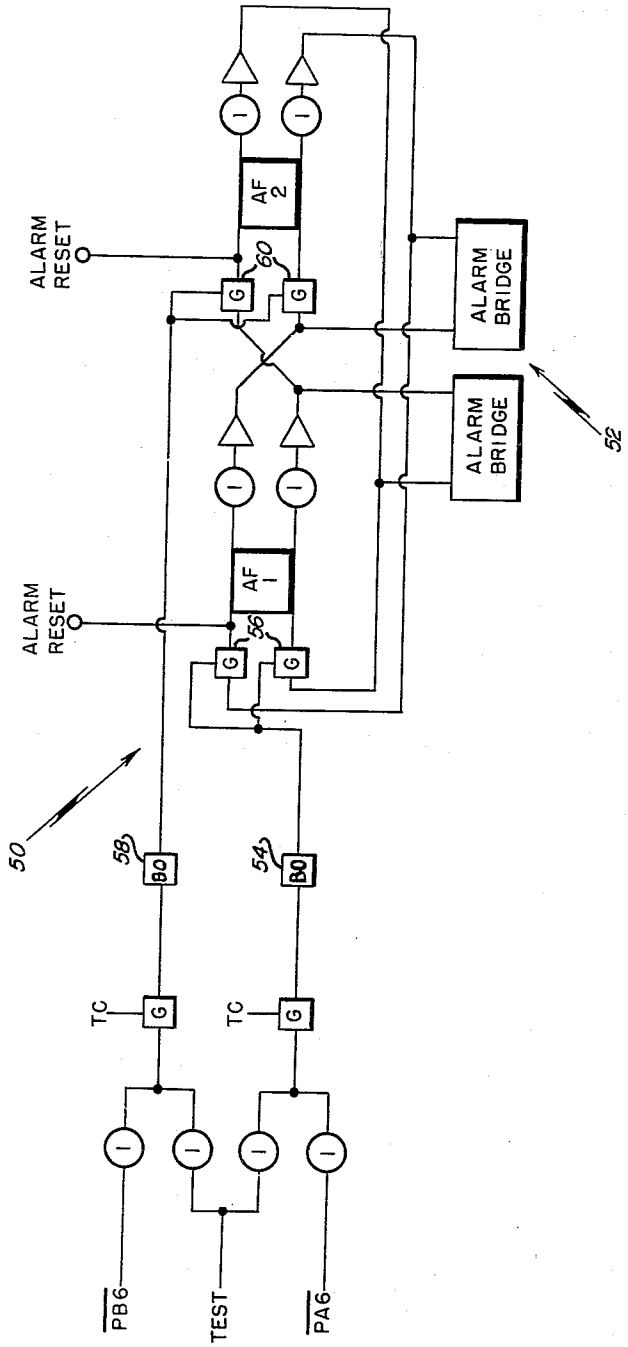
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FIG. 3



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FIG. 4



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2,966,113

INFORMATION HANDLING APPARATUS

Alan J. Deerfield, Franklin, and Lynn W. Marsh, Jr., Marblehead, Mass., assignors to Minneapolis-Honeywell Regulator Company, Minneapolis, Minn., a corporation of Delaware

Filed Nov. 5, 1958, Ser. No. 772,054

10 Claims. (Cl. 101—93)

A general object of the present invention is to provide a new and improved checking circuit for use with an information handling apparatus. More specifically, the present invention is concerned with a checking apparatus for use with a data printer or the like where such printer receives coded signals for effecting a printing operation and where coded signals are generated in a manner to represent the cyclic operation of the printer.

A typical printer to which the present invention is adapted to be used is a "line at a time" printer. Such a printer may comprise, for example, a rotating drum having a plurality of characters which are to be printed are formed on the surface of the drum in a plurality of rows and columns. A printer using a rotating drum such as this may be arranged to operate so that a paper on which the printing is to take place is positioned adjacent to the rotating drum and a plurality of hammers move in synchronism with the characters on the drum and in accordance with the characters selected to be printed to produce a suitable printed impression on the paper. A representative form of printer of this type is illustrated and described in a patent of Leo Rosen, et al., bearing Number 2,805,620, issued September 10, 1957. In such a printer, a complete line of print is normally associated with a full rotation of the drum of the printer.

In order to check the operation of the aforementioned type of printer, it has been found desirable to incorporate in the checking circuitry means for checking the start and end of each revolution of the print wheel or print drum associated with a particular printing cycle. This special checking feature is achieved in the present invention by selecting and sensing a particular character which, in effect, defines the starting of the print cycle and then again sensing the same character which defines the end of the print cycle. If the character at the start of the print cycle and the character at the end of the print cycle are the same, the check circuits will not interrupt the operation of the apparatus. In the event that there is no identity between the starting character and the ending character, an error condition will be indicated, the latter of which may be used to interrupt the operation of the apparatus.

It is therefore a still further object of the present invention to provide a new and improved checking circuit for a "line at a time" printer wherein the start and the end of a particular printing cycle are defined in terms of a unique character selected in synchronism with the operation of the printer mechanism.

Another more specific object of the present invention is to provide a new and improved checking circuit for a rotating drum type printer wherein a comparison is made between a character uniquely associated with the starting of a print cycle and a character uniquely associated with the ending of a print cycle, and wherein a comparison is made to ensure that there is the necessary relation between the two characters.

The foregoing objects and features of novelty which

characterize the invention as well as other objects of the invention are pointed out with particularity in the claims annexed to and forming a part of the present specification. For a better understanding of the invention, its advantages and specific objects attained with its use, reference should be had to the accompanying drawings and descriptive matter in which there is illustrated and described a preferred embodiment of the invention.

Of the drawings:

Figure 1 is a diagrammatic representation of the overall system circuitry associated with the present checking scheme;

Figure 2 illustrates one of the adder or accumulator circuits associated with one portion of the checking circuitry;

Figure 3 illustrates a further adder or accumulator section associated with a further portion of the present checking circuitry; and

Figure 4 illustrates circuitry which may be used for comparing the checking data stored in the two accumulators of Figures 2 and 3.

Referring first to Figure 1, the numeral 10 identifies in block form a printing device which may well be of the type described in the above mentioned Rosen et al. patent. This printer is assumed here to be a line-at-a-time printer which incorporates a rotating drum having formed on the surface thereof a plurality of characters in prearranged columns and rows. The selection of a particular character in a line of print will be made by appropriately actuated electrical hammers which effect a suitable printing of the embossed character on the surface of the drum onto a print receiving medium.

Data for actuating the printer 10 may be derived from a suitable data source 12. The data source 12 may comprise a suitable data decoder 14 which is adapted to take one preselected digital code and convert it into a code compatible with the code associated with the printer. Further, the data source may take the form of a character emitter 16 which may well be suitable circuitry manually plugged to select particular characters for printing in a manner well known in the art. The digital characters received from the emitter 16 and decoder 14 are generally stored in a suitable storage circuit 18 and arranged in a predetermined format for the particular line to be printed. In a copending application of Allan J. Deerfield et al. entitled "Information Handling Apparatus" filed November 4, 1958, and bearing Serial Number 772,053, there is disclosed circuitry which is useful in arranging the digital data for a particular line in selected fields in accordance with a predetermined manually plugged scheme. Such apparatus as disclosed in this last mentioned application is well adapted for use with the present described checking circuitry.

Once a particular line of print has been suitably stored in the printer storage circuitry 18, a print out operation commences and the characters to be printed are appropriately selected in sequence in accordance with the order in which the characters appear on the surface of the printer drum. In order to effect the desired synchronization between the operation of the print wheel or print drum, there is provided a pattern generator 20 which is adapted to produce in coded digital form characters corresponding to the characters appearing in sequence on the surface of the print wheel or drum. When there is a predetermined matching of the character generated by the pattern generator with a particular character in print storage, a signal will be supplied to the printer so that the printing may take place. A representative showing of a pattern generator operating in conjunction with the print storage circuits will be found in a copending application of Alan J. Deerfield entitled "Elec-

trical Apparatus," said application having been filed August 4, 1958, and bearing Serial Number 752,857. Reference should be made to this last mentioned application in order to understand more fully the nature of the operation of the print storage circuits and the pattern generator insofar as providing signals for driving the printer is concerned.

The digital code associated with the described circuitry is assumed to be a six bit alpha-numeric code which is capable of defining a plurality of alphabetic characters and numerical digits. The checking in the present circuitry is achieved by a pair of accumulator or adder circuits **22** and **24**. Each of these adder circuits **22** and **24** include six separate adder or accumulator stages which correspond to the six bits of the code being handled by the apparatus. Thus, the adder section **22** includes a plurality of stages PA1, PA2, PA3, PA4, PA5 and PA6. The gating of information into the adder circuit **22** is controlled by a plurality of gates **26**, **28**, **30**, **32**, **34** and **36**. The controlling of the gates **26** through **36** is achieved by way of suitable signal source **38** which is adapted to open the gates so long as an odd number of characters are being processed insofar as any one particular character is concerned. The other inputs to the gating sections **26** through **36** are derived from either the emitter **16** or the decoder **14** and will take the form of a six bit code representing a character which is to be processed.

In one embodiment of the invention, the adder stages PA1 through PA6 each were adder or accumulator stages operating modulo 2. Each stage, as illustrated, is adapted to operate on a different level of the six levels in the code and thereby accumulate, modulo 2, a number of bits that are processed through the input gates **26** through **36**. As long as an odd number of characters are being processed of any particular character, the gating circuits **26** through **36** are open. If an even number of characters are processed insofar as a particular character is concerned, the gates **26** through **36** are not opened. The reason for this will be apparent when it is noted that the adding of the bit positions of an even number of characters having the same code will result in no change in the setting of the modulo 2 adder sections PA1 through PA6.

An additional code pattern is adapted to be gated into the adder stages **22** by way of the gate **40**. The character associated with the gating circuit **40** will be a character derived from the pattern generator **20** and is adapted to be selectively gated into the adder **22** at an appropriate time TS which is directly related to the print cycle of the printer **10**.

The adder **24**, considered more specifically, comprises six adder or accumulator stages PB1, PB2, PB3, PB4, PB5, and PB6. Each of these adder stages is adapted to operate or accumulate modulo 2 in the corresponding level of the bit positions of the characters applied to the input thereof. The input characters are derived from the pattern generator **20** and are appropriately gated into the adder stages from a pattern generator storage circuit **42**. The gating in the pattern generator storage circuit is controlled by a suitable counter circuit **44** which is connected to count the number of any particular character that has been printed in the course of a print out at the printer **10**. If an odd number of characters had been printed, a gating signal source **46** produces a signal indicating that the particular character in the pattern generator storage circuit should be inserted into the adder **24**.

A further gating circuit **48** is adapted to gate a character into the adder circuits **24** from the pattern generator **20**. This gating circuit **48** is controlled by a timing signal TE which defines the end of a particular print cycle.

After a particular print cycle has been completed, it is desired that a comparison be made between the accumulated results in the adders **22** and **24**. For this comparison, there is provided a suitable comparison circuit **50** which is adapted to receive data shifted serially, and simultaneously, from the adder circuits **22** and **24**. In the event that the results in the two adder circuits **22** and **24** are not identical, the comparison circuitry **50** will provide a suitable signal for actuating an alarm **52**.

Referring next to Figure 2, the detail of the adder or accumulator circuit **22** is illustrated in logical form. Here, the individual adder stages PA1 through PA6 are illustrated as binary flip-flops which are adapted to operate modulo 2 in an accumulating sense with respect to bits that are applied to their inputs. Each of the accumulator stages PA1 through PA6 has on its input an accumulator gate AG. By definition, this accumulator gate is adapted to produce an output to change the binary state of the associated flip-flop PA if there is an F6 timing signal in combination with a print generator signal PG. Further, connected to the accumulator gate is a second gate having a timing signal F9 applied thereto as well as a signal representing a particular bit position from an emitter register ER. The timing signal F9 is directly related to the timing for drop-in of a character from the input character register ER.

In order to shift the information out of the register, there are provided a plurality of gates having as the shift signals therefor a timing signal D3. The D3 timing signals are applied to the input gates on all of the coupling lines between the respective PA stages so that when the D3 signals are applied the information in the stages may be shifted serially from the low order stage PA1 out through the high order stage PA6 and then to the comparison circuitry illustrated in connection with Figure 4.

During the normal transfer of characters from the input source **12**, of Figure 1, into the printer storage circuit **18**, the information will be handled a character at a time and these characters will, in the course of the transfer, be inserted into the adder stage **22** by way of the ER inputs and the gates having the character readin signal F9 applied thereto. The signals passed through the respective input gates and the accumulator gates will then be applied to the stages PA1 through PA6 in accordance with whether or not a one may exist in any particular code position or bit position of the character being processed. If an odd number of characters are being processed, as indicated by a signal from the circuit **38**, the F9 signal will be present and the character, of which there are an odd number, will be dropped into the stages PA1 through PA6 in accordance with the particular code for that character. If there were an even number of characters, the F9 timing signal will not open the respective gates for the register inputs ER and consequently the character will not be inserted into the respective PA adder stages.

At the start of any particular printer cycle, the print wheel or print drum on the printer **10** may have a predetermined character in print position. At the time that it is desired to start a printing cycle, the particular character which is then in a printing position may be selected to define the start of the printing cycle. The timing signal TS will be used to create the signal F6 shown in Figure 2 which will permit the insertion into the stages PA1 through PA6 of the particular character in the printing position as indicated by the output of the print or pattern generator **20**.

The circuitry of Figure 3 illustrates the logical detail of the added stage **24** associated with the output of the printer. This adder stage is basically the same as that of the adder stage **22** as illustrated in Figure 2 and will be seen to comprise a series of six flip-flops PB1 through PB6 connected with input gates corresponding to the input gates used in Figure 2. In Figure 3, the serial shift signal source is a signal E3 and this signal is utilized for shifting serially the data which has been accumulated in the respective adder sections PB1 through PB6 to the output terminals of the high order stage PB6 and thence to the adder comparison circuits of Figure 4.

The timing signal associated with the character readin from the pattern generator storage register **42** produces the signal F4. This timing signal is appropriately synchronized with the operation of the print generator storage circuit **42** so that when a predetermined character has been selected and resides in the print generator storage circuit **42**, the character can then be inserted into the adder circuits illustrated in Figure 3. This insertion will be by way of the accumulator gates AG on the input of the respective adder stages PB.

At the end of a printer cycle, the timing signal TE, as illustrated in Figure 1, creates the pattern generator readin signal F7. This F7 signal acts on the respective accumulator gate AG and will permit the gating in of the pattern generator signals PG into the respective stages in accordance with their level in the code. If the circuit has operated properly, the character from the pattern generator dropped into the adder circuit **22** in Figure 2 at time TS will be the same character as is dropped into the adder circuit **24** at the end of the cycle as defined by the timing signal TE.

It will thus be seen that if the character has been inserted in both of the adder circuits of Figure 2 and Figure 3, even though at different times, the net result in the adders should not be different at the time that a readout is effected to the comparison circuits of Figure 4.

Referring to Figure 4, there is here illustrated a representative checking circuitry in which it is possible to make a comparison of the outputs of the adders **22** and **24** of Figures 2 and 3 respectively. The inputs are applied by way of the terminals $\overline{PB6}$ and $\overline{PA6}$ and are appropriately combined with a test signal and applied to a pair of gates having a timing check signal TC applied thereto. For each bit serially shifted out of the adder circuit **22**, a bit will be passed through to a blocking oscillator **54**, the latter of which supplies a signal to a pair of gating circuits **56** on the input of a flip-flop AF1.

The output of the adder **24** of Figure 3 which takes the form of a $\overline{PB6}$ signal will create a pulse in a blocking oscillator circuit **58** when each one bit is transferred. The output of this blocking oscillator will be applied to a pair of gates **60** on the input of a flip-flop AF2.

The outputs of the flip-flop AF1 are connected to input gate legs on the gates **60** while the outputs of the flip-flops AF2 are connected to the input gate legs of the gate **56** on the input of the flip-flop AF1. The outputs of the two flip-flops each include a pair of inverters which condition the signals for proper solarity relationship with respect to the inputs of the opposite pair.

In operation, the flip-flops AF1 and AF2 are normally switched into the reset state after the alarm reset has been actuated. Each time that the signal TC is present to condition the input of the circuit for the passing of the outputs of the two adder circuits **22** and **24**, each bit received in the respective blocking oscillators **54** and **58** produce pulses on the gating circuits of the two flip-flops so that they will alternately switch from one stable state to the opposite stable state each time a pulse is received. In the event that there should be a lack of time identity of the pulses received from the two adders, one of the flip-flops will be switched while the other will not. Should this event occur, an appropriate alarm circuit is connected to the outputs of the two flip-flops and will produce a suitable indication of the fact that an error condition exists. The alarm bridge circuits may well be of the type illustrated in the above mentioned copending application of Alan J. Deerfield. It will be apparent, however, that other forms of comparison checking circuits may be used to check the identity of the sums that have been accumulated in the respective adder stages in the adders **22** and **24**.

Considering next the overall system operation insofar as the checking circuit is concerned, it is assumed first that, referring to Figure 1, the adder circuits **22** and **24** are each reset to a predetermined state.

Information which is to be printed in the particular line of print will be derived either from the decoder circuit **14** or the emitter **12** until the appropriate storage circuits for the printer have been loaded to define a particular line of print. As soon as a particular line of print has been established, the printer will begin to operate and upon receipt of the print cycle start signal TS, the first character of the print wheel will be dropped into the adder **22** by way of the accumulator gates AG as discussed in connection with Figure 2.

During the time that the characters are being transferred into the printer storage circuit **18**, the respective characters, when the number of any particular character is odd, will be dropped into the adder circuits of the adder **22** where the corresponding bits, where a one is present, will be added modulo 2.

As the printer operates after the timing cycle or the printing cycle has been initiated, for each character printed, where the number of characters is odd, the corresponding character produced by the pattern generator, and stored in the pattern generator storage circuit **42**, will be dropped into the adder circuits **24** where again corresponding bit positions will be added modulo 2 in the respective stages of the adder.

At the end of the printing cycle, the last character up on the print wheel should correspond to the first character which was dropped into the adder **22** by the timing signal TS. Consequently, when the TE signal signifying the end of the timing period has been received at the gate **48**, the character signals from the pattern generator will be dropped into the adder circuits **24** in the manner discussed above in connection with Figure 3.

After the characters associated with a particular line of print have been selected and processed by the printer, the checking operation will be completed by generating serial shift signals in the manner discussed in connection with Figure 2 and Figure 3 whereby the accumulated totals in the adder circuits are shifted serially out to the comparison circuits of Figure 4. As pointed out above, as long as there is a corresponding bit by bit relationship existing between the bits in the two adder stages, no error will be indicated. However, if for any reason there is not a correspondence of bits from the outputs of the two adder circuits, either due to a lack of information correspondence or a circuit failure, the alarm bridge will become unbalanced and the alarm circuits will operate.

It will be apparent from the foregoing description that the coded information received at the input of the circuit is in the form of a multi-bit code. In the process of converting this code for use with the printer, a single pulse at a selected time is generated to effect the printing operation. This single pulse is then used to recreate the information in multi-bit coded form so that the entire operation may be checked on a bit-by-bit basis. This check then provides for a very accurate check of the entire data manipulation even though the identity of the original code is effectively lost in the process.

From the foregoing description it will also be readily apparent that the present apparatus provides an accurate check of the transfer of data to an input selection source to an output device on a bit-by-bit basis. Further, the apparatus provides for checking to insure that in any particular print cycle that the print wheel associated with the printing operation has traversed through a single cycle. By utilizing this new and improved checking circuitry, it is possible to achieve a higher degree of accuracy in data manipulating problems, and particularly manipulating problems associated with the operation of a printer.

While, in accordance with the provisions of the statutes, there has been illustrated and described the best forms of the invention known, it will be apparent to those skilled in the art that changes may be made in the apparatus described without departing from the spirit of the invention as set forth in the appended claims and that in some

cases, certain features of the invention may be used to advantage without a corresponding use of other features.

Having now described the invention, what is claimed as new and novel and for which it is desired to secure by Letters Patent is:

1. Apparatus for checking the operation of a data printer comprising a character signal source adapted to have multi-bit characters on the output thereof, a printer adapted to print a plurality of like characters at the same time, said printer comprising a drum having a predetermined number of characters on the peripheral surface thereof, a print character generator connected to be synchronized with the operation of said printer, a first adder connected to said character signal source, a second adder connected to said print character generator, said first and second adders adding bit positions in each character received from the respective character sources, means connecting said print character generator to one of said adders at the start of each print cycle, means connecting said print character generator to the other of said adders at the end of each print cycle, and checking means connected to said first and second adders to check the sums in said adders for correspondence at the end of each print cycle.

2. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character selection signal source, circuit means coupling said signal source to said printer to selectively print the characters on said printer, a character signal generating means sensing the characters printed by said printer, a first character bit adder connected to said character selection signal source, timing means connecting said character signal generating means to said first adder at the start of each print cycle, a second character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said second adder at the end of each print cycle, and adder comparison means connected to said first and second adders to compare the sums therein after the end of each print cycle.

3. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character selection signal source, a first multiple character sensing means producing a control signal indicative of the presence of an even multiple number of characters from said selection signal source, circuit means coupling said signal source to said printer to selectively print the characters on said printer, a character signal generating means sensing the characters printed by said printer, a first character bit adder connected to said character selection signal source, means connecting said first multiple character sensing means to said first adder to inhibit said adder upon the presence of said control signal, timing means connecting said character signal generating means to said first adder at the start of each print cycle, a second character bit adder connected to said character signal generating means, a second multiple character sensing means producing a second control signal indicative of the presence of an even number of a particular character having been printed by said printer, means connecting said second multiple character sensing means to said second adder to inhibit said second adder in the event an even number of a particular character have been printed, timing means connecting said character signal generating means to said second adder at the end of each print cycle, and adder comparison means connected to said first and second adders to compare the sums therein after the end of each print cycle.

4. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character selection signal source, circuit means coupling said signal source to said printer to selectively print the characters on said printer, a character signal generating means sensing the characters printed by said printer, a first modulo 2 character bit adder connected to said character selection signal source, timing means connecting said character signal generating means to said first adder at the start of each print cycle, a second modulo 2 character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said second adder at the end of each print cycle, and adder comparison means connected to said first and second adders to compare the sums therein after the end of each print cycle.

5. Apparatus for checking the operation of a data printer comprising a print character generator connected to be synchronized with the operation of said printer, a first adder, a second adder, said first and second adders being adapted to add the bit positions in a character received from said character generator, means connecting said print character generator to one of said adders at the start of each print cycle, means connecting said print character generator to the other of said adders at the end of each print cycle, and checking means connected to said first and second adders to check the sums in said adders for correspondence at the end of each print cycle.

6. Apparatus for checking the operation of a data printer comprising a print character generator connected to be synchronized with the operation of said printer, a first storage circuit, a second storage circuit, means connecting said print character generator to one of said circuits at the start of each print cycle, means connecting said print character generator to the other of said circuits at the end of each print cycle, and checking means connected to said first and second storage circuits to check the data in said circuits for correspondence at the end of each print cycle.

7. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character signal generating means sensing the characters printed by said printer, a first character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said first adder at the start of each print cycle, a second character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said second adder at the end of each print cycle, and adder comparison means connected to said first and second adders to compare the sums therein after the end of each print cycle.

8. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character signal generating means connected to said printer, a first character bit storage means connected to said character signal generating means, timing means connecting said character signal generating means to said first storage means at the start of each print cycle, a second character bit storage means connected to said character signal generating means, timing means connecting said character signal generating means to said second storage means at the end of each print cycle, and comparison means connected to said first and second storage means to compare the data therein after the end of each print cycle.

9. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character signal generating means connected to operate synchronously with said printer, a printer operational checking circuit including a signal comparison means, and means including timing means having a signal only at the start and end of a print cycle for connecting said character signal generating means to said checking circuit at the start and end of each print cycle to determine if the character from said signal generating means at the start of a print cycle is the same as the character from

said signal generating means at the end of the print cycle.

10. In combination, a printer comprising a rotating drum having a plurality of characters formed on the periphery thereof in prearranged rows and columns, a character signal generating means connected to operate synchronously with said printer, a first modulo 2 character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said first adder at the start of each print cycle, a second modulo 2 character bit adder connected to said character signal generating means, timing means connecting said character signal generating means to said second adder at the end of each print cycle, and adder comparison means connected to said first and second adders to compare the sums therein after the end of each print cycle.

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