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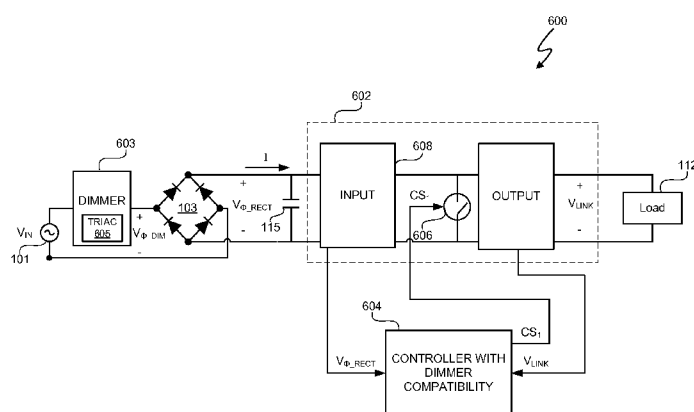
(54) Title: SWITCHING POWER CONVERTER CONTROL WITH TRIAC-BASED LEADING EDGE DIMMER COMPATI-
BILITY

Figure 6

(57) Abstract: In at least one embodiment, a controller allows triac -based dimmer to properly function and dim a load whose voltage is regulated by a switching power converter. In at least one embodiment, the switching power converter includes a switch to control voltage conversion of an input voltage to the switching power converter, wherein phase delays are introduced in the input voltage by a triac -based dimmer during a dimming period. In at least one embodiment, the controller is configured to control the switch of the switching power converter to establish an input resistance of the switching power converter during a dimming portion of the input voltage, wherein the input resistance allows the triac -based dimmer to phase modulate a supply voltage to the dimmer so that an output voltage of the dimmer has a substantially uninterrupted phase delay during each half-cycle of the supply voltage during the dimming period.

**SWITCHING POWER CONVERTER CONTROL WITH TRIAC-BASED
LEADING EDGE DIMMER COMPATIBILITY**

CROSS REFERENCE TO RELATED APPLICATIONS

(1) U.S. Patent Application No. 11/967,269, entitled “Power Control System Using a Nonlinear Delta-Sigma Modulator with Nonlinear Power Conversion Process Modeling,” inventor John L. Melanson, Attorney Docket No. 1745-CA, and filed on December 31, 2007 describes exemplary methods and systems and is incorporated by reference in its entirety. Referred to herein as Melanson I.

(2) U.S. Patent Application No. 11/967,271, entitled “Power Factor Correction Controller with Feedback Reduction,” inventor John L. Melanson, Attorney Docket No. 1756-CA, and filed on December 31, 2007 describes exemplary methods and systems and is incorporated by reference in its entirety. Referred to herein as Melanson II.

(3) U.S. Patent Application No. 11/967,273, entitled “System and Method with Inductor Flyback Detection Using Switch Date Charge Characteristic Detection,” inventor John L. Melanson, Attorney Docket No. 1758-CA, and filed on December 31, 2007 describes exemplary methods and systems and is incorporated by reference in its entirety. Referred to herein as Melanson III.

(4) U.S. Patent Application No. 11/967,275, entitled “Programmable Power Control System,” inventor John L. Melanson, Attorney Docket No. 1759-CA, and filed on December 31, 2007 describes exemplary methods and systems and is incorporated by reference in its entirety. Referred to herein as Melanson IV.

(5) U.S. Patent Application Serial No. 11/967,272, entitled "Power Factor Correction Controller With Switch Node Feedback", inventor John L. Melanson, Attorney Docket No. 1757-CA, and filed on December 31, 2007 describes exemplary methods and systems and is incorporated by reference in its entirety. Referred to herein as Melanson V.

BACKGROUND OF THE INVENTION

Field of the Invention

(6) The present invention relates in general to the field of signal processing, and more specifically to a system and method that includes switching power converter control with triac-based leading edge dimmer compatibility.

DESCRIPTION OF THE RELATED ART

(7) Power control systems often utilize a switching power converter to convert alternating current (AC) voltages to direct current (DC) voltages or DC-to-DC. Power control systems often provide power factor corrected and regulated output voltages to many devices that utilize a regulated output voltage. Switching power converters have been used as interfaces between triac-based dimmers and loads. The load can be virtually any load that utilizes converted power, such as one or more light emitting diodes (LEDs).

(8) LEDs are becoming particularly attractive as main stream light sources in part because of energy savings through high efficiency light output and environmental incentives such as the reduction of mercury. LEDs are semiconductor devices and are driven by direct current. The lumen output intensity (i.e. brightness) of the LED approximately varies in direct proportion to the current flowing through the LED. Thus, increasing current supplied to an LED increases the intensity of the LED and decreasing current supplied to the LED dims the LED. Current can be modified by either directly reducing the direct current level to the white LEDs or by reducing the average current through duty cycle modulation.

(9) Dimming a light source saves energy when operating a light source and also allows a user to adjust the intensity of the light source to a desired level. Many facilities, such as homes and buildings, include light source dimming circuits (referred to herein as “dimmers”). Power control systems with switching power converters are used to control constant current light sources. However, conventional dimmers, such as a triac-based dimmer, that are designed for use with resistive loads, such as incandescent light bulbs, often do not perform well when supplying a raw, phase modulated signal to a reactive load such as a switching power converter.

(10) Figure 1 depicts a power control system 100, which includes a switching power converter 102. Voltage source 101 supplies an AC supply voltage V_{IN} to a triac-based dimmer 104. The voltage source 101 is, for example, a public utility, and the supply voltage V_{IN} is, for example, a 60 Hz/110 V line voltage in the United States of America or a 50 Hz/220 V line voltage in Europe. Dimmer 104 receives the supply voltage V_{IN} and generates a dimmer voltage V_{Φ_DIM} . During a dimming period, dimmer 104 phase modulates the supply voltage V_{IN} by introducing phase delays α into the beginning of each half cycle of dimmer voltage V_{Φ_DIM} . “ α ” represents an amount of time between the beginning and leading edge of each half cycle of dimmer voltage V_{Φ_DIM} . (“Introducing phase delays” is also referred to as “chopping”). The portion of the dimmer voltage V_{Φ_DIM} having a phase delay α is referred to as the “dimming portion”. As subsequently described in more detail, the amount of phase delay α depends upon the amount of selected dimming. When dimmer 104 is not in a dimming period, i.e. dimmer 104 is not set to phase modulate the supply voltage V_{IN} , the phase delay α is zero, and dimmer 104 simply passes the supply voltage V_{IN} to full bridge diode rectifier 103. Rectifier 103 rectifies the dimmer voltage V_{Φ_DIM} and supplies a rectified, time-varying, line input voltage V_{Φ_RECT} to the switching power converter 102.

(11) The power control system 100 includes a PFC and output voltage controller 114 to control power factor correction and regulate an output voltage V_{LINK} of switching power converter 102. The PFC and output voltage controller 114 controls an ON (i.e. conductive) and OFF (i.e. nonconductive) state of switch 108 by varying a state of pulse width modulated control signal CS_0 . Switching between states of switch 108 regulates the transfer of energy from the rectified line input voltage V_{Φ_RECT}

through inductor 110 to capacitor 106. The inductor current i_L ramps ‘up’ when the switch 108 is ON. The inductor current i_L ramps down when switch 108 is OFF and supplies current i_L to recharge capacitor 106. The time period during which inductor current i_L ramps down is commonly referred to as the “inductor flyback time”.

During the inductor flyback time, diode 111 is forward biased. Diode 111 prevents reverse current flow into inductor 110 when switch 108 is OFF. In at least one embodiment, the switching power converter 102 operates in discontinuous current mode, i.e. the inductor current i_L ramp up time plus the inductor flyback time is less than the period of the control signal CS_0 . When operating in continuous conduction mode, the inductor current i_L ramp-up time plus the inductor flyback time equals the period of control signal CS_0 .

(12) The switch 108 is a field effect transistor (FET), such as an n-channel FET. Control signal CS_0 is a gate voltage of switch 108, and switch 108 conducts when the pulse width of CS_0 is high. Thus, the ‘ON time’ of switch 108 is determined by the pulse width of control signal CS_0 .

(13) Capacitor 106 supplies stored energy to load 112. The capacitor 106 is sufficiently large so as to maintain a substantially constant output voltage V_{LINK} , as established by PFC and output voltage controller 114. As load conditions change, the output voltage V_{LINK} changes. The PFC and output voltage controller 114 responds to the changes in output voltage V_{LINK} and adjusts the control signal CS_0 to restore a substantially constant output voltage V_{LINK} as quickly as possible. Power control system 100 includes a small, filter capacitor 115 in parallel with switching power converter 102 to filter any high frequency signals from the input voltage V_{Φ_RECT} .

(14) The goal of power factor correction technology is to make the switching power converter 102 appear resistive to the voltage source 101. Thus, PFC and output voltage controller 114 attempts to control the inductor current i_L so that the average inductor current i_L is linearly and directly related to the line input voltage V_{Φ_RECT} . Prodić, *Compensator Design and Stability Assessment for Fast Voltage Loops of Power Factor Correction Rectifiers*, IEEE Transactions on Power Electronics, Vol. 22, No. 5, Sept. 2007, pp. 1719-1729 (referred to herein as “Prodić”), describes an example of PFC and output voltage controller 114.

(15) In at least one embodiment, the values of the pulse width and duty cycle of control signal CS_o depend on sensing two signals, namely, the input voltage V_{Φ_RECT} and the capacitor voltage/output voltage V_{LINK} . PFC and output voltage controller 114 receives the input voltage V_{Φ_RECT} and the output voltage V_{LINK} respectively via a wide bandwidth current loop 116 and a slower voltage loop 118. The input voltage V_{Φ_RECT} is sensed from node 120 between the diode rectifier 103 and inductor 110. The output voltage V_{LINK} is sensed from node 122 between diode 111 and load 112. The current loop 116 operates at a frequency f_c that is sufficient to allow the PFC and output voltage controller 114 to respond to changes in the line input voltage V_{Φ_RECT} and cause the inductor current i_L to track the input voltage V_{Φ_RECT} to provide power factor correction. The current loop frequency is generally set to a value between 20 kHz and 130 kHz. The voltage loop 118 operates at a much slower frequency f_v , typically 10-20Hz. By operating at 10-20Hz, the voltage loop 118 regulates slow variations in the output voltage V_{LINK} due to AC line voltage fluctuations in amplitude.

(16) Figure 2 (labeled prior art) depicts a triac-based power and dimming system 200 that includes a triac-based dimmer 202. Potentiometer 204 conducts current I to charge capacitor 206. During a dimming period, diac 208 blocks current to triac 210 until capacitor 206 reaches a breakover voltage of diac 208. When capacitor 206 reaches the breakover voltage, diac 208 conducts, and capacitor 206 discharges through diac 208. When capacitor 206 discharges, capacitor 206 supplies a current to triac 210, and triac 210 conducts. The time between when the supply voltage V_{IN} crosses zero and when the triac 210 conducts represents the phase delay α of dimmer voltage V_{Φ_DIM} . The resistance of potentiometer 204 sets the value of phase delay α . The resistance R of potentiometer 204 and capacitance C of capacitor 206 form an RC time constant that determines a phase delay α (Figure 3) of dimmer voltage V_{DIM} . Increasing R increases the phase delay α , and decreasing R decreases the phase delay α . When R is decreased sufficiently, the phase delay α is essentially zero, and, thus, $V_{\Phi_DIM} = V_{IN}$. The value of R is set by potentiometer 204. The value of C and the range of R are matters of design choice.

(17) When the phase delay α is zero, dimmer 202 stops dimming. In at least one embodiment, when dimmer 202 is dimming and the supply voltage V_{IN} reaches 0,

diac 208 and triac 210 stop conducting. When dimming, the alternating conduction/nonconduction of triac 210 modulates the phase of the supply voltage V_{IN} . Resistor 214, capacitor 216, and inductor 218 provide high frequency rejection for dimmer 202.

(18) Referring to Figures 1 and 2, controller 114 operates switch 108 to provide power factor correction so that input current i_L tracks changes in input voltage V_{Φ_RECT} . In at least one embodiment, when the input voltage V_{Φ_RECT} approaches a zero crossing, a very low input resistance is presented. Presenting a very low input resistance to a triac-based dimmer 104 can cause the triac 210 to turn ON and OFF multiple times during a single half cycle of input voltage V_{Φ_RECT} . As discussed in more detail below, oscillations in the conduction of triac 210 during a single half cycle of input voltage V_{Φ_RECT} can cause problems, such as flicker in a lamp when load 112 includes a lamp.

(19) Figure 3 depicts a series of *ideal* voltage waveforms 300 that represent two respective cycles of waveforms present in an *ideal* power and dimming system 200 during two dimming periods. Referring to Figures 1, 2, and 3, supply voltage V_{IN} is a sine wave depicted with two exemplary cycles 302 and 304. Dimmer 104 generates the phase modulated voltage V_{Φ_DIM} by chopping each half cycle of supply voltage V_{IN} to *ideally* generate one, leading edge phase delay α_1 for each respective half cycle of cycle 306. The phase delays α of the phase modulated signal V_{Φ_DIM} increase as the dimming level increases, i.e. as phase delays α increase, less power is delivered to load 112. If load 112 is a lamp, dimming level increases correspond to decreases in brightness of the lamp. Half cycle 308 indicates a longer phase delay α_2 corresponding to a decrease in dimming level. The exemplary leading edge phase delays α_1 and α_2 represent the elapsed time between a beginning of a half cycle and a leading edge of dimmer voltage V_{Φ_DIM} . The cycles 310 and 312 of rectified input voltage V_{Φ_RECT} have the same respective phase delays α_1 and α_2 as the phase modulated signal V_{Φ_DIM} . The phase delayed portions of voltages V_{Φ_DIM} and V_{Φ_RECT} represented by α_1 and α_2 are also referred to as the “dimming portion” of voltages V_{Φ_DIM} and V_{Φ_RECT} .

(20) As previously mentioned, conventional dimmers, such as triac-based dimmer 202, that are designed for use with resistive loads, such as incandescent light bulbs, often do not perform well when supplying a phase modulated signal V_{Φ_DIM} to a reactive load such as switching power converter 102. For example, when supplying a reactive load, the dimmer 202 can miss generating phase delays in some cycles of phase modulated signal V_{Φ_DIM} and can generate ripple during the phase delays. Exemplary problems with at least one conventional triac-based dimmer when used with a reactive load are described in Rand et al., “Issues, Models and Solutions for Triac Modulated Phase Dimming of LED Lamps”, June, 2007, pages 1398-1404 of Power Electronics Specialists Conference, 2007. PESC 2007, published by the Institute of Electrical and Electronic Engineers, ISBN 978-1-4244-0655-5. Thus, although the rectified input voltage V_{Φ_RECT} *ideally* has one phase delay per cycle during dimming, when driving a reactive load, such as a switching power converter 102, problems such as missing phase delays and multiple phase delays α in a single half cycle of the rectified input voltage V_{Φ_RECT} exist.

(21) Although minor ripple may be present during the dimming portion of the input voltage V_{Φ_RECT} , the multiple phase delays α during a single half cycle of input voltage V_{Φ_RECT} cause significant interruptions in the initial phase delay α of the input voltage V_{Φ_RECT} . In at least one embodiment, triac 210 (Figure 2) turning ON and OFF multiple times during a single half cycle of input voltage V_{Φ_RECT} causes the significant interruptions in the initial phase delay α of the input voltage V_{Φ_RECT} . When triac 210 (Figure 2) turns ON and OFF multiple times during a dimming portion of a half cycle of input voltage V_{Φ_RECT} , the input voltage V_{Φ_RECT} increases and decreases multiple times during the dimming portion of the half cycle of input voltage V_{Φ_RECT} . Multiple oscillations of the input voltage V_{Φ_RECT} during a half cycle of the input voltage V_{Φ_RECT} can cause problems such as flicker of a lamp load.

(22) Conventional solutions to the problem of interfacing a triac-based dimmer with a reactive switching power converter 102 involve adding additional components to, for example, discharge the filter capacitor 115 during the dimming portion of dimmer voltage V_{Φ_DIM} .

(23) Figure 4 depicts an LED driver circuit 400 available from Supertex, Inc. of Sunnyvale, CA, USA. LED driver circuit 400 represents one embodiment of light source driver circuit 106. The LED driver circuit 400 is described in more detail in Supertex design note DN-H05 available from Supertex, Inc. The LED driver circuit 400 includes two extra circuits, damper circuit 402 and bleeder circuit 404 to provide compatibility with a dimmer, such as dimmer 104. According to DN-H05, the damper circuit 402 provides damped charging of the driver's input filter circuit at P16. The damper circuit 402 provides resistive damping to prevent AC line input current oscillations due to a sudden rise of an AC line voltage, such as the edges of dimmer voltage V_{Φ_DIM} . The bleeder circuit 404 provides a nominal 1 kohm load to a rectified AC line at P21 to suppress a voltage rise at the input capacitors C21-C23 due to leakage current of diac 208 and triac 210 (Figure 2) during dimming portions of dimmer voltage V_{Φ_DIM} which could otherwise cause flicker of a lamp driven by LED driver circuit 400.

(24) Figure 5 depicts a unity power factor LED lamp driver 500, which represents one embodiment of light source driver circuit 106. The LED lamp driver 500 is described in more detail in Supertex application note AN-H52 available from Supertex, Inc. LED lamp driver 500 includes damping circuitry 502 to add a load to dimmer 104 during dimming portions of the dimmer voltage V_{Φ_DIM} . The damping circuitry 502 includes a bleeder resistor R_{BL} that is connected by transistor M2 during the dimming portions of dimmer voltage V_{Φ_DIM} to lamp driver 500. When transistor M2 conducts, the bleeder resistor R_{BL} provides an added load to the AC line at V_{IN} to dampen the dimmer voltage V_{Φ_DIM} during dimming portions. Adding an extra transistor M2 and resistor R_{BL} increases the system cost of lamp driver 500.

(25) It would be desirable to reduce or eliminate the extra components of LED driver circuit 400 and LED lamp driver 500 that provide a load to dimmer 104 during the dimming portion of dimmer voltage V_{Φ_DIM} . It would also be desirable to reduce or eliminate the power consumption of resistive loads added by LED driver circuit 400 and LED lamp driver 500 that provide a load to dimmer 104 during the dimming portion of dimmer voltage V_{Φ_DIM} .

SUMMARY OF THE INVENTION

(26) In one embodiment of the present invention, a controller is configured to control a switching power converter and provide compatibility between the switching power converter and a triac-based dimmer. The switching power converter includes a switch to control voltage conversion of an input voltage to the switching power converter. The controller includes one or more components to control the switch of the switching power converter to establish an input resistance of the switching power converter during a dimming portion of the input voltage. The input resistance allows the triac-based dimmer to generate a phase modulated input voltage to the switching power converter having a substantially uninterrupted phase delay during each half-cycle of the input voltage during a dimming period.

(27) In another embodiment of the present invention, a method to control a switching power converter and provide compatibility between the switching power converter and a triac-based dimmer, wherein the switching power converter includes a switch to control voltage conversion of an input voltage to the switching power converter, includes controlling the switch of the switching power converter to establish an input resistance of the switching power converter during a dimming portion of the input voltage. The input resistance allows the triac-based dimmer to generate a phase modulated input voltage to the switching power converter having a substantially uninterrupted phase delay during each half-cycle of the input voltage during a dimming period.

(28) In a further embodiment of the present invention, an electronic system includes a switching power converter to convert an input voltage to the switching power converter. The switching power converter includes a switch to control voltage conversion of the input voltage to the switching power converter into the output voltage. The input voltage to the switching power converter is phase modulated during dimming periods by a triac-based dimmer. The electronic system also includes a controller, coupled to the switching power converter, to control the switch of the switching power converter to establish an input resistance of the switching power converter during a dimming portion of the input voltage. The input resistance allows the triac-based dimmer to generate a phase modulated input voltage to the switching

power converter having a substantially uninterrupted phase delay during each half-cycle of the input voltage during a dimming period.

BRIEF DESCRIPTION OF THE DRAWINGS

(29) The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the several figures designates a like or similar element.

(30) Figure 1 (labeled prior art) depicts a power control system having a switching power converter.

(31) Figure 2 (labeled prior art) depicts a triac-based power and dimming system.

(32) Figure 3 (labeled prior art) depicts a series of *ideal* voltage waveforms that represent two respective cycles of waveforms present in an *ideal* power and dimming system of Figure 2.

(33) Figure 4 (labeled prior art) depicts an LED driver circuit with resistive damping.

(34) Figure 5 (labeled prior art) depicts a unity power factor LED lamp driver with resistive damping.

(35) Figure 6 depicts a power system, which includes a switching power converter controlled by controller with dimmer compatibility.

(36) Figure 7 depicts a circuit model of the power system of Figure 6 when the controller operates in maintenance mode.

(37) Figure 8 depicts a power system, which is one embodiment of the power system of Figure 6.

(38) Figure 9 depicts an embodiment of a controller in the power system of Figure 8.

(39) Figure 10 depicts an exemplary triac compatibility algorithm.

(40) Figure 11 depicts an exemplary triac compatibility algorithm having two maintenance modes.

DETAILED DESCRIPTION

(41) In at least one embodiment, a controller allows triac-based dimmer to properly function and dim a load whose voltage is regulated by a switching power converter. In at least one embodiment, the switching power converter includes a switch to control voltage conversion of an input voltage to the switching power converter, wherein phase delays are introduced in the input voltage by a triac-based dimmer during a dimming period. In at least one embodiment, the controller is configured to control the switch of the switching power converter to establish an input resistance of the switching power converter during a dimming portion of the input voltage, wherein the input resistance allows the triac-based dimmer to phase modulate a supply voltage to the dimmer to generate a dimmer output voltage having a substantially uninterrupted phase delay during each half-cycle of the supply voltage during the dimming period. In at least one embodiment, the input resistance allows the triac-based dimmer to phase modulate the supply voltage so that the output voltage of the dimmer has a single, uninterrupted phase delay during each half cycle of the input voltage. In at least one embodiment, phase modulating the supply voltage introduces a leading edge phase delay in each cycle of the input voltage, and each phase delay has a duration of less than one-half of the period of each cycle of the input voltage.

(42) In at least one embodiment, the controller has two modes of operation, a power factor correction (PFC) mode and a maintenance mode. In at least one embodiment, the maintenance mode has an active maintenance mode, and, in at least one embodiment, the maintenance mode has both the active maintenance mode and a quiet maintenance mode. In the PFC mode, the controller controls the switching power converter to provide power factor correction and voltage regulation. When the input voltage to the switching power converter is below a first threshold voltage, the controller enters the active maintenance mode. In at least one embodiment, when the

input voltage further drops below a second threshold voltage, the controller enters a quiet maintenance mode.

(43) In the maintenance mode, the controller sets an operational frequency and pulse width of a control signal that respectively controls a switching frequency and ON time of the switching power converter switch so that an input resistance to the triac-based dimmer allows the dimmer to phase modulate the supply voltage during each half-cycle of the supply voltage during the dimming period. In at least one embodiment, the switching power converter includes a filter capacitor across input terminals of the switching power converter. In the maintenance mode, the controller controls the input resistance of the switching power converter to allow the filter capacitor to discharge sufficiently to allow the triac-based dimmer to phase modulate the supply voltage during each half-cycle of the input voltage during the dimming period with a substantially uninterrupted phase delay. In at least one embodiment, the dimming period is substantially uninterrupted when the triac of the triac-based dimmer does not include multiple oscillations between conduction and nonconduction during each half cycle of the input voltage. In at least one embodiment, when the input voltage to the switching power converter further decreases below a second predetermined threshold, the controller ceases operating the switch until the input voltage increases above the first predetermined threshold.

(44) Figure 6 depicts power system 600, which includes a switching power converter 602 controlled by controller 604 with dimmer compatibility. Voltage source 101 and triac-based dimmer 603 generate the phase modulated dimmer voltage V_{Φ_DIM} as previously described. Dimmer 603 includes triac 605, and, in at least one embodiment, dimmer 603 and triac 605 are respectively configured identically to dimmer 202 and triac 210. Full bridge diode rectifier 103 rectifies dimmer voltage V_{Φ_DIM} to generate the rectified input voltage V_{Φ_RECT} to the switching power converter 602. Filter capacitor 115 provides, for example, high frequency filtering of the rectified input voltage V_{Φ_RECT} . Switching power converter 602 converts the input voltage V_{Φ_RECT} into a regulated output voltage V_{LINK} to supply a voltage to load 112. Load 112 can be any type of load including a load having one or more LEDs. The particular configuration of input section 608 and output section 610 is a matter of design choice. The switching power converter 602 can be any kind of switching

power converter 602, such as a buck converter, boost converter, boost-buck converter, and a Cúk converter.

(45) Controller 604 generates switch control signal CS_1 to control conductivity of switch 606. In at least one embodiment, switch 606 is identical to switch 108 (Figure 1). Controller 604 monitors the input voltage V_{Φ_RECT} and the link voltage V_{LINK} . Controller 604 controls switch 606 to provide power factor correction and regulate link voltage V_{LINK} . During PFC mode, controller 604 provides power factor correction for switching power converter 602 after any phase delay α of input voltage V_{Φ_RECT} . (A phase delay α of 0 indicates an absence of dimming). Control of power factor correction and the output voltage V_{OUT} of switching power converter 102 is, for example, described in the exemplary embodiments of Melanson I, II, III, IV, and V.

(46) During a dimming portion of input voltage V_{Φ_RECT} , controller 604 controls switch 606 so that switching power converter 602 has an input resistance that allows sufficient current to flow through triac 605. Allowing sufficient current to flow through triac 605 allows the triac 605 to properly operate. In at least one embodiment, proper operation of dimmer 603 occurs when dimmer 603 is set to provide a phase delay in input voltage V_{Φ_RECT} and dimmer 603 phase supply voltage V_{IN} to generate an input voltage V_{Φ_RECT} with a substantially uninterrupted phase delay during each half cycle of input voltage V_{Φ_RECT} during a dimming period. Exemplary waveforms of voltages V_{Φ_DIM} and V_{Φ_RECT} indicating proper operation of dimmer 603 are set forth in Figure 3. In at least one embodiment, proper operation of triac 605 includes preventing the triac 605 from oscillating during subsequent dimming periods.

(47) In at least one embodiment, controller 604 has two modes of operation, PFC mode and maintenance mode. In at least one embodiment, the maintenance mode has two modes of operation, the active maintenance mode and the quiet maintenance mode. During any phase delay α of input voltage V_{Φ_RECT} , controller 604 operates in maintenance mode. During maintenance mode, controller 604 causes switching power converter 602 to have an input resistance that allows dimmer 603 to generate a phase modulated input voltage V_{Φ_RECT} with a substantially uninterrupted phase delay α during each half-cycle of the input voltage V_{Φ_RECT} during the dimming period. In

at least one embodiment, controller 604 establishes an input resistance R_{EFF} during the maintenance mode that allows the triac-based dimmer 603 to phase modulate the supply voltage V_{IN} so that input voltage V_{Φ_RECT} has a single, uninterrupted phase delay during each half cycle of the input voltage V_{Φ_RECT} . In at least one embodiment, phase modulating the supply voltage V_{IN} introduces a leading edge phase delay α in each cycle of the input voltage V_{Φ_RECT} , and each phase delay α has a duration of less than one-half of the period of each cycle of the input voltage V_{Φ_RECT} .

(48) During PFC mode, the switching frequency of switch 606 is nominally 40 kHz - 120 kHz. However, switching at such high frequencies during a phase delay of input voltage V_{Φ_RECT} is inefficient because very little voltage is presented to the load 112 during the phase delay of input voltage V_{Φ_RECT} . Thus, power is consumed by switch 606 with very little power delivered to load 112.

(49) Figure 7 depicts a circuit model 700 of power system 600 when controller 604 operates in maintenance mode. Referring to Figures 6 and 7, in maintenance mode, controller 604 generates control signal CS_1 so that the input impedance of switching power converter 602 appears as a resistive load 602E having an effective resistance R_{EFF} . The effective resistance R_{EFF} of load 602E is a matter of design choice. In at least one embodiment, the effective resistance R_{EFF} , as established by controller 604, provides a sufficient discharge path for capacitor 115 to allow current to keep the triac 605 conducting during the dimming portion of voltage V_{Φ_DIM} . In at least one embodiment, controller 604 causes switch 606 to switch as slowly as possible to establish an effective resistance R_{EFF} that allows the triac of dimmer 603 to properly operate. In at least one embodiment, controller 604 establishes the effective resistance R_{EFF} to be between 2 kohms and 5 kohms.

(50) Although the effective resistance R_{EFF} appears as an actual resistance to dimmer 603, effective resistance R_{EFF} does not dissipate energy as a physical resistor does. Instead, charge from the input current I is eventually transferred to load 112.

(51) Figure 8 represents power system 800, and power system 800 represents one embodiment of power system 600. Power system 800 includes a switching power converter 802, and, in one embodiment is identical to switching power converter 102.

Power system 800 also includes controller 804 with dimmer compatibility. Controller 804 operates in maintenance mode in the dimming portion of input voltage V_{ϕ_RECT} and otherwise operates in PFC mode.

(52) Signal plot 806 depicts input current i_L during one period tt of control signal CS_1 with switching power converter 802 operating in discontinuous conduction mode. During a dimming portion of input voltage V_{ϕ_RECT} , controller 804 operates in maintenance mode. In at least one embodiment, when operating in maintenance mode, controller 804 operates in the active maintenance mode. In at least one embodiment, when operating in maintenance mode, controller 804 operates in the active maintenance mode or the quiet maintenance mode during the dimming portion of input voltage V_{ϕ_RECT} depending upon a value of the input voltage V_{ϕ_RECT} .

(53) In at least one embodiment, when operating in the active maintenance mode, controller 804 establishes a switching frequency f_{sw} and amount of conduction time t_1 of switch 606 to present an effective resistance R_{EFF} to dimmer 603. Switching frequency $f_{sw} = 1/tt$. In at least one embodiment, controller 804 determines an average of input current i_L (I_{L_avg}) for a given value of input voltage V_{ϕ_RECT} to determine the value of effective resistance R_{EFF} . The effective resistance R_{EFF} is related to the average input current I_{L_avg} and the value of input voltage V_{ϕ_RECT} by Ohm's law in Equation [1]:

$$R_{EFF} = V_{\phi_RECT} / I_{L_avg} \quad [1]$$

(54) When switch 606 conducts for t_1 seconds, the input current i_L increases. After t_1 seconds, input current i_L decreases for t_2 seconds. This pattern repeats for each period of tt seconds. In at least one embodiment, for a given pulse width t_1 and period tt of control signal CS_1 , the average input current i_L is derived and set forth in Equation [2]:

$$I_{L_avg} = \frac{V_{\phi_RECT} * t_1^2 * \left(1 + \frac{V_{\phi_RECT}}{V_{LINK} - V_{\phi_RECT}} \right)}{2 * tt * L} \quad [2]$$

I_{L_avg} represents the average input current i_L , V_{ϕ_RECT} represents the rectified input voltage to switching power converter 802, V_{LINK} represents the output voltage of switching power converter 802, t_I represents the pulse width of control signal CS_1 and, thus, the conduction time of switch 606, tt represents the period of control signal CS_1 , and L represents the inductance of inductor 110.

(55) From Equations [1] and [2], the effective resistance R_{EFF} is set forth in Equation [4]:

$$R_{EFF} = \frac{2 * tt * L}{t_1^2 * \left(1 + \frac{V_{\phi_RECT}}{V_{LINK} - V_{\phi_RECT}} \right)} \quad [4]$$

If $V_{\phi_RECT} \ll V_{LINK}$, the effective resistance R_{EFF} is approximated by Equation [5]:

$$R_{EFF} = \frac{2 * tt * L}{t_1^2} \quad [5]$$

Rearranging Equation [5] yields Equation [6], which solves for the pulse width t_I of control signal CS_1 in terms of the period of control signal CS_1 , the inductance value L of inductor 110, and the effective resistance R_{EFF} of switching power converter 802:

$$t_1 = \sqrt{\frac{2 * tt * L}{R_{EFF}}} \quad [6]$$

(56) Thus, in at least one embodiment, when operating in the active maintenance mode, controller 804 sets a value for the period of control signal CS_1 and utilizes Equation [6] to calculate a pulse width t_I of control signal CS_1 , i.e. an amount of conduction time t_I of switch 606, to present an effective resistance R_{EFF} to dimmer 603. Equation [5] can also be rearranged to determine a period tt of control signal CS_1 based upon a pulse width t_I . The particular inductance value L of inductor 110 is a matter of design choice. In one embodiment, an effective resistance value R_{EFF} of 5 kohms is sufficient to discharge capacitor 115 and allow the triac of dimmer 603 to operate properly. For a period tt of 0.5 msec and a 1 mH value for inductor L , to

achieve an effective resistance R_{EFF} of 5 kohms, controller 804 determines t_I to be approximately 14 μsec .

(57) In at least one embodiment, the inductance value of inductor L, the period tt of control signal CS_1 , and the pulse width t_I of control signal CS_1 are preset in a memory (not shown) of controller 804 in accordance with the relationship in Equation [5].

Presetting the values of L, tt , and t_I eliminates a need for controller 804 to determine the values and/or actually calculate the pulse width t_I .

(58) Thus, in at least one embodiment, controller 804 can set the period tt and pulse width t_I of control signal CS_1 using, for example, preset determinations of period tt and pulse width t_I . In at least one embodiment, controller 804 can calculate values of period tt and pulse width t_I .

(59) In at least one embodiment, controller 804 dithers the value of period tt and pulse width t_I to mitigate electromagnetic interference. In at least one embodiment, when dithering, controller 804 stores multiple values of period tt and values of pulse width t_I in accordance with Equation [5] and utilizes the values of period tt and pulse width t_I in accordance with a dithering algorithm. The dithering algorithm is a matter of design choice and is, for example, a pseudo-random selection algorithm. The exact manner of storing and/or determining the values of variables and results in Equation [4] and/or Equation [5] are a matter of design choice.

(60) The particular implementation of controller 804 is a matter of design choice. Controller 804 can be implemented using analog, digital, or analog and digital components.

(61) Figure 9 depicts controller 900, and controller 900 represents one embodiment of controller 804. Figure 10 depicts an exemplary triac compatibility algorithm 1000 executed by controller 900 that determines whether controller 900 operates in PFC mode or the active maintenance mode. Referring to Figures 9 and 10, controller 900 includes a processor 902 configured to execute code stored in memory 904. In at least one embodiment, the code stored in memory 904 implements triac compatibility algorithm 1000.

(62) In operation 1002, processor 902 monitors the input voltage V_{Φ_RECT} . In operation 1003, if input voltage V_{Φ_RECT} is greater than or equal to active mode threshold voltage V_{TH0} , controller 900 operates in PFC mode 1004 until operation 1002 determines that input voltage V_{Φ_RECT} is less than the active mode threshold voltage V_{TH0} . If V_{Φ_RECT} is less than active mode threshold voltage V_{TH0} , then controller 900 operates in active maintenance mode 1006. Controller 900 can be implemented in any of a variety of ways. In at least one embodiment, controller 900 includes an analog-to-digital converter (ADC) to convert the input voltage V_{Φ_RECT} into a digital value and compares the digital value to the active mode threshold voltage V_{TH0} . The ADC can also be a separate component exterior to the processor. In at least one embodiment, the controller 900 includes analog comparators to compare the value of input voltage V_{Φ_RECT} to the active mode threshold V_{TH0} and generate a comparison signal. In at least one embodiment, the comparison signal is used as a basis for determining whether controller 900 operates in PFC mode 1004 or active maintenance mode 1006. The processor 902 can be any type of processor including a digital signal processor. Memory 904 can be any type of memory including a read only memory or a read-write type memory.

(63) In at least one embodiment, the active mode threshold voltage V_{TH0} is set so that the active maintenance mode 1006 is not entered until the input voltage V_{Φ_RECT} is close to a zero crossing and below a breakover voltage of the diac in dimmer 603. In at least one embodiment, the breakover voltage of the diac is 30V, and the active mode threshold voltage V_{TH0} is set to 20V. Once the active threshold voltage V_{TH0} is reached, controller 900 will operate switch 606 to generate an effective input resistance R_{EFF} of switching power converter 802 to allow the triac 605 to properly operate. When the input voltage V_{Φ_RECT} rises above the active threshold voltage V_{TH0} , in at least one embodiment, the dimming portion of input V_{Φ_RECT} is over, i.e. dimmer 603 has ceased chopping the supply voltage V_{IN} , and the controller 900 operates to provide power factor correction for switching power converter 802. The particular execution frequency of triac compatibility algorithm 1000 is a matter of design choice and is preferably sufficient to allow triac compatibility algorithm 1000 to accurately respond to changes in the input voltage V_{Φ_RECT} to allow triac 605 to function properly.

(64) When controller 900 enters active maintenance mode 1006, controller 900 generates control signal CS_1 with a switch period tt of 0.5 msec (i.e. $f_{sw} = 2$ kHz) and a pulse period of 14 μ sec. In at least one embodiment, the period tt is dithered to the spread the spectrum of the control signal CS_1 and mitigate electromagnetic radiation at the switching frequency f_{sw} . After entering active maintenance mode 1006, triac compatibility algorithm 1000 continues to monitor the input voltage V_{Φ_RECT} and compare the input voltage V_{Φ_RECT} to active mode threshold voltage V_{TH0} .

(65) Figure 11 depicts a triac compatibility algorithm 1100, which, in at least one embodiment, is represented by code stored in memory 904 and executable by processor 902. Referring to Figures 8, 9, 10, and 11, in general, triac compatibility algorithm 1000 effectively removes charge from capacitor 115 and, thus, lowers the input voltage V_{Φ_RECT} to allow sufficient current to flow into switching power converter 802 so that the triac of dimmer 603 operates properly during a dimming portion of the input voltage V_{Φ_RECT} . If the input voltage V_{Φ_RECT} remains below a second threshold value V_{TH1} , triac compatibility algorithm 1100 causes controller 900 to enter quiet maintenance mode 1104 to increase the period tt of control signal CS_1 and, thus, further reduce the amount of switching of switch 606. Thus, by monitoring a comparison between input voltage V_{Φ_RECT} and thresholds V_{TH0} and a lower threshold V_{TH1} and having active and quiet maintenance modes, controller 900 operates switching power converter more efficiently using triac compatibility algorithm 1100 relative to triac compatibility algorithm 1000. If the input voltage V_{Φ_RECT} rises above the active threshold voltage V_{TH0} , in at least one embodiment, the dimming portion is over, i.e. dimmer 603 has ceased chopping the supply voltage V_{IN} , and the controller 900 operates to provide power factor correction for switching power converter 802.

(66) Operation 1102 of triac compatibility algorithm 1100 monitors a comparison between input voltage V_{Φ_RECT} and threshold voltages V_{TH0} and V_{TH1} . Triac compatibility algorithm 1100 includes operations 1002 and 1004. If operation 1002 determines that input voltage V_{Φ_RECT} is greater than active mode threshold voltage V_{TH0} , controller 900 enters PFC mode 1004. If operation 1002 determines that the input voltage V_{Φ_RECT} is less than the active mode threshold voltage V_{TH0} , then

operation 1106 determines whether the input voltage V_{Φ_RECT} is less than the quiet mode threshold voltage V_{TH1} .

(67) If operation 1106 determines that the input voltage V_{Φ_RECT} is greater than or equal to the quiet threshold voltage V_{TH1} , triac compatibility algorithm 1100 causes controller 900 to enter active maintenance mode 1006. If the input voltage V_{Φ_RECT} is less than the quiet threshold voltage V_{TH1} , triac compatibility algorithm 1100 causes controller 900 to enter the quiet maintenance mode 1104. The quiet maintenance mode 1104 further reduces switching of switch 606. In at least one embodiment, the quiet threshold voltage V_{TH1} is 15V. When the input voltage V_{Φ_RECT} decreases below the quiet threshold voltage V_{TH1} , in at least one embodiment, it is assumed that controller 900 does not need to pulse switch 606 to remove charge from capacitor 115. Thus, in the quiet maintenance mode 1104, controller 900 generates control signal CS_1 so that switch 606 does not conduct.

(68) The particular execution frequency of triac compatibility algorithm 1100 is a matter of design choice and is preferably sufficient to allow triac compatibility algorithm 1100 to accurately respond to changes in the input voltage V_{Φ_RECT} to allow triac 605 to function properly.

(69) Accordingly, a controller controls a switching power converter to allow the switching power converter to allow a triac-based dimmer to dim a load, such as a lighting fixture having LEDs as light sources.

(70) Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

- 1 1. A controller to control a switching power converter and provide
2 compatibility between the switching power converter and a triac-based dimmer,
3 wherein the switching power converter includes a switch to control voltage
4 conversion of an input voltage to the switching power converter, the controller
5 comprising:
6 one or more components to control the switch of the switching power
7 converter to establish an input resistance of the switching power
8 converter during a dimming portion of the input voltage, wherein the
9 input resistance allows the triac-based dimmer to generate a phase
10 modulated input voltage to the switching power converter having a
11 substantially uninterrupted phase delay during each half-cycle of the
12 input voltage during a dimming period.
- 1 2. The controller of claim 1 wherein the controller is further configured to
2 provide power factor correction and voltage regulation after the dimming portion of
3 the input voltage.
- 1 3. The controller of claim 1 wherein when the input voltage is below a
2 first threshold voltage, the controller is configured to establish the input resistance of
3 the switching power converter to allow the triac-based dimmer to phase modulate the
4 input voltage with a substantially uninterrupted phase delay during each half-cycle of
5 the input voltage during a dimming period.
- 1 4. The controller of claim 3 wherein the controller is further configured to
2 provide power factor correction and voltage regulation unless the input voltage to the
3 switching power converter is below the first threshold voltage.
- 1 5. The controller of claim 1 wherein the switching power converter
2 include an inductor and the controller is configured to generate a pulse width
3 modulated control signal to establish the input resistance using at least values of the
4 inductor, a period of the control signal, and a pulse width of the control signal.

1 6. The controller of claim 5 wherein one or more values of the inductor,
2 pulse width, and period are stored in a memory of the controller.

1 7. The controller of claim 5 wherein the controller is further configured to
2 dither the period and the pulse width of the control signal.

1 8. The controller of claim 1 wherein the controller is further configured to
2 provide power factor correction and voltage regulation unless the input voltage to the
3 switching power converter is below a first threshold voltage, when the input voltage is
4 below the first threshold voltage, the controller establishes the input resistance of the
5 switching power converter to allow the triac-based dimmer to phase modulate the
6 input voltage with a substantially uninterrupted phase delay during each half-cycle of
7 the input voltage during a dimming period, and when the input voltage is below a
8 second threshold voltage the controller ceases operation of the switch.

1 9. The controller of claim 1 wherein the dimming period is substantially
2 uninterrupted when the triac of the triac-based dimmer introduces a single phase delay
3 in the input voltage to the switching power converter during each half cycle of the
4 input voltage during the dimming period.

1 10. The controller of claim 1 wherein the phase modulated input voltage to
2 the switching power converter has a single phase delay during each half-cycle of the
3 input voltage during the dimming period.

1 11. A method to control a switching power converter and provide
2 compatibility between the switching power converter and a triac-based dimmer,
3 wherein the switching power converter includes a switch to control voltage
4 conversion of an input voltage to the switching power converter, the method
5 comprising:
6 controlling the switch of the switching power converter to establish an input
7 resistance of the switching power converter during a dimming portion
8 of the input voltage, wherein the input resistance allows the triac-based

9 dimmer to generate a phase modulated input voltage to the switching
10 power converter having a substantially uninterrupted phase delay
11 during each half-cycle of the input voltage during a dimming period.

1 12. The method of claim 11 further comprising:
2 providing power factor correction and voltage regulation after the dimming
3 portion of the input voltage.

1 13. The method of claim 11 further comprising:
2 establishing the input resistance of the switching power converter to allow the
3 triac-based dimmer to phase modulate the input voltage with a
4 substantially uninterrupted phase delay during each half-cycle of the
5 input voltage during a dimming period when the input voltage is below
6 the first threshold voltage.

1 14. The method of claim 13 further comprising:
2 providing power factor correction and voltage regulation unless the input
3 voltage to the switching power converter is below the first threshold
4 voltage.

1 15. The method of claim 11 wherein the switching power converter
2 include an inductor, the method further comprising:
3 generating a pulse width modulated control signal to establish the input
4 resistance using at least values of the inductor, a period of the control
5 signal, and a pulse width of the control signal.

1 16. The method of claim 15 the method further comprising:
2 utilizing one or more values of the inductor, pulse width, and period stored in
3 a memory of the controller to generate a pulse width modulated control
4 signal.

1 17. The method of claim 15 the method further comprising:
2 dithering the period and the pulse width of the control signal.

1 18. The method of claim 11 further comprising:
2 providing power factor correction and voltage regulation unless the input
3 voltage to the switching power converter is below a first threshold
4 voltage;
5 establishing the input resistance of the switching power converter to allow the
6 triac-based dimmer to phase modulate the input voltage with a
7 substantially uninterrupted phase delay during each half-cycle of the
8 input voltage during a dimming period when the input voltage is below
9 the first threshold voltage; and
10 ceasing operation of the switch when the input voltage is below a second
11 threshold voltage the controller.

1 19. The method of claim 11 wherein controlling the switch of the
2 switching power converter further comprises controlling the switch of the switching
3 power converter so that the dimming period is substantially uninterrupted when the
4 triac of the triac-based dimmer introduces a single phase delay in the input voltage to
5 the switching power converter during each half cycle of the input voltage during the
6 dimming period.

1 20. The method of claim 11 wherein controlling the switch of the
2 switching power converter further comprises controlling the switch of the switching
3 power converter so that the phase modulated input voltage to the switching power
4 converter has a single phase delay during each half-cycle of the input voltage during
5 the dimming period.

1 21. An electronic system comprising:
2 a switching power converter to convert an input voltage to the switching
3 power converter, wherein the switching power converter includes a
4 switch to control voltage conversion of the input voltage to the
5 switching power converter into the output voltage and the input voltage
6 to the switching power converter is phase modulated during dimming
7 periods by a triac-based dimmer; and

8 a controller, coupled to the switching power converter, to control the switch of
9 the switching power converter to establish an input resistance of the
10 switching power converter during a dimming portion of the input
11 voltage, wherein the input resistance allows the triac-based dimmer to
12 generate a phase modulated input voltage to the switching power
13 converter having a substantially uninterrupted phase delay during each
14 half-cycle of the input voltage during a dimming period.

1 22. The electronic system of claim 21 further comprising a load coupled to
2 the switching power converter.

1 23. The electronic system of claim 22 wherein the load comprises at least
2 one light emitting diode.

1 24. The electronic system of claim 21 further comprising the triac-based
2 dimmer coupled to the switching power converter.

1 25. The electronic system of claim 21 wherein the phase modulated input
2 voltage to the switching power converter has a single phase delay during each half-
3 cycle of the input voltage during the dimming period.

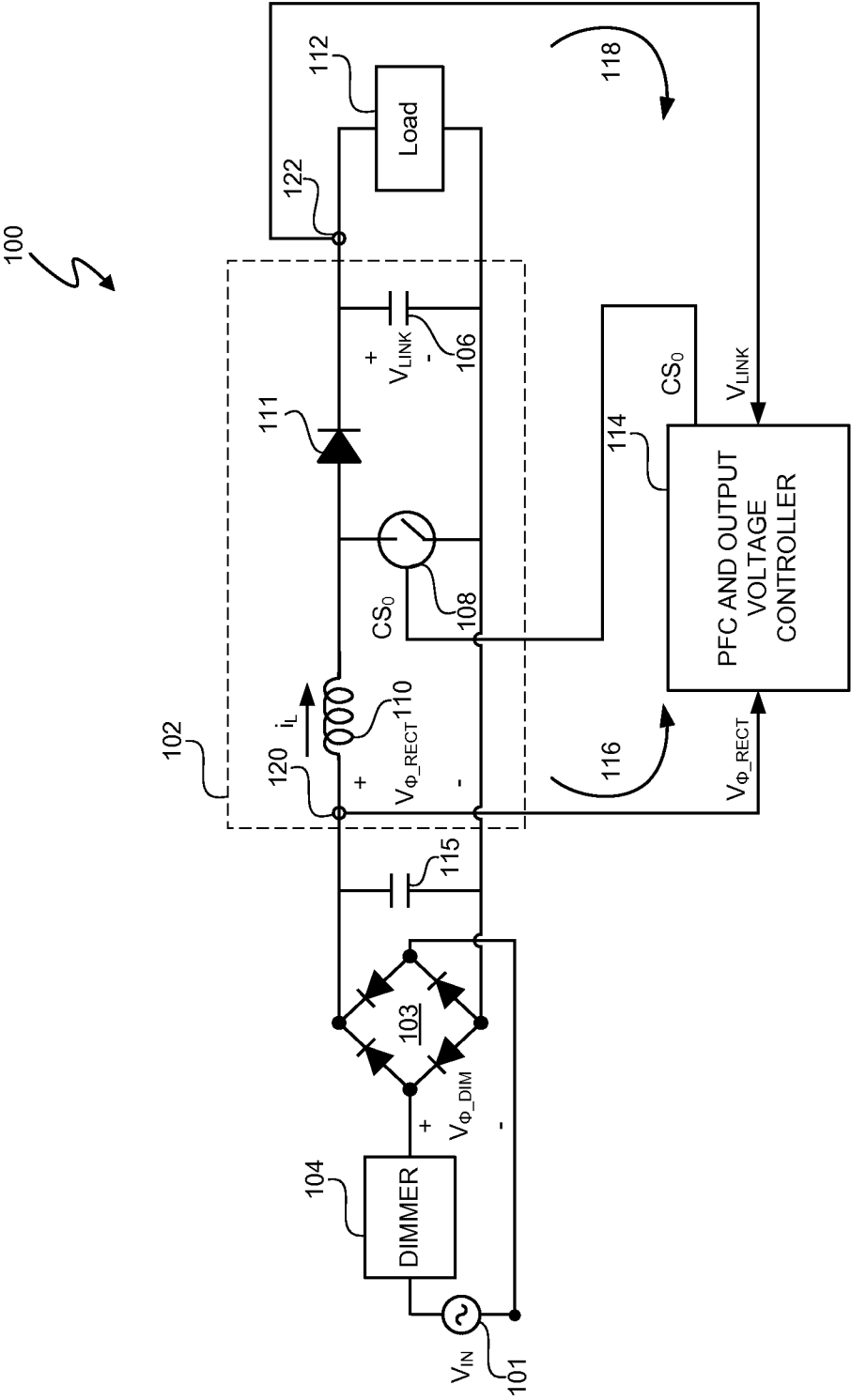


Figure 1 (prior art)

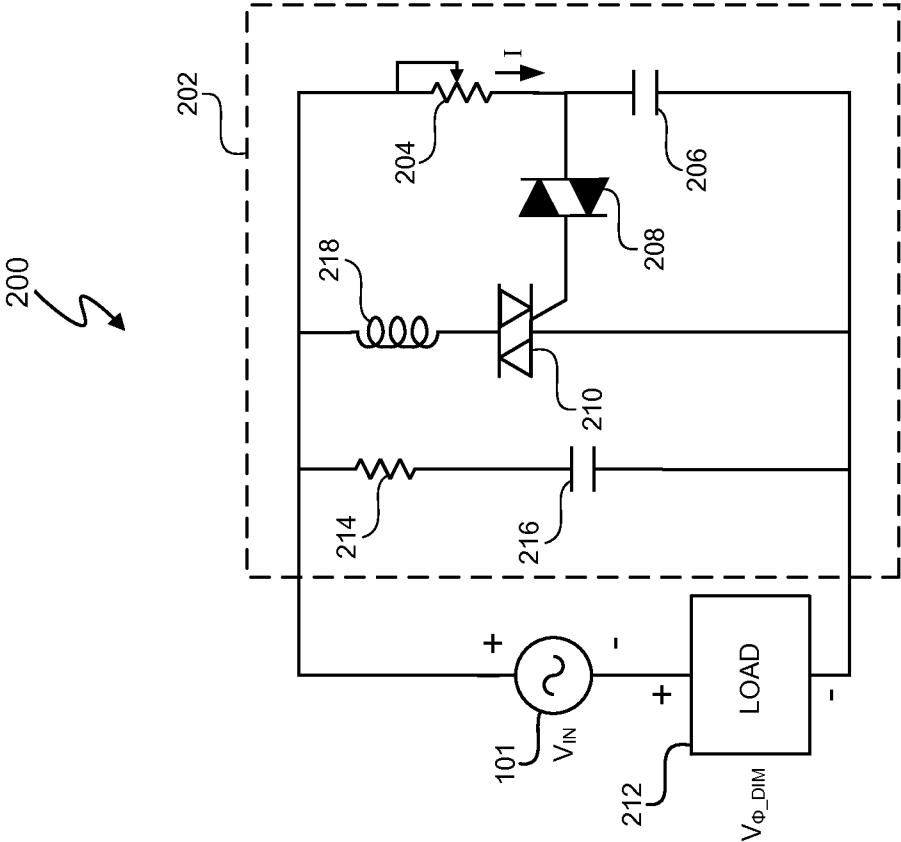


Figure 2 (prior art)

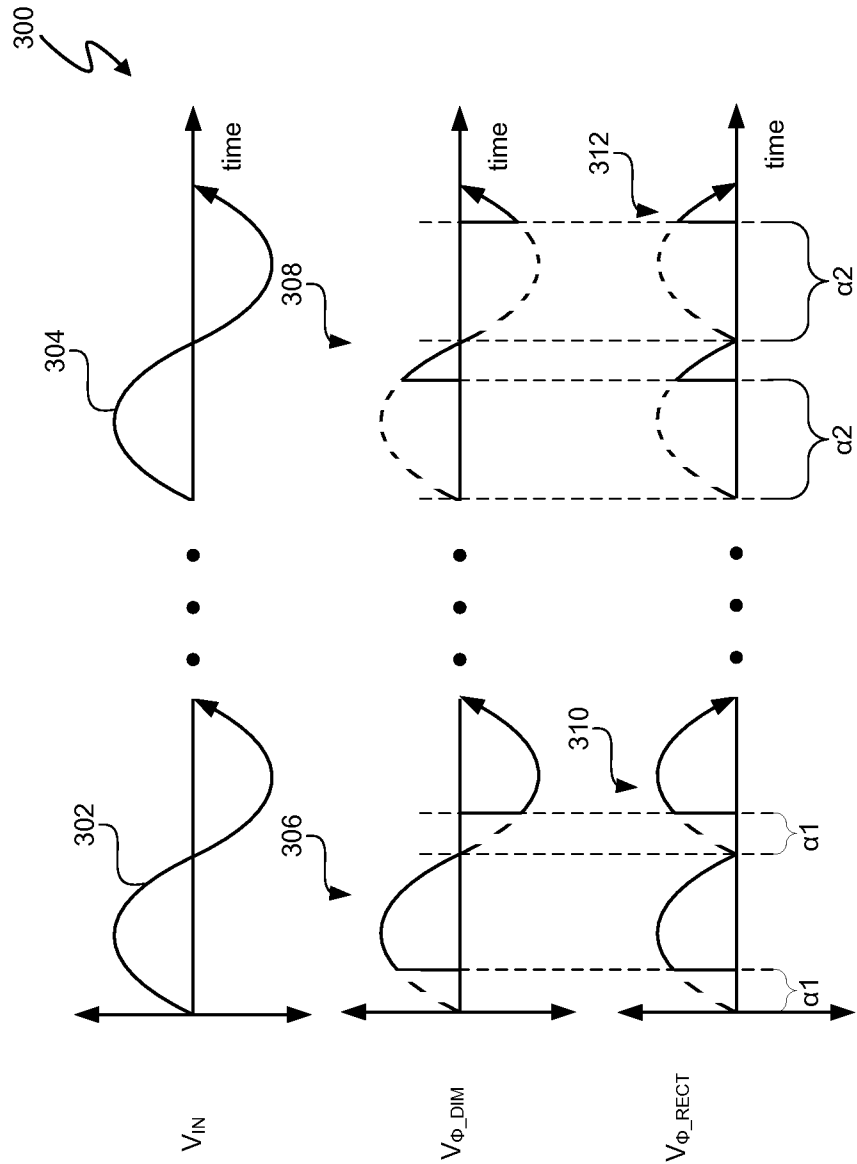
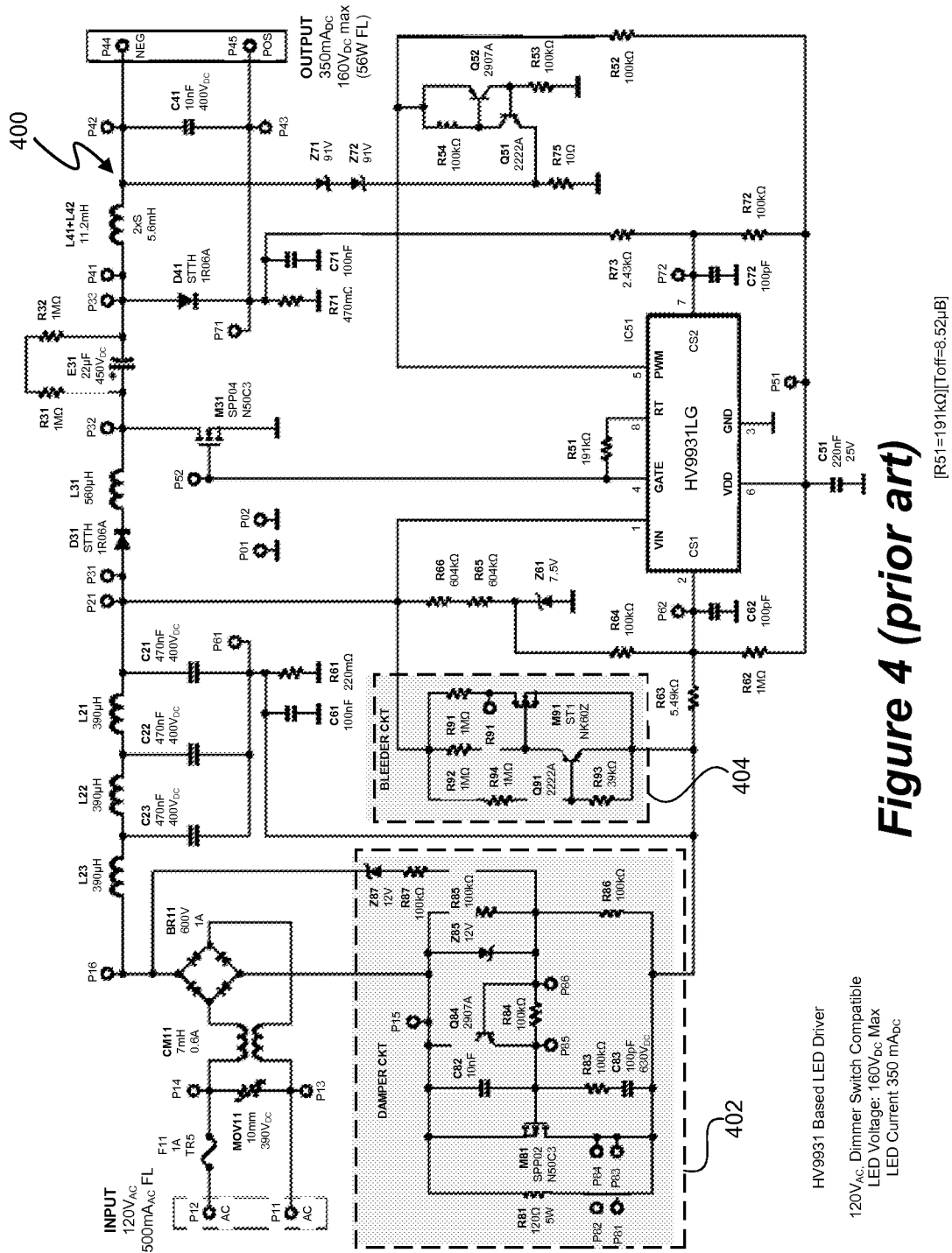


Figure 3 (prior art)



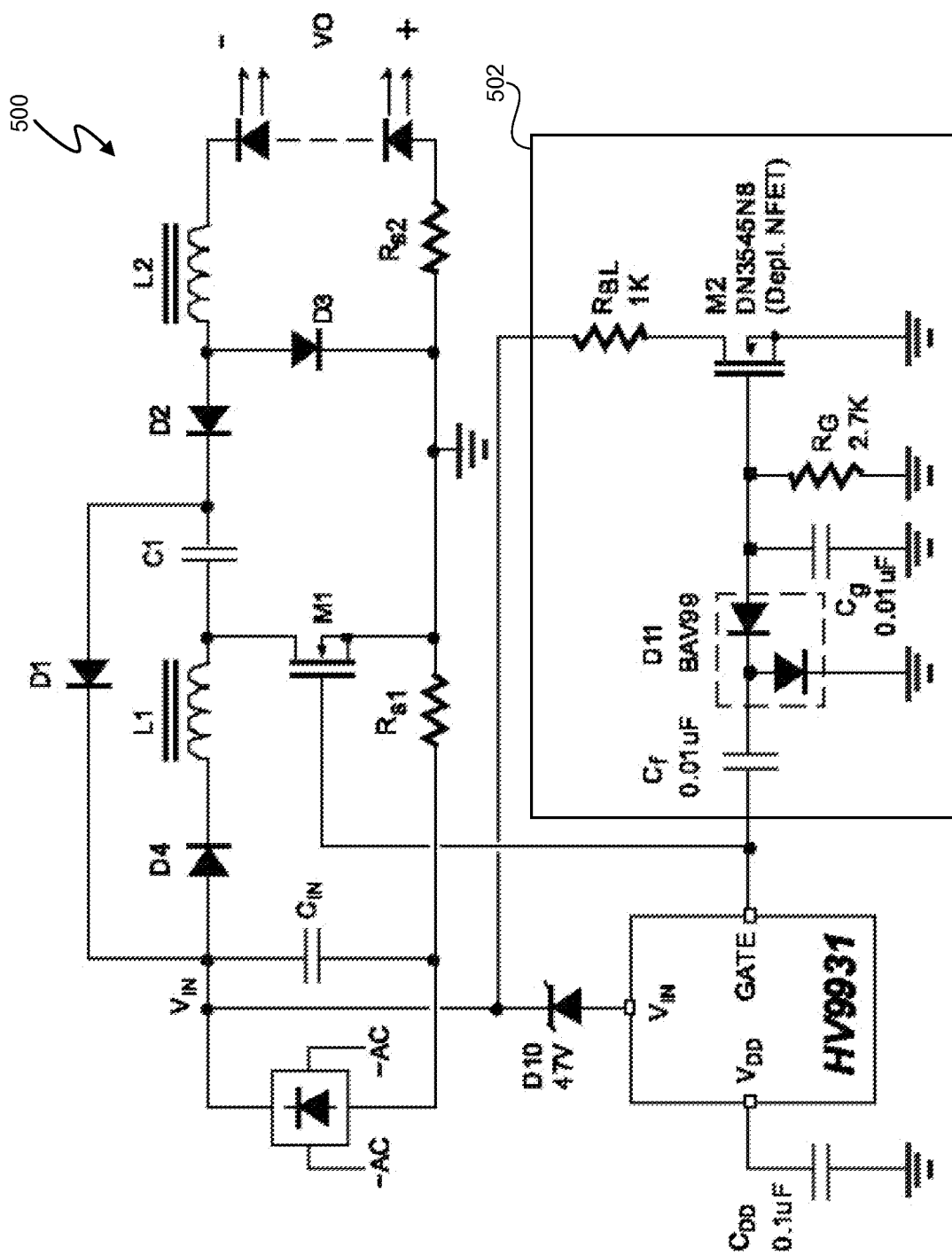


Figure 5 (prior art)

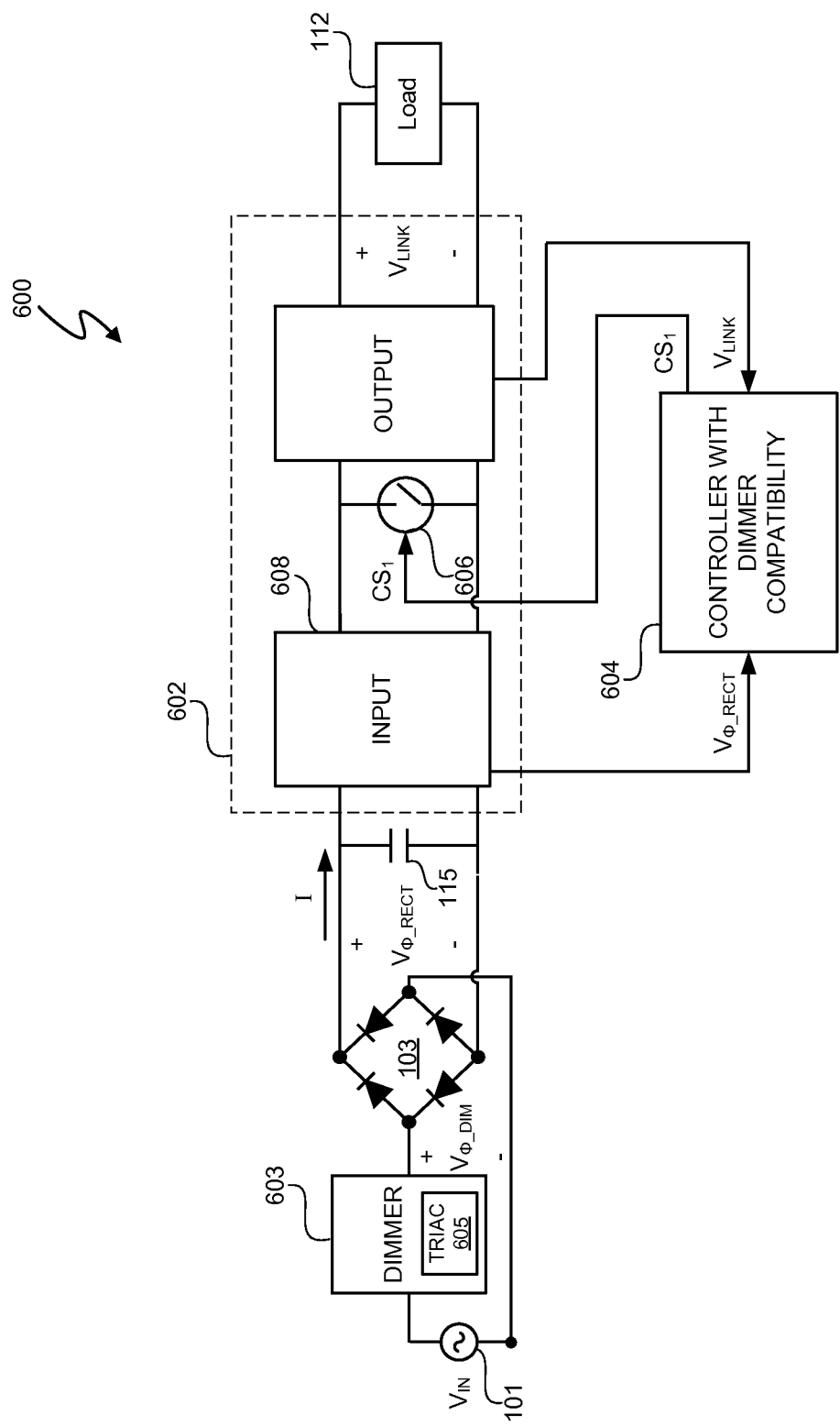


Figure 6

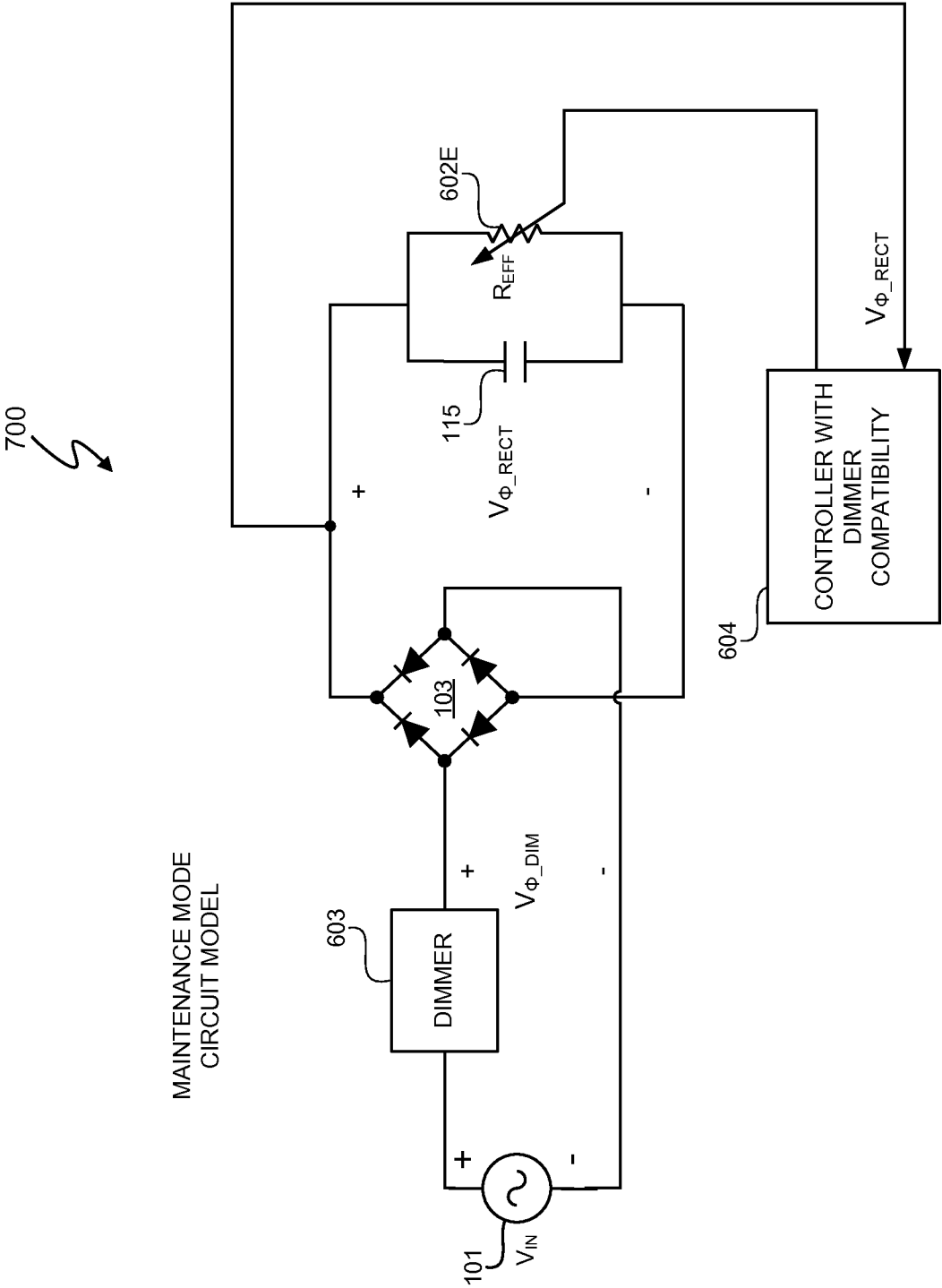


Figure 7

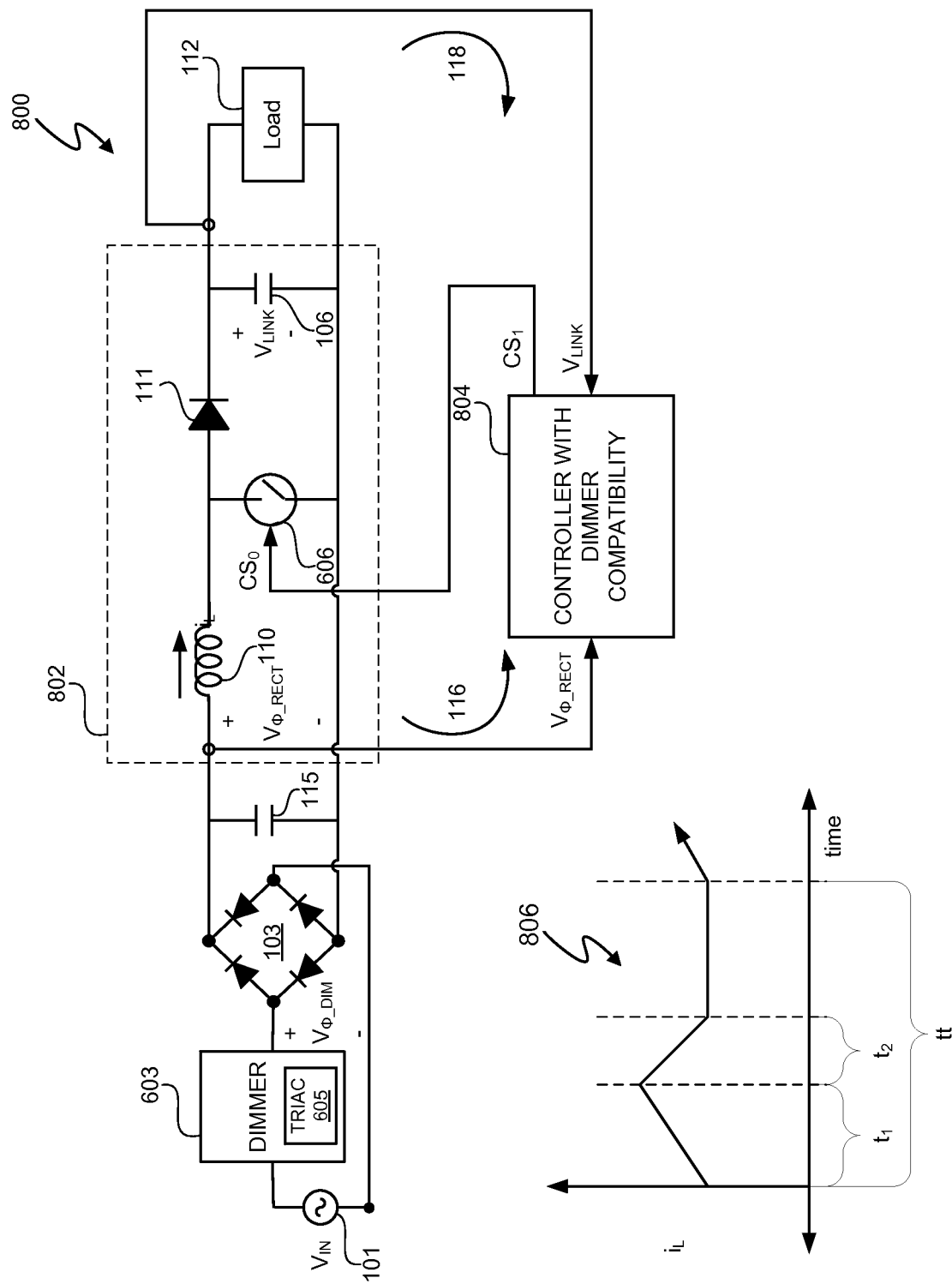


Figure 8

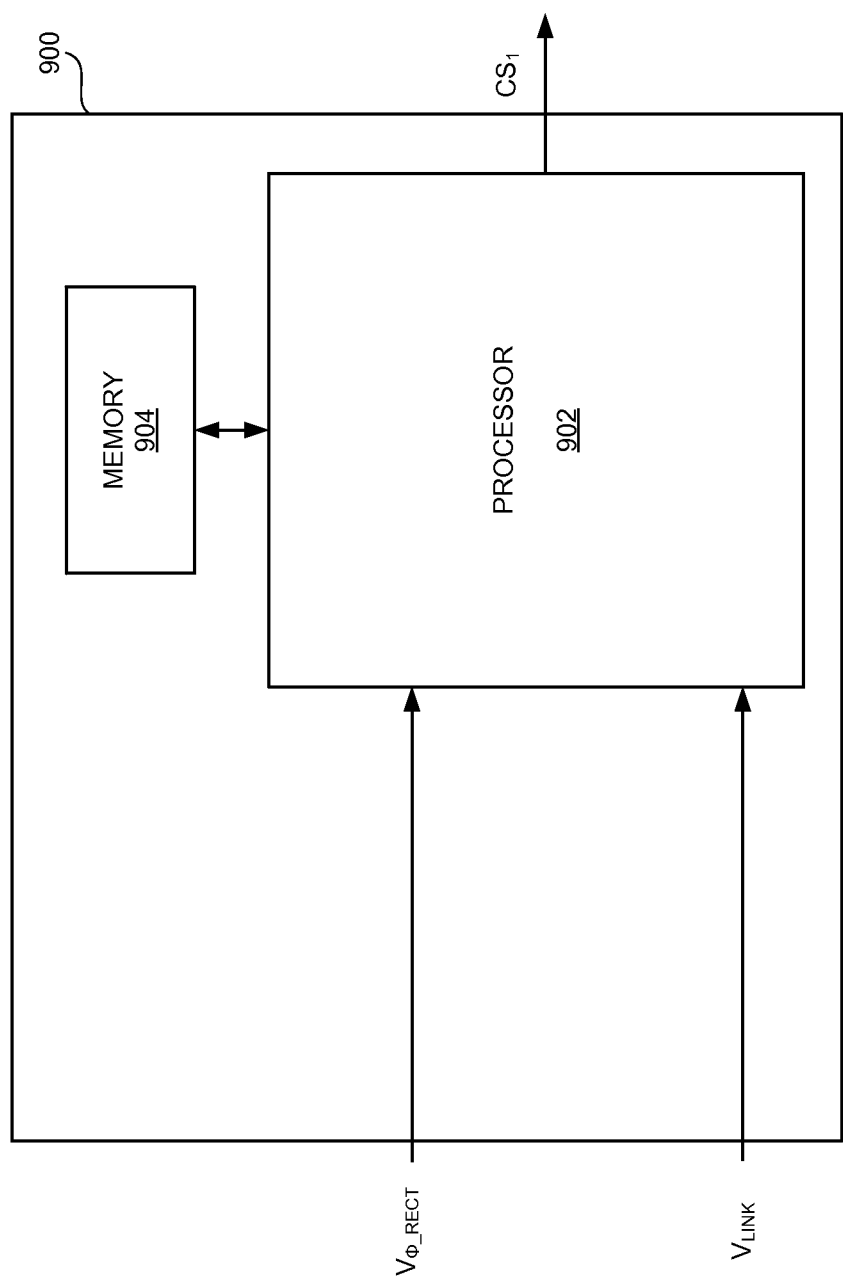
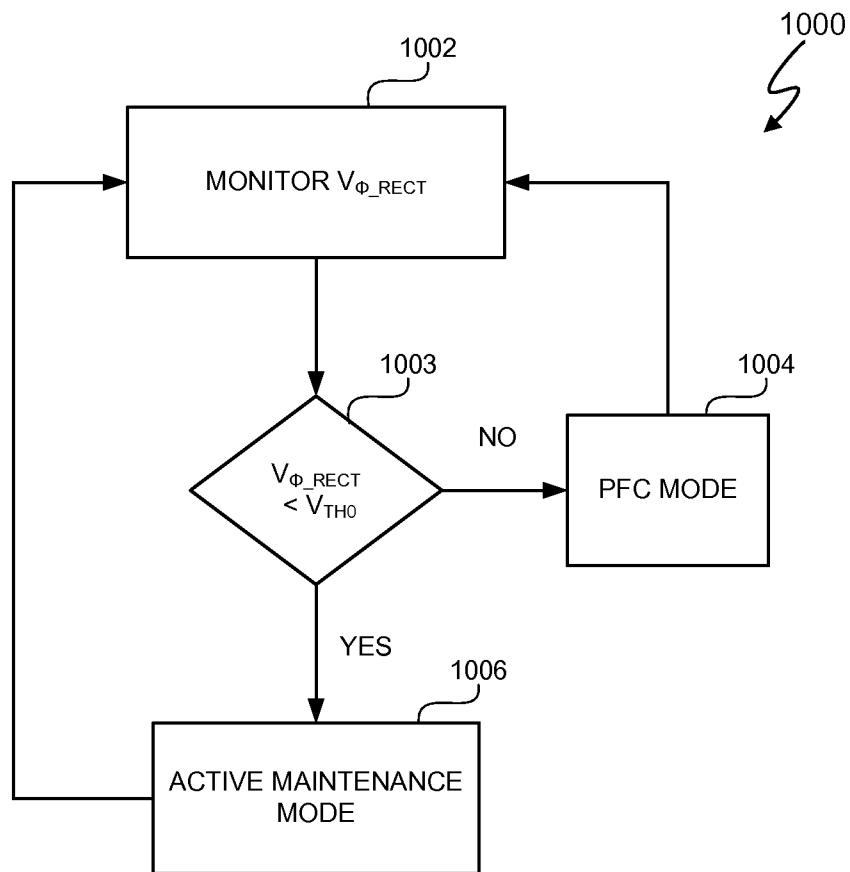
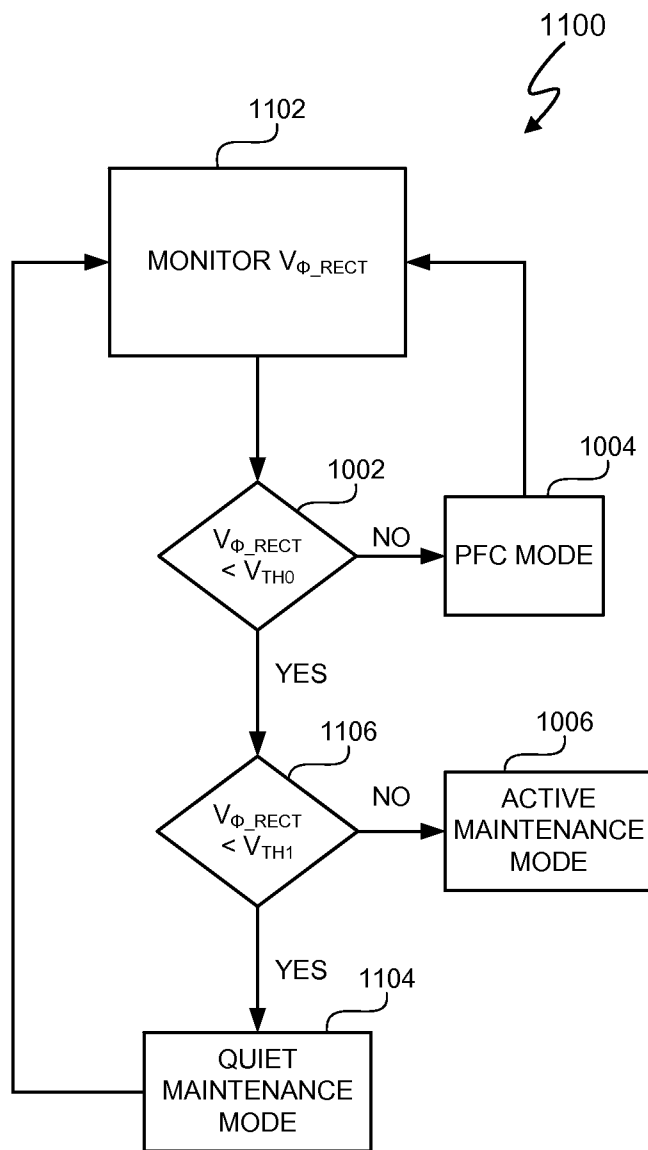


Figure 9

**Figure 10**

**Figure 11**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/51757

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G05F 1/00 (2009.01)

USPC - 315/291

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 315/291

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 315/209R, 226, 276, 291, 294 (keyword limited - see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE
Search Terms: dimmer, triac, power converter, control voltage, half-cycle, phase modulated, dimmer, switching converter, threshold, input resistance, phase delay, LED, light emitting diode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,407,514 B1 (Glaser et al.) 18 June 2002 (18.06.2002), entire document, especially; abstract, col. 1, ln 64 - col. 2, ln 12, col. 3, ln 1-15, Fig. 1	1 - 25
Y	US 7,180,250 B1 (Gannon) 20 February 2007 (20.02.2007), entire document, especially; abstract, col. 3, ln 24-34, 38-43, col. 4, ln 47-54	1 - 25
Y	US 5,055,746 A (Hu et al.) 08 October 1991 (08.10.1991), entire document, especially; abstract, col. 2, ln 54-58, col. 3, ln 1-11	2, 4, 8, 12, 14, 18

☐ Further documents are listed in the continuation of Box C.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 August 2009 (28.08.2009)

Date of mailing of the international search report

15 SEP 2009

Name and mailing address of the ISA/US

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