Title: METHOD FOR ANNEALING SILICON THIN FILMS USING CONDUCTIVE LAYER AND POLYCRYSTALLINE SILICON THIN FILMS PREPARED THEREFROM

Abstract: The present invention provides a method of annealing silicon thin film, which comprises providing a conductive layer underneath a silicon thin film, applying an electric field to the conductive layer to induce Joule heating and thereby to generate intense heat, and carrying out crystallization, elimination of crystal lattice defects, dopant activation, thermal oxidation and the like, of the silicon thin film; and a polycrystalline silicon thin film having high quality prepared by the method. The annealing method of the invention provides a polycrystalline silicon thin film which has virtually no crystal lattice defects, which is completely free from contamination by catalyst metal appearing in polycrystalline silicon thin films produced by crystallization methods such as MIC and MILC, and at the same time, is not accompanied by surface protrusions appearing in polycrystalline silicon thin films produced by ELC, while not incurring thermal deformation of glass substrate.
METHOD FOR ANNEALING SILICON THIN FILMS USING
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TECHNICAL FIELD

The present invention relates to a method of annealing silicon thin film and a
polycrystalline silicon thin film prepared by the method, and more particularly, to a
method of annealing silicon thin film, which includes providing a conductive layer
underneath a silicon thin film; applying an electric field to the conductive layer to
induce Joule heating to generate intense heat; and carrying out crystallization,
elimination of crystal lattice defects, dopant activation, thermal oxidation and the like of
the silicon thin film; and to a polycrystalline silicon thin film of high quality prepared
by the method.

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BACKGROUND ART

In general, amorphous silicon (a-Si) has disadvantages such as poor mobility of
electrons that act as charge carriers, low aperture ratio, and incompatibility to the
CMOS process. On the other hand, a polycrystalline silicon (Poly-Si) thin film device
allows an operating circuit that is necessary for inputting an image signal to pixels to be
formed on a substrate, as done in a pixel TFT-array, while this process has been
impossible with an amorphous silicon TFT (a-Si TFT). A polycrystalline silicon thin
film device does not require connection between a plurality of terminals and a driver IC, and therefore this feature makes it possible to enhance productivity and reliability as well as reducing the panel thickness. Furthermore, since a polycrystalline silicon TFT process can directly utilize the microfabrication technique for silicon LSI, formation of a microstructure in wires or the like becomes possible. Accordingly, since there is no restriction of pitch for TAB mounting of the driver IC, while such restriction is obvious in an amorphous silicon TFT, reduction in pixel size is easily achieved, and a large number of pixels can be embodied at a small viewing angle. When compared with a thin film transistor employing amorphous silicon, a thin film transistor employing polycrystalline silicon in an active layer has a high switching ability, and the location of channel in the active layer is determined through self-alignment, thus allowing the device to be small-sized and to be formed by CMOS. For such reasons, the polycrystalline silicon thin film transistor can be used as a pixel switching element in active matrix type flat panel displays (for example, liquid crystalline displays and organic EL devices) or the like, and now it is on the rise as an essential element for large screen displays and practicalization of COG (Chip On Glass) products with built-in drivers.

Such polycrystalline silicon TFTs may be manufactured at a high temperature or at a low temperature. However, in the case of manufacturing the TFTs at a high temperature, expensive materials such as quartz are required for the substrate, and thus it is not suitable for large screen displays. Therefore, active research is being conducted on the method of mass production for polycrystalline silicon from amorphous silicon thin film under a low temperature condition.

Examples of the method of forming polycrystalline silicon at a low temperature
include Solid Phase Crystallization (SPC), Metal Induced Crystallization (MIC), Metal Induced Lateral Crystallization (MILC), Excimer Laser Crystallization (ELC) and the like.

The SPC method is advantageous in obtaining a homogeneous crystal structure using inexpensive equipments. However, since a high crystallization temperature and a long processing time are required, the method is disadvantageous in that a substrate having relatively low heat deflection temperature, such as glass substrate, cannot be used, and productivity is low. According to the SPC method, crystallization is achieved only when amorphous silicon thin film is subjected to annealing typically at a temperature of 600 to 700°C for about 1 to 24 hours. Further, in the case of polycrystalline silicon prepared by the SPC method, twin-growth is observed upon solid-state phase transition from the amorphous phase to the crystalline phase, and therefore crystal grains have a large amount of crystal lattice defects. These factors cause reduction in the mobility of electrons and holes in the produced polycrystalline silicon TFT and an increase in the threshold voltage.

The MIC method has an advantage in which contact between amorphous silicon and a specific metal allows crystallization of the amorphous silicon at a temperature far lower than the crystallization temperature of the SPC method. Examples of the metal that enables use of the MIC method include Ni, Pd, Ti, Al, Ag, Au, Co, Cu, Fe, Mn and the like. These metals react with amorphous silicon to form an eutectic phase or a silicide phase, thereby promoting low temperature crystallization. However, when the MIC method is applied to the actual process of polycrystalline silicon TFT manufacture, there is a high possibility of metal contamination in the channel.
The MILC method is an adaptation of the MIC method, which includes, instead of depositing metal on a channel, forming a gate electrode thereon, then depositing a thin metal layer of on the source and drain in the self-aligned structure to prompt metal-induced crystallization, and subsequently inducing lateral crystallization toward the channel. The metals most frequently used in the MILC method are Ni and Pd. Although the polycrystalline silicon produced by MILC exhibits excellent crystallinity and high field effect mobility compared with that produced by the SPC method, the former is reported to show a high leakage current characteristic. Thus, even though the MILC method reduces the problem of metal contamination as compared with the MIC method, the problem has not been completely solved yet. On the other hand, another available method is Field Aided Lateral Crystallization (FALC), as an improvement of MILC. The FALC method shows a higher crystallization rate compared with the MILC method and exhibits anisotropy in the direction of crystallization, yet this method does not provide a perfect solution for the metal contamination problem.

The crystallization methods such as MIC, MILC and FALC are effective in that the crystallization temperature is lowered, as compared with the SPC method; however, their common drawbacks are that the duration of crystallization is still too long, and crystallization is induced by metal. Accordingly, this means they are not free from the metal contamination problem. Meanwhile, a recently developed ELC method enables preparation of polycrystalline silicon thin film on a glass substrate through a low temperature process, while solving the metal contamination problem. The amorphous silicon thin film deposited by Low Pressure Chemical Vapor Deposition (LPCVD) or Plasma Enhanced Chemical Vapor Deposition (PECVD) has a very large absorption coefficient with respect to an ultraviolet region (λ = 308 nm) which corresponds to the
wavelength of an excimer laser, and therefore melting of amorphous silicon thin film can easily occur at an appropriate energy density. When amorphous silicon thin film is subjected to crystallization by means of excimer laser, it is also accompanied with the following course of melting and solidification during a very short time. From this point of view, the ELC method is, in a strict sense, not a low temperature process. However, the ELC process involves a procedure in which crystallization is accomplished during the processes of melting and solidification which proceed very rapidly in a local melting area existing under the significant influence of the excimer laser, and therefore it is possible to produce polycrystalline silicon within an extremely short time (within a few tens of nanoseconds) without damaging the substrate. That is, when laser light is irradiated very briefly on amorphous silicon of a preformed array composed of glass substrate/dielectric layer/amorphous silicon thin film, only the amorphous silicon thin film is selectively heated, and crystallization is accomplished without damaging the glass substrate disposed underneath. Also, the advantages of the polycrystalline silicon produced during phase transition from liquid phase to solid phase are that a thermodynamically stable grain structure is obtained, and crystal defects in the grains can be markedly reduced, as compared with the polycrystalline silicon produced through solid phase crystallization. Thus, the polycrystalline silicon produced by the ELC method is superior to the products of the other crystallization methods.

Nevertheless, the ELC method has several serious drawbacks such as, for example, a problem with the laser system in which irradiation dose of the laser beam itself is not uniform; a problem with the laser process in which the area that can be used for processing with a laser energy density required in obtaining large crystal grains is extremely limited; and a problem that shot marks are left behind on the large-sized
silicon film. These factors cause irregularity in the grain size of the polycrystalline silicon thin film which constitutes an active layer of polycrystalline silicon TFT. In addition, the polycrystalline silicon produced under phase transition from liquid phase to solid phase undergoes volume expansion, a serious problem of protrusion is observed from a point where grain boundaries are formed, toward the surface. This phenomenon exerts direct influence on the gate dielectric layer in the post-processes, such that dielectric breakdown voltage is reduced, and device reliability such as hot carrier stress is critically affected, due to irregular flatness at the polycrystalline silicon/gate dielectric layer interface.

In recent years, a method of Sequential Lateral Solidification (SLS) has been developed in order to solve the stability problem of the above-described ELC method and is being successfully used in stabilizing the process region of laser energy density. However, this method still could not eliminate the problems of shot mark and protrusions toward the surface. In view of the current rapid growth of the flat panel display industry, the technology using laser in the crystallization process for the arrays having a size of 1 m × 1 m or larger, which need to be mass-produced in the near future, still has problems. Moreover, the instruments needed in conducting the ELC method and SLS method are very expensive, thus requiring high start-up and maintenance costs.

For the purpose of solving such problems of the prior art, the inventors of the present invention have suggested for the first time in KP 2004-37952, a method of conducting crystallization of silicon by preheating silicon thin film at a temperature of a range where deformation of substrate does not occur during the process, in order to generate an intrinsic carrier therein so that resistance is lowered to a value enabling Joule heating, and then applying an electric field directly to the preheated silicon film so
as to induce Joule heating by means of movement of the carrier. This method is an innovative method in view of producing polycrystalline silicon thin film having high quality at a relatively low temperature within a short time.

However, there is still a demand for a method which allows crystallization to be carried out at even a lower temperature, preferably at room temperature, within a short time, that can be applied for various applications, while more effectively achieving crystallization, dopant activation, operation of a thermal oxide film process, and elimination of crystal lattice defects.

The demand for a method of crystallization of amorphous silicon thin film has increased, in which the advantages of laser crystallization methods are exhibited such that the substrate disposed underneath is not damaged because the process is completed within a short time, and grains having high quality with virtually no defects can be generated under the high temperature phase transition; while at the same time, the disadvantages of the laser crystallization methods, such as irregular irradiation doses due to localization of the process area, restrictions in the process operation, and use of expensive equipments, are overcome. In particular, in the case of the active matrix organic light-emitting diode which has recently come into the spotlight for its applicability to the next-generation flat panel displays, the device operates in current-driven mode, whereas TFT-LCD operates in voltage-driven mode. Thus, the uniformity of grain size is a critical factor in large-size substrates. In reality, the flat panel display industry faces limitations when using a low temperature crystallization method involving ELC or SLS which makes use of laser. In consideration of such facts, expectations of a new technology for producing polycrystalline silicon thin film having high quality by means of low temperature crystallization in a non-laser mode are very
DISCLOSURE OF THE INVENTION

[Technical problem]

The present invention is intended to simultaneously solve the above problems of the prior art and the technical problems existing in the related art.

Specifically, it is an object of the invention to provide a method in which a conductive layer and a dielectric layer are successively formed on a dielectric layer formed on a transparent substrate, then a silicon thin film is formed thereon, and an electric field is applied to the conductive layer so as to induce Joule heating to generate intense heat, this intense heat in turn enabling crystallization, elimination of lattice defects, crystal growth, dopant activation and the like, in the above-mentioned amorphous silicon thin film within a very short time without damaging the substrate. Also, the invention provides a method in which, unlike the laser crystallization involving phase transition from liquid phase to solid phase, phase transition occurs in the solid state from one solid phase to another, thereby it being possible to continuously carry out deposition of amorphous silicon and successive deposition of a gate oxide film in the same reactor. That is to say, the invention provides a method which enables crystallization in an amorphous silicon/gate oxide film structure.

It is another object of the invention to provide polycrystalline silicon thin films having high quality obtained by the above-described methods.

[Solutions to the technical problem]
In order to achieve the above objects, the method of annealing silicon thin film suggested in the invention includes the steps of forming a conductive layer and then a dielectric layer successively on a dielectric layer formed on a transparent substrate; then forming a silicon thin film thereon; applying an electric field to the conductive layer so as to induce Joule heating to generate intense heat; and heat treating the silicon thin film by conduction of the intense heat generated.

The silicon thin film may be exemplified by an amorphous silicon thin film to be crystallized, an amorphous/polycrystalline mixed-phase silicon thin film, a low temperature polycrystalline silicon thin film, or a doped polycrystalline silicon thin film for dopant activation.

According to the invention, intense heat is generated within a relatively short time by applying an electric field to the conductive layer disposed underneath the silicon thin film, and this heat is transferred to the silicon thin film mainly by conduction and allows implementation of crystallization of amorphous silicon, elimination of crystal defects, dopant activation, thermal oxidation and the like. The substrate underneath does not undergo thermal deformation even though an intense heat to enable heat treatment of the silicon thin film is generated. It is because the total heat capacity of the silicon thin film which is relatively very thin compared with the substrate is very small, and thus the increase of the temperature elevation in the silicon thin film due to heat conduction is significantly higher than that in the substrate.

This result shares a similar aspect with the crystallization process of the ELC method, which is a laser crystallization method of producing polycrystalline silicon thin films having high quality, from the aspect that the process is completed at a very high
temperature within a short time. However, the method of conducting crystallization of an amorphous silicon thin film and an amorphous/polycrystalline silicon thin film over the entire area of the array, through a crystallization process similar to the laser crystallization method, by introducing a conductive layer in between a dielectric layer in the lower part and a silicon thin film in the upper part and applying an electric field to the conductive layer, and the method of conducting heat treatment to achieve elimination of crystal lattice defects and grain growth in a polycrystalline silicon thin film over the entire area of the array, as described in the invention, are all new methods that have never been reported so far.

In the case of heat treating a doped silicon thin film according to the method of the invention, the silicon thin film used herein may be a doped amorphous silicon thin film, a doped amorphous/polycrystalline mixed-phase silicon thin film, or a doped polycrystalline silicon thin film.

The conductive layer according to the invention is preferably an ITO thin film, a transparent conductive thin film of different types, or a metallic thin film, and it is more preferably an ITO thin film. Since the ITO thin film is a conductive transparent film, it is particularly suitable for a display device.

Optionally, the substrate may be preheated, before application of an electric field to the conductive layer, to the extent that deformation of the substrate does not occur.

The invention also provides a high quality polycrystalline silicon thin film crystallized by the above-described annealing method, or a polycrystalline silicon thin film having a dopant activated by the same method. The above-described problems occur when employing the method of laser crystallization that carries out a localized
crystallization process, whereas the method of the invention simultaneously carries out a crystallization process over the entire area of the thin film disposed above the conductive layer to which an electric field is applied, thus allowing rapid crystallization and activation and providing a high quality polycrystalline silicon thin film.

The annealing method of the invention and the polycrystalline silicon thin films obtained thereby have the following features or advantages compared with the conventional art.

First, the process for implementing crystallization is very simple and economically advantageous. The ELC method, one of the latest techniques, carries out the process by repeatedly scanning with a line beam, and the SLS method carries out the process by irradiating with laser through a patterned mask and then repeatedly scanning with a laser beam which moves with precision over a very short distance. Thus, non-uniformity in the intensity of laser beam across the entire area of the array is unavoidable. However, the method of the invention makes it possible to carry out crystallization and elimination of defects in an amorphous silicon thin film, an amorphous/polycrystalline mixed-phase thin film or a polycrystalline silicon thin film within a very short time across the entire area of the array, without any deformation of the substrate. Moreover, the ELC method requires, as a preliminary step to irradiation with laser, an additional dehydrogenating annealing process for removing hydrogen from the amorphous silicon thin film such that it is more complicated than the method of the invention.

Secondly, the equipment for implementing the process of the invention is inexpensive, and techniques already established in the art can be used. The ELC
method or the like which provides an excellent crystallization effect employs expensive equipment including a laser apparatus. On the other hand, since the equipment required in carrying out the method of the invention is already well established in the semiconductor and flat panel display industries, the process of the invention can be carried out by directly applying the conventional techniques or through slight modification of the conventional techniques.

Thirdly, the method of the invention is suitable for mass production of polycrystalline silicon thin films having uniformity and high quality. According to the invention, crystallization proceeds over the entire area of the array at a low temperature within a short time, and thus the method of the invention is advantageous in treating a substrate having a large area. The polycrystalline silicon thin film obtained by the above method can provide a crystallization product having high quality with no surface protrusions.

Fourthly, the method of the invention can be used in a low temperature dopant activation process. There is possibility that the method of the invention may be effectively applied to the crystallization as well as to the heat treatment for activation of an ion-implanted dopant in the vicinity of a source/drain electrode in the TFT structure at a low temperature.

Fifthly, the method of the invention is capable of continuous deposition of a gate oxide film in a manner similar to that of an amorphous silicon TFT production process. In a TFT of MOSFET structure, the film quality of the gate oxide film as well as the silicon/gate oxide film interface play very important roles in the electrical properties of a TFT device. In an amorphous TFT production process, amorphous silicon and a gate
oxide film are sequentially deposited in the same chamber using the PECVD method, and thus the properties of the silicon/gate oxide film interface are excellent. On the contrary, in the case of an LTPS production process, since the crystallization technique currently employed for mass production is a laser process, deposition of amorphous silicon is carried out by the PECVD method, and laser crystallization is carried out after dehydrogenation in a heat treatment furnace. On the polycrystalline silicon thin film that has been crystallized by using a laser, a gate oxide film is deposited according to the PECVD method. In other words, continuous deposition that is employed in the amorphous silicon TFT production process is impossible. However, since the crystallization technique of the invention is a non-laser process, continuous deposition is possible.

Sixthly, a high temperature polycrystalline silicon process can be embodied at a low temperature. In the case of a high temperature polycrystalline silicon process using quartz as transparent substrate, a low temperature polycrystalline silicon film having a relatively large grain-size (but having many crystal lattice defects such as twin) is prepared by heat treatment for an extended time at a temperature of 600°C or lower, and thereafter a gate oxide film is deposited. In the case of a low temperature polycrystalline silicon process, the oxide film is deposited by the PECVD method because of the temperature limitations of the glass substrate, whereas in the case of the high temperature polycrystalline silicon process, there is no limitation on the substrate temperature, and thus a thermal oxidation process is employed. When the thermal oxidation process is used at a temperature of 900°C or higher, it is possible to produce a gate oxide film having excellent film texture, and also the crystal lattice defects present in the low temperature polycrystalline silicon film which is disposed underneath the
gate oxide film, are eliminated during the thermal oxidation process. According to the
invention, since a temperature of 1000°C or higher is reached instantaneously
(preferably, within 1 second), it becomes possible to implement the thermal oxidation
process on a glass substrate that is vulnerable to heat, by a method of repeating field
application under an atmosphere of oxygen, ozone or steam.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram illustrating the constitution of a specimen for
preparation of polycrystalline silicon thin film according to one embodiment of the
invention;

Fig. 2 is a schematic diagram illustrating the method of simultaneously carrying
out crystallization of amorphous silicon thin film and heat treatment for dopant
activation, after the respective formation of the source/drain and gate, according to one
embodiment of the invention;

Fig. 3 is a schematic diagram illustrating the method of simultaneously carrying
out the process of crystallization of amorphous silicon thin film and the process of
thermal oxidation by applying an electric field by the same method as in Fig. 1 under an
oxygen atmosphere, according to one embodiment of the invention;

Fig. 4 is a schematic diagram illustrating the method of heat treating a
polycrystalline silicon thin film that has been crystallized preliminarily through low
temperature heat treatment by applying an electric field by the same method as in Fig. 1,
according to one embodiment of the invention;
Fig. 5 is a schematic diagram illustrating the method of forming a thermal oxide film on the polycrystalline silicon thin film that has been crystallized preliminarily through low temperature heat treatment by applying an electric field by the same method as in Fig. 1 under an oxygen atmosphere, according to one embodiment of the invention;

Fig. 6 is a schematic diagram illustrating the method of depositing an amorphous silicon thin film and continuously depositing a gate oxide film thereon in the same CVD reactor, and then heat treating the amorphous silicon thin film by applying an electric field by the same method as in Fig. 1, according to one embodiment of the invention;

Fig. 7 is a schematic diagram illustrating the method of depositing an amorphous silicon thin film and a gate oxide film continuously, and then heat treating a polycrystalline silicon thin film that has been crystallized preliminarily through low temperature heat treatment by applying an electric field by the same method as in Fig. 1, according to one embodiment of the invention;

Fig. 8 is a graph illustrating the power density measured in accordance with the time for field application during the application of an electric field to the conductive layer in Example 1;

Fig. 9 shows (a) a photograph of a specimen of Example 1 having an amorphous silicon thin film of before application of an electric field, at room temperature, (b) a photograph showing luminescence of the silicon thin film caused by high temperature heating due to Joule heating upon field application, and (c) a photograph of the specimen with the silicon thin film converted to a polycrystalline silicon thin film after one field application at room temperature;
Fig. 10 is a graph illustrating the results of Raman analysis of the polycrystalline silicon thin film of Example 1 after annealing;

Fig. 11 is a photograph (magnification: × 60,000) showing the results of Bright Field TEM analysis of the polycrystalline silicon thin film of Example 1 after annealing;

Fig. 12 shows (a) a photograph of a specimen of Example 2 having an amorphous silicon thin film before application of an electric field, at room temperature; (b) a photograph showing luminescence of the silicon thin film caused by high temperature heating due to Joule heating upon field application, and (c) a photograph of the specimen with the silicon thin film converted to a polycrystalline silicon thin film after one field application at room temperature; and

Fig. 13 is a photograph (magnification: × 100,000) showing the results of Dark Field TEM analysis of the polycrystalline silicon thin film of Example 2 after annealing.

Reference Numerals

10  Substrate
20  First Dielectric Layer
30  Conductive Layer
40  Second Dielectric Layer
50  Amorphous Silicon Thin Film
60  Thermal Oxide Film
70  Continuously Deposited Gate Oxide Film
BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, embodiments of the invention will be described in detail with reference to drawings, which are not, however, intended to limit the scope of the invention.

5 Fig. 1 shows a schematic diagram of the constitution of the substrate according to one embodiment of the invention for crystallization of amorphous silicon thin film.

According to Fig. 1, on substrate 10, a first dielectric layer 20, a conductive layer 30, a second dielectric layer 40 and an amorphous silicon (a-Si) thin film 50 are successively formed, and an electric field is applied to the conductive layer 30.

10 The material for substrate 10 is not particularly limited, and transparent substrate materials such as, for example, glass, quartz and plastics can be used, while glass is more preferred in the economical aspect. However, according to the recent research trend in the field of flat panel display, researches are being conducted extensively on plastic-based substrates having excellent impact resistance and processability, and the method of the invention can be directly applied to such plastic-based substrates.

The first dielectric layer 20 is used for the purpose of preventing effluence of substance contained in the substrate 10, which may possibly be generated in the subsequent processes, for example, an alkali substance in the case of a glass substrate. This layer is generally formed by depositing silicon oxide (SiO₂) or silicon nitride, and the thickness is preferably in the range of 2,000 to 5,000 Å, without being limited to this range. Depending on the progress of technology in the future, an amorphous silicon thin film may be possibly formed directly on the substrate without the dielectric layer 20, and since the method of the invention is applicable to such structure, it is to be
understood that the scope of the invention includes such structure.

Conductive layer 30 is a thin layer of electrically conductive material and can be formed by, for example, sputtering, vacuum evaporation or the like. The conductive layer 30 needs to maintain a uniform thickness so as to have uniform heating during Joule heating process caused by the following field application.

The second dielectric layer 40 takes the role of preventing contamination of the amorphous silicon thin film 50 by the conductive layer 30 during the annealing process, and the role of insulating the TFT device. The layer can be formed from the same materials as those used for the first dielectric layer 20.

The amorphous silicon thin film 50 can be formed by, for example, low pressure chemical vapor deposition, high pressure chemical vapor deposition, plasma enhanced chemical vapor deposition (PECVD), sputtering, vacuum evaporation or the like, but the PECVD method is preferably used. The thickness of the thin film is preferably in the range of 300 to 1000 Å, without being limited to this range.

Prior to the application of an electric field to the conductive layer 30, the above-mentioned constituents, namely, 10, 20, 30, 40 and 50, or at least substrate 10, may be preliminarily heated to an appropriate temperature range. This appropriate temperature range means a temperature range where substrate 10 is not damaged throughout the process, and preferably corresponds to a range of temperature lower than the heat deflection temperature of the substrate 10. The method of preheating is not particularly limited, and for example, methods such as placing the array in a general heat treatment furnace and irradiating radiant heat of a lamp or the like, may be used.

Application of an electric field to the conductive layer 30 is carried out by
applying energy with a power density that can generate sufficiently intense heat to
induce crystallization of amorphous silicon thin film 50 as described above by Joule
heating. The amount of this energy is determined by various factors such as resistance
of the conductive material, and length and thickness of the conductive layer 30, and thus
5 cannot be specified. The electric current to be applied may be direct current or
alternating current. The duration of the field application may be 1/1,000,000 to 100
seconds as the time taken for continuous application, and it is preferably from 1/10,000
to 10 seconds, and more preferably from 1/1,000 to 1 second. Such application of an
electric field can be repeated a number of times on a regular basis or an irregular basis.
10 Therefore, the total heat treatment time may be longer than the above-described
duration of field application, but this heat treatment time is very short when compared
with at least the treatment times of conventional crystallization methods.

In some cases, a structure in which the positions of the conductive layer 30 and
the amorphous silicon thin film 50 are exchanged may be also used.

Fig. 2 presents, as another embodiment of the invention, a schematic diagram
illustrating the process of simultaneously carrying out crystallization and dopant
activation by applying an electric field by using the same method as in Fig. 1. After
deposition of amorphous silicon thin film 50, the patterning process is accomplished
with respect to individual TFT devices through a lithography process. A gate oxide film
42 is deposited thereon by the PECVD method, and then a gate electrode 44 is
deposited by sputtering. In order to form the gate electrode 44, patterning is performed
by a lithography process and an etching process. Thus prepared self-aligned gate
structure is ion-implanted with a dopant to form a source and drain, and then by
applying an electric field by the same method as in Fig. 1, crystallization and dopant
activation are simultaneously carried out. Since the ITO thin film 30, which is the conductive layer, does not electrically short-circuit, the above-described process is possible.

Fig. 3 presents, as another embodiment of the invention, a schematic diagram illustrating the method of simultaneously carrying out the processes of crystallization and thermal oxidation by applying an electric field by using the same method as in Fig. 1. Since the temperature of the amorphous silicon thin film 50 is elevated to at least 1000°C or higher upon Joule heating according to the invention, a thermal oxidation process under an oxygen atmosphere is possible. Optionally, the process can be carried out under an ozone atmosphere or steam atmosphere, or even in deionized water, instead of an oxygen atmosphere. In general, during the production of TFT device, a thermal oxide film having excellent properties cannot be used because of the thermal weakness of glass substrate 10, and a PECVD oxide film is deposited. However, according to the invention, since an electric field is applied for only a short time, production of a very thin thermal oxide film 60 can be carried out simultaneously with the crystallization, in a manner such that electric fields are repeatedly applied under an oxygen atmosphere. By depositing thereon a relatively thick oxide film (not shown in the figure) by the PECVD method, the process of the TFT production can be embodied, and the characteristics of Si/SiO₂ interface can be improved in this way.

Fig. 4 presents, as another embodiment of the invention, a schematic diagram illustrating the method of heat treating a polycrystalline silicon thin film that has been preliminarily crystallized through low temperature heat treatment, by applying an electric field by the same method as in Fig. 1. In general, a low temperature polycrystalline silicon thin film has an advantage that the size of crystal grains is larger...
than that of high temperature polycrystalline silicon, but it contains many crystal lattice defects such as twin in the grains. According to the method of the invention, since a high temperature process can be carried out without thermal deformation of the glass substrate 10, a large-sized polycrystalline silicon thin film which is free from crystal lattice defects can be produced by the method of conducting high temperature heat treatment of polycrystalline silicon thin film 52 that has been preliminarily crystallized at a low temperature by applying an electric field.

Fig. 5 presents, as another embodiment of the invention, a schematic diagram illustrating the method of forming a thermal oxide film on a polycrystalline silicon thin film that has been preliminarily crystallized through low temperature heat treatment, by applying an electric field by using the same method as in Fig. 1 under an atmosphere of oxygen, ozone or steam or in deionized water. The process illustrated in Fig. 5 is the same process as the process for producing high temperature polycrystalline silicon thin film using a quartz substrate in general. In the case of the thermal oxidation process, it is impossible to use a glass substrate because a high temperature above 900°C under an oxygen atmosphere is required. In the case of the method of the invention, since a high temperature is reached within an extremely short time, it is possible to form thermal oxide film 60 without incurring thermal deformation of the glass substrate 10. However, the thermal oxidation process is achieved through repetition of heating upon field application and cooling upon field removal. Since the thickness of the thermal oxide film 60 deposited by the process of the invention is very small, an additional PECVD oxide film process is added to form a gate oxide film (not shown in the figure). That is to say, implementation of the process of the invention can result in improvement of the characteristics of the interface between the gate oxide film and the polycrystalline
silicon thin film. Furthermore, a large quantity of crystal lattice defects present in the low temperature polycrystalline silicon can be removed during the thermal oxidation process.

Fig. 6 presents, as another embodiment of the invention, a schematic diagram illustrating the method of continuously depositing amorphous silicon thin film 50 and gate oxide film 70 in the same CVD chamber, and then conducting heat treatment by applying an electric field by using the same method as in Fig. 1. In general, the gate oxide film formed by continuous deposition is advantageous in that the interface properties are excellent, but it cannot be used in a laser process. Since the method of the invention is a non-laser process, a gate oxide film formed by continuous deposition can be used, thereby resulting in an improvement of the device properties and simplification of the process.

Fig. 7 presents, as another embodiment of the invention, a schematic diagram illustrating the method of continuously depositing amorphous silicon thin film 50 and gate oxide film 70, and then heat treating the thin film 52 that has been preliminarily crystallized through low temperature heat treatment, by applying an electric field by using the same method as in Fig. 1. By using this method, a polycrystalline silicon thin film having large-sized grains and a small quantity of defects, and a gate oxide film having excellent interface properties can be obtained at the same time.

The Joule heating as used in the method of the invention, which takes place in the conductive layer by the field application, is defined as heating with a heat generated due to resistance of a conductive material upon flow of an electric current.

The amount of energy per unit time applied to the conductive layer by Joule
heating due to field application can be expressed by the following formula:

$$W = V \times I$$

In the above formula, $W$ is defined as the amount of energy per unit time supplied by Joule heating, $V$ as the voltage applied to both ends of the conductive layer, and $I$ as the current.

It can be seen from the above formula that as the voltage ($V$) increases, and/or as the current ($I$) increases, the amount of energy per unit time applied to the conductive layer by Joule heating also increases. When the temperature of the conductive layer increases by Joule heating, there occurs heat conduction to the silicon thin film disposed above the conductive layer and the substrate (for example, glass substrate) disposed underneath the conductive layer. Thus, in order to elevate the temperature of the silicon thin film to a temperature which enables crystallization or dopant activation, by heat conduction without incurring thermal deformation of the glass substrate, an appropriate voltage and current are applied to the specimen for a short time in the method of the invention. In case the amount of applied energy is sufficient, the process can be completed with a single shot, while in case the amount is insufficient, the crystallization process can be accomplished with several shots at an appropriate time interval.

As described above, according to the conventional MIC method, MILC method and other crystallization methods, there have been cases where an electric field or magnetic field is applied in order to accelerate vertical induction or lateral induction of catalytic metal at a low temperature, and other cases where an electric field is applied to a very small specimen (for example, 250 μm × 50 μm) for a very short time (in the order of μsec) through a patterning process to achieve crystallization through a metallic
conductive film (Cr) disposed above. However, in none of these cases, crystallization was carried out over the entire area of the substrate without a patterning process, by applying an electric field to a conductive layer disposed underneath the silicon thin film requiring heat treatment, more particularly, to the conductive layer disposed underneath the silicon thin film across the dielectric layer, and using the conductive heat generated by Joule heating of the conductive layer.

Another factor for comparison of the invention with the conventional methods is the duration of the electric field application, and the duration of the field application (duration of a single application) in the method of the invention is preferably from 1/1,000 to 1 sec as described above. Such a short time for crystallization allows crystallization or dopant activation to be achieved in the silicon thin film above without deformation of the substrate underneath (for example, glass substrate), in spite of the conductive layer being heated to a very high temperature.

EXAMPLES

Hereinafter, the invention will be described in detail with reference to Examples, which are not intended to limit the scope of the invention by any means.

[Example 1]

A SiO₂ layer (first dielectric layer) having a thickness of 3000 Å was formed on a glass substrate having a size of 2 cm in width × 2 cm in length × 0.7 mm in thickness, by the PECVD method. An ITO thin film (conductive layer) having a thickness of 1000 Å was deposited on the first dielectric layer by sputtering, and then a SiO₂ layer (second
dielectric layer) having a thickness of 1000 Å was deposited thereon by PECVD. An amorphous silicon thin film having a thickness of 500 Å was deposited on the second dielectric layer by PECVD. Thus, an array including an amorphous silicon thin film as shown in Fig. 1 was prepared. Resistance of the conductive layer was measured to be 20 Ω.

The process of applying an electric field of 300 V-15 A for 0.05 second to the conductive layer of thus prepared specimen was repeated five times in total at room temperature. As a result, field application was carried out for approximately 0.25 second in total. The amount of energy applied to the conductive layer in such a single field application was 1125 Watt/cm². The waveform of power density measured in accordance with the application time during field application to the conductive layer is presented in Fig. 8.

In Fig. 9, (a) is a photograph of the specimen showing the amorphous silicon thin film at room temperature before field application, (b) is a photograph showing luminescence of the silicon thin film caused by high temperature heating due to Joule heating during field application, and (c) is a photograph of the specimen having the silicon thin film converted to a polycrystalline silicon thin film after one field application. From the luminescence phenomenon in (b), it can be conjectured that an instantaneous temperature at the conductive layer is elevated to at least 1000°C or above. Such intense heat is conducted to the silicon thin film disposed above and induces crystallization of the amorphous silicon.

Fig. 10 shows the results of performing a Raman analysis of the silicon thin film after such heat treatment. It can be seen from Fig. 10 that the amorphous silicon thin
film has been converted 100% to a polycrystalline state.

Fig. 11 shows the results of performing a Bright Field TEM analysis of the silicon thin film after such heat treatment. In Fig. 11, the microstructure of the polycrystalline silicon thin film prepared according to the invention exhibits the structure of a polycrystalline silicon thin film prepared at high temperature. That is, although the crystal grain size is smaller than that of a low temperature polycrystalline silicon thin film, the morphology of the grain is polygonal, and the quantity of crystal lattice defects, such as twins, in the grain has been significantly reduced. It was confirmed that in spite of such crystallization heat treatment, the glass substrate disposed underneath the conductive layer did not undergo deformation at all.

[Example 2]

A SiO₂ layer (first dielectric layer) having a thickness of 3000 Å was formed on a glass substrate having a size of 2 cm in width × 2 cm in length × 0.7 mm in thickness, by the PECVD method. An ITO thin film (conductive layer) having a thickness of 1500 Å was deposited on the first dielectric layer by sputtering, and then a SiO₂ layer (second dielectric layer) having a thickness of 1000 Å was deposited thereon by PECVD. An amorphous silicon thin film having a thickness of 500 Å was deposited on the second dielectric layer by PECVD. Thus, an array including an amorphous silicon thin film as shown in Fig. 1 was prepared. Resistance of the conductive layer was measured to be 10 Ω.

The process of applying an electric field of 300 V-30 A for 0.009 second to the conductive layer of thus preheated specimen was repeated fifty times in total. The amount of energy per unit time applied to the conductive layer in the field applications
was 3000 Watt/cm².

In Fig. 12, (a) is a photograph of the specimen showing the amorphous silicon thin film at room temperature before the field application, (b) is a photograph showing luminescence of the silicon thin film caused by high temperature heating due to Joule heating during the field application, and (c) is a photograph of the specimen having the silicon thin film converted to a polycrystalline silicon thin film after one field application. From the white luminescence phenomenon in (b), it can be conjectured that an instantaneous temperature at the conductive layer is elevated to at least 1000°C or above. Such intense heat is conducted to the silicon thin film disposed above and induces crystallization of the amorphous silicon.

Fig. 13 shows the results of performing a Dark Field TEM analysis of the silicon thin film after such heat treatment. In Fig. 11, the microstructure of the polycrystalline silicon thin film prepared according to the invention exhibits the structure of a nanosized polycrystalline silicon thin film. This microstructure is only achieved with difficulties at a high temperature, solid-phase crystallization which is carried out in a tube furnace or by means of RTA (Rapid Thermal Annealing), and it is a structure reported for the first time by the invention. In the method of the invention, since the heating rate exceeds at least 100,000°C/sec, a microstructure formed at a high temperature is reflected intactly. On the other hand, even in the case of RTA with the highest heating rate among conventional heat treatment methods, because the heat treatment rate is only about 100°C/sec, phase transition to polycrystalline silicon occurs in the course of heating, and thus the desired microstructure formed at a high temperature cannot be reflected. The polycrystalline silicon produced in this Example has grains of very small size and shows grains of equiaxed morphology. This structure
is a microstructure which cannot be obtained in other heat treatment methods, and since uniformity in the grain size is assured, the structure is expected to be very suitable for OLED applications. It was confirmed that in spite of such crystallization heat treatment, the glass substrate disposed underneath the conductive layer did not undergo deformation at all.

INDUSTRIAL APPLICABILITY

As described above, the annealing method according to the present invention provides a polycrystalline silicon thin film which is completely free from the problem of contamination by catalyst metal appearing in polycrystalline silicon thin films produced by crystallization methods such as the MIC and MILC methods, and at the same time, is not accompanied by surface protrusions appearing in polycrystalline silicon thin films produced by the ELC method, while not causing thermal deformation of the glass substrate and markedly reducing the quantity of crystal lattice defects. This technique for preparation of polycrystalline silicon thin film constitutes the features of the invention which has not been reported in the related art.

A person having ordinary skill in the art that pertains to the invention would be able to carry out various modifications and applications based on the description above.
WHAT IS CLAIMED IS:

1. A method of annealing silicon thin film, comprising the steps of forming a conductive layer on a first dielectric layer disposed on a transparent substrate, subsequently forming a second dielectric layer and then a silicon thin film thereon, applying an electric field to the conductive layer to induce Joule heating and thereby to generate intense heat, and heat treating the silicon thin film by means of thus generated intense heat.

2. The method according to claim 1, wherein crystallization of an amorphous silicon thin film, an amorphous/polycrystalline mixed-phase silicon thin film, or a polycrystalline silicon thin film is carried out by the annealing method.

3. The method according to claim 1, wherein crystallization and dopant activation of a doped amorphous silicon thin film, a doped amorphous/polycrystalline mixed-phase silicon thin film, or a doped polycrystalline silicon thin film are carried out by the annealing method.

4. The method according to claim 1, wherein crystallization and thermal oxidation of an amorphous silicon thin film, an amorphous/polycrystalline mixed-phase silicon thin film, or a polycrystalline silicon thin film are simultaneously carried out by the annealing method under an oxygen, ozone or steam atmosphere.

5. The method according to claim 1, wherein thermal oxidation of a polycrystalline silicon thin film is carried out by the annealing method under an oxygen, ozone or steam atmosphere.

6. The method according to claim 1, wherein the substrate is a glass substrate or a
plastic substrate.

7. The method according to claim 1, wherein the conductive layer is an ITO thin film or a transparent conductive film of other types.

8. The method according to claim 1, wherein the conductive layer is a metallic thin film.

9. The method according to claim 1, wherein the dielectric layer is a silicon oxide layer or a silicon nitride layer.

10. The method according to claim 1, which further comprises a step of preheating the array to a temperature range in which deformation of the substrate does not occur, before applying an electric field to the conductive layer.

11. The method according to claim 1, wherein a gate dielectric film is deposited on the silicon layer by continuous deposition in the same reactor.

12. A polycrystalline silicon thin film prepared by the method according to any one of claims 1 to 11.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 21/324

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 G02F 1/1343, 1/136, H01L 21/20, 21/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

KOREAN PATENTS AND APPLICATIONS FOR INVENTION SINCE 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

KIPONET

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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  "O" document referring to an oral disclosure, use, exhibition or other means
  "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

14 NOVEMBER 2005 (14.11.2005)

Date of mailing of the international search report

15 NOVEMBER 2005 (15.11.2005)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
920 Dunsan-dong, Seo-gu, Daejeon 302-701,
Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer

KIM, Kap Byung
Telephone No. 82-42-481-5730
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[Fig. 8]  

[Fig. 9]  

(a)  

(b)  

(c)  

SUBSTITUTE SHEET (RULE 26)
Fig. 10

Fig. 11

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