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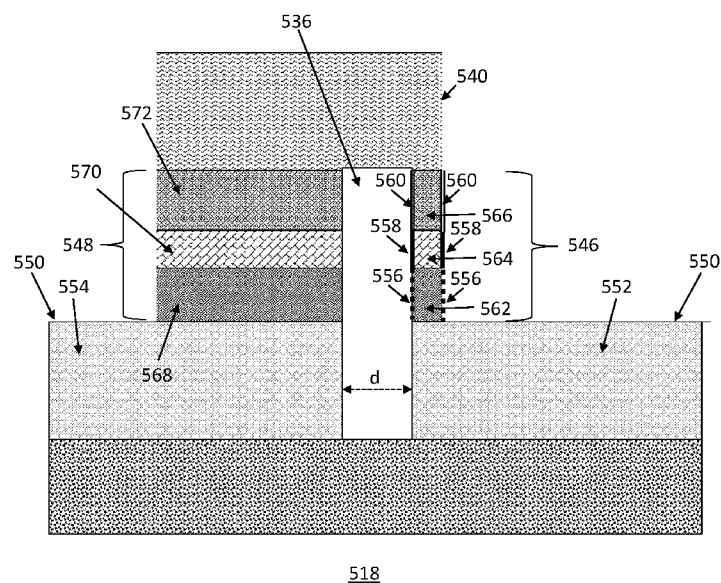
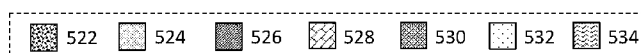


FIG. 5J



(57) Abstract: Described herein are structures that include Josephson Junctions (JJs) to be used in quantum circuits. An exemplary method for fabricating JJs includes providing a stack of a base superconductive (SC) wire layer, a junction base SC layer, and a junction tunnel barrier layer, and providing an opening through the stack. The method also includes filling the opening with a sacrificial material, and providing a top SC wire layer patterned to form a bridge over the opening and a window for removal of the sacrificial material under the bridge. The method further includes patterning the stack to form the JJ and an interconnect portion, separated from one another by the opening, and removing the sacrificial material through the window to provide a gap between the JJ and the interconnect portion. Such a method advantageously allows producing high performance JJs and can be efficiently used in large-scale manufacturing.

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JOSEPHSON JUNCTIONS FORMED BY PARTIALLY SUBTRACTIVE FABRICATIONTechnical Field

[0001] This disclosure relates generally to the field of quantum computing, and more specifically, to Josephson Junctions for use in quantum circuits and to methods of fabricating thereof.

Background

[0002] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0003] To provide a more complete understanding of the present disclosure and features and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying figures, wherein like reference numerals represent like parts, in which:

[0004] FIG. 1A provides a schematic illustration of a superconducting quantum circuit, according to some embodiments of the present disclosure.

[0005] FIG. 1B provides a schematic illustration of an exemplary physical layout of a superconducting quantum circuit, according to some embodiments of the present disclosure.

[0006] FIG. 1C provides a schematic illustration of an exemplary transmon, according to some embodiments of the present disclosure.

[0007] FIG. 2 provides a schematic illustration of an exemplary quantum computing device, according to some embodiments of the present disclosure.

[0008] FIGs. 3A-3C provide a schematic illustration of a photoresist mask provided over a substrate for fabricating a Josephson Junction using a double-angle shadow evaporation approach.

[0009] FIGs. 4A-4C provide a schematic illustration of fabricating Josephson Junctions using a conventional double-angle shadow evaporation approach.

[0010] FIGs. 5A-5J provide a schematic illustration of partially subtractive fabrication of Josephson Junctions, according to some embodiments of the present disclosure.

[0011] FIG. 6 provides a flow chart of a method for partially subtractive fabrication of Josephson Junctions, according to some embodiments of the present disclosure.

[0012] FIG. 7 provides a schematic illustration of a Josephson Junction fabricated using the partially subtractive fabrication method described herein, according to some embodiments of the present disclosure.

Detailed Description

Overview

[0013] As previously described herein, quantum computing, or quantum information processing, refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. One example of quantum-mechanical phenomena is the principle of quantum superposition, which asserts that any two or more quantum states can be added together, i.e. superposed, to produce another valid quantum state, and that any quantum state can be represented as a sum of two or more other distinct states. Quantum entanglement is another example of quantum-mechanical phenomena. Entanglement refers to groups of particles being generated or interacting in such a way that the state of one particle becomes intertwined with that of the others. Furthermore, the quantum state of each particle cannot be described independently. Instead, the quantum state is given for the group of entangled particles as a whole. Yet another example of quantum-mechanical phenomena is sometimes described as a “collapse” because it asserts that when we observe (measure) particles, we unavoidably change their properties in that,

once observed, the particles cease to be in a state of superposition or entanglement (i.e. by trying to ascertain anything about the particles, we collapse their state).

[0014] Put simply, superposition postulates that a given particle can be simultaneously in two states, entanglement postulates that two particles can be related in that they are able to instantly coordinate their states irrespective of the distance between them in space and time, and collapse postulates that when one observes a particle, one unavoidably changes the state of the particle and its' entanglement with other particles. These unique phenomena make manipulation of data in quantum computers significantly different from that of classical computers (i.e. computers that use phenomena of classical physics). Classical computers encode data into binary values, commonly referred to as bits. At any given time, a bit is always in only one of two states – it is either 0 or 1. Quantum computers use so-called quantum bits, referred to as qubits (both terms “bits” and “qubits” often interchangeably refer to the values that they hold as well as to the actual devices that store the values). Similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1. However, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states. Entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0015] Compared to well-established and thoroughly researched classical computers, quantum computing is still in its infancy, with the highest number of qubits in a solid-state quantum processor currently being about 10. One of the main challenges resides in protecting qubits from decoherence so that they can stay in their information-holding states long enough to perform the necessary calculations and read out the results. For this reason, materials, structures, and fabrication methods used for building qubits should continuously focus on reducing spurious (i.e. unintentional and undesirable) two-level systems (TLS's), thought to be the dominant source of qubit decoherence. In general, as used in quantum mechanics, a two-level (also referred to as “two-state”) system is a system that can exist in any quantum superposition of two independent and physically distinguishable quantum states. Also for the reason of protection from decoherence, qubits are often operated at cryogenic temperatures, typically just a few degrees or even just a few millidegrees above absolute zero because

cryogenic temperatures minimize the detrimental effects of spurious TLS's. None of these challenges ever had to be addressed for classical computers.

[0016] As the foregoing illustrates, ability to manipulate and read out quantum states, making quantum-mechanical phenomena visible and traceable, and ability to deal with and improve on the fragility of quantum states of a qubit present unique challenges not found in classical computers. These challenges explain why so many current efforts of the industry and the academics continue to focus on a search for new and improved physical systems whose functionality could approach that expected of theoretically designed qubits. Physical systems for implementing qubits that have been explored until now include e.g. superconducting qubits, single trapped ion qubits, Silicon (Si) quantum dot qubits, photon polarization qubits, etc.

[0017] Out of the various physical implementations of qubits listed above, superconducting qubits are promising candidates for building a quantum computer.

[0018] All of superconducting qubits operate based on the Josephson effect, which refers to a macroscopic quantum phenomenon of supercurrent, i.e. a current that, due to zero electrical resistance, flows indefinitely long without any voltage applied, across a device known as a Josephson Junction. Josephson Junctions are integral building blocks in superconducting quantum circuits where they form the basis of quantum circuit elements that can approximate functionality of theoretically designed qubits. Therefore, improvements with respect to fabricating Josephson Junctions for use in superconducting qubits are always desirable. In particular, it would be desirable to have methods for fabricating Josephson Junctions that have adequate performance and can be manufactured on large scale.

[0019] Described herein are structures that include Josephson Junctions (JJs) to be used in quantum circuit components, in particular in superconducting qubits of quantum circuits disposed on a substrate, and a method for fabricating such structures. The proposed method may result in high performance JJs, compared to JJs fabricated using existing techniques. In addition, the proposed method can be efficiently used in large-scale manufacturing, providing a substantial improvement with respect to conventional approaches, such as e.g. double-angle shadow evaporation approach, which include fabrications steps that are not suitable for implementing with larger wafer sizes used by leading edge device manufactures.

[0020] In one aspect of the present disclosure, the proposed method includes providing over a substrate a stack of a base superconductive (SC) wire layer, a junction base SC layer disposed over the base SC wire layer, and a junction tunnel barrier layer disposed over the junction base SC layer. The method also includes providing an opening through the stack (i.e. the opening extends from the surface to the bottom of the stack and ends at a layer on which the stack is disposed, e.g. at the substrate), filling the opening with a sacrificial material, and providing a top SC wire layer patterned to form a bridge over the opening and a window for removal of the sacrificial material under the bridge. The method further includes patterning the stack to form the JJ and an interconnect portion, separated from one another by the opening, and removing the sacrificial material through the window to provide a gap between the JJ and the interconnect portion. Such an approach is referred to in the following as a “partially subtractive fabrication” to highlight the fact that it involves subtractive patterning in combination with addition of the sacrificial material.

[0021] For the purposes of the present disclosure, the terms such as “upper,” “lower,” “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0022] The phrase “A and/or B” means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term “between,” when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation “A/B/C” means (A), (B), and/or (C).

[0023] The description uses the phrases “in an embodiment” or “in embodiments,” which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions

such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale.

[0024] As used herein, terms indicating what may be considered an idealized behavior, such as e.g. "superconducting" or "lossless", are intended to cover functionality that may not be exactly ideal but is within acceptable margins for a given application. For example, a certain level of loss, either in terms of non-zero electrical resistance or non-zero amount of spurious TLS's may be acceptable such that the resulting materials and structures may still be referred to by these "idealized" terms. One metric of interest may be the decay rate associated with these losses (e.g. losses either from TLS's or residual resistance), and as long as the decay rate associated with these mechanisms is not worse than needed in order to achieve a fault-tolerant quantum calculation, then the losses are deemed acceptable and the idealized terms (e.g. superconducting or lossless) - appropriate. Specific values associated with an acceptable decay are expected to change over time as fabrication precision will improve and as fault-tolerant schemes may become more tolerant of higher decay rates. An adapted version of this metric, as well as other metrics suitable for a particular application in determining whether certain behavior may be referred to using idealized terms, are within the scope of the present disclosure.

[0025] Furthermore, while the present disclosure includes references to microwave signals, this is done only because current qubits are designed to work with such signals because the energy in the microwave range is higher than thermal excitations at the temperature that qubits are operated at. In addition, techniques for the control and measurement of microwaves are well known. For these reasons, typical frequencies of qubits are in 5-10 gigahertz (GHz) range, in order to be higher than thermal excitations, but low enough for ease of microwave engineering. However, advantageously, because excitation energy of qubits is controlled by the circuit elements, qubits can be designed to have any frequency. Therefore, in general, qubits could be designed to operate with signals in other ranges of electromagnetic spectrum and embodiments of the present disclosure could be modified accordingly. All of these alternative implementations are within the scope of the present disclosure.

[0026] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may

be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0027] Furthermore, in the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0028] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure. However, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment(s). Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

Basics of Josephson Junctions

[0029] As previously briefly explained above, quantum computing refers to the use of quantum mechanical properties to perform calculations. Some of these properties include superposition and entanglement. Just as classical computers are composed of bits that can either be in a 1 or a 0 state, a quantum computer is composed of quantum bits (i.e., qubits) which have states of $|0\rangle$ and $|1\rangle$. Quantum mechanics allows for superpositions of the $|0\rangle$ and $|1\rangle$ states with a general form of $a|0\rangle + b|1\rangle$ where a and b are complex numbers. When a qubit state is measured, it collapses to either state $|0\rangle$ with a probability of that happening being $|a|^2$, or to state $|1\rangle$ with a probability of the latter being $|b|^2$. Taking into account the fact that $|a|^2 + |b|^2 = 1$ (since the total probability must sum to unity) and ignoring an overall phase factor

which does not have any observable effects, the general state can be re-written as $\cos \frac{\theta}{2} |0\rangle + e^{i\varphi} \sin \frac{\theta}{2} |1\rangle$, where φ is the phase difference between the two states.

[0030] Entanglement occurs when the interaction between two particles (e.g. two qubits) is such that the states of the two cannot be specified independently, but rather can only be specified for the whole system. This causes the states of the two qubits to be linked together such that measurement of one of the qubits, causes the state of the other qubit to collapse.

[0031] In order to realize a quantum computer, a physical system that can act as a qubit is needed. Such a system needs to have at least two states to act as 0 and 1 states. Note that it is not necessary to have a system with exactly only two states if the spacing between each energy level is different, such that each level can be addressed individually. As previously described herein, one type of physical system that could be used to implement qubits is based on use of superconducting materials (superconducting/superconductive qubits).

[0032] In some implementations, namely when superconducting qubits are implemented as transmon qubits, two basic elements of superconducting quantum circuits are inductors and capacitors. However, circuits made using only these two elements cannot make a system with two energy levels because, due to the even spacing between the system's energy levels, such circuits will produce harmonic oscillators with a ladder of equivalent states. A nonlinear element is needed to have an effective two-level quantum state system, or qubit. Josephson Junction is an example of such non-linear, non-dissipative circuit element.

[0033] Josephson Junctions may form the central circuit elements of a superconducting quantum computer. A Josephson Junction may include a thin layer of an insulating material, typically referred to as a barrier or a tunnel barrier, sandwiched between two layers of superconductor. The Josephson Junction acts as a superconducting tunnel junction. Cooper pairs tunnel across the barrier from one superconducting layer to the other. The electrical characteristics of this tunneling are governed by so-called Josephson relations which provide the basic equations governing the dynamics of the Josephson effect:

$$I = I_c \sin \varphi \quad (1)$$

$$V = \frac{\hbar}{2e} \dot{\varphi} \quad (2)$$

[0034] In these equations, φ is the phase difference in the superconducting wave function across the junction, I_c (the critical current) is the maximum current that can tunnel through the junction, which depends on the barrier thickness and the area of the junction, V is the voltage across the Josephson Junction, I is the current flowing through the Josephson Junction, $\hbar$ is the reduced Planck's constant, and e is electron's charge. Equations (1) and (2) can be combined to give an equation (3):

$$V = \frac{\hbar}{2eI_c \cos \varphi} \dot{\varphi} \quad (3)$$

[0035] Equation (3) looks like the equation for an inductor with inductance L :

$$L = \frac{\hbar}{2eI_c \cos \varphi} \quad (4)$$

[0036] Since inductance is a function of φ , which itself is a function of I , the inductance of a Josephson Junction is non-linear, which makes an LC circuit formed using a Josephson Junction as the inductor have uneven spacing between its energy states.

Exemplary quantum circuits

[0037] The foregoing provides an illustration of using a Josephson Junction in a transmon, which is one type of superconducting qubit. In other classes of superconducting qubits, Josephson Junctions combined with other circuit elements have similar functionality of providing the non-linearity necessary for forming an effective two-level quantum state, or qubit. In other words, when implemented in combination with other circuit elements (e.g. capacitors in transmons or superconducting loops in flux qubits), one or more Josephson Junctions allow realizing a quantum circuit element which has uneven spacing between its energy levels resulting in a unique ground and excited state system for the qubit. This is illustrated in FIG. 1A, providing a schematic illustration of a superconducting quantum circuit 100, according to some embodiments of the present disclosure. As shown in FIG. 1A, an exemplary superconducting quantum circuit 100 includes two or more qubits 102 (reference numerals following after a dash, such as e.g. qubit 102-1 and 102-2 indicate different instances of the same or analogous element). Each of the superconducting qubits 102 may include one or more Josephson Junctions 104 connected to one or more other circuit elements 106, which,

in combination with the Josephson Junction(s) 104, form a non-linear circuit providing a unique two-level quantum state for the qubit. The circuit elements 106 could be e.g. capacitors in transmons or superconducting loops in flux qubits.

[0038] As also shown in FIG. 1A, an exemplary superconducting quantum circuit 100 typically includes means 108 for providing external control of qubits 102 and means 110 for providing internal control of qubits 102. In this context, “external control” refers to controlling the qubits 102 from outside of, e.g. an integrated circuit (IC) chip comprising the qubits, including control by a user of a quantum computer, while “internal control” refers to controlling the qubits 102 within the IC chip. For example, if qubits 102 are transmon qubits, external control may be implemented by means of flux bias lines (also known as “flux lines” and “flux coil lines”) and by means of readout and drive lines (also known as “microwave lines” since qubits are typically designed to operate with microwave signals), described in greater detail below. On the other hand, internal control lines for such qubits may be implemented by means of resonators, e.g., coupling and readout resonators, also described in greater detail below.

[0039] Any one of the qubits 102, the external control means 108, and the external control means 110 of the quantum circuit 100 may be provided on, over, or at least partially embedded in a substrate (not shown in FIG. 1A).

[0040] As previously described herein, within superconducting qubit implementations, three classes are typically distinguished: charge qubits, flux qubits, and phase qubits. Transmons, a type of charge qubits with the name being an abbreviation of “transmission line shunted plasma oscillation qubits”, are particularly encouraging because they exhibit reduced sensitivity to charge noise. FIG. 1B provides a schematic illustration of an exemplary physical layout of a superconducting quantum circuit 100B where qubits are implemented as transmons, according to some embodiments of the present disclosure.

[0041] Similar to FIG. 1A, FIG. 1B illustrates two qubits 102. In addition, FIG. 1B illustrates flux bias lines 112, microwave lines 114, a coupling resonator 116, a readout resonator 118, and wirebonding pads 120 and 122. The flux bias lines 112 and the microwave lines may be viewed as examples of the external control means 108 shown in FIG. 1A. The coupling resonator 116 and the readout resonator 118 may be viewed as examples of the internal control means 110 shown in FIG. 1A.

[0042] Running a current through the flux bias lines 112, provided from the wirebonding pads 120, allows tuning (i.e. changing) the frequency of the corresponding qubits 102 to which each line 112 is connected. In general, it operates in the following manner. As a result of running the current in a particular flux bias line 112, magnetic field is created around the line. If such a magnetic field is in sufficient proximity to the qubit 102, e.g. by a portion of the flux bias line 112 being provided next to the qubit 102, the magnetic field couples to the qubit, thereby changing the spacing between the energy levels of the qubit. This, in turn, changes the frequency of the qubit since the frequency is directly related to the spacing between the energy levels via Planck's equation. The Planck's equation is $E=h\nu$, where E is the energy (in this case the energy difference between energy levels of a qubit), h is the Planck's constant and ν is the frequency (in this case the frequency of the qubit). As this equation illustrates, if E changes, then ν changes. Provided there is sufficient multiplexing, different currents can be sent down each of the flux lines allowing for independent tuning of the various qubits.

[0043] The state(s) of each qubit 102 may be read by way of its corresponding readout resonator 118. As explained below, the qubit 102 induces a resonant frequency in the readout resonator 118. This resonant frequency is then passed to the microwave lines 114 and communicated to the pads 122.

[0044] To that end, a readout resonator 118 may be provided for each qubit. The readout resonator 118 may be a transmission line that includes a capacitive connection to ground on one side and is either shorted to the ground on the other side (for a quarter wavelength resonator) or has a capacitive connection to ground (for a half wavelength resonator), which results in oscillations within the transmission line (resonance), with the resonant frequency of the oscillations being close to the frequency of the qubit. The readout resonator 118 is coupled to the qubit by being in sufficient proximity to the qubit 102, more specifically in sufficient proximity to the capacitor of the qubit 102, when the qubit is implemented as a transmon, either through capacitive or inductive coupling. Due to a coupling between the readout resonator 118 and the qubit 102, changes in the state of the qubit 102 result in changes of the resonant frequency of the readout resonator 118. In turn, because the readout resonator 118 is in sufficient proximity to the microwave line 114, changes in the resonant frequency of the readout resonator 118 induce changes in the current in the microwave line 114, and that current can be read externally via the wire bonding pads 122.

[0045] The coupling resonator 116 allows coupling different qubits together in order to realize quantum logic gates. The coupling resonator 116 is similar to the readout resonator 118 in that it is a transmission line that includes capacitive connections to ground on both sides (i.e. a half wavelength resonator), which also results in oscillations within the coupling resonator 116. Each side of the coupling resonator 116 is coupled (again, either capacitively or inductively) to a respective qubit by being in sufficient proximity to the qubit, namely in sufficient proximity to the capacitor of the qubit, when the qubit is implemented as a transmon. Because each side of the coupling resonator 116 has coupling with a respective different qubit, the two qubits are coupled together through the coupling resonator 116. In this manner, state of one qubit depends on the state of the other qubit, and the other way around. Thus, coupling resonators may be employed in order to use a state of one qubit to control a state of another qubit.

[0046] In some implementations, the microwave line 114 may be used to not only readout the state of the qubits as described above, but also to control the state of the qubits. When a single microwave line is used for this purpose, the line operates in a half-duplex mode where, at some times, it is configured to readout the state of the qubits, and, at other times, it is configured to control the state of the qubits. In other implementations, microwave lines such as the line 114 shown in FIG. 1B may be used to only readout the state of the qubits as described above, while separate drive lines such as e.g. drive lines 124 shown in FIG. 1B, may be used to control the state of the qubits. In such implementations, the microwave lines used for readout may be referred to as readout lines (e.g. readout line 114), while microwave lines used for controlling the state of the qubits may be referred to as drive lines (e.g. drive lines 124). The drive lines 124 may control the state of their respective qubits 102 by providing, using e.g. wirebonding pads 126 as shown in FIG. 1B, a microwave pulse at the qubit frequency, which in turn stimulates (i.e. triggers) a transition between the 0 and 1 state of the qubit. By varying the length of this pulse, a partial transition can be stimulated, giving a superposition of the 0 and 1 states of the qubit.

[0047] Flux bias lines, microwave lines, coupling resonators, drive lines, and readout resonators, such as e.g. those described above, together form interconnects for supporting propagation of microwave signals. Further, any other connections for providing direct electrical interconnection between different quantum circuit elements and components, such

as e.g. connections from electrodes of Josephson Junctions to plates of the capacitors or to superconducting loops of superconducting quantum interference devices (SQUIDS) or connections between two ground lines of a particular transmission line for equalizing electrostatic potential on the two ground lines, are also referred to herein as interconnects. Still further, the term “interconnect” may also be used to refer to elements providing electrical interconnections between quantum circuit elements and components and non-quantum circuit elements, which may also be provided in a quantum circuit, as well as to electrical interconnections between various non-quantum circuit elements provided in a quantum circuit. Examples of non-quantum circuit elements which may be provided in a quantum circuit may include various analog and/or digital systems, e.g. analog to digital converters, mixers, multiplexers, amplifiers, etc.

[0048] In various embodiments, the interconnects as shown in FIG. 1B could have different shapes and layouts. For example, some interconnects may comprise more curves and turns while other interconnects may comprise less curves and turns, and some interconnects may comprise substantially straight lines. In some embodiments, various interconnects may intersect one another, in such a manner that they don’t make an electrical connection, which can be done by using e.g. a bridge, bridging one interconnect over the other. As long as these interconnects operate in accordance with use of these interconnects as known in the art for which some exemplary principles were described above, quantum circuits with different shapes and layouts of the interconnects than those illustrated in FIG. 1B are all within the scope of the present disclosure.

[0049] Coupling resonators and readout resonators may be configured for capacitive coupling to other circuit elements at one or both ends in order to have resonant oscillations, whereas flux bias lines and microwave lines may be similar to conventional microwave transmission lines because there is no resonance in these lines. Each one of these interconnects may be implemented as any suitable architecture of a microwave transmission line, such as e.g. a coplanar waveguide, a stripline, a microstrip line, or an inverted microstrip line. Typical materials to make the interconnects include aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), and niobium titanium nitride (NbTiN), all of which are particular types of superconductors. However, in various embodiments, other suitable superconductors and alloys of superconductors may be used as well.

[0050] FIG. 1C illustrates an exemplary transmon 128 which could be used as any one of the qubits 102, according to some embodiments of the present disclosure. Presence of a capacitor 130 of such a size that capacitive energy is significantly larger than the Josephson energy in a qubit of FIG. 1C indicates that the qubit is a transmon. The capacitor 130 is configured to store energy in an electrical field as charges between the plates of the capacitor.

[0051] The capacitor 130 is depicted as an interdigitated capacitor, a particular shape of capacitor that provides a large capacitance with a small area, however, in various embodiments, other shapes and types of capacitors may be used as well. For example, such a capacitor could be implemented simply as two parallel plates with vacuum in between. Furthermore, in various embodiments, the capacitor 130 may be arranged in any direction with respect to the SQUID or a single Josephson Junction, not necessarily as shown in FIG. 1C.

[0052] In addition, the transmon illustrated in FIG. 1C includes two Josephson Junctions 132 incorporated into a superconducting loop 134. The two Josephson Junctions 132 and the superconducting loop 134 together form a superconducting quantum interference device (SQUID). Magnetic fields generated by the flux bias line 112 connected to the qubit extend to the SQUID (i.e. current in the flux bias line 112 create magnetic fields around the SQUID), which, in turn, tunes the frequency of the qubit.

[0053] In other embodiments, a SQUID could include only one Josephson Junction, or a transmon could be implemented with a single Josephson Junction without the superconducting loop. A single Josephson Junction without the SQUID is insensitive to magnetic fields, and thus, in such an implementation, flux bias lines 112 may not be used to control the frequency of the transmon.

[0054] While FIGs. 1A and 1B illustrate examples of quantum circuits comprising only two qubits 102, embodiments with any larger number of qubits are possible and are within the scope of the present disclosure. At least some of the one or more qubits 102 shown in FIGs. 1A-1C may comprise Josephson Junction structures fabricated using the partially subtractive fabrication approach as described herein.

[0055] While FIGs. 1B and 1C illustrate embodiments specific to transmons, subject matter disclosed herein is not limited in this regard and may include other embodiments of quantum

circuits implementing other types of superconducting qubits that would also utilize Josephson Junctions as described herein, all of which are within the scope of the present disclosure. Furthermore, partially subtractive fabrication methods and resulting Josephson Junctions disclosed herein may be used in quantum circuits implementing qubits other than superconducting qubits, all of which are also within the scope of the present disclosure.

[0056] In various embodiments, quantum circuits employing Josephson Junctions fabricated using the subtractive fabrication methods described herein, e.g. quantum circuits such as the one shown in FIGs. 1A-1C, may be used to implement components associated with a quantum integrated circuit (IC). Such components may include those that are mounted on or embedded in a quantum IC, or those connected to a quantum IC. The quantum IC may be either analog or digital and may be used in a number of applications within or associated with quantum systems, such as e.g. quantum processors, quantum amplifiers, quantum sensors, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a quantum system.

Exemplary quantum computing device

[0057] FIG. 2 provides an illustration of an exemplary quantum computing device 200, e.g. a quantum computer, according to some embodiments of the present disclosure. The quantum computing device 200 may include any of the Josephson Junctions described herein, e.g. Josephson Junctions fabricated using the subtractive fabrication methods described herein.

[0058] A number of components are illustrated in FIG. 2 as included in the quantum computing device 200, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 200 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 200 may not include one or more of the components illustrated in FIG. 2, but the quantum computing device 200 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 200 may not include a display device 206, but may include display device interface circuitry (e.g., a

connector and driver circuitry) to which a display device 206 may be coupled. In another set of examples, the quantum computing device 200 may not include an audio input device 218 or an audio output device 208, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 218 or audio output device 208 may be coupled.

[0059] The quantum computing device 200 may include a processing device 202 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 202 may include a quantum processing device 226 (e.g., one or more quantum processing devices), and a non-quantum processing device 228 (e.g., one or more non-quantum processing devices). The quantum processing device 226 may include one or more of the quantum circuits 100 disclosed herein, and may perform data processing by performing operations on the qubits 102 that may be generated in the quantum circuits 100, and monitoring the result of those operations. For example, as discussed above, different qubits may be allowed to interact, the quantum states of different qubits may be set or transformed, and the quantum states of qubits may be read (e.g., by another qubit via a coupling resonator or externally via a readout resonator). The quantum processing device 226 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 226 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 226 may also include support circuitry to support the processing capability of the quantum processing device 226, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0060] As noted above, the processing device 202 may include a non-quantum processing device 228. In some embodiments, the non-quantum processing device 228 may provide peripheral logic to support the operation of the quantum processing device 226. For example, the non-quantum processing device 228 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The

non-quantum processing device 228 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 226. For example, the non-quantum processing device 228 may interface with one or more of the other components of the quantum computing device 200 (e.g., the communication chip 212 discussed below, the display device 206 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 226 and conventional components. The non-quantum processing device 228 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), crypto processors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0061] The quantum computing device 200 may include a memory 204, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 226 may be read and stored in the memory 204. In some embodiments, the memory 204 may include memory that shares a die with the non-quantum processing device 228. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0062] The quantum computing device 200 may include a cooling apparatus 224. The cooling apparatus 224 may maintain the quantum processing device 226 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 226. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 228 (and various other components of the quantum computing device 200) may not be cooled by the cooling apparatus 224, and may instead operate at room temperature. The cooling apparatus 224 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0063] In some embodiments, the quantum computing device 200 may include a communication chip 212 (e.g., one or more communication chips). For example, the

communication chip 212 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0064] The communication chip 212 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 212 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 212 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 212 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 212 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 200 may include an antenna 222 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0065] In some embodiments, the communication chip 212 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 212 may include multiple

communication chips. For instance, a first communication chip 212 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 212 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 212 may be dedicated to wireless communications, and a second communication chip 212 may be dedicated to wired communications.

[0066] The quantum computing device 200 may include battery/power circuitry 214. The battery/power circuitry 214 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 200 to an energy source separate from the quantum computing device 200 (e.g., AC line power).

[0067] The quantum computing device 200 may include a display device 206 (or corresponding interface circuitry, as discussed above). The display device 206 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0068] The quantum computing device 200 may include an audio output device 208 (or corresponding interface circuitry, as discussed above). The audio output device 208 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0069] The quantum computing device 200 may include an audio input device 218 (or corresponding interface circuitry, as discussed above). The audio input device 218 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0070] The quantum computing device 200 may include a global positioning system (GPS) device 216 (or corresponding interface circuitry, as discussed above). The GPS device 216 may be in communication with a satellite-based system and may receive a location of the quantum computing device 200, as known in the art.

[0071] The quantum computing device 200 may include an other output device 210 (or corresponding interface circuitry, as discussed above). Examples of the other output device

210 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0072] The quantum computing device 200 may include an other input device 220 (or corresponding interface circuitry, as discussed above). Examples of the other input device 220 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0073] The quantum computing device 200, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

Detailed description of proposed structures and methods of fabrication thereof

[0074] In order to highlight the advantages offered by Josephson Junction structures fabricated using the partially subtractive process as proposed herein, it would be helpful to first explain how conventional Josephson Junctions are fabricated using a so-called double-angle shadow evaporation approach (also sometimes referred to as “double-angle shadow evaporation” or “hanging resist” approach). The name “double-angle shadow evaporation/evaporation” reflects the fact that the method involves metal deposition, typically carried out metal evaporation, at two different angles of incidence with respect to the substrate (hence, double-angle). The name further reflects the fact that metal deposition is performed through a hanging photoresist mask which casts a shadow on at least a part of the substrate, obscuring metal deposition on that part (hence, shadow evaporation/evaporation).

[0075] FIGs. 3A-3C provide a schematic illustration of one example of a photoresist mask 300 provided over a substrate 302 for fabricating Josephson Junctions using a double-angle shadow evaporation approach. Each of FIGs. 3A-3C provides a view of the same photoresist mask 300 over the substrate 302, but perspectives of these views are different. FIG. 3A provides a top-

down view (i.e. a view from a point above the substrate 302). FIG. 3B provides a cross-sectional view with a cross-section of the structure of FIG. 3A taken along a horizontal dashed line shown in FIG. 3A. Finally, FIG. 3C provides a cross-sectional view with a cross-section of the structure of FIG. 3A taken along a vertical dashed line shown in FIG. 3A. A legend provided within a dashed box at the bottom of FIGs. 3A-3C illustrates patterns used to indicate different elements shown in FIGs. 3A-3C, so that the FIGs are not cluttered by many reference numerals.

[0076] Josephson Junctions may be created by a double-angle shadow evaporation approach using a two-layer photoresist mask 300 that includes a bottom photoresist layer 304 and a top photoresist layer 306 as shown in FIGs. 3A-3C. The bottom layer 306 is undercut from the top layer 304 in that some portions of the top layer 304 hang, or are suspended, over the bottom layer 306. The bottom layer 306 is undercut in such a manner that the top layer 304 of photoresist forms a suspended bridge 308, known as a Dolan bridge, over a section of the substrate 302. Ways for fabricating such undercuts in photoresist are well-known in the art of photolithographic processing and, therefore, are not described here in detail.

[0077] In order to form a Josephson Junction, metals are then deposited through the photoresist mask 300 with the suspended bridge. Conventionally, this is done as illustrated in FIGs. 4A-4C.

[0078] Each of FIGs. 4A-4C illustrates a result of different subsequent fabrication steps. FIG. 4C provides two views of the same structure. The view on the right side of FIG. 4C is a top-down view (i.e. a view similar to that shown in FIG. 3A). The view on the left side of FIG. 4C is a cross-sectional view with a cross-section of the structure of FIG. 4C taken along a horizontal dashed line shown in FIG. 4C (i.e. a view similar to that shown in FIG. 3B). Each of FIGs. 4A and 4B only provide a cross-sectional view similar to that of the left side of FIG. 4C but at an earlier fabrication step. Similar to FIGs. 3A-3C, a legend provided within a dashed box at the bottom of FIGs. 4A-4C illustrates patterns used in the figures to indicate different elements shown in FIGs. 4A-4C. Moreover, similar reference numerals in FIGs. 3A-3C and FIGs. 4A-4C are used to illustrate analogous elements in the figures. For example, reference numerals 302 and 402, shown, respectively, in FIGs. 3 and 4 refer to a substrate, reference numerals 304 and 404 - to a bottom mask layer, and so on. When provided with reference to one of the FIGs. 3A-3C and FIGs. 4A-4C, discussions of these elements are applicable to other figures, unless stated

otherwise. Thus, in the interests of brevity, discussions of similar elements are not repeated for each of the figures but, rather, the differences between the figures are described.

[0079] As previously described herein, a Josephson Junction comprises a thin layer of dielectric sandwiched between two layers of superconductors, the dielectric layer acting as the barrier in a superconducting tunnel junction. According to the double-angle shadow evaporation approach, such a device is conventionally fabricated by, first, depositing a layer of a first superconductor 410 on the substrate 402, as shown in FIG. 4A, through the two-layer mask such as e.g. the one shown in FIGs. 3A-3C. The first superconductor is deposited at an angle with respect to the substrate 402, as shown in FIG. 4A with an angle θ_1 . Slanted dotted-dashed lines in FIG. 4A illustrate the direction of deposition of the first superconductor 410. A layer of the first superconductor 410 may have a thickness between e.g. 10 and 300 nanometers (nm), e.g. between 40 and 100 nm.

[0080] The first superconductor 410 forms a base electrode of the future Josephson Junction. A layer of insulator 411 (also referred to herein as a “dielectric layer 411” or a “dielectric 411”), shown in FIGs. 4B and 4C, is then provided over the first superconductor 410 to form a tunnel barrier of the future Josephson Junction. The tunnel barrier is formed by oxidizing the first superconductor 410, thus creating a layer of first superconductor oxide on its surface. Such an oxide may have a thickness between e.g. 1 and 5 nm, typically for qubit applications between 1 and 2 nm.

[0081] The fact that the choice of a tunnel barrier in a double-angle shadow evaporation method is constrained to an oxide of the base electrode superconductor limits the choice of the superconductor used as the first superconductor 410 in that the superconductor must be such that a controlled layer of oxide may be created on it. In practice, aluminum oxide is the only controlled oxide that may be formed from a metal. Therefore, currently aluminum is the only superconducting metal that is used for the base electrode of Josephson Junctions fabricated using the double-angle shadow evaporation technique.

[0082] After the layer of dielectric 411 is provided on the first superconductor 410, a second superconductor 412 is deposited through the mask but at a different angle with respect to the substrate 402 than θ_1 . FIG. 4B illustrates the second angle as an angle θ_2 and slanted dotted-dashed lines in FIG. 4B illustrate the direction of deposition of the second superconductor 412.

In some embodiments, the first and the second superconductors 410, 412 are deposited at the opposite angles, if measured with respect to a normal to the substrate 402. Conventionally, the second superconductor 420 is aluminum because the first superconductor must be aluminum, as described above. A layer of the second superconductor 412 may have a thickness between e.g. 10 and 300 nm, typically between 40 and 100 nm. The second superconductor 412 forms a counter electrode (i.e. counter to the base electrode formed by the first superconductor 410) of the future Josephson Junction.

[0083] The first and second superconductors 410, 412 are usually deposited using a non-conformal process, such as e.g. evaporative deposition. After deposition of the second superconductor 412, the deposition mask is removed, removing with it any first and/or second superconductor 410, 412 deposited on top of it.

[0084] In general, the above-described process of creating patterned structures of one or more target materials (in this case, structures made of the first and second superconductors 410, 412) on the surface of a substrate using a sacrificial material such as photoresist is referred to as a lift-off method. Lift-off is a type of an additive technique, as opposed to subtracting techniques like etching, and may be applied in cases where a direct etching of structural material would have undesirable effects on one or more layers below.

[0085] After the deposition mask is removed, the resulting Josephson Junction is left on the substrate 402 as shown in FIG. 4C as a Junction 414. The Junction 414 is formed by the small region of overlap under the photoresist bridge 408 (i.e. the area under the bridge 408 where the first superconductor 410, covered with a layer of a thin insulating material is overlapped by the second superconductor 412). Dimensions of the Junction 414 along x-axis and y-axis, shown in FIG. 4C as d_x and d_y , respectively, are typically between 50 and 1000 nm for any of d_x and d_y .

[0086] Furthermore, as a result of performing the double-angle shadow evaporation as described above, junctions of the first and second superconductors may also form on each side of the Josephson Junction 414, such junctions shown in FIGs. 4B and 4C as Junctions 416. However, because these junctions are of much larger dimensions than the Josephson Junction 414, e.g. measured several thousands of nm in the x-direction and hundreds of nm or more in

the y-direction, they are essentially infinite for the Josephson effect to take place and, therefore, act as superconductors rather than Josephson Junctions.

[0087] One problem with the fabrication approach described above is that it includes steps that are not suitable for manufacturing on the larger wafer sizes used in the semiconductor industry. For example, angled metal deposition step does not produce a uniform film across the wafer and would prohibit uniform qubit performance across large area. Moreover, the fabrication approach described above relies on lift-off of metal films to produce wires remaining on the wafer. The lift-off technique is not amenable to the chemical waste systems of wafer cleaning tools and would not facilitate high volume manufacturing or even an extension to many qubits on a single wafer.

[0088] Another problem with the double-angle shadow evaporation approach described above is that the resulting Josephson Junction is surrounded by dielectric material on several sides. For example, as shown on the left-side (i.e. cross-section) view of FIG. 4C indicating the boundaries of the Josephson Junction 414 with vertical dashed lines, the dielectric 411 that forms the tunnel barrier of the Josephson Junction 414 extends further, outside of the boundaries of the Josephson Junction 414, e.g. into the area 418 immediately adjacent to the Josephson Junction, because the dielectric 411 is provided across the entire bottom superconductor 410. The right-side (i.e. top) view of FIG. 4C illustrates that the dielectric material 411 surrounds the Josephson Junction 414 on three of the four sides. As described above, one major source of loss, and thus decoherence in superconducting qubits are spurious TLS's caused by defects in the areas surrounding Josephson Junctions. Dielectrics surrounding the tunnel barriers and superconductors of Josephson Junctions, such as e.g. the dielectric portions 418 shown in FIG. 4C, may be one of the causes of spurious TLS's, leading to qubit decoherence.

[0089] Yet another problem with the use of the double-angle shadow evaporation approach is that it limits materials that may be employed in forming Josephson Junctions. As described above, Josephson Junctions fabricated the double-angle shadow evaporation approach can only use Al as the superconductor for the base electrode. This may be problematic because interconnects in quantum circuits are typically made from other superconducting materials such as e.g. Nb, TiN and NbTiN and interfaces between the different superconducting materials used for Josephson Junctions and interconnects present yet another source of losses. Any

losses are especially significant in context of quantum circuits where, sometimes, energy as small as that of a single photon is to be transmitted, making loss tolerance very low.

[0090] FIGs. 5A-5J provide a schematic illustration of partially subtractive fabrication of Josephson Junctions, according to some embodiments of the present disclosure. The fabrication process described below improves on some of the challenges of the existing fabrication approaches described above. For one, the partially subtractive fabrication process described herein is more suitable for large-scale manufacturing at least in that it does not require angled evaporation and lift-off. In addition, employing such fabrication process allows fabricating Josephson Junctions with no dielectric around them, thus reducing the amount of spurious TLS's in the vicinity of Josephson Junctions. Still further, using the partially subtractive fabrication process as described herein advantageously extends the arsenal of superconducting materials which may be employed as base and top electrodes of Josephson Junctions to include those besides Al.

[0091] A legend provided within a dashed box at the bottom of FIGs. 5A-5J illustrates patterns used to indicate different elements shown in FIGs. 5A-5J, so that the FIGs are not cluttered by many reference numerals. FIGs. 5A-5J will now be described with reference to FIG. 6 providing a flow chart of a method 600 for partially subtractive fabrication of Josephson Junctions, according to some embodiments of the present disclosure. In particular, FIGs. 5A-5I illustrate a sequence of structures 502, 504, 506, 508, and so on until structure 518, each of which illustrates an exemplary result of a corresponding one of different subsequent fabrication processes 602, 604, 606, 608, and so on until process 618 shown in FIG. 6. Thus, each structure 5XX corresponds to a respective process box 6XX of the method 600, e.g. a structure 502 illustrates an exemplary result of a fabrication process 602, a structure 504 illustrates an exemplary result of a fabrication process 604, a structure 506 illustrates an exemplary result of a fabrication process 606, and so on. Furthermore, each of FIGs. 5A-5I provides two views of the same structure. Namely, the view on the left side of each of FIGs. 5A-5I is a cross-sectional view with a cross-section of the structures taken along a y-z plane, e.g. along a plane indicated with a dashed line AA in FIGs. 5A and 5B (FIGs. 5C-5I illustrate the same cross-sections, but the plane AA is not shown there specifically in order to not clutter the drawings), while the view on the right side of each of FIGs. 5A-5I is a top-down view of an x-y plane. FIG. 5J illustrates a magnified view of a cross-section of the structure 516 shown in FIG. 5I.

[0092] Although the operations discussed below with reference to the method 600 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 600 may be illustrated with reference to one or more of the embodiments discussed above, but the method 600 may be used to manufacture any suitable quantum circuit element comprising one or more Josephson Junctions according to any embodiments disclosed herein.

[0093] The method 500 may begin with providing a stack 535 of various layers over a substrate 522 (process 602 of FIG. 6, result of which is illustrated with a structure 502 of FIG. 5A).

[0094] The substrate 522 may comprise any substrate suitable for realizing quantum circuit components described herein. In one implementation, the substrate 522 may be a crystalline substrate such as, but not limited to a silicon or a sapphire substrate, and may be provided as a wafer or a portion thereof. In other implementations, the substrate may be non-crystalline. In general, any material that provides sufficient advantages (e.g. sufficiently good electrical isolation and/or ability to apply known fabrication and processing techniques) to outweigh the possible disadvantages (e.g. negative effects of spurious TLS's), and that may serve as a foundation upon which a quantum circuit may be built, falls within the spirit and scope of the present disclosure. Additional examples of substrates include silicon-on-insulator (SOI) substrates, III-V substrates, and quartz substrates.

[0095] In some embodiments, the substrate 522 may be cleaned to remove surface-bound organic and metallic contaminants, as well as subsurface contamination, prior to deposition of the stack in process 602. In some embodiments, cleaning may be carried out using e.g. a chemical solutions (such as peroxide), and/or with ultraviolet (UV) radiation combined with ozone, and/or oxidizing the surface (e.g., using thermal oxidation) then removing the oxide (e.g. using hydrofluoric acid (HF)).

[0096] Josephson Junctions may be realized in what may be referred to as a “trilayer” architecture, or in what may be referred to as a “bilayer” architecture. Trilayer architecture implies that a Josephson Junction includes three layers – namely, the base electrode, the tunnel barrier, and the top electrode, in addition to two wireup superconductors providing electrical connectivity to the base electrode and the top electrodes of the Josephson Junction.

Thus, when a trilayer Josephson Junction is implemented over a substrate, there are at least five layers present over the substrate: the first wireup superconductor (also referred to as a “base superconductor (SC) wire layer”), the base electrode of the Josephson Junction, the tunnel barrier of the Josephson Junction, the top electrode of the Josephson Junction, and the second wireup superconductor (also referred to as a “top SC wire layer”), the layers listed in order in which they are provided over the substrate starting from the layer closest to the substrate. On the other hand, bilayer architecture implies that the top wireup superconductor also acts as the top electrode of the Josephson Junction. Thus, when a bilayer Josephson Junction is implemented over a substrate, there are four layers present over the substrate: the base SC wire layer, the base electrode of the Josephson Junction, the tunnel barrier of the Josephson Junction, and the top SC wire layer which also happens to be the top electrode of the Josephson Junction. FIGs. 5A-5J illustrate examples of a trilayer Josephson Junction. However, the method 600 is applicable to both the trilayer and the bilayer architecture, the differences between which are identified in the description below. Therefore, both trilayer and bilayer Josephson Junctions as described herein, and methods of fabrication thereof as described herein, are within the scope of the present disclosure.

[0097] In case the Josephson Junction being fabricated is a trilayer junction, the stack 535 of various layers provided over the substrate 522 includes four layers: a base wireup superconductor layer 524 (indicated in FIG. 6 as a “base SC wire layer”) for providing electrical connectivity to a base electrode of the Josephson Junction, a base superconductor layer 526 (indicated in FIG. 6 as a “JJ base SC”) for forming the base electrode of the Junction, a top superconductor layer 530 (not indicated in FIG. 6 because FIG. 6 is general enough to also be applicable to bilayer JJs) for forming the top electrode of the Junction, and a tunnel barrier layer 528 (indicated in FIG. 6 as a “JJ tunnel barrier”) provided between the base electrode layer 526 and the top electrode layer 530.

[0098] The base SC wire 524 layer may comprise any conducting or superconducting material suitable for serving as an interconnect in a quantum circuit, such as e.g. aluminum (Al), niobium (Nb), niobium nitride (NbN), niobium titanium nitride (NbTiN), titanium nitride (TiN), molybdenum rhenium (MoRe), etc., or any alloy of two or more superconducting/conducting materials. Similarly, each of the JJ base SC 526 and the JJ top SC 530 layers may comprise any conducting or superconducting material suitable for serving as base and top electrodes of a

Josephson Junction, respectively. Each of the base SC wire 524, the JJ base SC 526 and the JJ top SC 530 layers may be deposited over the substrate 442 using any known techniques for depositing conducting/superconducting materials, such as e.g. atomic layer deposition (ALD), physical vapor deposition (PVD) (e.g. evaporative deposition, magnetron sputtering, or e-beam deposition), chemical vapor deposition (CVD), or electroplating.

[0099] In various embodiments, the thickness of the layer of the base SC wire 524 may be between 20 and 500 nm including all values and ranges therein, e.g. between 40 and 200 nm, e.g. 50 nm. In various embodiments, the thickness of each of the JJ base SC 526 and the JJ top SC 530 may be between 10 and 300 nm including all values and ranges therein, e.g. between 40 and 100 nm.

[00100] As used herein, the term “thickness” refers to a dimension of a certain element or layer as measured along the z-axis as illustrated in FIGs. 5A-5J, while the term “width” refers to a dimension of a certain element or layer as measured along the y-axis as illustrated in FIGs. 5A-5J.

[00101] The JJ tunnel barrier 528 could be selected as any dielectric material of sufficiently high quality (i.e. low losses in terms of spurious TLS's), such as e.g. silicon oxide, hafnium oxide, or aluminum oxide.

[00102] In some embodiments, the JJ tunnel barrier 528 may include an oxide deposited over the JJ base SC 526 using e.g. chemical vapor deposition or/and plasma-enhanced chemical vapor deposition, as typically done in conventional processing. In still other embodiments, the JJ tunnel barrier 528 may include a dielectric material formed over the JJ base SC 526 using coating techniques involving cross-linking of liquid precursors into solid dielectric materials. In some embodiments, the surface of the JJ base SC 526 may be cleaned or treated prior to applying the dielectric to reduce surface contamination and minimize interface traps and/or promote adhesion, for example using chemical or plasma clean, or applying heat in a controlled environment. In some embodiments, an “interface layer” may be applied between the JJ base SC 526 and the JJ tunnel barrier 528 to prevent, decrease, or minimize spontaneous and uncontrolled formation of other interfacial layers. In some embodiments, an adhesion promoter or adhesion layer may be applied prior to application of the dielectric.

[00103] In various embodiments, the thickness of the JJ tunnel barrier 528 may be between 1 and 8 nm including all values and ranges therein, e.g. between 1 and 5 nm, e.g. 2-3 nm.

[00104] In case the Josephson Junction being fabricated is a bilayer junction, the stack 535 of various layers provided over the substrate 522 in process 602 would include three of the four layers described above for the trilayer architecture, with the missing layer being the top superconductor layer 530.

[00105] The method 600 may then proceed with forming an opening 536 in the stack 535 deposited in the process 602 (process 604 of FIG. 6, result of which is illustrated with a structure 504 of FIG. 5B). As shown with the line AA shown on the top view of FIG. 5B, in order to properly illustrate the opening, the side view of FIG. 5B and subsequent figures is shown as a cross-section along a line that goes through the openings 536.

[00106] Dimensions and a shape of the opening 536 could depend on e.g. the sacrificial material later used to fill the opening, dimensions and shape of the top SC wire layer 534 to be deposited later on, dimensions of the Josephson Junction to be formed, and the etching process used to form the opening 536. For example, in some embodiments, the opening may be rectangular in shape in the x-y plane, as shown in the top view in FIG. 5B. However, in other embodiments, any other openings 536, arranged in any suitable location and in any suitable shape/geometry may be used, all of which being within the scope of the present disclosure.

[00107] The opening 536 extends from the surface of the stack (i.e. from the surface of the JJ top SC 530 in case of a trilayer JJ, or from the surface of the JJ tunnel barrier 528 in case of a bilayer JJ) to the bottom of the stack (i.e. to the bottom of the JJ base SC 526), e.g. to the substrate 522 in case the JJ base SC 526 is provided on the substrate 522.

[00108] In various embodiments, the width of the opening 536 could be between 10 and 500 nm, including all values and ranges therein, e.g. between 20 and 200 nm.

[00109] In various embodiments, any kind of etching techniques in combination with patterning may be used to form the opening 536.

[00110] For example, a patterning technique employing photoresist or other masks defining the dimensions and location of the opening 536 in the stack may be used. An exemplary photoresist patterning technique could include depositing a photoresist over the layer of interest, in this case – over the surface of the stack deposited in the process 602. The photoresist may be a positive or negative resist and may include for example, poly(methyl methacrylate), poly(methyl glutarimide), DNQ/novolac, or SU-8 (an epoxy based negative resist). The photoresist may be chemically amplified containing a photoacid generator and may be based on polymers or co-polymers which contain aromatic rings or alicyclic norbornene derivatives (e.g. for etch resistance), and have protecting groups such as t-butyl. The polymers may include polystyrene or acrylate polymers. The photoresist may be deposited by a casting process such as, for example, spin-coating. The photoresist may then be patterned by optically projecting an image of a desired pattern onto the photoresist using photolithography, such as optical photolithography, immersion photolithography, deep UV lithography, extreme UV lithography, or other techniques. A developer, such as tetramethylammonium hydroxide TMAH (with or without surfactant) at a concentration of in the range of 0.1 N to 0.3 N, may be applied to the photoresist, such as by spin-coating, and portions of the photoresist are removed to expose regions of the underlying layer correlating to the desired pattern. In some embodiments, baking of the substrate may occur before or after any of the above actions. For example, the substrate may be prebaked to remove surface water. After application of the photoresist, a post application bake may occur, wherein at least a portion of the solvents in the photoresist are driven off. After exposure to light, a post-exposure bake may occur to induce chemical reactions, such as de-protecting the photoresist. After patterning, the resist may be hard baked.

[00111] Once patterning has been done to expose portions of the underlying surface of the stack 535 in a patterned mask that defines location and arrangement of the future opening 536, exposed portions of the underlying stack are then chemically etched. During the etch, the exposed portions of the stack are removed until a desired depth is achieved, forming the opening 536 in the stack 535. If photoresist patterning is used for creating a mask for forming the opening 536, the remaining photoresist may then optionally removed via e.g. a process such as ashing, where the photoresist is exposed to oxygen or fluorine, which combines with the photoresist to form ash.

[00112] Next, the opening 536 is filled with an insulating sacrificial material 532 (process 606 of FIG. 6, result of which is illustrated with a structure 506 of FIG. 5C). Since the sacrificial material 532 will need to later be etched to achieve undercutting of the sacrificial material under the bridge over a Josephson Junction to provide a gap between at least a portion of the Josephson Junction and an interconnect for providing the current to the Josephson Junction, e.g. using isotropic etching, etching properties of potential candidate materials are to be considered when selecting a suitable material to be used as the sacrificial material 532. Again, besides appropriate etching characteristics, some other considerations in selecting a suitable material for the sacrificial material 532 may include e.g. possibilities of smooth film formation, low shrinkage and outgassing, and good dielectric properties (such as e.g. low electrical leakage, suitable value of a dielectric constant, and thermal stability). Examples of dielectric materials that may be used as the sacrificial material 532 include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane, polytetrafluoroethylene or poly(methyl methacrylate) (PMMA), fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass.

[00113] In some embodiments, the sacrificial material 532 may be deposited over the surface of the stack 535 and into the opening 536 using e.g. chemical vapor deposition or/and plasma-enhanced chemical vapor deposition, as typically done in conventional processing. In still other embodiments, the sacrificial material 532 may include a dielectric material formed over the surface of the stack 535 and in the opening 536 using coating techniques involving cross-linking of liquid precursors into solid dielectric materials.

[00114] The method 600 may then proceed with performing a planarization of the sacrificial material 532 to the surface of the stack 535 (process 608 of FIG. 6, result of which is illustrated with a structure 508 of FIG. 5D). During this process, the sacrificial material 532 is removed in order to expose surfaces 538 of the top layer of the stack 535 which may be covered with the sacrificial material 532 as a result of depositing that material into the openings 536. Thus, during planarization, the sacrificial material 532 is removed to expose the surface 538 of the JJ top SC 530 in case of a trilayer JJ, or to expose the surface 538 of the JJ tunnel barrier 528 in case of a bilayer JJ.

[00115] In various embodiments, planarization may be performed using either wet or dry planarization processes. In one embodiment, planarization may be performed using chemical mechanical planarization (CMP), which may be understood as a process that utilizes a polishing surface, an abrasive and a slurry to remove the overburden and planarize the surface.

[00116] Next, a layer of a top SC wire material 534 is provided on the surface 538 of the stack 535 with the opening 536 filled with the sacrificial material 532 (process 610 of FIG. 6, result of which is illustrated with a structure 510 of FIG. 5E). Considerations described above with reference to the base SC wire material 524 are applicable to the top SC wire material 534 and deposition thereof and, therefore, in the interest of brevity, are not repeated here. In some embodiments, the top SC wire material 534 may be the same as the material of the base SC wire material 524 or/and as the material JJ base SC 526. In some embodiments, the top SC wire material 534 may be the same as the material of the JJ top SC 530 in case of a trilayer JJ.

[00117] In some embodiments, the surface of the stack 535 may be cleaned or treated prior to applying the top SC wire material 534 to reduce surface contamination and minimize interface traps and/or promote adhesion, for example using a chemical or plasma clean, or applying heat in a controlled environment. In some embodiments, an adhesion promoter or adhesion layer may be applied prior to application of the top SC wire material 534.

[00118] In various embodiments, the thickness of the top SC wire material 534 may be between 20 and 500 nm including all values and ranges therein, e.g. between 40 and 200 nm, e.g. 50 nm.

[00119] The method 600 may then proceed with patterning the layer of the top SC wire material 534 to form a structure that will serve as a top SC wire bridge over the opening 536 and will provide at least one etch window (process 612 of FIG. 6, result of which is illustrated with a structure 512 of FIG. 5F). An example of such structure is shown as a rectangular structure 540 shown in FIG. 5F. However, in other embodiments, the top SC wire bridge structure 540 could have any other shapes/geometries suitable for forming a bridge over the opening and one or more windows over the opening, the window(s) configured to allow removal of the sacrificial material under the bridge, all of which shapes/geometries being within the scope of the present disclosure. With the rectangular structure 540 shown in FIG. 5F, portion 542 indicated with a dotted line “bridges” the portion of the stack to the left of the

opening 536 and the portion of the stack 535 to the right of the opening, while 544-1 and 544-2 indicates two etch windows.

[00120] The dimension of the structure 540 in the y-direction is to be such as to allow formation of a Josephson Junction on one side of the opening 536 and formation of what may be considered as bulk superconductor on the other side of the opening. Example shown in FIG. 5F illustrates the portion of the stack 535 on the right side of the opening 536 as the portion where a Josephson Junction is to be formed, while the portion on the left side of the opening will serve as a bulk superconductor of an interconnect to be formed. In various embodiments, the structure 540 may be between 100 nm and 10 micrometers (micron) in the y-direction, including all values and ranges therein.

[00121] The dimension of the structure 540 in the x-direction is also to be such as to allow formation of a Josephson Junction on one side of the opening 536 and formation of what may be considered as bulk superconductor on the other side of the opening. In various embodiments, the structure 540 may be between 50 nm and 5 micron in the x-direction, including all values and ranges therein.

[00122] In various embodiments, any kind of conventional patterning techniques may be used to form the bridge structure 540 at the desired location on the surface of the stack 535, over the opening 536, such as e.g. patterning techniques employing photoresist or other masks as described above.

[00123] The method 600 may then proceed with patterning the stack 535 to form a future Josephson Junction 546 and a future interconnect portion 548, the Josephson Junction and the interconnect portion separated from one another by the opening 536 and electrically connected by the bridge 542 (process 614 of FIG. 6, result of which is illustrated with a structure 514 of FIG. 5G). Patterning of the stack 535 may involve patterning the stack so that the shape of the stack in each x-y plane down to the upper surface 550 of the base SC layer 524 is the same as that of the top wire bridge structure 540 patterned from the top SC wire layer in the process 612, as shown in FIG. 5G. To that end, patterning techniques as those used to form the opening 536 through the stack may be used, as described above. Unlike the patterning of the opening 536 where the layers of the stack were removed until the layer underlying the base SC wire 524, e.g. the substrate 522, was exposed, removal of the layers of the stack in the

process 614 proceeds only until surface 550 of the base SC wire layer 524 is exposed. FIG. 5G illustrates surfaces 550 of the base SC wire layer 524 being exposed as a result of the patterning of the process 614. The boundaries of the future Josephson Junction 546 and the future interconnect portion 548 are indicated in FIG. 5G with dotted lines.

[00124] The method 600 may then proceed with patterning the stack 535 to electrically isolate the Josephson Junction 546 from the interconnect portion 548 except for the electrical connection by the bridge 542 (process 616 of FIG. 6, result of which is illustrated with a structure 516 of FIG. 5H). To that end, conventional patterning techniques, such as e.g. those described above, may be used to remove portions of the base SC wire 524 until the Josephson Junction 546 and the interconnect portion 548 are electrically separated except for the electrical connection by the bridge 542. An example of that shown in FIG. 5H illustrates that the stack 535 may be removed down to the layer underlying the base SC wire layer 524, e.g. down to the substrate 522, so that a portion of the stack 535 on one side of the opening 536 where a Josephson Junction is to be formed (shown as a portion 552 on the right side of the stack in the example of FIG. 5H) is electrically separated from a portion on the other side of the opening that is to serve as a bulk superconductor of the interconnect 548 (shown as a portion 554 on the left side of the stack in the example of FIG. 5H).

[00125] The method 600 may end with removing the sacrificial material 532 through the window 544 to provide a gap between at least a portion of the Josephson Junction and the interconnect portion (process 618 of FIG. 6, result of which is illustrated with a structure 518 of FIG. 5I). In some embodiments, removal of the sacrificial material 532 may be carried out by an etching process, such as e.g. an isotropic etch, where the sacrificial material 532 in the opening 536 under the bridge 542 is also etched even though it is not exposed via the window 544 (i.e. at least a portion of the sacrificial material 532 under the bridge 542 is undercut). Isotropic etching etches in multiple directions (both vertically and horizontally), unlike e.g. dry etching which only etches in a single direction, and, therefore, can be used to achieve undercutting of the sacrificial material 532 under the bridge 542, thereby providing a void or a gap between at least a portion of the Josephson Junction 546 and the interconnect portion 548.

[00126] In some embodiments, the gap 536 may comprise vacuum since fabrication and operation of the quantum systems is typically carried out under vacuum. In this context, it is

understood that “vacuum” is an idealized term in that a perfect vacuum (i.e. zero pressure) can never be achieved in practical situations. Therefore, the term “vacuum” is used to cover non-zero pressures as long as they are sufficiently low to be considered nearly vacuum. In other embodiments, the gap 536 could contain air or any other gas or a mixture of gasses.

[00127] Any substance suitable for isotropically etching the sacrificial material 532 may be used in the process 618. In various embodiments, an etchant may be e.g. corrosive liquid, such as e.g. hydrofluoric acid (HF) or a chemically active ionized gas (i.e. plasma). As a result of the isotropic etching, a gap is formed between the portions 552 and 554 of the stack 535 so that the stack is electrically connected only via the bridge 542 of the top SC wire 534. Consequences of this are explained in greater detail with reference to FIG. 5J which provides a magnified version of the cross-section structure 518 illustrated in FIG. 5I.

[00128] As shown in FIG. 5J, as a result of the fabrication method 600 as described above, portions of the stack 535 down to the surface 550 of the base SC wire 524 are provided both on the right side 552 and on the left side 554 of the opening 536. The opening 536 does not show any of the sacrificial material 532 in the example of FIG. 5J because the sacrificial material 536 has been completely etched out, which may be particularly advantageous because the sacrificial material 536 may be prone to having spurious TLS's which are undesirable for quantum circuits. In other embodiments, some of the sacrificial material 526 may remain, as long as the Josephson Junction 546 is still electrically isolated from the interconnect portion 548 as described herein.

[00129] A width of the gap between the Josephson Junction 546 and the interconnect portion 548 may be equal to that of the opening 536.

[00130] Because the opening 536 was formed in the stack 535 and because other parts of the stack 535 were etched to form the Josephson Junction 546, the edges 558 of the tunnel barrier layer 558 portion (indicated in FIG. 5J with a solid thick line) of the Josephson Junction 546 are aligned with edges 556 of the base electrode layer 556 portion (indicated in FIG. 5J with a dotted thick line) of the Josephson Junction 546, both for the bilayer and trilayer junctions. In case the Josephson Junction is a trilayer Junction, as is shown in FIG. 5J, the edges 558 of the tunnel barrier layer portion are further aligned with edges 560 of the top electrode layer 530 portion of the Josephson Junction 546. Therefore, in case the Josephson Junction is a

trilayer Junction, the edges 556 of the base electrode layer 556 portion are also aligned with the edges 560 of the top electrode layer 530 portion.

[00131] Both for the bilayer and trilayer junctions, the edges 558 of the tunnel barrier layer and the edges 556 of the base electrode layer are exposed to a gas or a vacuum. In other words, the edges 558 of the tunnel barrier layer and the edges 556 of the base electrode layer are not surrounded by any solid dielectric material, which is advantageous in that eliminating such dielectric material around the Josephson Junction 546 reduces potential sources of spurious TLS's, as described above. In case the Josephson Junction is a trilayer Junction, as is shown in FIG. 5J, the edges 560 of the top electrode layer 530 portion are also exposed to a gas or a vacuum, i.e. not surrounded by any solid dielectric material.

[00132] The interconnect portion 548 together with the top SC wire bridge structure 540 formed in the top SC wire layer 534 form an interconnect for providing electrical interconnection between the top electrode layer of the Josephson Junction (which could be the top electrode layer 530 in case of a trilayer JJ or which could be a portion of the top SC wire layer 534 itself in case of a bilayer JJ) and further components of a quantum circuit, such as e.g. a SQUID loop or a capacitor of a superconducting qubit.

[00133] As shown in FIG. 5J, the interconnect portion 548 is substantially perpendicular to the substrate 552, both for the bilayer and the trilayer architectures.

[00134] For a bilayer JJ, the interconnect portion 548 is substantially parallel to a stack of a portion 562 of the base electrode layer 526 and a portion 564 of the tunnel barrier layer 528 of the Josephson Junction 546. In particular, the interconnect portion 548 includes a portion 568 of the base conductive layer 526 in a single plane with the portion 556 of the base electrode layer of the Josephson Junction 546 and a portion 570 of the dielectric tunnel barrier layer 530 in a single plane with the portion 558 of the tunnel barrier layer of the Josephson Junction 546. For a bilayer JJ, the top SC wire bridge structure 540 formed in the top SC wire layer 534 may be considered to be a second portion of the interconnect, which portion is provided in a plane substantially parallel to a plane of the substrate 522, and which portion acts as the top electrode of the Josephson Junction 546.

[00135] For a trilayer JJ, the interconnect portion 548 is substantially parallel to a stack of the portion 562 of the base electrode layer 526, the portion 564 of the tunnel barrier layer 528, and a portion 566 of the top electrode layer 530 of the Josephson Junction 546. In particular, the interconnect portion 548 includes the portion 568 of the base conductive layer 526 in a single plane with the portion 562 of the base electrode layer of the Josephson Junction 546, the portion 570 of the dielectric tunnel barrier layer 530 in a single plane with the portion 564 of the tunnel barrier layer of the Josephson Junction 546, and a portion 572 of the top conductive layer 530 in a single plane with the portion 566 of the top electrode layer of the Josephson Junction 546. For a trilayer JJ, the top SC wire bridge structure 540 formed in the top SC wire layer 534 may be considered to be a second portion of the interconnect, which portion is provided in a plane substantially parallel to a plane of the substrate 522, and which portion is in electrical contact with the top electrode of the Josephson Junction 546.

[00136] It should be noted that, as can be seen in FIG. 5J, as a result of carrying out the fabrication method as described above, the interconnect portion 548 also includes a stack of layers formed as a junction of the base electrode layer 526, the tunnel barrier layer 528, and the top electrode layer (which could be the layer 530 for the trilayer architecture or the layer 534 for the bilayer architecture), similar to the layers of the Josephson Junction 546. However, because the dimensions of the interconnect portion 548 are of much larger dimensions than the Josephson Junction 546, e.g. measured several thousands of nm in the x-direction and hundreds of nm or more in the y-direction, the interconnect portion 548 is essentially infinite for the Josephson effect to take place and, therefore, acts as a superconductor rather than a Josephson Junction. That is why the interconnect portion 548 may serve as an interconnect configured to support provision of current to the Josephson Junction 546. This also defines the size of the top SC wire bridge structure 540 formed in the top SC wire layer 534 and explains the asymmetry in the top SC wire bridge structure 540 having a larger part on the side 554 of the interconnect than on the side 552 of the Josephson Junction.

[00137] In various embodiments, Josephson Junctions as described herein, e.g. the Josephson Junction 546, could be a part of a superconducting qubit, e.g. a part of a charge qubit, in particular a part of a transmon, or a part of a flux qubit.

[00138] FIG. 7 provides a schematic illustration of a structure 700 comprising a Josephson Junction 746 fabricated using the partially subtractive fabrication method described

herein, according to some embodiments of the present disclosure. As can be seen, FIG. 7 is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. As shown, FIG. 7 represents a cross-section view similar to that shown on FIG. 5J but with real world process limitations shown explicitly, as could be visible in e.g. a scanning electron microscopy (SEM) image or a transmission electron microscope (TEM) image of a structure. In such an image of a real structure, possible processing defects could also be visible.

[00139] FIG. 7 uses similar reference numerals to illustrate element analogous to those shown in FIG. 5J. For example, reference numerals 722 and 522, shown, respectively, in FIGs. 7 and 5J refer to a substrate, reference numerals 724 and 524 – to a base SC wire layer, and so on. Discussions of elements 5XX provided above for FIGs. 5A-5J are applicable to similar elements 7XX shown in FIG. 7 and, therefore, in the interests of brevity, are not repeated for FIG. 7.

[00140] Some Examples in accordance with various embodiments of the present disclosure are now described.

[00141] Example 1 provides a quantum circuit component. The component includes a substrate (e.g. 522); a Josephson Junction (e.g. 546) provided over the substrate, the Josephson Junction including a base electrode layer (e.g. 526), a top electrode layer (e.g. 530 or 534), and a tunnel barrier layer (e.g. 528) provided between the base electrode layer and the top electrode layer. Edges (e.g. 558) of the tunnel barrier layer in a plane of the tunnel barrier layer are aligned with edges (e.g. 556) of the base electrode layer.

[00142] Example 2 provides the quantum circuit component according to Example 1, where the edges of the tunnel barrier layer and the edges of the base electrode layer are exposed to a gas or a vacuum. Thus, these edges are not surrounded by a solid dielectric material.

[00143] Example 3 provides the quantum circuit component according to Examples 1 or 2, further including an interconnect (e.g. 548+534) configured to provide electrical interconnection between the top electrode layer and a further component of the quantum

circuit (such an interconnect is configured to support provision of current to the Josephson Junction).

[00144] Example 4 provides the quantum circuit component according to Example 3, where the further component of the quantum circuit includes a superconducting quantum interference device (SQUID).

[00145] Example 5 provides the quantum circuit component according to Example 3, where the further component of the quantum circuit includes a capacitor of a superconducting qubit.

[00146] Example 6 provides the quantum circuit component according to any one of Examples 3-5, where the interconnect includes a first portion (e.g. 548) substantially perpendicular to the substrate and separated from the Josephson Junction by a gap (536).

[00147] Example 7 provides the quantum circuit component according to Example 6, where a width (d) of the gap is between 10 and 500 nm.

[00148] In the embodiments according to Examples 1-7, the Josephson Junction could be either a trilayer JJ (i.e. a device where the interconnect for supporting provision of current to the JJ is provided in addition to the top electrode of the Josephson Junction), or a bilayer JJ (i.e. a device where the interconnect for supporting provision of current to the JJ also acts as the top electrode of the Josephson Junction).

[00149] Example 8 provides the quantum circuit component according to Examples 6 or 7, where the first portion (e.g. 548) is substantially parallel to a stack of the base electrode layer and the tunnel barrier layer of the Josephson Junction.

[00150] Example 9 provides the quantum circuit component according to any one of Examples 6-8, where the first portion includes a base conductive layer in a single plane with the base electrode layer of the Josephson Junction and a dielectric layer in a single plane with the tunnel barrier layer of the Josephson Junction.

[00151] Example 10 provides the quantum circuit component according to any one of Examples 3-9, where the interconnect includes a second portion (e.g. 534) in a plane

substantially parallel to a plane of the substrate, and where the second portion includes the top electrode of the Josephson Junction.

[00152] In the embodiments according to Examples 8-10, the Josephson Junction is a bilayer Josephson Junction.

[00153] Example 11 provides the quantum circuit component according to Examples 6 or 7, where the first portion (e.g. 548) is substantially parallel to a stack of the base electrode layer, the tunnel barrier layer, and the top electrode layer of the Josephson Junction.

[00154] Example 12 provides the quantum circuit component according to any one of Examples 6, 7, and 11, where the first portion includes a base conductive layer in a single plane with the base electrode layer of the Josephson Junction, a dielectric layer in a single plane with the tunnel barrier layer of the Josephson Junction, and top conductive layer in a single plane with the top electrode layer of the Josephson Junction.

[00155] Example 13 provides the quantum circuit component according to any one of Examples 3-7 and 11-12, where the interconnect includes a second portion (e.g. 534) in a plane substantially parallel to a plane of the substrate, and where a part of the second portion is in contact with the top electrode layer of the Josephson Junction.

[00156] Example 14 provides the quantum circuit component according to any one of Examples 1-7 and 11-13, where the edges of the tunnel barrier layer are further aligned with edges (e.g. 560) of the top electrode layer.

[00157] Example 15 provides the quantum circuit component according to Example 14, where the edges of the tunnel barrier layer, the edges of the base electrode layer, and the edges of the top electrode layer are exposed to a gas or a vacuum.

[00158] In the embodiments according to Examples 11-15, the Josephson Junction is a trilayer Josephson Junction.

[00159] Example 16 provides a quantum integrated circuit package, including a substrate; and a first superconductive qubit and a second superconductive qubit provided over the substrate, where each of the first superconductive qubit and the a second superconductive qubit includes a Josephson Junction including a base electrode layer, a top electrode layer, and

a tunnel barrier layer provided between the base electrode layer and the top electrode layer, and where edges of the tunnel barrier layer are aligned with edges of the base electrode layer.

[00160] Example 17 provides the quantum integrated circuit package according to Example 16, where the first superconductive qubit and the second superconductive qubit are coupled by a coupling resonator.

[00161] Example 18 provides a quantum computing device, including one or more integrated circuit packages according to Examples 16 or 17.

[00162] Example 19 provides the quantum computing device according to Example 18, further including a cooling apparatus configured to maintain the first superconductive qubit and the second superconductive qubit at a cryogenic temperature during operation of the first superconductive qubit and the second superconductive qubit.

[00163] Example 20 provides a method for fabricating at least a Josephson Junction (e.g. 546) of a quantum circuit component. The method includes providing (e.g. 602), over a substrate, a stack of a base superconductive wire layer, a junction base superconductive layer provided over the base superconductive wire layer, and a junction tunnel barrier layer provided over the junction base superconductive layer. The method also includes providing (e.g. 604) an opening through the stack (i.e. the opening extends from the surface to the bottom of the stack and ends at a layer on which the stack is disposed, e.g. at the substrate) and filling (e.g. 606, 608) the opening with a sacrificial material. The method further includes providing (e.g. 610) a top superconductive wire layer over the stack and the sacrificial material in the opening and patterning (e.g. 612) the top superconductive wire layer to form a bridge (e.g. 542) over the opening and a window (e.g. 544) over the opening, the window configured to allow removal of the sacrificial material under the bridge. In addition, the method includes patterning (e.g. 614) the stack to form the Josephson Junction (e.g. 546) and an interconnect portion (e.g. 548), the Josephson Junction and the interconnect portion separated from one another by the opening and electrically connected by the bridge; further patterning (e.g. 616) the stack to electrically isolate the Josephson Junction from the interconnect portion except for the electrical connection by the bridge; and removing (e.g. 618) the sacrificial material through the window to provide a gap between at least a portion of the Josephson Junction and the interconnect portion.

[00164] Example 21 provides the method according to Example 20, where filling the opening with the sacrificial material includes depositing a layer of the sacrificial material over the stack with the opening and polishing the layer of the sacrificial material until an upper surface of the sacrificial material in the opening is aligned with an upper surface of the stack.

[00165] Example 22 provides the method according to Examples 20 or 21, where patterning the stack to form the Josephson Junction includes patterning the junction base superconductive layer to form a base electrode layer of the Josephson Junction and patterning the junction tunnel barrier layer to form a tunnel barrier layer of the Josephson Junction.

[00166] Example 23 provides the method according to any one of Examples 20-22, where the stack further includes a junction top superconductive layer provided over the junction tunnel barrier layer, and where patterning the stack to form the Josephson Junction includes patterning the junction top superconductive layer to form a top electrode layer of the Josephson Junction.

[00167] Example 24 provides the method according to any one of Examples 20-23, where removing the sacrificial material includes performing an isotropic etch of the sacrificial material.

[00168] Example 25 provides the method according to any one of Examples 20-24, where a width (d) of the gap is between 10 and 500 nm.

[00169] In various embodiments, a Josephson Junction as described above could be a part of a superconducting qubit, e.g. a part of a charge qubit, in particular a part of a transmon, or a part of a flux qubit.

[00170] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[00171] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the

disclosure to the specific implementations disclosed in the specification and the claims.

Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims:

1. A quantum circuit component comprising:

a substrate;

a Josephson Junction provided over the substrate, the Josephson Junction comprising a base electrode layer, a top electrode layer, and a tunnel barrier layer provided between the base electrode layer and the top electrode layer,

wherein edges of the tunnel barrier layer are aligned with edges of the base electrode layer.
2. The quantum circuit component according to claim 1, wherein the edges of the tunnel barrier layer and the edges of the base electrode layer are exposed to a gas or a vacuum.
3. The quantum circuit component according to claim 1, further comprising an interconnect configured to provide electrical interconnection between the top electrode layer and a further component of the quantum circuit.
4. The quantum circuit component according to claim 3, wherein the further component of the quantum circuit comprises a superconducting quantum interference device (SQUID).
5. The quantum circuit component according to claim 3, wherein the further component of the quantum circuit comprises a capacitor of a superconducting qubit.
6. The quantum circuit component according to any one of claims 3-5, wherein the interconnect comprises a first portion substantially perpendicular to the substrate and separated from the Josephson Junction by a gap.
7. The quantum circuit component according to claim 6, wherein a width (d) of the gap is between 10 and 500 nanometers.

8. The quantum circuit component according to claim 6, wherein the first portion is substantially parallel to a stack of the base electrode layer and the tunnel barrier layer of the Josephson Junction.

9. The quantum circuit component according to claim 6, wherein the first portion comprises a base conductive layer in a single plane with the base electrode layer of the Josephson Junction and a dielectric layer in a single plane with the tunnel barrier layer of the Josephson Junction.

10. The quantum circuit component according to any one of claims 3-5, wherein the interconnect comprises a second portion in a plane substantially parallel to a plane of the substrate, and wherein the second portion comprises the top electrode of the Josephson Junction.

11. The quantum circuit component according to claim 6, wherein the first portion is substantially parallel to a stack of the base electrode layer, the tunnel barrier layer, and the top electrode layer of the Josephson Junction.

12. The quantum circuit component according to claim 6, wherein the first portion comprises a base conductive layer in a single plane with the base electrode layer of the Josephson Junction, a dielectric layer in a single plane with the tunnel barrier layer of the Josephson Junction, and top conductive layer in a single plane with the top electrode layer of the Josephson Junction.

13. The quantum circuit component according to claim 12, wherein the interconnect comprises a second portion in a plane substantially parallel to a plane of the substrate, and wherein a part of the second portion is in contact with the top electrode layer of the Josephson Junction.

14. The quantum circuit component according to any one of claims 1-5, wherein the edges of the tunnel barrier layer are further aligned with edges of the top electrode layer.

15. The quantum circuit component according to claim 14, wherein the edges of the tunnel barrier layer, the edges of the base electrode layer, and the edges of the top electrode layer are exposed to a gas or a vacuum.

16. A quantum integrated circuit package, comprising:

a substrate; and

a first superconductive qubit and a second superconductive qubit provided over the substrate,

wherein each of the first superconductive qubit and the a second superconductive qubit comprises a Josephson Junction comprising a base electrode layer, a top electrode layer, and a tunnel barrier layer provided between the base electrode layer and the top electrode layer, and wherein edges of the tunnel barrier layer are aligned with edges of the base electrode layer.

17. The quantum integrated circuit package according to claim 16, wherein the first superconductive qubit and the second superconductive qubit are coupled by a coupling resonator.

18. A quantum computing device, comprising one or more integrated circuit packages according to claims 16 or 17.

19. The quantum computing device according to claim 18, further comprising a cooling apparatus configured to maintain the first superconductive qubit and the second superconductive qubit at a cryogenic temperature during operation of the first superconductive qubit and the second superconductive qubit.

20. A method for fabricating at least a Josephson Junction of a quantum circuit component, the method comprising:

providing, over a substrate, a stack of a base superconductive wire layer, a junction base superconductive layer, and a junction tunnel barrier layer;

providing an opening through the stack;

filling the opening with a sacrificial material;

providing a top superconductive wire layer over the stack and the sacrificial material in the opening;

patterning the top superconductive wire layer to form a bridge over the opening and a window over the opening, the window configured to allow removal of the sacrificial material under the bridge;

patterning the stack to form the Josephson Junction and an interconnect portion, the Josephson Junction and the interconnect portion separated from one another by the opening and electrically connected by the bridge;

further patterning the stack to electrically isolate the Josephson Junction from the interconnect portion except for the electrical connection by the bridge; and

removing the sacrificial material through the window to provide a gap between at least a portion of the Josephson Junction and the interconnect portion.

21. The method according to claim 20, wherein filling the opening with the sacrificial material comprises depositing a layer of the sacrificial material over the stack with the opening and polishing the layer of the sacrificial material until an upper surface of the sacrificial material in the opening is aligned with an upper surface of the stack.

22. The method according to claim 20, wherein patterning the stack to form the Josephson Junction comprises patterning the junction base superconductive layer to form a base electrode layer of the Josephson Junction and patterning the junction tunnel barrier layer to form a tunnel barrier layer of the Josephson Junction.

23. The method according to any one of claims 20-22, wherein the stack further comprises a junction top superconductive layer, and wherein patterning the stack to form the Josephson Junction comprises patterning the junction top superconductive layer to form a top electrode layer of the Josephson Junction.

24. The method according to any one of claims 20-22, wherein removing the sacrificial material comprises performing an isotropic etch of the sacrificial material.

25. The method according to any one of claims 20-22, wherein a width (d) of the gap is between 10 and 500 nanometers.

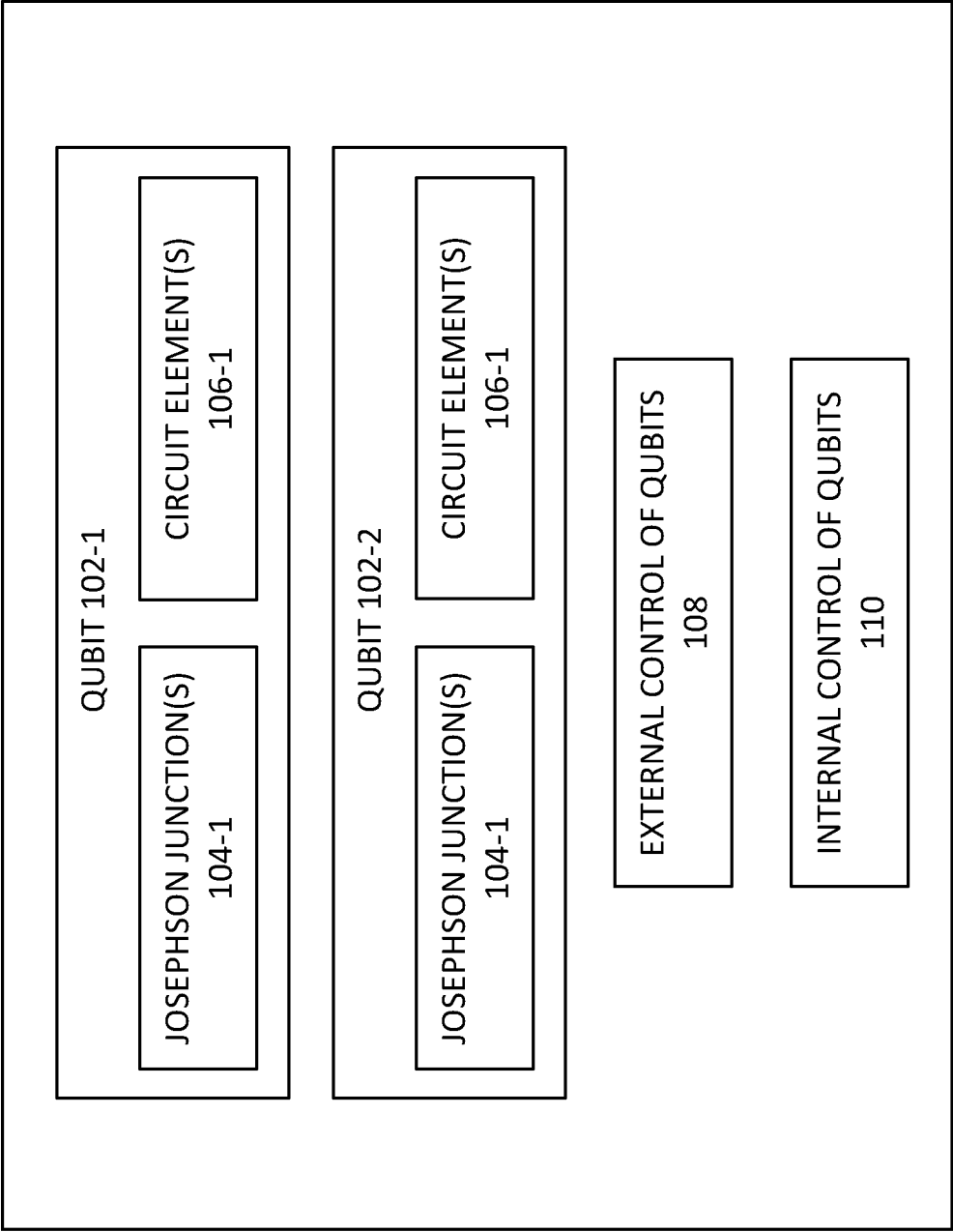


FIG. 1A

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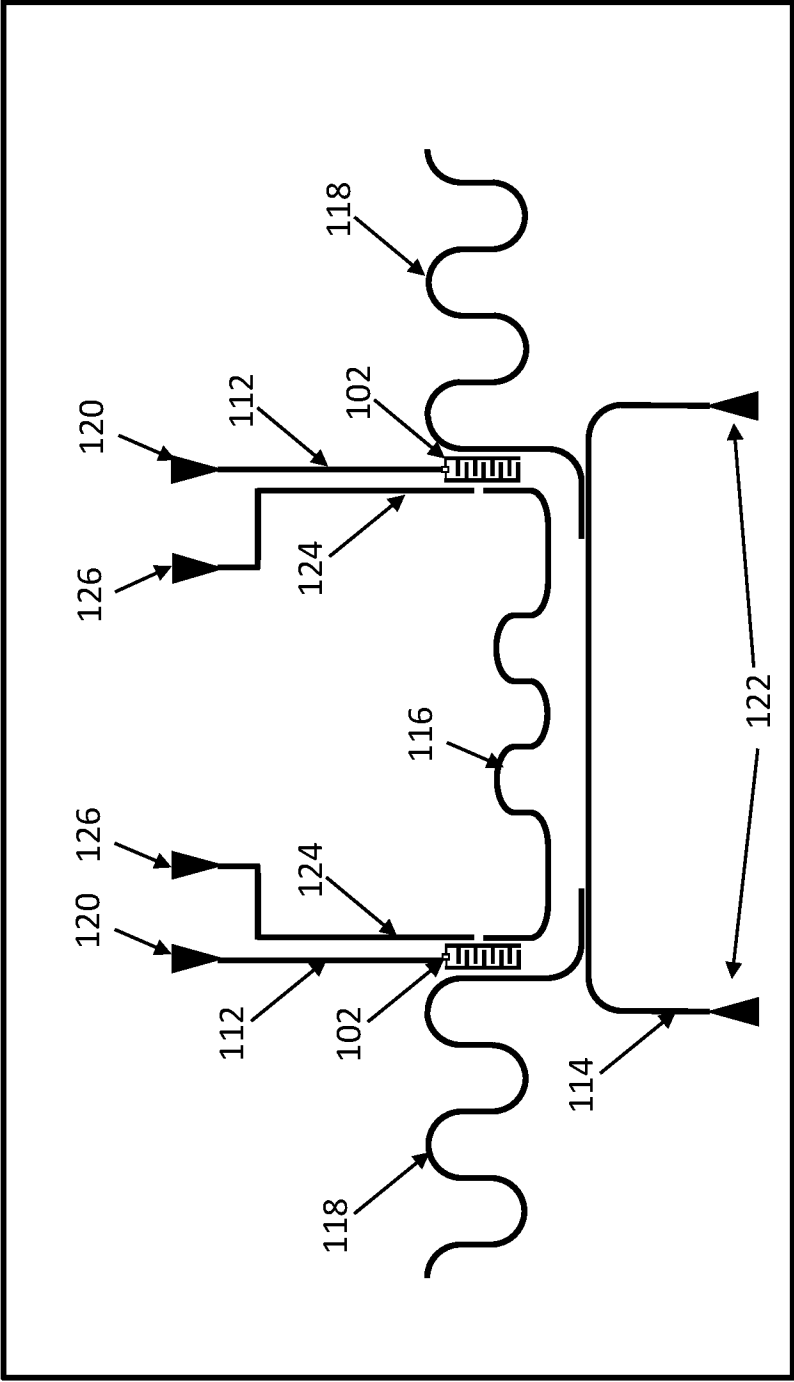
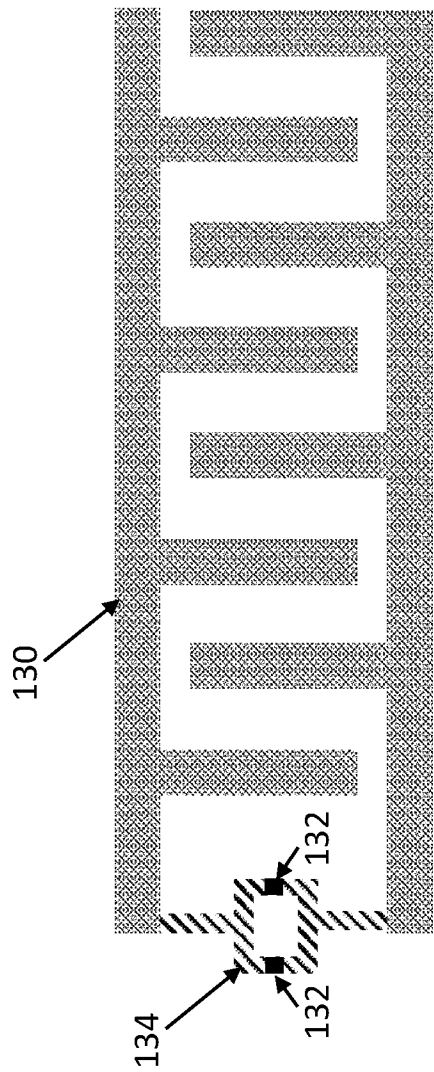


FIG. 1B

100B



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FIG. 1C

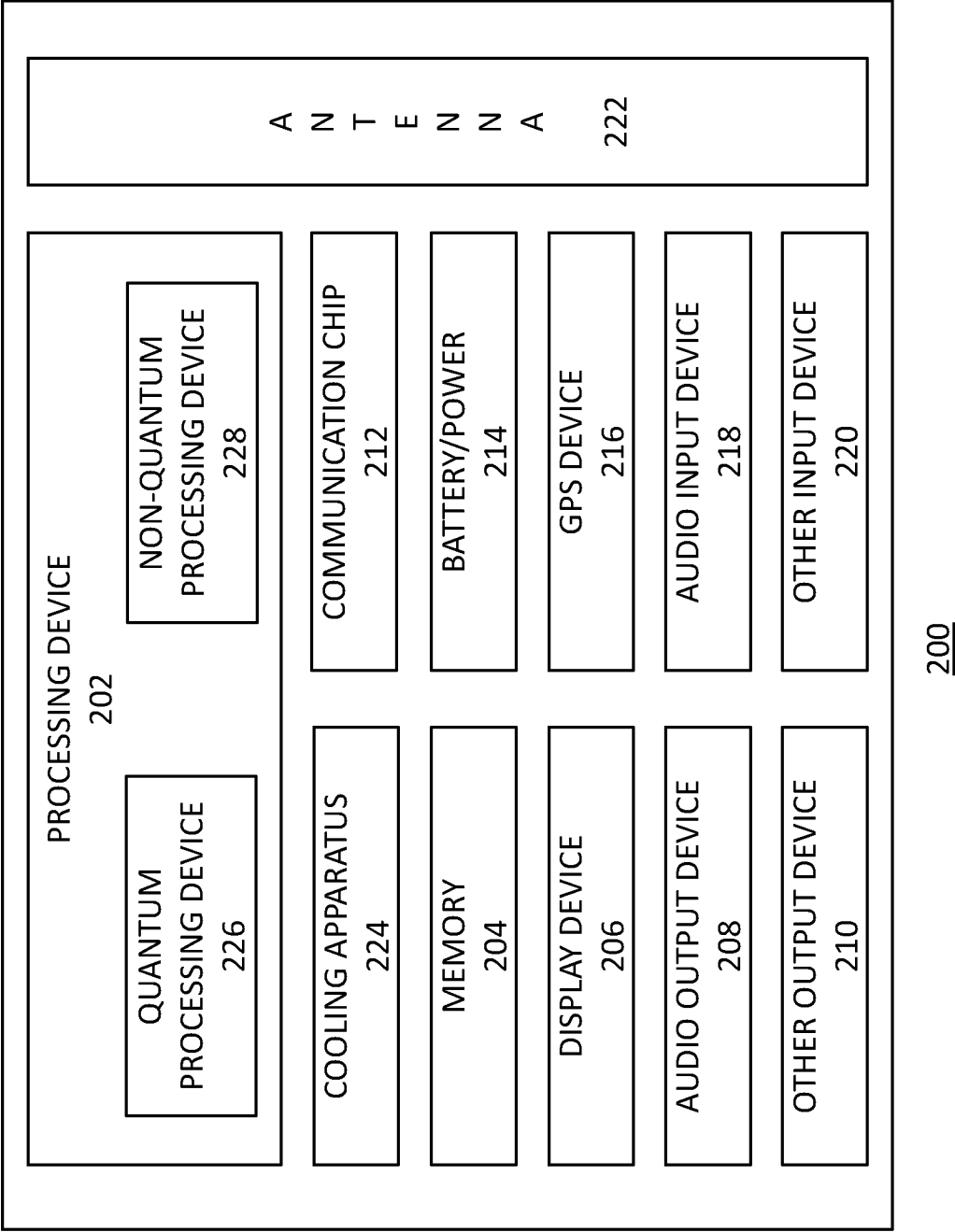


FIG. 2

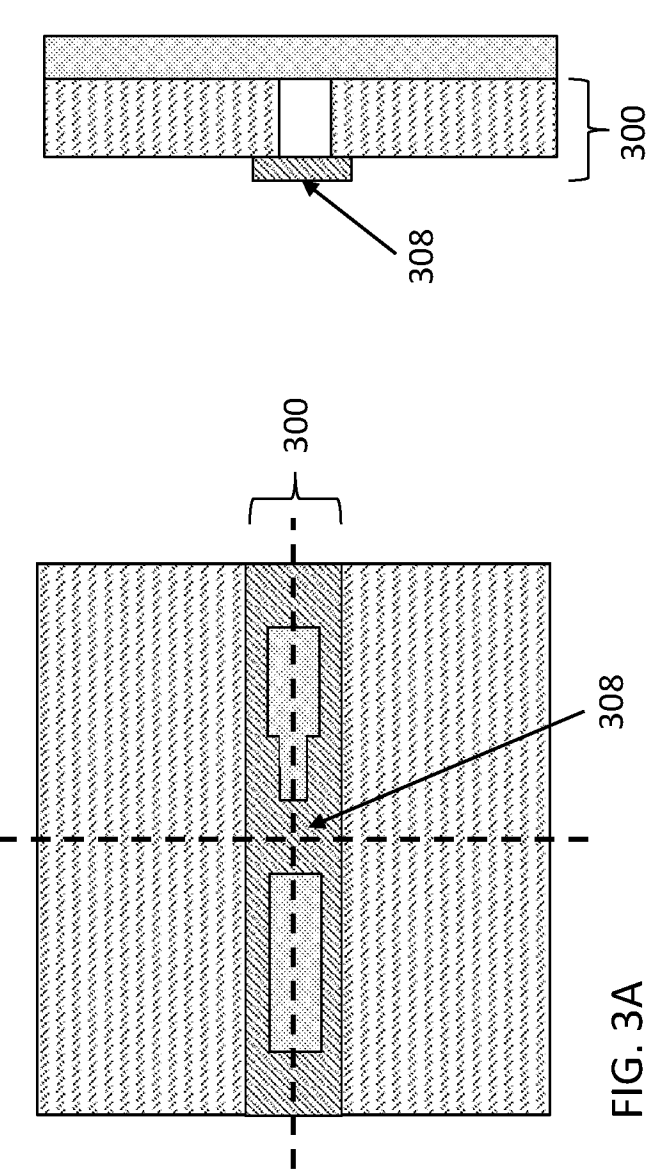


FIG. 3C

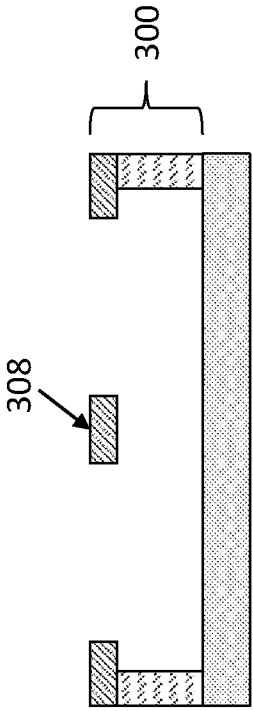
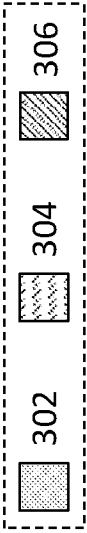
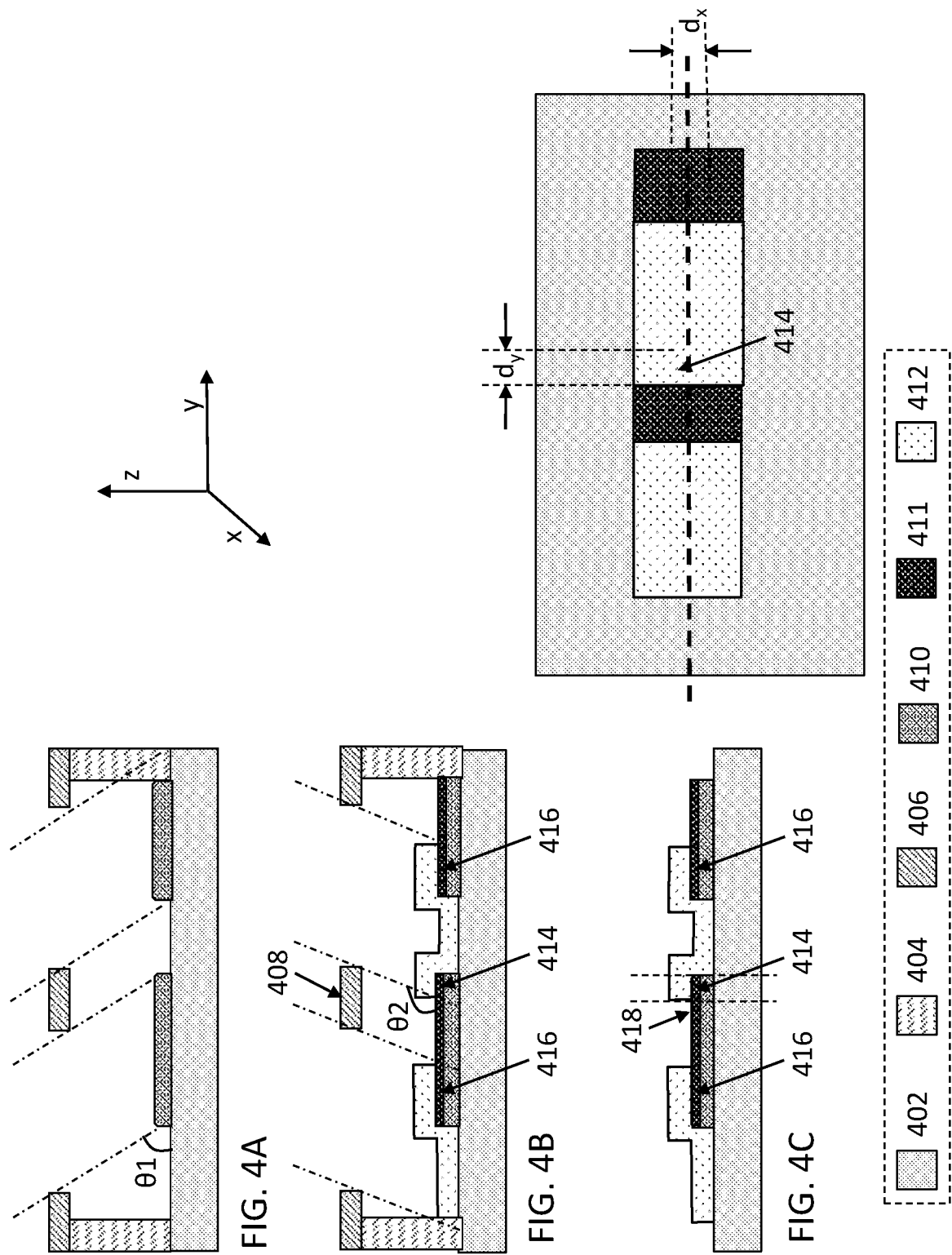
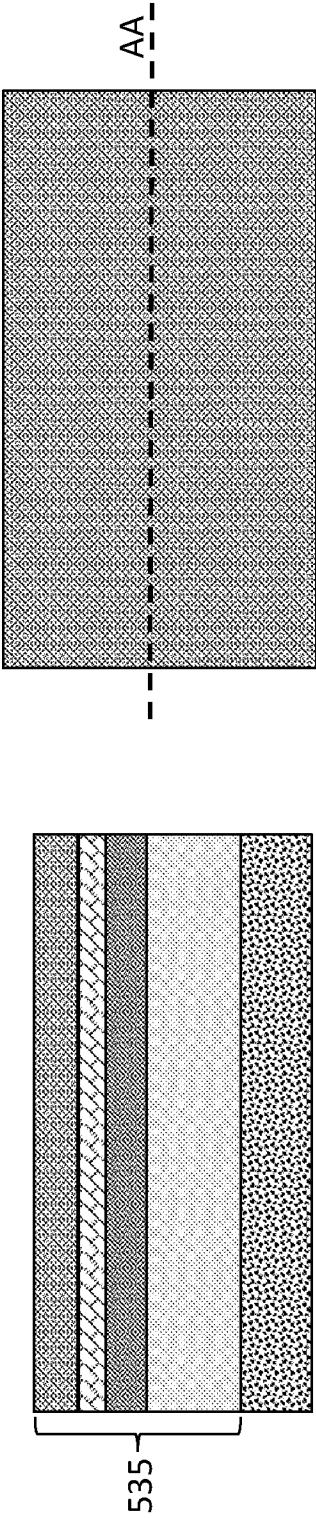


FIG. 3B

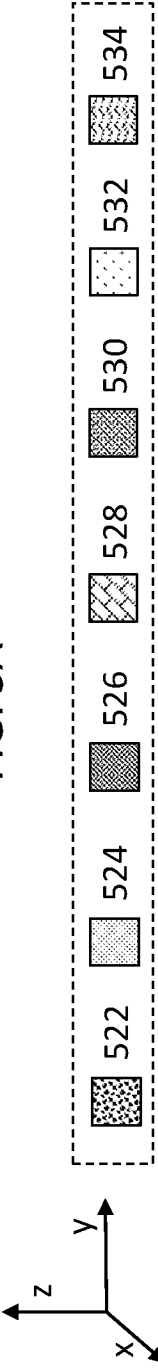


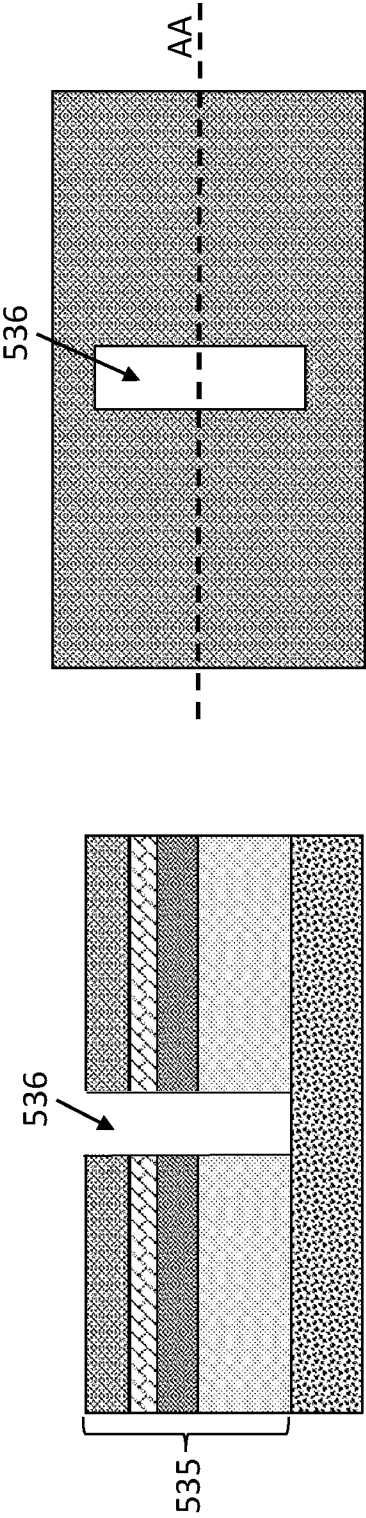




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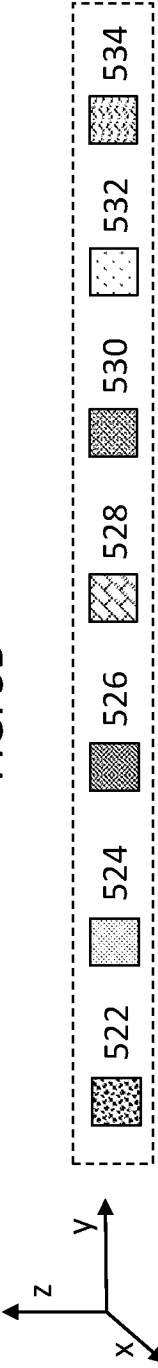
FIG. 5A

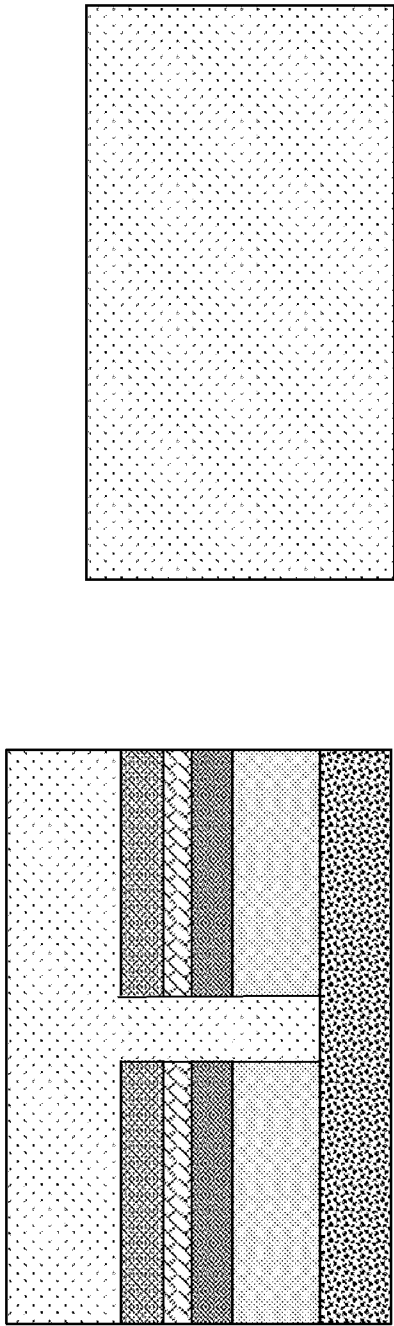




504

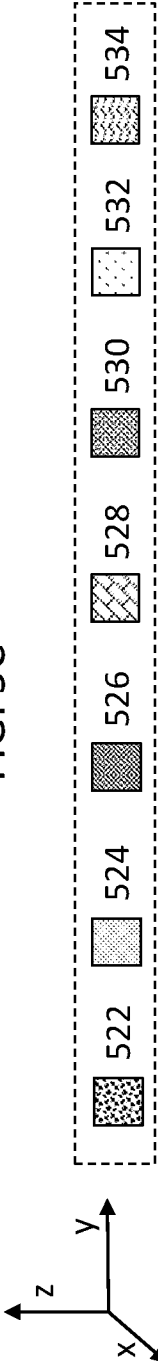
FIG. 5B

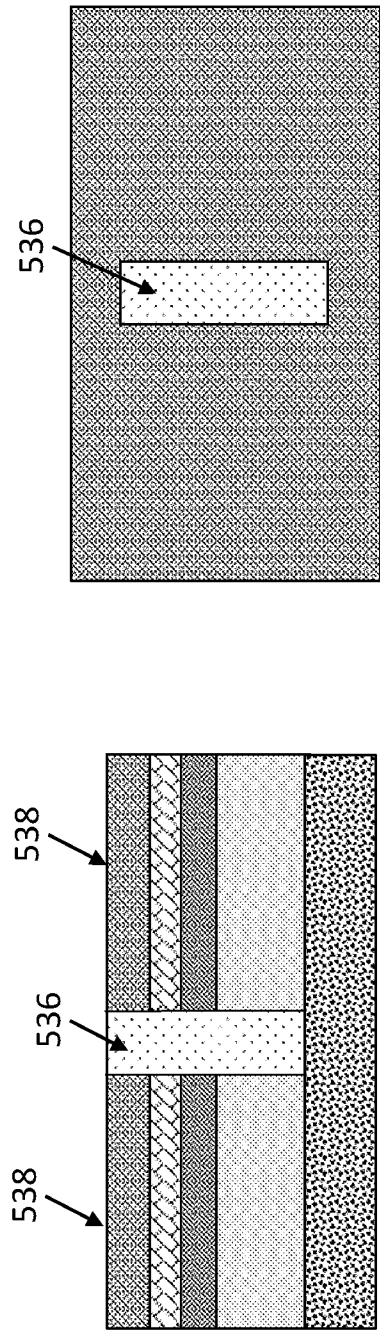




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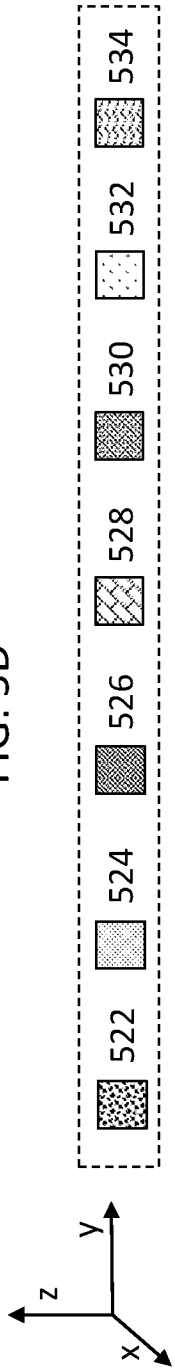
FIG. 5C

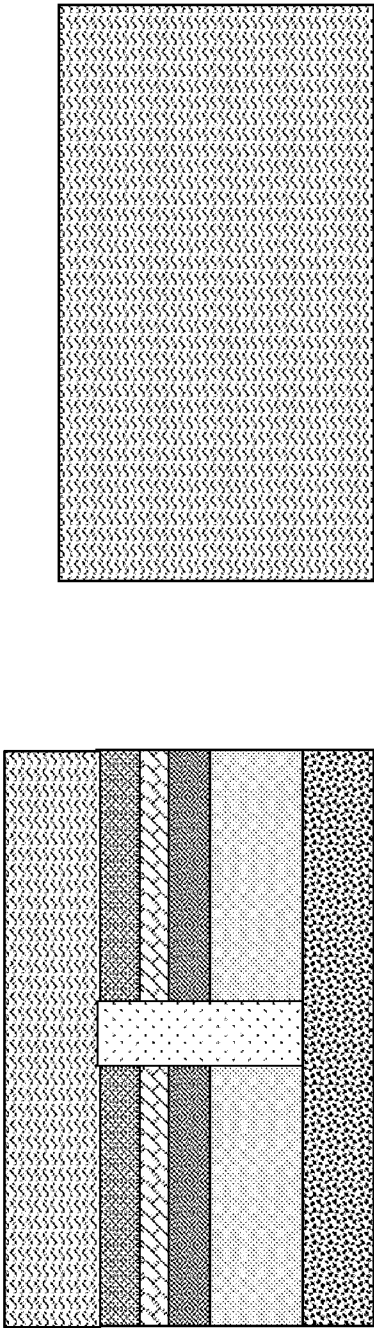




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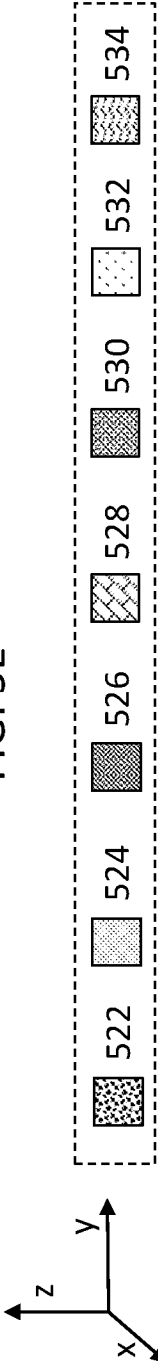
FIG. 5D

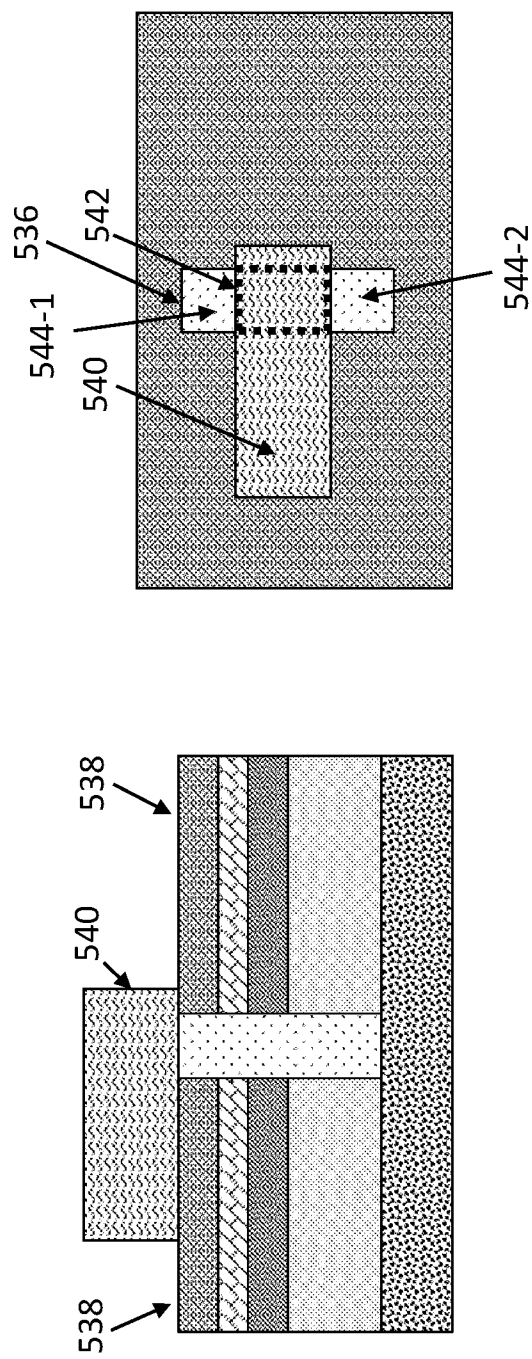




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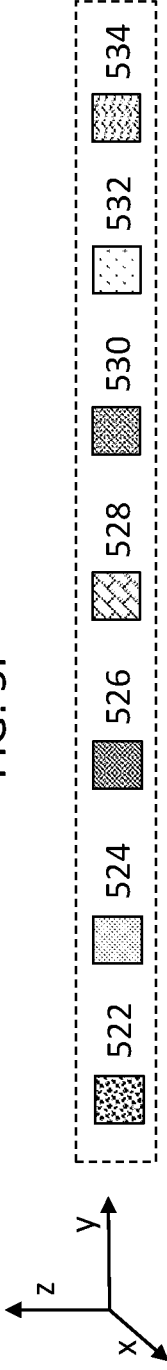
FIG. 5E

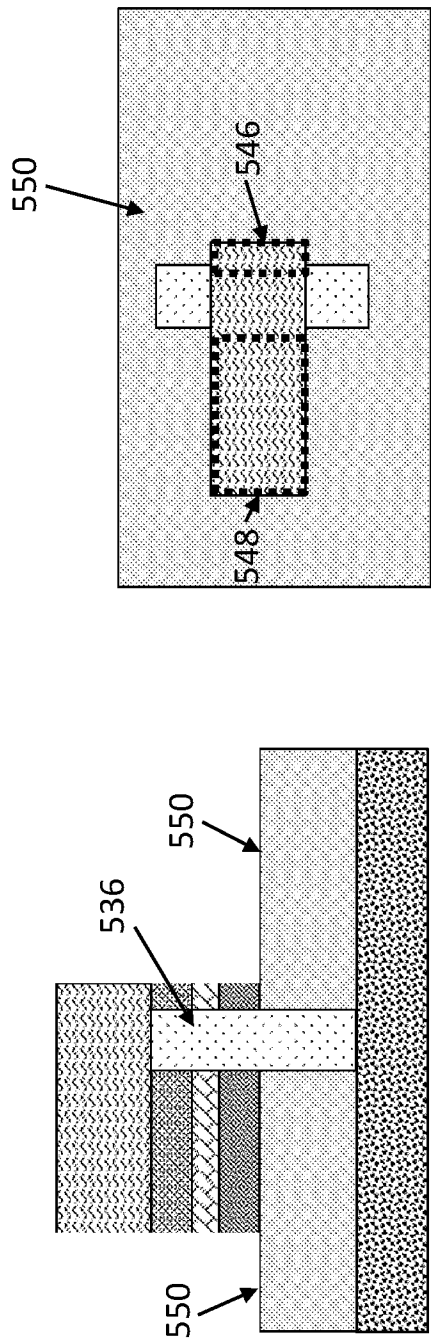




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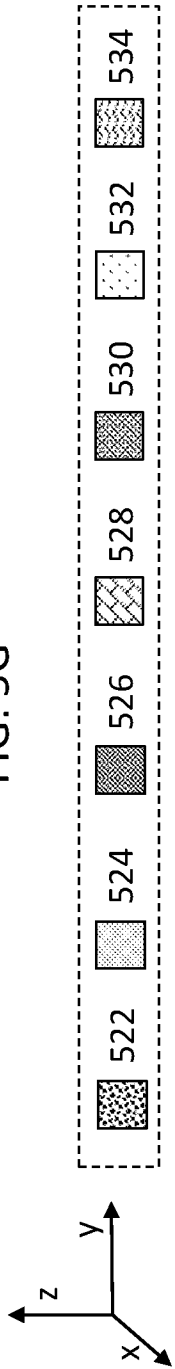
FIG. 5F

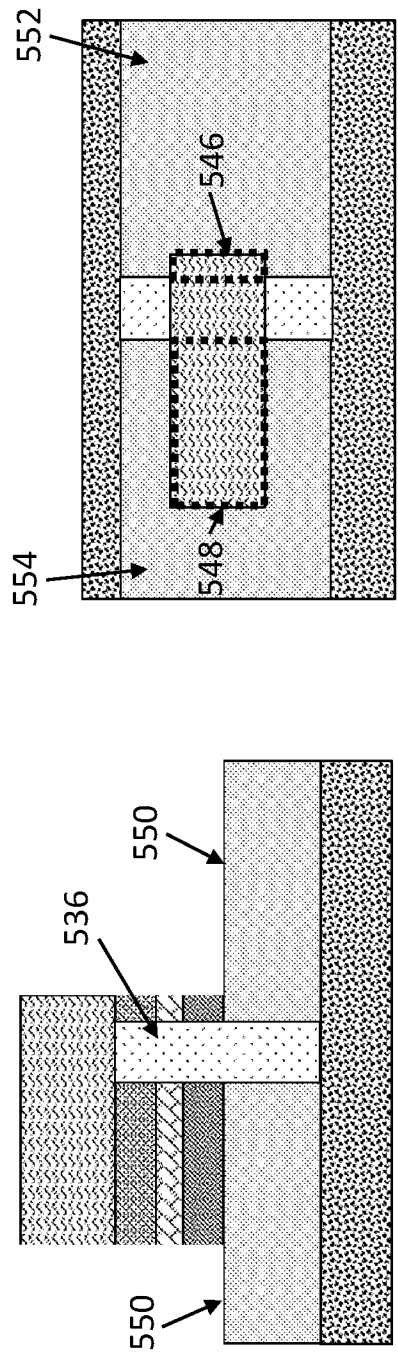




514

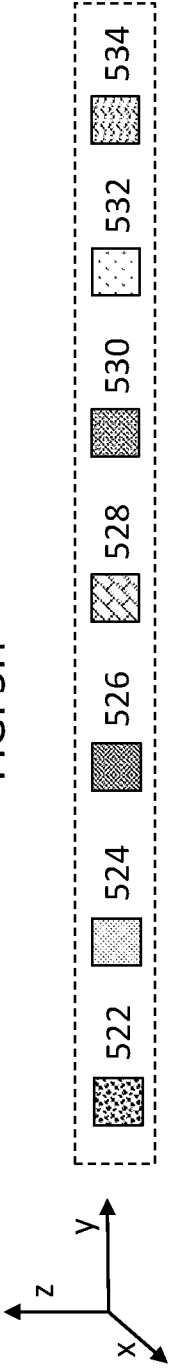
FIG. 5G

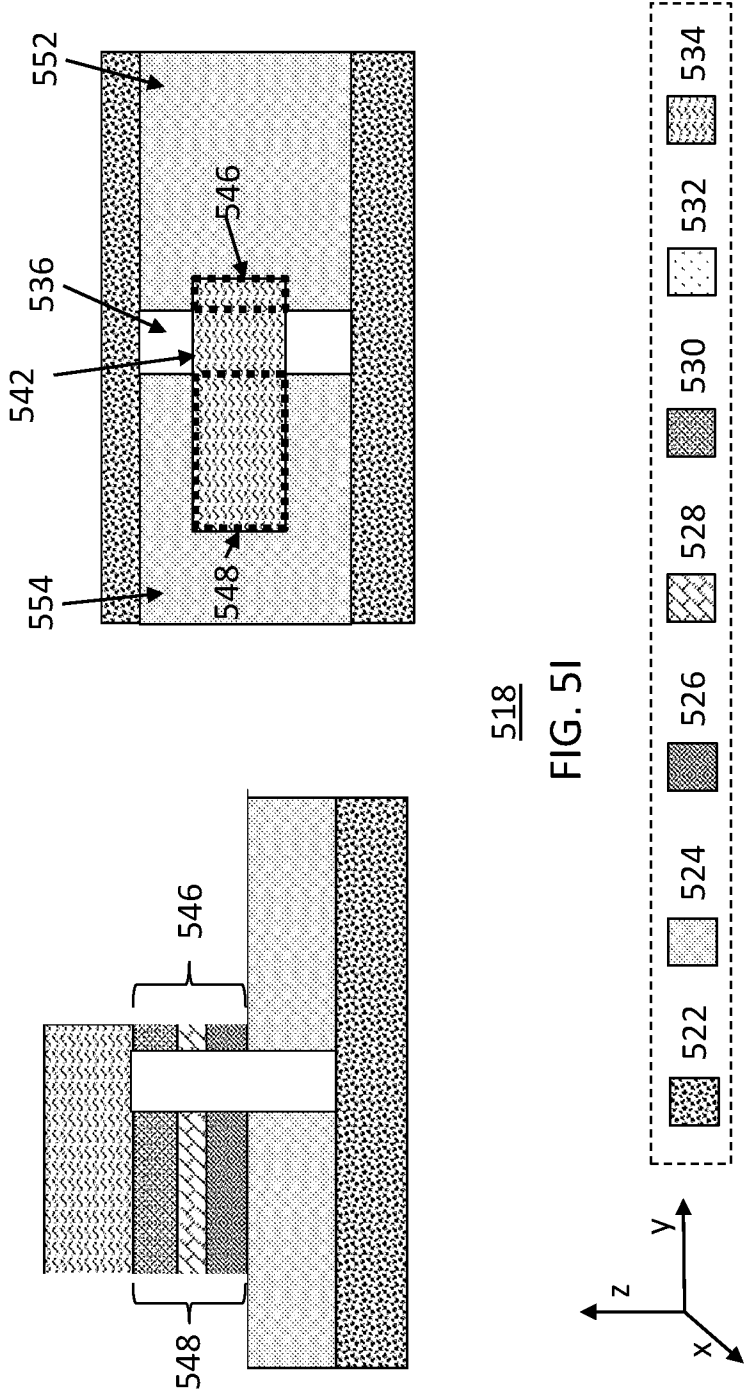


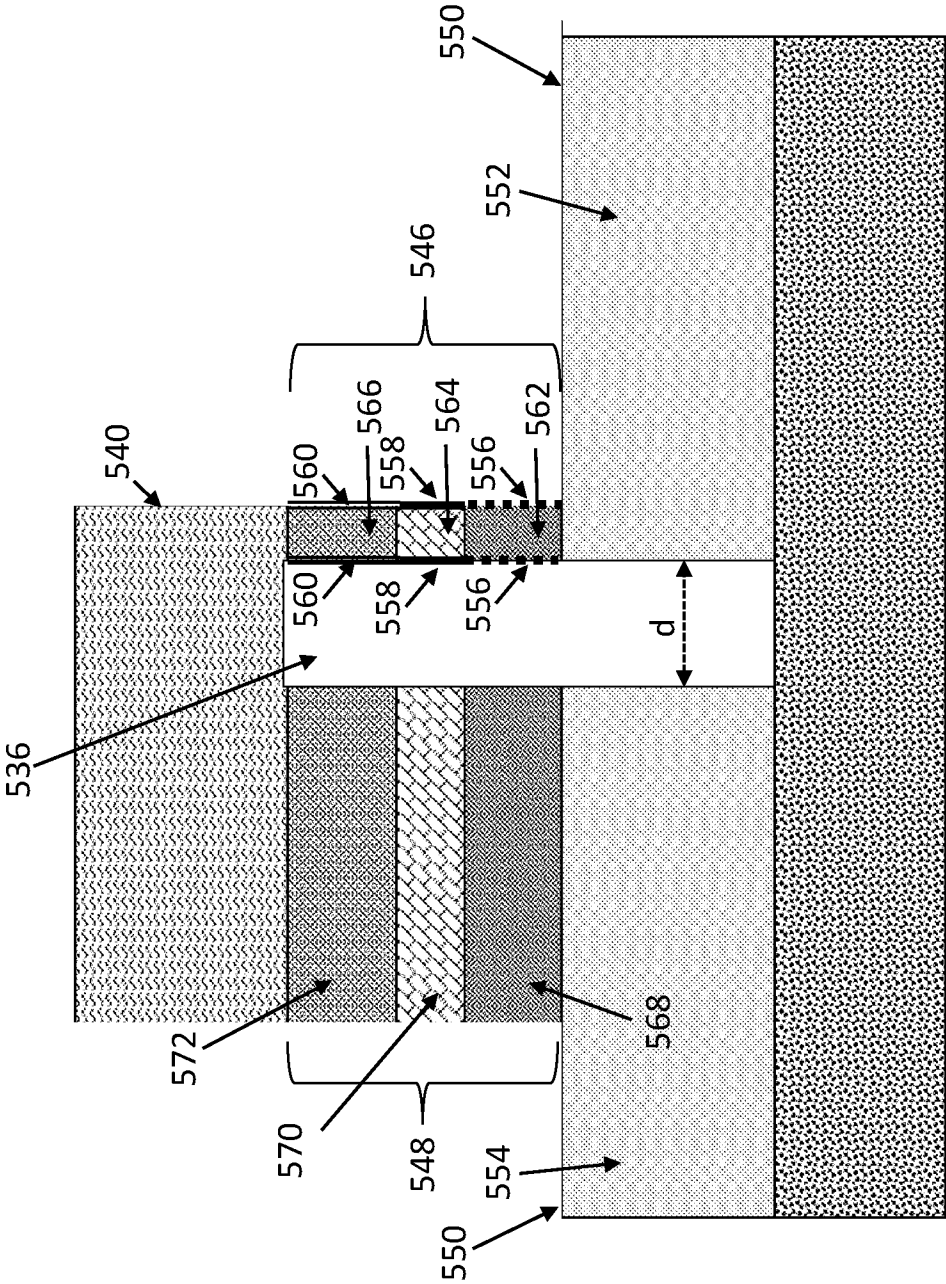


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FIG. 5H







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FIG. 5J

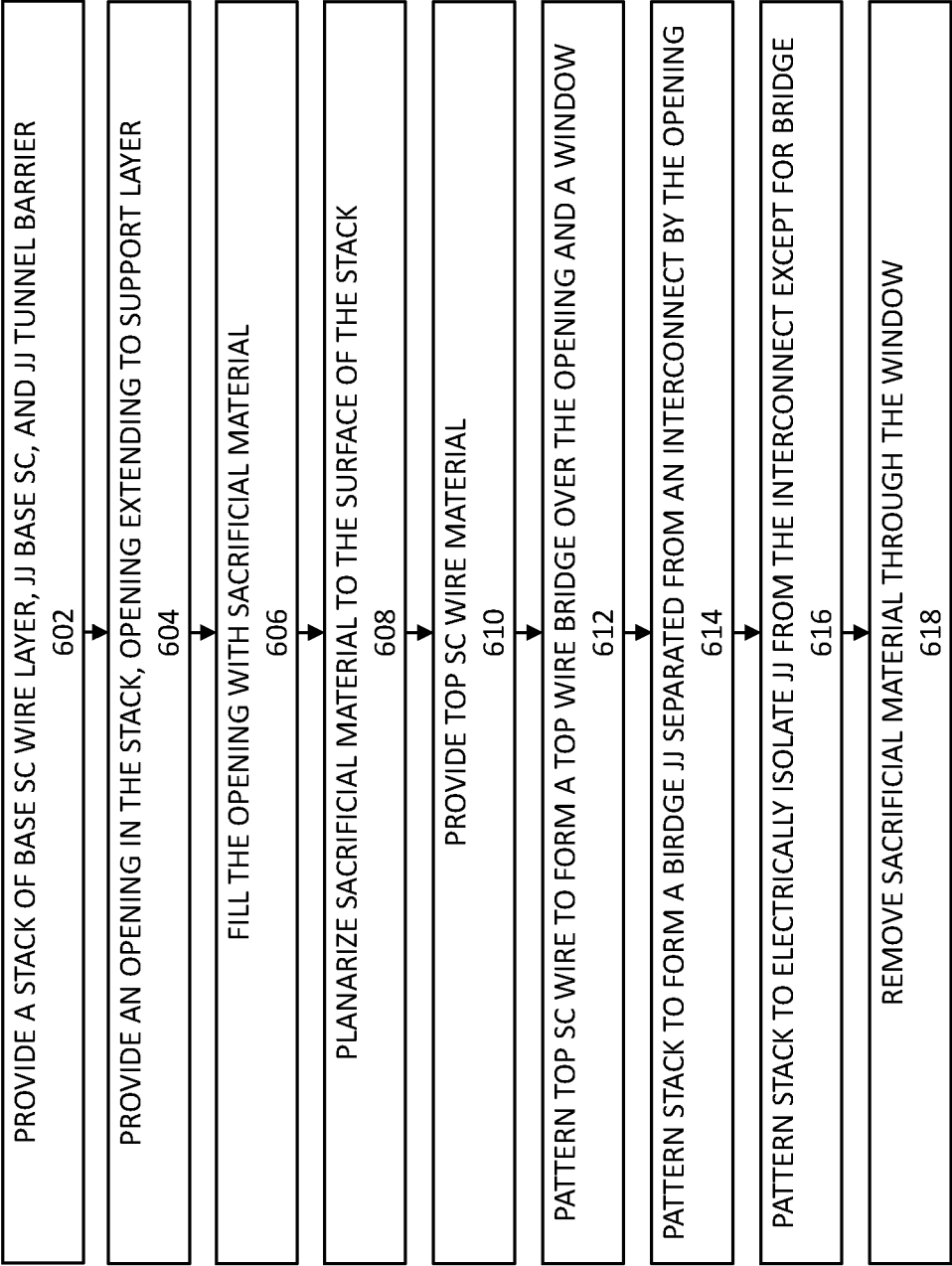
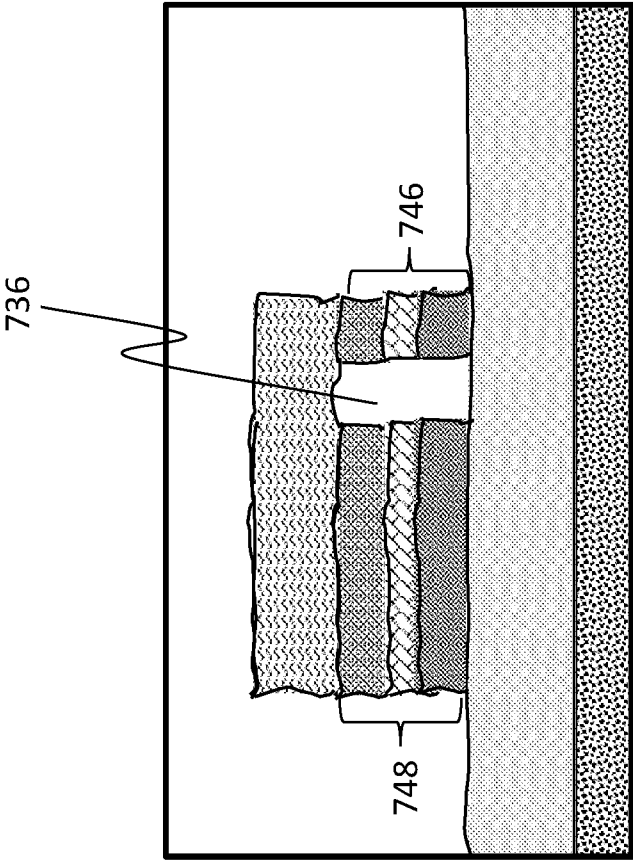


FIG. 6



700



FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER**H01L 39/02(2006.01)i, H01L 39/24(2006.01)i, H01L 29/66(2006.01)i, H01L 29/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 39/02; H01L 27/18; H01L 39/24; H01L 39/12; H01L 23/498; H01L 39/22; H01L 39/04; H01L 29/66; H01L 29/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: Josephson Junction, quantum, substrate, tunnel barrier, superconducting

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0133050 A1 (MICHAEL C. GAIDIS) 31 May 2012 See paragraphs [0003], [0017]; and figure 2.	1, 14, 16, 18
Y		2-13, 15, 17, 19
A		20-25
Y	US 2015-0187840 A1 (D-WAVE SYSTEMS INC.) 02 July 2015 See paragraphs [0070], [0074], [0083], [0085], [0090]; and figures 2, 3, 6B.	2-13, 15, 17, 19
Y	US 2015-0380631 A1 (THE UNITED STATES OF AMERICA AS REPRESENTED BY THE SECRETARY OF THE NAVY) 31 December 2015 See paragraph [0025]; and figure 2.	4
A	US 2015-0340584 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 26 November 2015 See paragraphs [0020]-[0031]; and figures 1A-4.	1-25
A	US 2015-0380632 A1 (HYPRES INC.) 01 December 2015 See paragraphs [0035]-[0048]; and figures 1-14.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 April 2017 (25.04.2017)

Date of mailing of the international search report

25 April 2017 (25.04.2017)

Name and mailing address of the ISA/KR

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Telephone No. +82-42-481-3580



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/045941

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