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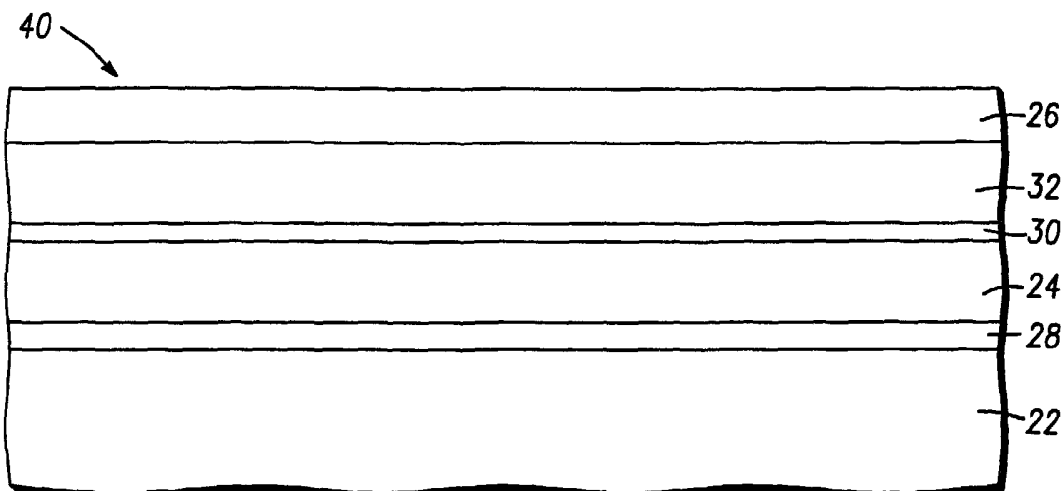
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(54) Title: EPITAXIAL SEMICONDUCTOR ON INSULATOR (SOI) STRUCTURES AND DEVICES



(57) Abstract: High quality epitaxial layers of monocrystalline materials (26) can be grown overlying monocrystalline substrates (22) such as large silicon wafers by forming a compliant substrate for growing the monocrystalline layers. An accommodating buffer layer (24) comprises a layer of monocrystalline oxide spaced apart from the silicon wafer (22) by an amorphous interface layer (28) of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. The accommodating buffer layer is lattice matched to both the underlying silicon wafer and the overlying monocrystalline material layer. A monocrystalline layer (26) is then formed over the accommodating buffer layer, such that a lattice constant of the monocrystalline layer substantially matches the lattice constant of a subsequently grown monocrystalline film.



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EPITAXIAL SEMICONDUCTOR ON INSULATOR (SOI) STRUCTURES AND DEVICES

Field of the Invention

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This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to semiconductor on insulator (SOI) structures and devices and to the fabrication and use of SOI structures, devices, and integrated circuits that include a monocrystalline material layer comprised of semiconductor material, and/or other types of material such as metals and non-metals.

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Background of the Invention

Semiconductor devices often include multiple layers of conductive, insulating, and semiconductive layers. Often, the desirable properties of such layers improve with the crystallinity of the layer. For example, the electron mobility and band gap of semiconductive layers improves as the crystallinity of the layer increases. Similarly, the free electron concentration of conductive layers and the electron charge displacement and electron energy recoverability of insulative or dielectric films improves as the crystallinity of these layers increases.

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For many years, attempts have been made to grow various monolithic thin films on a foreign substrate such as silicon (Si). To achieve optimal characteristics of the various monolithic layers, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow various monocrystalline layers on a substrate such as germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting layer of monocrystalline material to be of low crystalline quality.

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If a large area thin film of high quality monocrystalline material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in or

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using that film at a low cost compared to the cost of fabricating such devices beginning with a bulk wafer of semiconductor material or in an epitaxial film of such material on a bulk wafer of semiconductor material. In addition, if a thin film of high quality monocrystalline material could be realized beginning with a bulk wafer such as a silicon wafer, an integrated device structure could be achieved that took advantage of the best properties of both the silicon and the high quality monocrystalline material.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline film or layer over another monocrystalline material and for a process for making such a structure. In other words, there is a need for providing the formation of a monocrystalline substrate that is compliant with a high quality monocrystalline material layer so that true two-dimensional growth can be achieved for the formation of quality semiconductor structures, devices and integrated circuits having grown monocrystalline film having the same crystal orientation as an underlying substrate. This monocrystalline material layer may be comprised of a semiconductor material, and other types of material such as metals and non-metals.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying drawing figures, in which like references indicate similar elements, and in which:

FIGS. 1, 2, and 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIGS. 5-7 illustrate schematically, in cross-section, the formation of yet another embodiment of a device structure in accordance with the invention;

FIG. 8 illustrates schematically, in cross section, a monolithic integrated circuit in accordance with one embodiment of the invention; and

FIG. 9 illustrates schematically, in cross section, a monolithic integrated circuit in accordance with yet another embodiment of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

10 FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a monocrystalline material layer 26. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

20 In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and monocrystalline material layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the monocrystalline material layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

25 Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of, for example, a material from Group IV of the periodic table. Examples of Group IV

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semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like.

Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry.

5 Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous
10 intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the
15 crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline material layer 26 which may comprise a semiconductor material, or another type of material such as a metal or a non-metal.

20 Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying material layer. For example, the material could be an oxide or nitride having a lattice structure closely matched to the substrate and to the subsequently applied monocrystalline material layer. Materials that are suitable for the
25 accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such
30 as gallium nitride, aluminum nitride, and boron nitride may also be used for the

accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitrides may include three or more different metallic elements.

In accordance with one embodiment of the present invention, accommodating buffer layer 24 is a material having the empirical formula ABO_x , wherein A is magnesium (Mg), calcium (Ca), strontium (Sr), barium (Ba), or a combination of two or more of these, and B is titanium (Ti), zirconium (Zr), hafnium (Hf), or a combination of two or more of these. The composition of accommodating buffer layer 24 preferably is chosen such that it is at least partially, and preferably substantially, lattice matched to the overlying material layer.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

In general, layer 32 provides a transition in lattice constants between the lattice constant of accommodating buffer layer 24 and a subsequently deposited layer of monocrystalline material overlying graded layer 32. More particularly, the material for layer 32 is selected such that the lattice constant of layer 32 can be altered by changing the composition of layer 32, such that a bottom portion of layer 32 is lattice matched to accommodating buffer layer 24 and a top portion of layer 32 is lattice matched to the subsequently applied layer of monocrystalline material.

The material for graded monocrystalline layer 32 can be selected, as desired, for a particular structure or application. For example, the monocrystalline material of layer 32 may comprise a mixed Group IV semiconductor, where the lattice constant of the material is altered as a function of thickness of the film by varying the ratio of components in the film. In accordance with one embodiment of the invention, layer 32 comprises Si_yGe_{1-y} (y ranges from 0 to 1) where the concentration of germanium is low

(*i.e.*, 0%) near the surface of template 30 and high (*i.e.*, 100%) near the top of layer 32. In this case, the lower surface of layer 32 is closely lattice matched to material comprising accommodating buffer layer 24, whereas the top of layer 32 is lattice matched to germanium. In accordance with another embodiment of the invention, layer 5 32 comprises germanium, which is closely lattice matched to the material comprising accommodating buffer layer 24 (such as, for example, SrTiO₃). As used herein, the term “graded” may refer to monocrystalline layers comprising more than one semiconductor component in which the lattice constant of the monocrystalline material is altered as a function of thickness in the film by varying the components in the film 10 (*e.g.*, Si_yGe_{1-y} or SiC). Thus, structure 20 provides a suitable substrate for subsequent growth of monocrystalline material having a lattice constant that differs from the lattice constants of materials of either substrate 22 or accommodating buffer layer 24.

Appropriate materials for template 30 are discussed below. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at 15 selected sites and provide sites for the nucleation of the epitaxial growth of graded monocrystalline layer 32. When used, template layer 30 has a thickness ranging from about 1 to about 10 monolayers.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the 20 previously described semiconductor structure 20, except that an additional layer of monocrystalline material 26 is formed over graded layer 32. Layer 26 material may include insulating, semiconducting, or conducting materials. For example, layer 26 may include semiconductor materials such as Group IV materials; conducting materials such as metals; and insulating material such as oxides.

25 FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional monocrystalline layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline layer 38 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The
5 accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between
10 substrate 22 and additional monocrystalline layer 26 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing—*e.g.*, monocrystalline material layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline material layers over a monocrystalline substrate.
15 However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline material layers because it allows any strain in layer 26 to relax.

Additional monocrystalline layer 38 may include any of the materials described
20 throughout this application in connection with either of monocrystalline material layer 26 or additional buffer layer 32. For example, when monocrystalline material layer 26 comprises a semiconductor material, layer 38 may include monocrystalline Group IV materials.

In accordance with one embodiment of the present invention, additional
25 monocrystalline layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent monocrystalline layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline material.

In accordance with another embodiment of the invention, additional monocrystalline layer 38 comprises monocrystalline material (*e.g.*, a material discussed above in connection with monocrystalline layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include monocrystalline material layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one monocrystalline layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $\text{Ca}_z\text{Sr}_{1-z}\text{TiO}_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 32. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 5 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the graded layer from the substrate. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1 to 2 nm.

In accordance with this embodiment of the invention, monocrystalline layer 32 is a Group IV semiconductor layer comprising $\text{Si}_y\text{Ge}_{1-y}$, where y ranges from 0 to 1 having a thickness of about 1 nm to about 100 μm , preferably a thickness of about 0.1 μm to 10 μm , and more preferably about 0.1 to 5 μm . The thickness generally depends on the subsequently deposited material (*e.g.*, layer 26 of Figs. 2-3). The compositions of other compound semiconductor materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. To facilitate the epitaxial growth of the graded layer on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Sr-Si, SiO_x , Sr-Si-O, Ti-Si, Ti-Ge, Sr-Ge-O, Sr-Ge, GeO_x .

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline SrZrO_3 , BaZrO_3 , SrTiO_3 , or BaTiO_3 . For example, a monocrystalline oxide layer of $\text{Sr}(\text{Zr,Ti})\text{O}_3$ can grow at a temperature of about 700° C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or titanate materials is suitable for the growth of a monocrystalline material layer which comprises semiconductor materials such as germanium (Ge), having a thickness of about 1.0 nm to 10 μm . A suitable template for this structure is 1-10 monolayers of Ti-Ge, Sr-Ge-O, Sr-Ge, or GeO_x , and preferably 1-2 monolayers of one of these materials. By way of an example, for a $\text{Sr}(\text{Zr,Ti})\text{O}_3$ accommodating buffer layer, the surface is terminated with 1-2 monolayers of titanium followed by deposition of 1-2 monolayers of germanium to form a Ti-Ge template. A monocrystalline layer of germanium is then grown on the template layer. The resulting lattice structure of the semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) Ge of less than 2.5%, and preferably less than about 1.0%.

Example 3

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline graded layer 32 and template layer 30 can be the same as those described above in Example 1. In accordance with one aspect of this embodiment, layer 32 includes $\text{Si}_y\text{Ge}_{1-y}$, in which the silicon composition varies from 0 to about 50%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of layer 32 from SiGe to Ge serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline material which in this Example is a Ge layer.

Example 4

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline material layer 26 may be the same as those described above in connection with Example 4.

Amorphous layer 36 is an amorphous layer which is suitably formed of a combination of amorphous intermediate layer materials (*e.g.*, layer 28 materials as described above) and accommodating buffer layer materials (*e.g.*, layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x , $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ (where z ranges from 0 to 1), and Si which combine or mix, at least partially, during an anneal process to form amorphous layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of monocrystalline material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline material that can be grown epitaxially over a monocrystalline material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the

same materials as those comprising layer 26. For example, if layer 26 includes SiGe, layer 38 also includes SiGe. However, in accordance with other embodiments of the present invention, layer 38 includes materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38
5 comprises silicon and is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar
10 manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a
15 substantial match in lattice constants is achieved. In this context the terms “substantially equal” and “substantially matched” mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a
20 grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that have a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host
25 crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of calcium strontium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Referring to FIGS. 2 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer 32, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of changing the lattice constant of layer 32 by varying the composition of layer 32. For example, if the grown crystal is SiGe and the accommodating buffer layer is monocrystalline $\text{Ca}_z\text{Sr}_{1-z}\text{TiO}_3$, substantial matching of crystal lattice constants of the two materials is achieved by varying a composition of a $\text{Si}_y\text{Ge}_{1-y}$ layer 32 from silicon to silicon-germanium. Crystalline layer 32 between the oxide and the grown monocrystalline material layer reduces strain in the grown monocrystalline material layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline material layer can thereby be achieved. Furthermore, layer 32 facilitates confinement of crystal defects at or near the interface of layers 32 and 36 and away from layer 26.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about five degrees off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkaline earth metals or combinations of alkaline earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface may exhibit an ordered 2x1 structure. If such an ordered 2x1 structure has not been achieved, the structure may be exposed to additional strontium until an ordered 2x1 structure is obtained. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkaline earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature, a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stoichiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered (100) monocrystal with the (100) crystalline orientation rotated by 45° with respect to the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the

subsequent growth of an epitaxial layer of a desired monocrystalline layer 32. For example, for the subsequent growth of a monocrystalline germanium layer, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-
5 2 monolayers of strontium-oxygen. Following the formation of this capping layer, silicon cap layer 31 may be formed using MBE growth techniques. Following the formation of the template (and, if desired, cap layer 31), layer 32 is formed by epitaxially growing, for example, a layer of germanium.

The structure illustrated in FIG. 2 can be formed by the process discussed above
10 with the addition of an additional monocrystalline layer 26 deposition step. Layer 26 is suitably formed overlying the template or cap layer using methods described above.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing monocrystalline layer 32 over the accommodating buffer layer, as described
15 above. The accommodating buffer layer, the amorphous oxide layer, and the cap layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer, the now
20 amorphous accommodating buffer layer, and a portion of cap layer 31 form a single amorphous layer 36. In accordance with one embodiment of the invention, layers 32 and 26 are then subsequently grown over layer 31. Alternatively, the anneal process may be carried out subsequent to growth of layer 32.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and
25 cap layer 31 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 5 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing, electron beam annealing, or "conventional" thermal annealing
30 processes (in the proper environment) may be used to form layer 36. When

conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 and/or 31 may be required to prevent degradation of the layer(s) during the anneal process.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline material layer comprising a germanium semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other monocrystalline material layers comprising other semiconductors, metals and other materials can be deposited overlying the monocrystalline graded layer.

Each of the variations of monocrystalline material layers, monocrystalline graded layers, and monocrystalline accommodating buffer layers preferably uses an appropriate template for initiating the growth of the monocrystalline layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of silicon to react with the zirconium as a precursor to depositing silicon germanium. Similarly, if the monocrystalline accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of silicon. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of silicon to react

with the capping material to form a template for the deposition of a monocrystalline material layer comprising graded monocrystalline materials such as SiGe and SiC.

FIGS. 5-7 schematically illustrate, in cross-section, the formation of another embodiment of a device structure in accordance with the invention. This embodiment includes a compliant layer that functions as a transition layer that uses clathrate or Zintl type bonding. More specifically, this embodiment utilizes an intermetallic template layer to reduce the surface energy of the interface between material layers thereby allowing for two dimensional layer by layer growth.

The structure illustrated in FIG. 5 includes a monocrystalline substrate 102, an amorphous interface layer 108 and an accommodating buffer layer 104. Amorphous intermediate layer 108 is grown on substrate 102 at the interface between substrate 102 and accommodating buffer layer 104 as previously described with reference to FIGS. 1 and 2. Amorphous interface layer 108 may comprise any of those materials previously described with reference to amorphous interface layer 28 in FIGS. 1 and 2 but preferably comprises a monocrystalline oxide material such as a monocrystalline layer of $\text{Ca}_z\text{Sr}_{1-z}\text{TiO}_3$ where z ranges from 0 to 1. Substrate 102 is preferably silicon but may also comprise any of those materials previously described with reference to substrate 22 in FIGS. 1-3.

A template layer 130 is deposited over accommodating buffer layer 104 as illustrated in FIG. 5 and preferably comprises a thin layer of Zintl type phase material composed of metals and metalloids having a great deal of ionic character. As in previously described embodiments, template layer 130 is deposited by way of MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to achieve a thickness of one monolayer. Template layer 130 functions as a "soft" layer with non-directional bonding but high crystallinity which absorbs stress build up between layers having lattice mismatch. Materials for template 130 may include, but are not limited to, materials containing Si, Ga, In, Sr, and Sb such as, for example, SrAl_2 , $(\text{MgCaYb})\text{Ga}_2$, $(\text{Ca,Sr,Eu,Yb})\text{In}_2$, BaGe_2As , and SrSn_2As_2 .

A monocrystalline graded material layer 126 is epitaxially grown over template layer 130 to achieve the final structure illustrated in FIG. 7. As a specific example, an

SrAl₂ layer may be used as template layer 130 and an appropriate monocrystalline material layer 126 such as a compound semiconductor material Si_yGe_{1-y}, where y ranges from 0 to 1, is grown over the SrAl₂. The Al-Ti (from the accommodating buffer layer of layer of Ca_zSr_{1-z}TiO₃ where z ranges from 0 to 1) bond is mostly metallic while the Al-Ge (from the Si_yGe_{1-y} layer) bond is weakly covalent. The Sr participates in two distinct types of bonding with part of its electric charge going to the oxygen atoms in the lower accommodating buffer layer 104 comprising Ca_zSr_{1-z}TiO₃ to participate in ionic bonding and the other part of its valence charge being donated to Al in a way that is typically carried out with Zintl phase materials. The amount of the charge transfer depends on the relative electronegativity of elements comprising the template layer 130 as well as on the interatomic distance. In this example, Al assumes an sp³ hybridization and can readily form bonds with monocrystalline material layer 126, which in this example, comprises semiconductor material Si_yGe_{1-y}.

The compliant substrate produced by use of the Zintl type template layer used in this embodiment can absorb a large strain without a significant energy cost. In the above example, the bond strength of the Al is adjusted by changing the volume of the SrAl₂ layer thereby making the device tunable for specific applications which include the monolithic integration of Si devices and the monolithic integration of high-k dielectric materials for CMOS technology.

FIG. 8 illustrates schematically, in cross section, a device structure 140 in accordance with a further embodiment of the invention. Device structure 140 includes a monocrystalline semiconductor substrate 142, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 142 includes two regions, 143 and 144. An electrical semiconductor component generally indicated by the dashed line 146 is formed, at least partially, in region 143. Electrical component 146 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated circuit such as a CMOS integrated circuit. For example, electrical semiconductor component 146 can be a CMOS integrated circuit configured to perform digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 143 can be formed by

conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 148 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 146.

Insulating material 148 and any other layers that may have been formed or
5 deposited during the processing of semiconductor component 146 in region 143 are removed from the surface of region 144 to provide a bare silicon surface in that region. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. A layer of strontium or strontium and oxygen is deposited onto the native oxide layer on the surface of region 144 and is
10 reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment of the invention a monocrystalline oxide layer is formed overlying the template layer by a process of molecular beam epitaxy. Reactants including calcium, strontium, titanium and oxygen are deposited onto the template layer to form the monocrystalline oxide layer. Initially during the deposition the partial
15 pressure of oxygen is kept near the minimum necessary to fully react with the calcium, strontium, and titanium to form the monocrystalline calcium strontium titanate layer. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the calcium strontium titanate reacts with silicon at the
20 surface of region 144 to form an amorphous layer of silicon oxide on the second region and at the interface between the silicon substrate and the monocrystalline oxide.

In accordance with an embodiment of the invention, the step of depositing the monocrystalline oxide layer is terminated by depositing a layer 150, which can be 1-10 monolayers of titanium, barium, strontium, barium and oxygen, titanium and oxygen, or
25 strontium and oxygen. A cap layer 152 of a monocrystalline semiconductor material is then deposited overlying the second template layer by a process of molecular beam epitaxy.

In accordance with one aspect of the present embodiment, after layer 152 formation, the monocrystalline titanate layer and the silicon oxide layer, which is
30 interposed between substrate 142 and the titanate layer, are exposed to an anneal

process such that the titanate and oxide layers form an amorphous oxide layer 154. A graded layer 156, comprising $\text{Si}_y\text{Ge}_{1-y}$ (where y ranges from 0 to 1) in accordance with one embodiment of the invention, is then epitaxially grown over layer 152, using the techniques described above in connection with layer 32 of FIG. 1. Alternatively, the above described anneal process can be performed before formation of template layer 152.

Next, a layer of monocrystalline material 158, such as Ge, is formed above graded layer 156. Layer 158 may be formed using any of the material and any of the techniques previously described herein in connection with layer 26.

In accordance with a further embodiment of the invention, a semiconductor component, generally indicated by a dashed line 160 is formed, at least partially, in compound semiconductor layer 158. Semiconductor component 160 can be formed by processing steps conventionally used in the fabrication of Ge devices. A metallic conductor schematically indicated by the line 162 can be formed to electrically couple device 146 and device 160, thus implementing an integrated device that includes at least one component formed in the silicon substrate and one device formed in the monocrystalline material layer. Although illustrative structure 140 has been described as a structure formed on a silicon substrate 142 and having a strontium or calcium strontium titanate layer and a germanium layer 158, similar devices can be fabricated using other monocrystalline substrates, oxide layers and other monocrystalline material layers as described elsewhere in this disclosure.

For example, FIG. 9 illustrates schematically, in cross section, a device structure 170 in accordance with a further embodiment of the invention. Device structure 170 includes a monocrystalline semiconductor substrate 172, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 172 includes two regions, 173 and 174. An electrical semiconductor component generally indicated by the dashed line 176 is formed, at least partially, in region 173. Electrical component 176 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated circuit such as a CMOS integrated circuit. For example, electrical semiconductor component 176 can be a CMOS integrated circuit configured to perform

digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 173 can be formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 178 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 176.

Insulating material 178 and any other layers that may have been formed or deposited during the processing of semiconductor component 176 in region 173 are removed from the surface of region 174 to provide a bare silicon surface in that region. A layer of strontium or strontium and oxygen is deposited onto the native oxide layer on the surface of region 174 and is reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment of the invention a monocrystalline oxide layer is formed overlying the template layer by a process of molecular beam epitaxy. Reactants including strontium, titanium and oxygen are deposited onto the template layer to form the monocrystalline oxide layer. Initially during the deposition the partial pressure of oxygen is kept near the minimum necessary to fully react with the strontium and titanium to form the monocrystalline strontium titanate layer. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the strontium titanate reacts with silicon at the surface of region 174 to form an amorphous layer of silicon oxide on the second region and at the interface between the silicon substrate and the monocrystalline oxide.

In accordance with an embodiment of the invention, the step of depositing the monocrystalline oxide layer is terminated by depositing a layer 180, which can be 1-10 monolayers of titanium, barium, strontium, barium and oxygen, titanium and oxygen, or strontium and oxygen. A cap layer 182 of a monocrystalline semiconductor material is then deposited overlying the second template layer by a process of molecular beam epitaxy.

In accordance with one aspect of the present embodiment, after layer 182 formation, the monocrystalline titanate layer and the silicon oxide layer, which is

interposed between substrate 172 and the titanate layer, are exposed to an anneal process such that the titanate and oxide layers form an amorphous oxide layer 184. A layer 186, comprising Ge in accordance with this embodiment of the invention, is then epitaxially grown over layer 182, using the techniques described above in connection with layer 32 of FIG. 1. Alternatively, the above described anneal process can be performed before formation of template layer 182.

Next, a layer of monocrystalline material 188, such as Ge, is formed above layer 186. Layer 188 may be formed using any of the material and any of the techniques previously described herein in connection with layer 26.

In accordance with a further embodiment of the invention, a semiconductor component, generally indicated by a dashed line 160 is formed, at least partially, in semiconductor layer 188. A metallic conductor schematically indicated by the line 162 can be formed to electrically couple device 176 and device 160, thus implementing an integrated device that includes at least one component formed in the silicon substrate and one device formed in the monocrystalline material layer.

Clearly, those embodiments specifically describing structures having two different Group IV semiconductor portions are meant to illustrate embodiments of the present invention and not limit the present invention. There are a multiplicity of other combinations and other embodiments of the present invention. For example, the present invention includes structures and methods for fabricating material layers which form semiconductor structures, devices and integrated circuits including other layers such as metal and non-metal layers. More specifically, the invention includes structures and methods for forming a compliant substrate which is used in the fabrication of semiconductor structures, devices and integrated circuits and the material layers suitable for fabricating those structures, devices, and integrated circuits.

In accordance with one embodiment of this invention, a monocrystalline semiconductor wafer can be used in forming monocrystalline material layers over the wafer. In this manner, the wafer is essentially a "handle" wafer used during the fabrication of semiconductor electrical components within a monocrystalline layer overlying the wafer. Therefore, electrical components can be formed within

semiconductor materials over a wafer of at least approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive “handle” wafer overcomes the fragile nature of some monocrystalline material wafers by placing them
5 over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within or using the monocrystalline material layer even though the substrate itself may include a different monocrystalline semiconductor material. Fabrication costs for some devices employing non-silicon
10 monocrystalline materials should decrease because larger substrates can be processed more economically and more readily compared to the relatively smaller and more fragile substrates (*e.g.*, conventional compound semiconductor wafers).

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various
15 modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. Benefits, other advantages, and solutions to problems have been described above with
20 regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms “comprises,” “comprising,” or any other variation thereof, are intended to cover a non-
25 exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

We Claim:

1. A semiconductor structure comprising:
 - a monocrystalline substrate;
 - 5 an accommodating buffer layer formed on the substrate;
 - a template formed on the monocrystalline accommodating buffer layer;and
 - a monocrystalline layer formed overlying the template, said
 - monocrystalline layer comprises a material selected from the group consisting of Si,
 - 10 SiC, Ge, and $\text{Si}_y\text{Ge}_{1-y}$, where y ranges from 0 to 1.
2. The semiconductor structure of claim 1, further comprising an amorphous layer interposed between the monocrystalline substrate and the accommodating buffer layer.
- 15 3. The semiconductor structure of claim 2, wherein the amorphous layer comprises silicon oxide.
4. The semiconductor structure of claim 2, wherein the amorphous layer is about 0.5 to about 5.0 nanometers thick.
- 20 5. The semiconductor structure of claim 1, wherein the accommodating buffer layer comprises an oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, and
- 25 perovskite oxides.
6. The semiconductor structure of claim 1, wherein the accommodating buffer layer comprises $\text{Ca}_z\text{Sr}_{1-z}\text{TiO}_3$, where z ranges from 0 to 1.

7. The semiconductor structure of claim 1, wherein the accommodating buffer layer is about 2 to about 100 nanometers thick.
8. The semiconductor structure of claim 1, wherein the accommodating buffer layer is about 5 nanometers thick.
9. The semiconductor structure of claim 1, wherein the monocrystalline graded layer is about 1 nanometer to about 100 microns thick.
10. The semiconductor structure of claim 9, wherein the monocrystalline graded layer is about 0.1 to about 5 microns thick.
11. The semiconductor structure of claim 1, further comprising a cap layer.
12. The semiconductor structure of claim 11, wherein the cap layer comprises monocrystalline silicon.
13. The semiconductor structure of claim 1, wherein the accommodating buffer layer includes an amorphous film.
14. The semiconductor structure of claim 1, wherein the accommodating buffer layer includes a monocrystalline film.
15. A microelectronic device formed using the semiconductor structure of claim 1.

16. A process for fabricating a semiconductor structure comprising the steps of:
providing a monocrystalline substrate;
epitaxially growing a monocrystalline accommodating buffer layer overlying the
monocrystalline semiconductor substrate;
- 5 forming an amorphous layer between the monocrystalline substrate and the
accommodating buffer layer; and
epitaxially growing a monocrystalline layer overlying the accommodating buffer
layer, wherein said monocrystalline layer comprises a material selected from the group
consisting of Si, SiC, Ge, and $\text{Si}_y\text{Ge}_{1-y}$, where y ranges from 0 to 1.
- 10
17. The process of claim 16, wherein the step of epitaxially growing a
monocrystalline accommodating buffer layer comprises epitaxially growing a
monocrystalline accommodating buffer layer comprising $\text{Ca}_z\text{Sr}_{1-z}\text{TiO}_3$, where z ranges
from 0 to 1.
- 15
18. The process of claim 16, further comprising a step of heating the
monocrystalline accommodating buffer layer and the amorphous layer to cause the
monocrystalline accommodating buffer layer to become amorphous.
- 20
19. The process of claim 18, wherein the step of heating includes rapid thermal
annealing.
20. The process of claim 19, further comprising the step of forming a first template
on the monocrystalline accommodating buffer layer.
- 25
21. The process of claim 20, further comprising forming a cap layer over the
template.
22. The process of claim 16, further comprising the step of forming a template
30 overlying the monocrystalline substrate.

23. The process of claim 16, further comprising epitaxially growing a monocrystalline material layer overlying the monocrystalline layer.
- 5 24. Forming a microelectronic device using the method of claim 16.

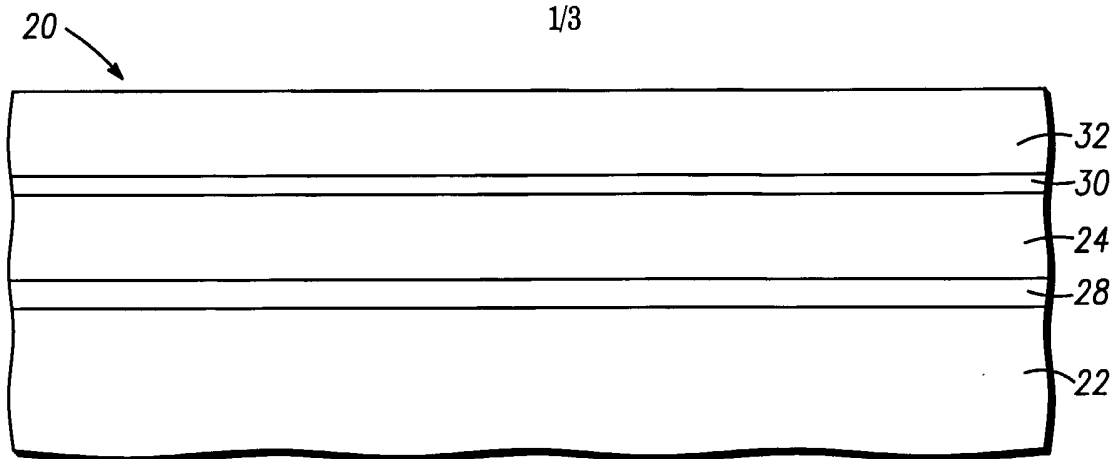


FIG. 1

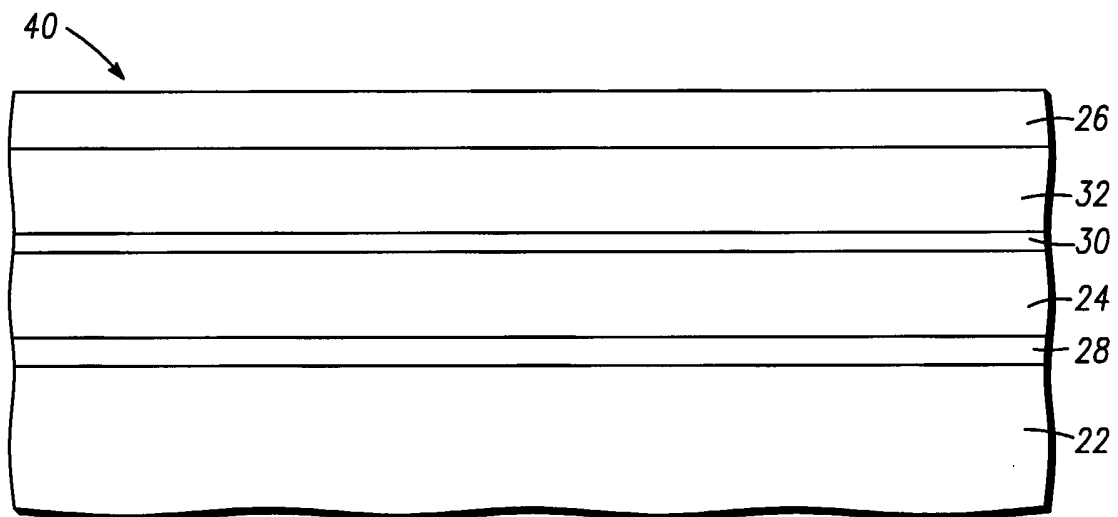


FIG. 2



FIG. 3

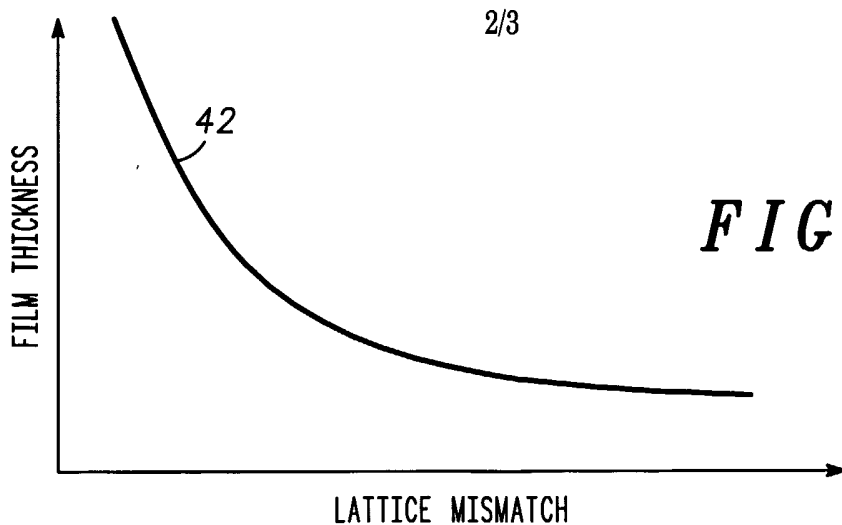


FIG. 4

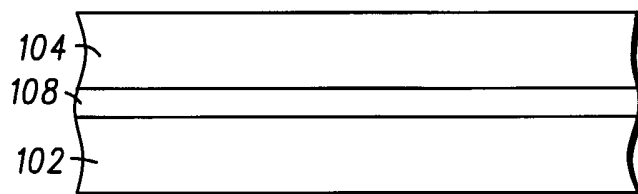


FIG. 5

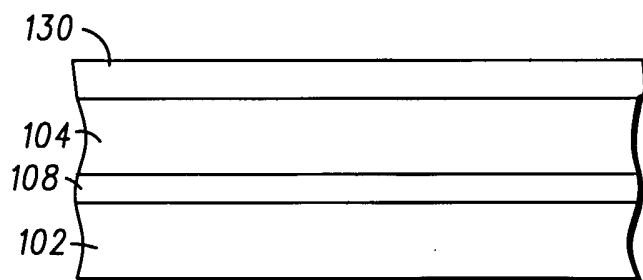


FIG. 6

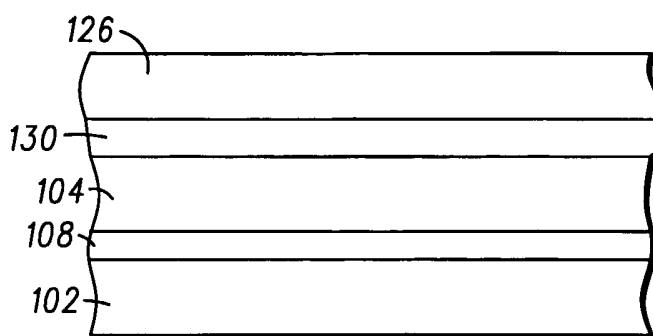


FIG. 7

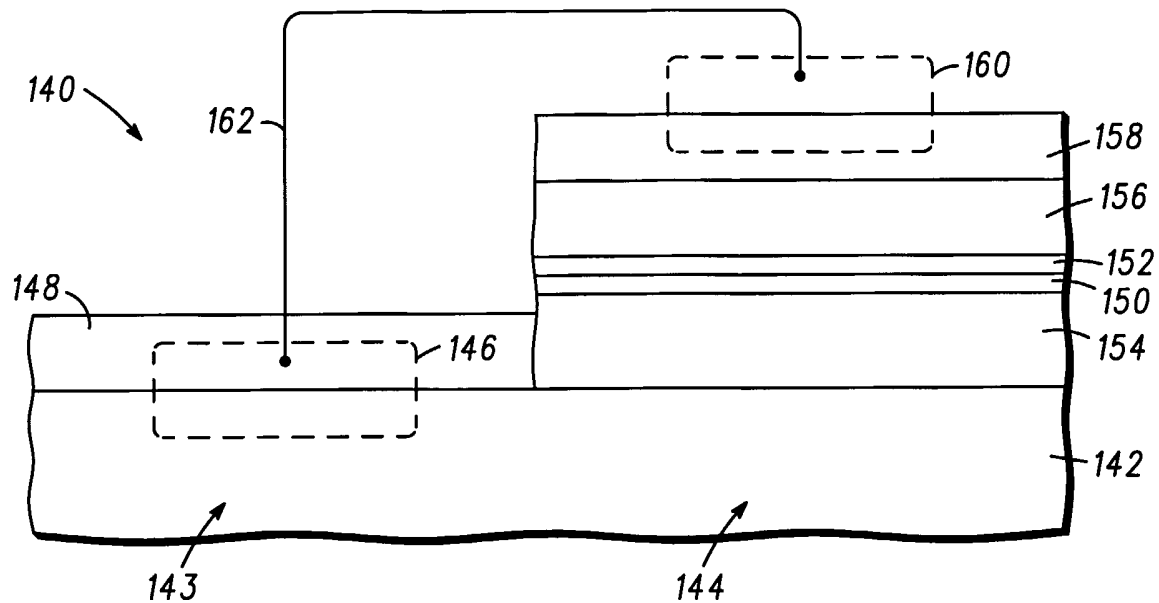


FIG. 8

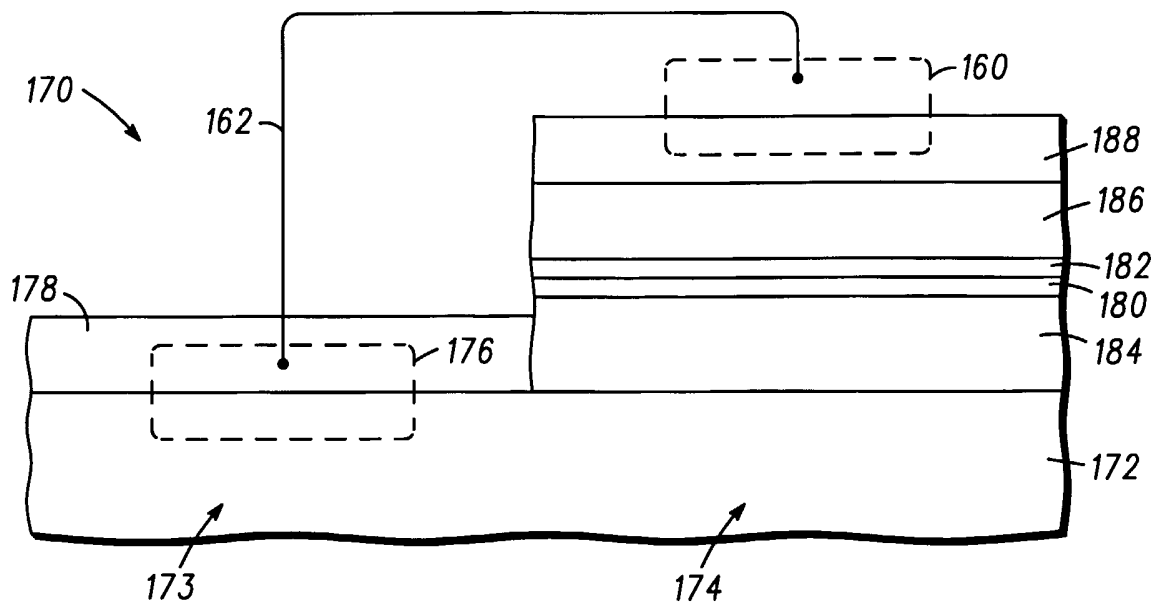


FIG. 9