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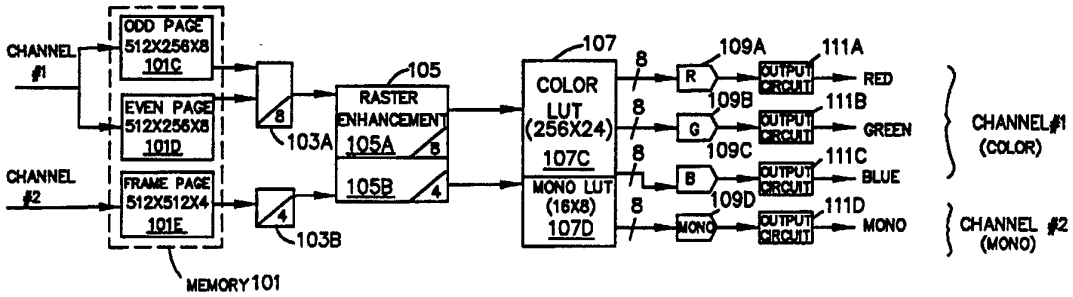

(57) Abstract

A reconfigurable video output architecture includes a memory for temporarily storing digital video data such that the memory is configurable between a single channel mode where the digital video data is a single video channel and a double channel mode where the digital video data includes first and second video channels. The architecture further includes a selector for selectively reading the memory and a look-up table for converting the digital video data into digital shade values. The look-up table is also configurable between a single channel mode and a double channel mode. A digital-to-analog converter is provided for converting the digital shade values into analog shade values, and an output circuit outputs at least one analog video signal.

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RECONFIGURABLE VIDEO OUTPUT ARCHITECTURE WITH RASTER ENHANCEMENT

BACKGROUND OF THE INVENTION

This invention relates to video output architectures. Particularly, the invention relates to a video output architecture which is configurable between single and multiple channel modes.

A video output architecture inputs digital data from a source and outputs one or more color or monochromatic ("mono") video signals. For example, one video output architecture might be designed to input digital data from one source and output a single color video signal consisting of red, blue, and green signals. On the other hand, another video output architecture might be designed to input digital data from another source and output this data as two separate mono video signals. Such output architectures are typically embodied in the form of a "video card" which plugs into a slot in a video control box. Thus, if it is desired to output to different numbers or types of displays, one video card must be exchanged with another appropriate to that application.

These known architectures have the disadvantage that it is necessary to design and maintain on hand different video cards for a number of various applications. This is particularly cumbersome when a number of systems are in operation at the same time, making it necessary to maintain a "library" of video cards to ensure that the proper card is available when necessary. Of course, whenever a new application is desired, it is necessary to incur the cost and inconvenience of designing and building a new card.

SUMMARY OF THE INVENTION

The invention overcomes the above-described disadvantages of the prior art by providing a reconfigurable video output architecture which can be configured to operate in single or multiple channel modes and output to various numbers of displays. Specifically, according to one embodiment, the invention comprises input means for inputting digital video data, the input means having a single channel mode for inputting a single channel of digital video data and at least one multiple mode for inputting multiple channels of digital video data; a look-up table for converting the digital video data into shade values, the look-up table being configurable to convert the single

channel of digital video data into shade values when the input means is in the single mode and to convert the multiple channels of digital video data into shade values when the input means is in the multiple mode; digital-to-analog conversion means for converting the shade values into analog signals; and output means for outputting at least one analog video signal.

In some aspects, the reconfigurable video output includes a raster enhancement device configurable between a single channel mode and a multiple channel mode.

In some aspects, the shade values are color values when the input means is in the single channel mode and the shade values are achromatic values when the input means is in the multiple channel mode.

In some aspects, when the input means is in the multiple channel mode the input means inputs two channels of digital video data and the output means outputs at least two analog mono video signals. In certain embodiments, when the input means is in the multiple channel mode the look-up table is partitioned into two sections each loaded with achromatic values.

In some aspects, when the input means is in the multiple channel mode the input means inputs two channels of digital video data and the output means outputs at least one analog mono video signal and at least one analog color video signal. In certain embodiments, when the input means is in the multiple channel mode the look-up table is partitioned into two sections, one of the sections being loaded with achromatic values and the other the section being loaded with color values.

In some aspects, when the input means is in the multiple channel mode the input means inputs three channels of digital video data and the output means outputs at least three analog mono video signals. In certain embodiments, when the input means is in the multiple channel mode the look-up table is partitioned into three sections each loaded with achromatic values.

In some aspects, the input means comprises a memory for temporarily storing the digital video data and a selector for selectively scanning the digital video data stored in the memory. In certain embodiments, the memory comprises at least two sub-memories, and wherein the digital video data is stored in one of the sub-memories while the selector scans digital video data stored in another of the sub-memories. In certain embodiments, when the input means is in the single channel mode, even pages of the

digital video data are stored in a first sub-memory and odd pages of the digital video data are stored in a second sub-memory; and wherein when the input means is in the multiple channel mode all pages of a first channel of digital video data are stored in the first sub-memory and all pages of a second channel of digital video data are stored in the second sub-memory.

In some aspects, when the input means is in the single channel mode digital video data corresponding to a single video signal and digital overlay data are stored in the memory; and wherein the selector substitutes the overlay data for portions of the single video signal. In certain embodiments, the digital overlay data has a predetermined width and height, and wherein the selector increases at least one of the width and height of the digital overlay data when substituting for portions of the single video signal.

In other embodiments, the reconfigurable video output architecture comprises a memory for temporarily storing digital video data, the memory being configurable between a single channel mode. The digital video data comprises a single video channel and a double channel mode wherein the digital video data comprises a first and a second video channel. A selector is included for selectively reading the memory and a look-up table is provided for converting the digital video data into digital shade values, the look-up table being configurable between a single channel mode and a double channel mode. Digital-to-analog conversion means converts the digital shade values into analog shade values; and output means for outputting at least one analog video signal.

In some aspects, the memory and the look-up table are further configurable to a triple channel mode.

In some aspects, when the memory and the look-up table are in the double channel mode the look-up table is partitioned into at least two sections, and the output means outputs at least two analog video signals. In certain embodiments, a first one of the sections contains color shade values and a second one of the sections contains mono shade values, and wherein the output means outputs a color video signal and a mono video signal.

In some aspects, when the memory and the look-up table are in the triple channel mode the look-up table is partitioned into at least three sections, and the output means outputs at least three analog video signals. In certain embodiments, the sections contain

mono shade values, and wherein the output means outputs at least three mono video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a is a block diagram illustrating the reconfigurable video output architecture of the invention according to one embodiment;

Fig. 1b is a timing diagram according to the embodiment of Fig. 1a.

Fig. 2a is a flow chart illustrating a write/scan function of the invention;

Fig. 2b is a flow chart illustrating a double draw function of the invention;

Fig. 3a is a schematic diagram of a first embodiment of the invention configured in the single channel mode;

Fig. 3b is a schematic diagram of the embodiment of Fig. 3a configured in the double channel mode;

Fig. 4a is a schematic diagram of a second embodiment of the invention configured in the single channel mode;

Fig. 4b is a schematic diagram of the embodiment of Fig. 4a configured in the double channel mode; and

Fig. 4c is a schematic diagram of the embodiment of Fig. 4a configured in the triple channel mode.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the invention will now be described in detail with reference to the accompanying figures.

Fig. 1 is a block diagram of one embodiment of the reconfigurable video output architecture of the invention. In this embodiment, digital video data are stored or generated by two data sources 3A, 3B. These two data sources may each output a different video channel or, in the alternative, one may supply a single video channel and the other may output overlay data such as characters to be superimposed on the video image. The reconfigurable video output architecture can be configured to output single or multiple video channels.

The video output architecture 1 includes a memory 5 comprising ping memory 5A and pong memory 5B, both of which accept data from both sources 3A, 3B. The

video data read into ping memory 5A and pong memory 5B are scanned by a memory select 7 in accordance with the output of a master timer 9. The separate ping and pong memories 5A, 5B are provided so that one memory can be scanned while the other is being updated. For example, while the data in ping memory 5A is being scanned by memory select 7, pong memory 5B is being updated. In the case where one of the data sources 3A, 3B is a video channel and the other contain verlay data, data from both data sources is read into the pong memory during the updating procedure. If, on the other hand, each of the data sources represents a separate channel, data from only one of the sources are read into the pong memory at a time. Then, during the vertical blanking period, the memory select 7 is switched to the pong memory under control of master timer 9 and the pong memory is scanned while the ping memory is updated.

The output of memory select 7 is applied to a raster enhancement device 11 which functions to improve the appearance of characters overlaid on a video image. The operation of raster enhancement device 11 will be described in more detail below. The raster enhanced data is applied to a look-up table (LUT) 13 which has been pre-loaded with shade values. The shade values may be red, green, and blue color values if a conventional RGB video signal is to be output, achromatic values if one or more mono signals are to be output, or any combination thereof.

Once the LUT 13 has "decoded" the digital data into digital shade values, the shade values are converted into analog values by D/A converter 15. The analog signals are then applied to an output circuit 17, which performs the necessary amplification and buffering functions to output one or more color or mono video signals. Any synchronization signals which are necessary for a desired video format are brought over from the master timer and inserted by the output circuit 17.

As illustrated in Fig. 1b, memory select 7 generates a ping/pong select signal which allows one of the memories to be scanned while the other is being updated. Both the ping and pong memories are divided into even and odd pages for storing even and odd fields of data, respectively. Thus, memory select 7 also generates an even/odd select signal which alternates between the even and odd fields during each memory scan sequence. As shown in Fig. 1b, the period between vertical blanking signals is typically 50 ms. Each memory scan sequence is commenced at a 50 ms boundary, and must be completed before the next boundary in reached.

Referring to Fig. 2a, the flow chart illustrating a write/scan function, in state ST1 the system waits until a 50 ms boundary is reached, and then initializes a variable "field" to zero (ST2). Next, it is determined whether the ping/pong select signal is high or low, i.e., whether the ping or the pong memory will be scanned during this sequence (ST3). If the ping memory is to be scanned, the master timer is given access to the ping memory (ST4) and new data is written into the pong memory (ST5). If, on the other hand, the pong memory is selected, the master timer is given access to the pong memory (ST6), and new data is written into the ping memory (ST7).

Next, variables X and Y are initialized to zero (ST8). These variables correspond to the coordinates of a given pixel within the image, which in this embodiment comprises a grid of 512 x 256 pixels. In ST9, it is determined whether the variable FIELD is even or odd. Because this variable was initialized to zero, the sequence proceeds to the even branch first. At ST10, the master timer scans address (X,2Y), and then X is incremented by 1 in ST11. This loop continues until X reaches 512 in ST12, at which time Y is incremented by 2 (ST13) and X is re-initialized to zero (ST14). This loop then continues until Y reaches 512 (ST15), at which time the field variable is incremented by one (ST16) and the procedure returns to ST8. The procedure will then proceed as explained above except that the odd field addresses (X, 2Y + 1) will be scanned (ST18). The procedure is repeated until field reaches 3 (ST17). When the third field has been scanned, the procedure ends and waits for the next 50 ms boundary to occur (ST19).

Where the data stored in the ping or pong memory includes overlay data, such data may have an undesirable appearance when superimposed on the video signal if it is only one pixel wide. To prevent this, memory select 7 executes a "double draw" function as data is scanned from the ping or pong memory. The double draw function expands the overlay data both horizontally and vertically by one pixel during the read-out process, thus improving its appearance. Particularly, referring to Fig. 2b, the flow chart for a double draw function, in step ST20 it is first determined whether a given data point d(x,y) being scanned is an overlay. If it is, this data point is output (ST21) and the procedure ends. If it is not, data point d(x-1,y) is examined to determine if it contains overlay data (ST22). If it does, the overlay data at that point is output and substituted for d(x,y) (ST23). If d(x-1,y) does not contain overlay data, point d(x,y-1) is examined

(ST24) and the data therein is substituted for d(x,y) if it contains an overlay data (ST25). If it does not, point d(x-1,y-1) is examined, and if this point contains overlay data that value is output and substituted for d(x,y) (ST27). If d(x-1,y-1) does not contain overlay data, the data at point d(x,y) is output (ST28) and the procedure moves on to the next point (ST29). The result of this procedure is that if any of the points in a 2x2 square defined by d(x-1,y-1) in the upper left corner and d(x,y) in the lower right corner contain overlay data, that data is substituted for d(x,y), and hence the overlay data is increased by one pixel in both the horizontal and vertical directions.

As mentioned above, the video output architecture 1 of Fig. 1 can be reconfigured to accept data from one or more sources and to drive one or more color or mono video displays. Fig. 3a is a block diagram illustrating a first embodiment of the invention configured in the single channel mode. Fig. 3b is a block diagram of the same embodiment configured in the double channel mode. This embodiment will be discussed in detail below.

In Fig. 3a a single video channel is written into a memory 31 having a capacity of 512 x 512 x 8. The memory 31 corresponds to either the ping or pong memory 5A, 5B of Fig. 1, but the use of the dual memories and the scanning therefrom described in detail above will be omitted from this description for the sake of simplicity. Memory 31 is divided internally into an odd page 31A and an even page 31B, each of which is 512 x 256 x 8. The odd numbered scan lines of the video input are written to the odd page 31A while the even lines are written to the even page 31B.

Data is read out of either the odd page 31A or the even page 31B of memory 31 by data selector 33 via one of two 8-bit data buses. Selector 33 is switched between the even and odd pages under control of a select signal on line 35, which is generated by an external controller (not shown).

The output of selector 33 is applied to a raster enhancement circuit 37, which comprises a DQ flip-flop 39, a selector 41 controlled by a select signal applied on line 40, and a second DQ flip-flop 43.

The output of raster enhancement circuit 37 is applied to a 256 x 24 look-up table (LUT) 45 which has been pre-loaded with red, green and blue (RGB) color data. The LUT 45 outputs digital RGB values corresponding to the 8-bit data output by the raster enhancement device 37. These digital RGB values are applied to three separate

digital to analog (D/A) converters 47A, 47B, and 47C, which convert the values to analog RGB signals. The analog RGB signals are then amplified by three very high slew rate and high bandwidth amplifiers 49A, 49B, and 49C. Sync input lines 51, 53 are connected to the outputs of amplifiers 49B and 49C, respectively, to insert the necessary composite sync signals. In the single channel mode illustrated in Fig. 3a, the sync insert on line 51 is off, while the sync insert on line 53, which is applied to the green channel, is turned on. The outputs of amplifiers 49A, 49B, and 49C are applied to high slew rate and high bandwidth output current buffers 55A, 55B, 55C, the outputs of which are used to drive a conventional RGB primary display and a repeater (duplicate) display.

Fig. 3b illustrates the embodiment of Fig. 3a configured in the double channel mode. Here, two separate channels are input to memory 31, which is internally divided into two 512 x 512 x 4 sub-memories 31C, 31D. The data are then read from these memories and applied to two identical parallel mono channels. These mono channels are produced by reconfiguring the components discussed above in the single channel mode to operate on two separate mono signals instead of a single color signal.

Particularly, data selector 33 has been partitioned into two data selectors 33A, 33B which select from one of two 4-bit inputs depending upon selection signals applied on lines 35A, 35B. Raster enhancement circuit 37 has also been partitioned into two circuits 37A, 37B, each of which comprises a 4-bit DQ flip-flop 39A, 39B, a 4-bit selector 41A, 41B, and another 4-bit DQ flip-flop 43A, 43B. The LUT 45 has been partitioned into a 256 x 8 section 45A which is not used, a 16 x 8 section 45B which has been pre-loaded with monochromatic shade values, and a second 16 x 8 section 45C loaded with monochromatic shade values. The outputs of sections 45B and 45C of the LUT are applied to D/A converters 47B, 47C, amplifiers 49B, 49C, and buffers 55B, 55C in the manner described above. A sync signal is inserted in each channel over lines 51 and 53, and the buffers 55B, 55C output two distinct mono channels and two repeater channels. D/A converter 47A, amplifier 49A, and buffer 55A are not used in this configuration.

Figs. 4a, 4b, and 4c illustrate a second embodiment of the invention, which is configurable between single, double, and triple channel modes. In Fig. 4a, the embodiment is shown configured in the single channel mode. In this configuration, data from a single video channel are input to odd page 101a and even page 101b of memory

101. The odd page and even page memories are each 512 x 256 x 12. A data selector device 103 then reads data from one of the odd page and even page memories via one of two 12-bit data buses and applies the selected data to the input of a raster enhancement circuit 105. The operation of the raster enhancement circuit is analogous to that described with reference to Figs. 3a, 3b and will not be repeated here. The output of raster enhancement circuit 105 is applied to a LUT 107, which has been partitioned into a color LUT 107A (4K x 24) and a mono LUT 107B (4K x 8). Color LUT 107A generates digital color values which are applied via 8-bit data buses to the inputs of D/A converters 109A, 109B, and 109C, respectively. The D/A converters convert the digital color values into analog signals, which are then applied to output circuits 111A, 111B, and 111C. At the same time, mono LUT 107B outputs mono data values via an 8-bit data bus to D/A converter 109D, which outputs an analog mono signal to output device 111D. Output devices 111A-D include amplifier and buffer output circuits such as those described with reference to Figs. 3a and 3b, and insert any necessary sync signals as described above. The outputs of output devices 111A, 111B, and 111C comprise the red, blue, and green components of a conventional RGB color video signal. The output of 111D, on the other hand, corresponds to a mono version of the same picture.

Fig. 4b illustrates the embodiment of Fig. 4a configured in the double channel mode. Here, memory 101 is partitioned into three sections, an odd page 101C, an even page 101D, and a frame page 101E. A first video channel is applied to the odd and even pages, and a second video channel is applied to the frame page. The data stored in pages 101C, 101D, and 101E are selected by data selector 103 (partitioned into selectors 103A, 103B) and applied to raster enhancement device 105, which has been partitioned into an 8-bit section 105A and a 4-bit section 105B. The output of raster enhancement circuit 105 is applied to color LUT 107 which is partitioned into a color LUT 107C (256 x 24) and a mono LUT 107D (16 x 8). The outputs of the LUT 107 are then applied to D/A converters 109A-109D and output circuits 111A-111D in the manner described above. However, in the configuration of Fig. 4b, the mono output from output circuit 111D corresponds to a different video channel than the composite color video signal output from output circuits 111A-111C.

Fig. 4c illustrates the embodiment of Figs. 4a and 4b configured in the triple channel mode. In this embodiment, memory 101 has been partitioned into three frame

pages 101F-101H. The frame pages are read by data selector 103 (partitioned into three 4-bit selectors 103C, 103D, 103E) via three 4-bit data buses, and the outputs thereof are applied to raster enhancement device 105, which has been partitioned into three 4-bit sections 105C, 105D, and 105E. The outputs of raster enhancement device 105 are applied to LUT 107, which has been partitioned into four 16 x 8 mono LUT 107E, 107F, 107G, and 107H. The outputs of these four mono LUTs are then applied to the D/A converters 109A-109D and output circuits 111A-111D as four separate channels, resulting in four separate mono outputs. The mono outputs from output devices 111C and 111D are duplicates, so the output actually corresponds to the three separate channels originally applied to the memory 101.

This invention has been described herein in considerable detail in order to comply with the Patent Statutes and to provide those skilled in the art with the information needed to apply the novel principles and to construct and use such specialized components as are required. However, it is to be understood that the invention can be carried out by specifically different equipment and devices, and that various modifications, both as to the equipment details and operating procedures, can be accomplished without departing from the scope of the invention itself.

What is claimed is:

CLAIMS

The embodiments of the invention in which an exclusive property or right is claimed are defined as follows:

1. A reconfigurable video output architecture, comprising:

input means for inputting digital video data, said input means having a single channel mode for inputting a single channel of digital video data and at least one multiple mode for inputting multiple channels of digital video data;

a look-up table for converting said digital video data into shade values, said look-up table being configurable to convert the single channel of digital video data into shade values when said input means is in the single mode and to convert said multiple channels of digital video data into shade values when said input means is in the multiple mode;

digital-to-analog conversion means for converting said shade values into analog signals; and

output means for outputting at least one analog video signal.

2. A reconfigurable video output architecture as claimed in claim 1, further comprising a raster enhancement device configurable between a single channel mode and a multiple channel mode.

3. A reconfigurable video output architecture as claimed in claim 1, wherein said shade values are color values when said input means is in the single channel mode and said shade values are achromatic values when said input means is in said multiple channel mode.

4. A reconfigurable video output architecture as claimed in claim 1, wherein when said input means is in said multiple channel mode said input means inputs two channels of digital video data and said output means outputs at least two analog mono video signals.

5. A reconfigurable video output architecture as claimed in claim 4, wherein when said input means is in said multiple channel mode said look-up table is partitioned into two sections each loaded with achromatic values.

6. A reconfigurable video output architecture as claimed in claim 1, wherein when said input means is in said multiple channel mode said input means inputs two channels of digital video data and said output means outputs at least one analog mono video signal and at least one analog color video signal.

7. A reconfigurable video output architecture as claimed in claim 6, wherein when said input means is in said multiple channel mode said look-up table is partitioned into two sections, one of said sections being loaded with achromatic values and the other said section being loaded with color values.

8. A reconfigurable video output architecture as claimed in claim 1, wherein when said input means is in said multiple channel mode said input means inputs three channels of digital video data and said output means outputs at least three analog mono video signals.

9. A reconfigurable video output architecture as claimed in claim 8, wherein when said input means is in said multiple channel mode said look-up table is partitioned into three sections each loaded with achromatic values.

10. A reconfigurable video output architecture as claimed in claim 1, wherein said input means comprises:

a memory for temporarily storing the digital video data; and

a selector for selectively scanning the digital video data stored in the memory.

11. A reconfigurable video output architecture as claimed in claim 10, wherein said memory comprises at least two sub-memories, and wherein the digital video data is

stored in one of said sub-memories while said selector scans digital video data stored in another of said sub-memories.

12. A reconfigurable video output architecture as claimed in claim 11, wherein when said input means is in the single channel mode even pages of the digital video data are stored in a first sub-memory and odd pages of the digital video data are stored in a second sub-memory, and wherein when said input means is in the multiple channel mode all pages of a first channel of digital video data are stored in said first sub-memory and all pages of a second channel of digital video data are stored in said second sub-memory.

13. A reconfigurable video output architecture as claimed in claim 10, wherein when said input means is in said single channel mode digital video data corresponding to a single video signal and digital overlay data are stored in said memory, and wherein said selector substitutes said overlay data for portions of said single video signal.

14. A reconfigurable video output architecture as claimed in claim 13, wherein said digital overlay data has a predetermined width and height, and wherein said selector increases at least one of said width and height of the digital overlay data when substituting for portions of said single video signal.

15. A reconfigurable video output architecture, comprising:

a memory for temporarily storing digital video data, said memory being configurable between a single channel mode wherein the digital video data comprises a single video channel and a double channel mode wherein the digital video data comprises a first and a second video channel;

a selector for selectively reading said memory;

a look-up table for converting the digital video data into digital shade values, said look-up table being configurable between a single channel mode and a double channel mode;

digital-to-analog conversion means for converting said digital shade values into analog shade values; and

output means for outputting at least one analog video signal.

16. A reconfigurable video output architecture as claimed in claim 15, wherein said memory and said look-up table are further configurable to a triple channel mode.

17. A reconfigurable video output architecture as claimed in claim 15, wherein when said memory and said look-up table are in the double channel mode said look-up table is partitioned into at least two sections, and said output means outputs at least two analog video signals.

18. A reconfigurable video output architecture as claimed in claim 17, wherein a first one of said sections contains color shade values and a second one of said sections contains mono shade values, and wherein said output means outputs a color video signal and a mono video signal.

19. A reconfigurable video output architecture as claimed in claim 16, wherein when said memory and said look-up table are in the triple channel mode said look-up table is partitioned into at least three sections, and said output means outputs at least three analog video signals.

20. A reconfigurable video output architecture as claimed in claim 19, wherein said sections contain mono shade values, and wherein said output means outputs at least three mono video signals.

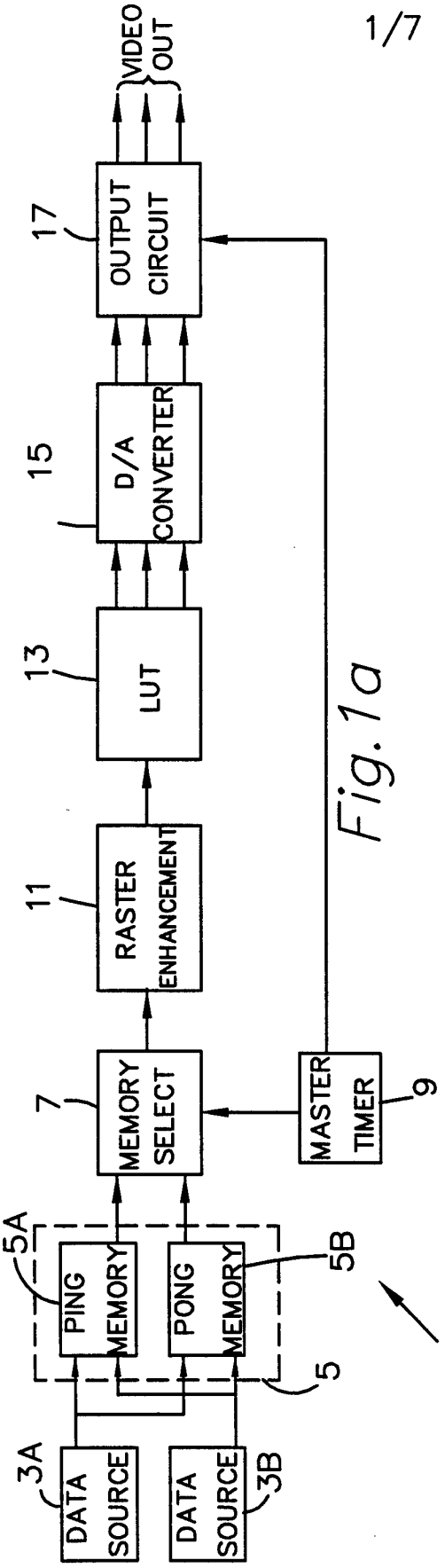
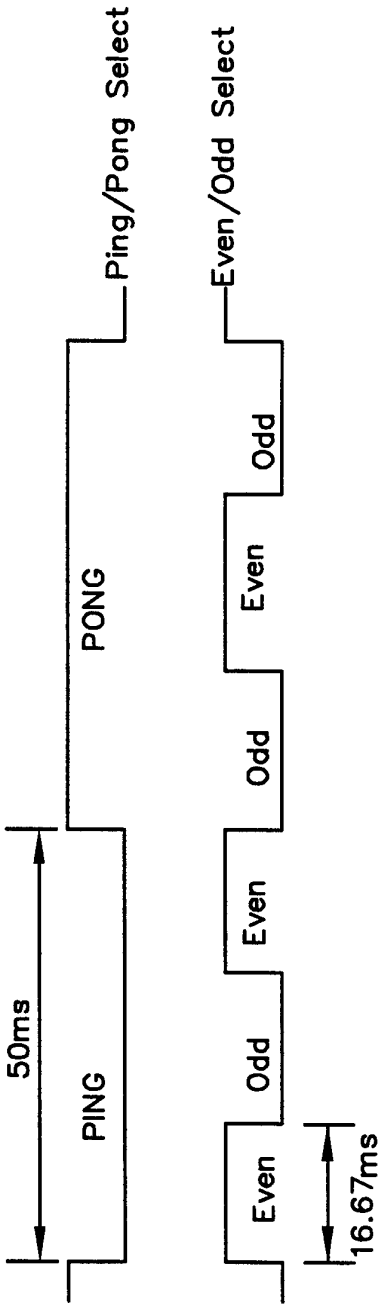

VIDEO OUT
17
OUTPUT CIRCUIT
15
D/A CONVERTER
13
LUT
11
RASTER ENHANCEMENT
7
MEMORY SELECT
MASTER TIMER
9
5A
PING MEMORY
PONG MEMORY
5B
5
1
3A
DATA SOURCE
DATA SOURCE
3B

Fig. 1a


Ping/Pong Select
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Even
Odd
Even
Odd
Even
16.67ms

Fig. 1b

Fig.2A

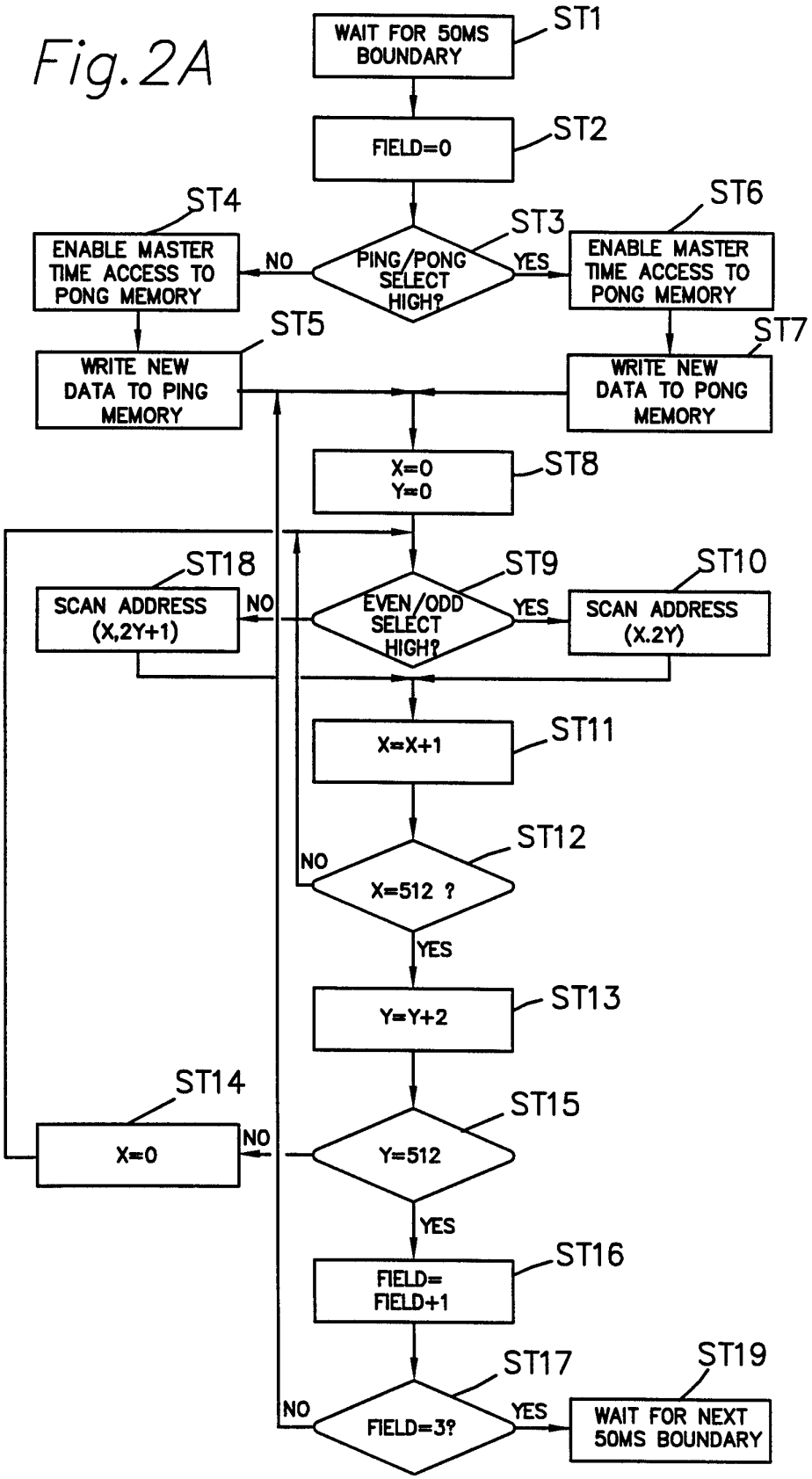
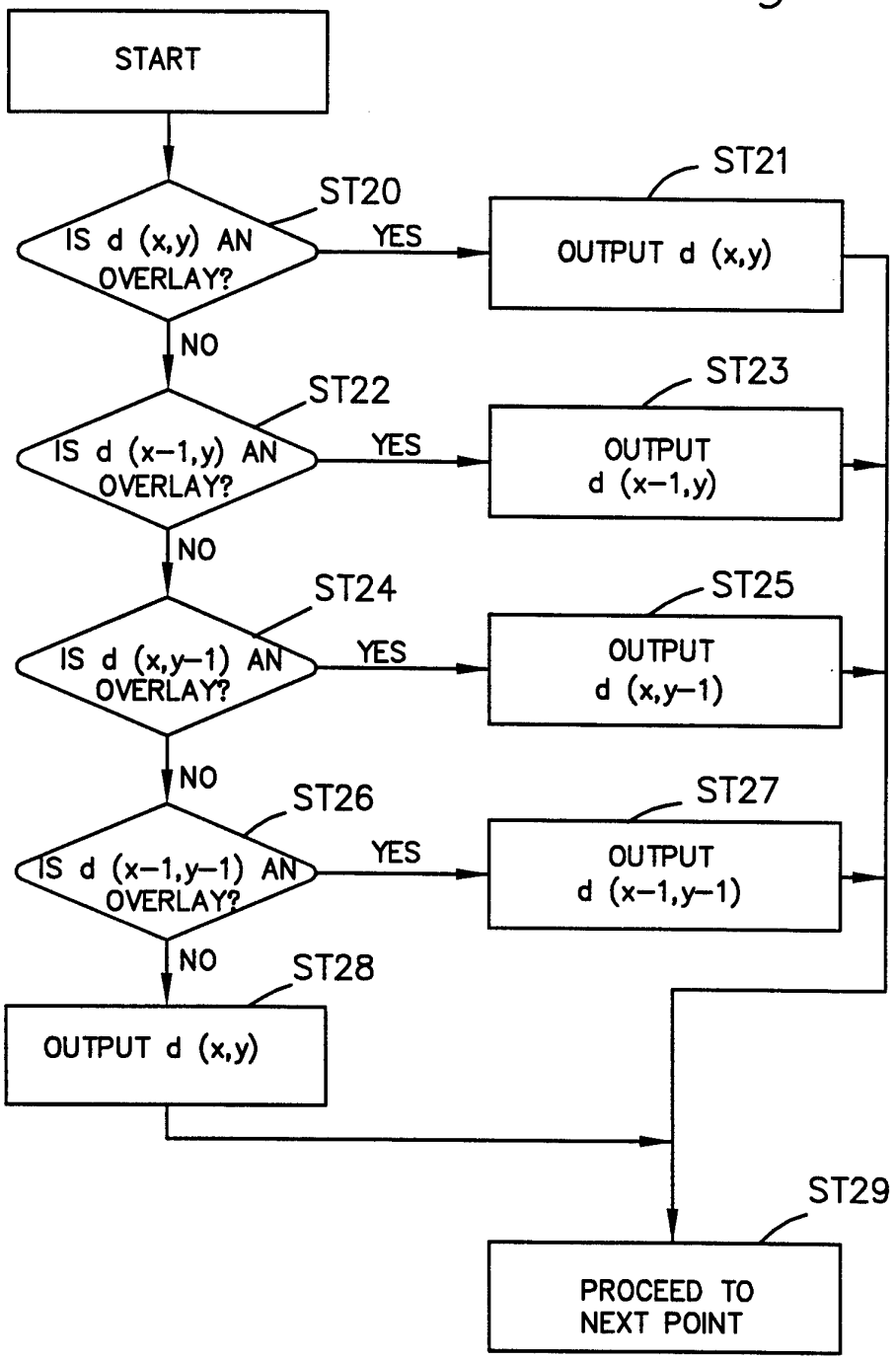

WAIT FOR 50MS BOUNDARY
ST1
FIELD=0
ST2
ST3
PING/PONG SELECT HIGH?
NO
YES
ST4
ENABLE MASTER TIME ACCESS TO PONG MEMORY
ST5
WRITE NEW DATA TO PING MEMORY
ST6
ENABLE MASTER TIME ACCESS TO PONG MEMORY
ST7
WRITE NEW DATA TO PONG MEMORY
X=0
Y=0
ST8
ST9
EVEN/ODD SELECT HIGH?
NO
YES
ST10
SCAN ADDRESS (X.2Y)
ST18
SCAN ADDRESS (X,2Y+1)
X=X+1
ST11
ST12
X=512 ?
NO
YES
Y=Y+2
ST13
ST14
X=0
NO
ST15
Y=512
YES
FIELD= FIELD+1
ST16
ST17
FIELD=3?
NO
YES
ST19
WAIT FOR NEXT 50MS BOUNDARY

Fig. 2B


START
ST20
IS d (x,y) AN OVERLAY?
YES
ST21
OUTPUT d (x,y)
NO
ST22
IS d (x−1,y) AN OVERLAY?
YES
ST23
OUTPUT d (x−1,y)
NO
ST24
IS d (x,y−1) AN OVERLAY?
YES
ST25
OUTPUT d (x,y−1)
NO
ST26
IS d (x−1,y−1) AN OVERLAY?
YES
ST27
OUTPUT d (x−1,y−1)
NO
ST28
OUTPUT d (x,y)
ST29
PROCEED TO NEXT POINT

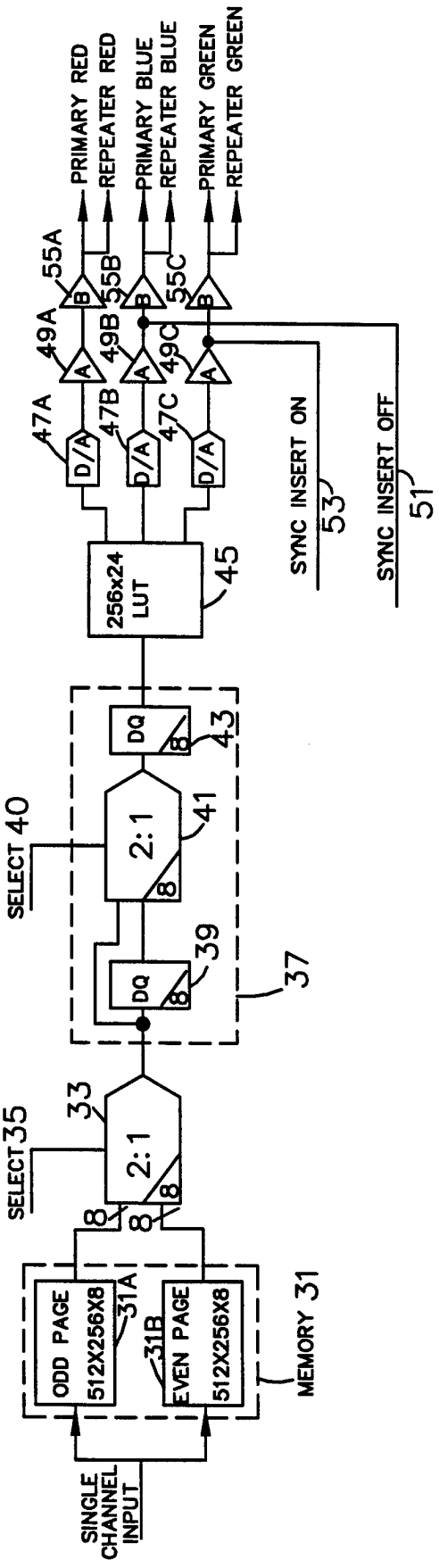

SINGLE CHANNEL INPUT
ODD PAGE 512X256X8
31A
EVEN PAGE 512X256X8
31B
MEMORY 31
8
8
SELECT 35
2:1
33
8
8
37
DQ
39
SELECT 40
2:1
41
8
DQ
43
8
256x24 LUT
45
D/A
47A
47B
47C
A
49A
49B
49C
B
55A
55B
55C
PRIMARY RED
REPEATER RED
PRIMARY BLUE
REPEATER BLUE
PRIMARY GREEN
REPEATER GREEN
SYNC INSERT ON
53
SYNC INSERT OFF
51

Fig. 3a

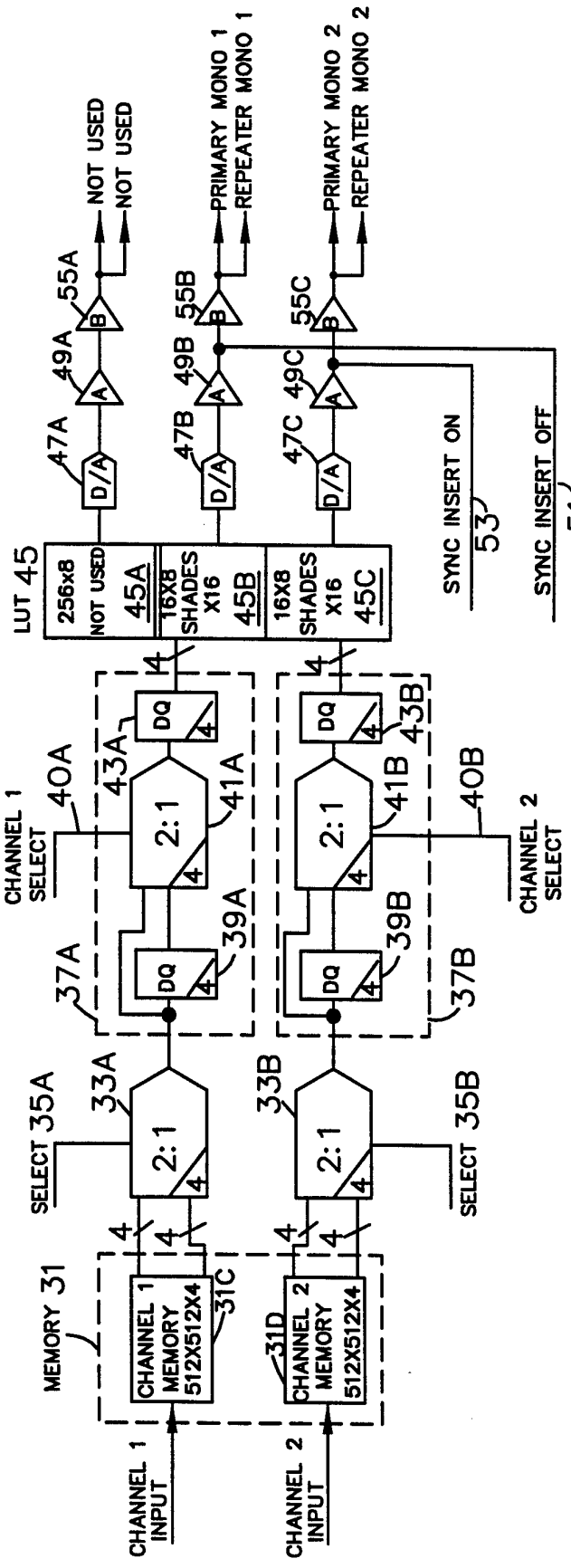

MEMORY 31
CHANNEL 1 MEMORY 512X512X4
31C
CHANNEL 2 MEMORY 512X512X4
31D
CHANNEL 1 INPUT
CHANNEL 2 INPUT
33A
33B
2:1
SELECT 35A
SELECT 35B
37A
37B
39A
39B
DQ
40A
40B
CHANNEL 1 SELECT
CHANNEL 2 SELECT
41A
41B
43A
43B
LUT 45
256x8 NOT USED 45A
16X8 SHADES X16 45B
16X8 SHADES X16 45C
47A
47B
47C
D/A
49A
49B
49C
A
B
55A
55B
55C
NOT USED
NOT USED
PRIMARY MONO 1
REPEATER MONO 1
PRIMARY MONO 2
REPEATER MONO 2
SYNC INSERT ON 53
SYNC INSERT OFF 51

Fig. 3b

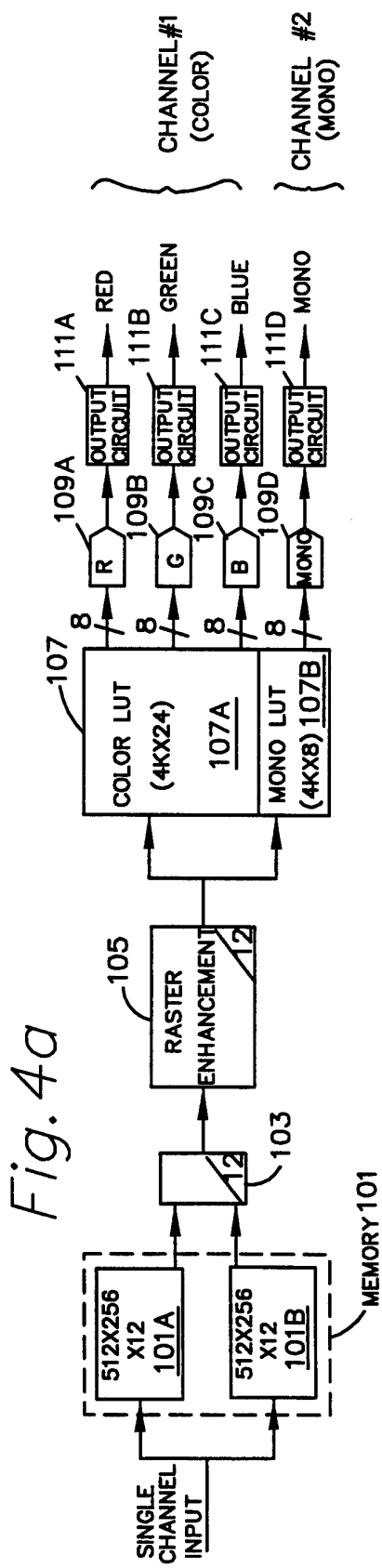

SINGLE CHANNEL INPUT
MEMORY 101
512X256 X12 101A
512X256 X12 101B
103
12
RASTER ENHANCEMENT 12
105
COLOR LUT (4KX24) 107A
MONO LUT (4KX8) 107B
107
8
109A R
109B G
109C B
109D MONO
111A OUTPUT CIRCUIT RED
111B OUTPUT CIRCUIT GREEN
111C OUTPUT CIRCUIT BLUE
111D OUTPUT CIRCUIT MONO
CHANNEL#1 (COLOR)
CHANNEL #2 (MONO)

Fig. 4a

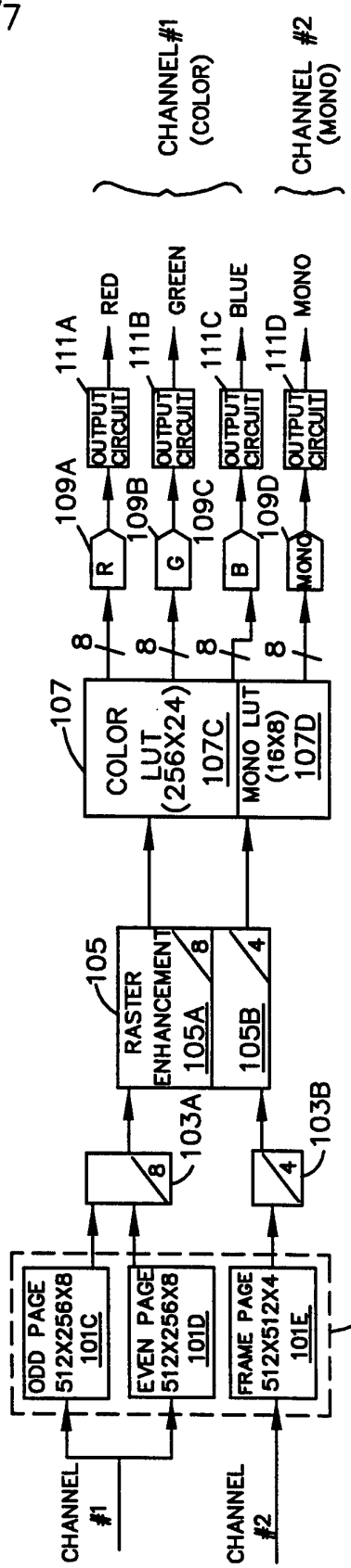

CHANNEL #1
CHANNEL #2
MEMORY 101
ODD PAGE 512X256X8 101C
EVEN PAGE 512X256X8 101D
FRAME PAGE 512X512X4 101E
103A
8
103B
4
RASTER ENHANCEMENT 105A 8 105B 4
105
COLOR LUT (256X24) 107C
MONO LUT (16X8) 107D
107
8
109A R
109B G
109C B
109D MONO
111A OUTPUT CIRCUIT RED
111B OUTPUT CIRCUIT GREEN
111C OUTPUT CIRCUIT BLUE
111D OUTPUT CIRCUIT MONO
CHANNEL#1 (COLOR)
CHANNEL #2 (MONO)

Fig. 4b

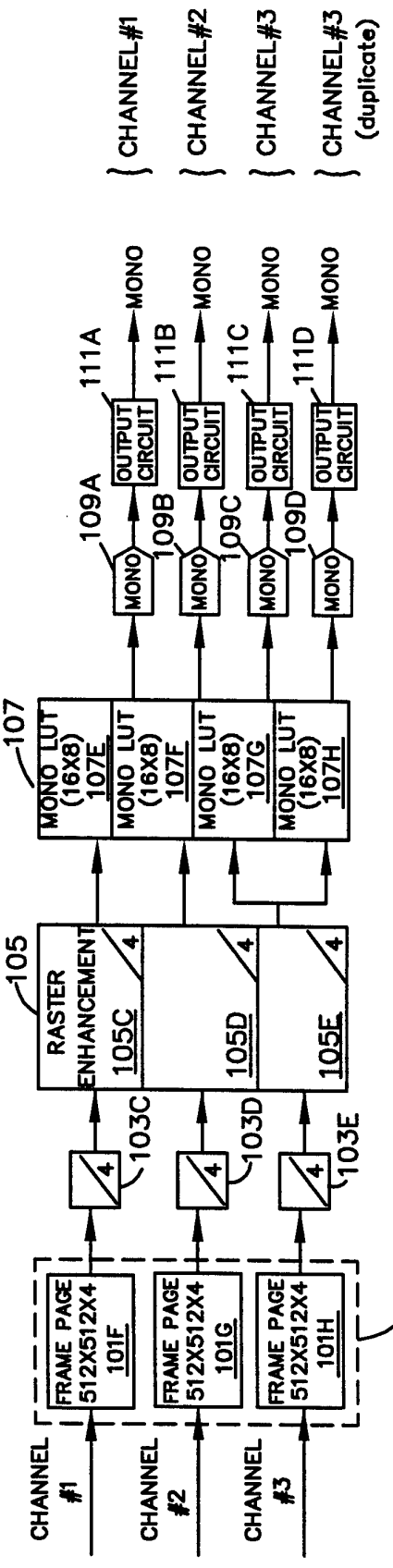

CHANNEL #1
CHANNEL #2
CHANNEL #3
FRAME PAGE 512X512X4 101F
FRAME PAGE 512X512X4 101G
FRAME PAGE 512X512X4 101H
MEMORY 101
4
103C
103D
103E
105
RASTER ENHANCEMENT
105C
105D
105E
107
MONO LUT (16X8) 107E
MONO LUT (16X8) 107F
MONO LUT (16X8) 107G
MONO LUT (16X8) 107H
MONO
109A
109B
109C
109D
OUTPUT CIRCUIT
111A
111B
111C
111D
CHANNEL#1
CHANNEL#2
CHANNEL#3
CHANNEL#3 (duplicate)

Fig. 4C

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 94/14673

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G09G1/16 G09G5/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G09G H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP,A,0 573 685 (SIEMENS AG) 15 December 1993	1,2,10
A	see column 6, line 30 - line 55 see column 7, line 49 - column 8, line 6 see column 8, line 25 - line 38 see column 9, line 7 - line 19 see column 12, line 42 - column 13, line 26 see figures 1-3	15

Y	US,A,4 789 854 (ISHII) 6 December 1988 see column 7, line 38 - column 8, line 64 see figures 7,9,10	1,2,10

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 May 1995	29.05.95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Farricella, L

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 482 746 (INTERNATIONAL BUSINESS MACHINES INC.) 29 April 1992 see page 3, line 39 - line 50 see page 6, line 6 - line 19 see figures 8,10 -----	1,3,5,7, 9,15-20

1

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 94/14673

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-573685	15-12-93	NONE	
US-A-4789854	06-12-88	JP-A- 62174794	31-07-87
EP-A-482746	29-04-92	JP-A- 4264617	21-09-92