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(54) Title: METHOD FOR ELECTROCHEMICAL POLISH IN CONSTANT VOLTAGE MODE

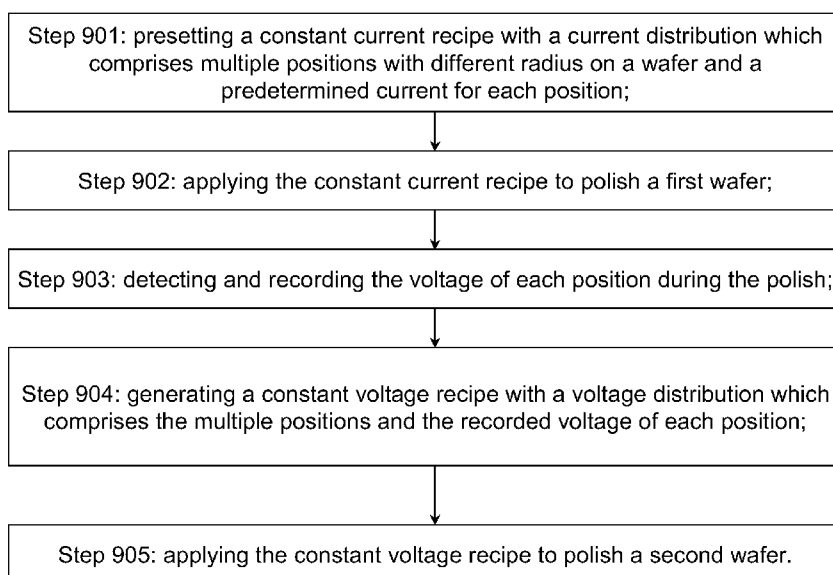


Figure 9

(57) Abstract: A method for electro-chemical polish in constant voltage mode, comprising: presetting a constant current recipe with a current distribution which comprises multiple positions with different radius on a wafer and a predetermined current for each position; applying the constant current recipe to polish a first wafer; detecting and recording the voltage of each position during the polish; generating a constant voltage recipe with a voltage distribution which comprises the multiple positions and the recorded voltage of each position; and applying the constant voltage recipe to polish a second wafer.

METHOD FOR ELECTROCHEMICAL POLISH IN CONSTANT VOLTAGE MODE

FIELD OF THE INVENTION

[0001] The present invention relates to electrochemical polish, and more particularly to a method for electrochemical polish in constant voltage mode.

BACKGROUND

[0002] Due to good results and short time needed, electrochemical polish now is used widely in semiconductor industry, and a constant current mode is chosen in that electrochemical polish reaction. In the constant current mode, the current is constant and stable, which indicates constant amount of hydrogen ions react with patterned wafer metal layer surface. When the bulk copper layer fully covers the patterned wafer surface, the hydrogen ions will uniformly react with copper layer on entire wafer until the bulk copper layer are removed. But as the copper remaining in the pattern trenches and the barrier materials (Ta, TaN, Ti, TiN, Co, Ru, etc.) has no reaction with electrolyte, the hydrogen ions concentration will rapidly increase around the copper remaining area, which makes the dishing and copper line's post surface feature vary from different line density and distribution.

[0003] In constant current mode, the amount of charged ions is constant, which is independent to patterned wafer's surface features and structures. It is to say in micro scale, the removal rate is uniform for the whole area, so the constant current mode will induce the dishing difference between different features due to the non-uniform distribution of Cu lines.

SUMMARY

[0004] The present invention is to provide a method to improve wafer-level global dishing and die-scale microcosmic dishing of semiconductor post metal layer planarization process, which is based on electrochemical polish mechanism.

[0005] In one embodiment, a method for electrochemical polish in constant voltage mode is disclosed, which comprises: preset a constant current recipe with a current distribution which comprises multiple positions with different radius on a wafer and a predetermined current for

each position; apply the constant current recipe to polish a first wafer; detect and record the voltage of each position during the polish; generate a constant voltage recipe with a voltage distribution which comprises the multiple positions and the recorded voltage of each position; and apply the constant voltage recipe to polish a second wafer.

[0006] In one embodiment, the predetermined current of the position is proportional to the radius of the position.

[0007] In one embodiment, the first wafer comprises a bare wafer, and a metal blanket is disposed on the bare wafer.

[0008] In one embodiment, the second wafer comprises a wafer with a plurality of patterned trenches or vias, and a metal layer is disposed on the wafer. The patterned trenches or vias are filled by the metal layer.

[0009] According to the present invention, a method for electrochemical polish in constant voltage mode is provided, which can overcome the bottleneck of the prior art by introducing the self-ending effect of constant voltage polish.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 illustrates a typical equipment for electrochemical polish.

[0011] Figure 2 illustrates a top view of polishing area and die-scale on the wafer.

[0012] Figure 3 illustrates a top view of die-scale and pad-scale on the wafer.

[0013] Figure 4 illustrates a top view of a defined cell.

[0014] Figure 5 illustrates a cross-sectional view A of the cell illustrated in Figure 4.

[0015] Figure 6 illustrates another cross-sectional view A of the cell illustrated in Figure 4.

[0016] Figure 7 illustrates a cross-sectional view B of the cell illustrated in Figure 4.

[0017] Figure 8 illustrates the post-process dishing of electrochemical polish in the constant voltage mode.

[0018] Figure 9 illustrates a flow chart of the method according to the present invention.

[0019] Figure 10 illustrates a current table used in the method according to the present invention.

[0020] Figure 11 illustrates a voltage table used in the method according to the present invention.

DETAILED DESCRIPTION

[0021] Illustrations are made to the present disclosure in connection with the accompanying drawings.

[0022] Referring to Figure 1, a typical equipment for electrochemical polish is provided. The equipment comprises a chuck 101, a nozzle 103 and a power supply 104, and both the chuck 101 and the nozzle 103 are electrically connected with the power supply 104. The chuck 101 is used as an anode for holding and rotating the wafer 102 during the polishing process. And the nozzle 103 is used as a cathode for ejecting charged electrolyte 105 onto the surface of the wafer 102, so that the metal ions react with the charged electrolyte 105 and are transferred to the nozzle 103. In the prior art, the power supply 104 is a constant current power supply so that the electrochemical polish can be undertaken in a constant current mode. While in the present invention, the constant current power supply is replaced by a constant voltage supply to undertake the electrochemical polish in a constant voltage mode.

[0023] In constant voltage mode according to the present embodiment, the amount of charged ions is variable, which depend on the resistance of entire polish system. To explain the function of constant voltage mode, a model of a polishing area will be introduced firstly. The polishing area is right above the nozzle 103, with the charged electrolyte 105 coming up from the nozzle 103.

[0024] Figure 2 illustrates a top view of polishing area and die-scale on the wafer 102. In this model, the polishing area is divided into several die-scales 201, and each die-scale 201 consists of a plurality of cells 202. The cell size depends on the model definition and it could be trend to nm scale. Due to the charged ions are shared by these cells 202, the total amount of charged ions is equal to the sum of each cell's amount of charged ions. Hence, all these cells 202 can be considered as parallel connection, which implies that the current is shared by all of the cells 202.

[0025] Figure 3 illustrates a top view of die-scale and pad-scale on the wafer. There are several pad-scales 203 in each die-scale 201. The cell 202 is located in the pad-scale 203, and the cell 202 is enlarged in Figure 3. Further, referring to Figure 4 to Figure 7, a top view and cross-sectional views of a defined cell 202 are given.

[0026] Generally, resistances of the electrochemical polish system include the equipment's resistance and the charged electrolyte's resistance. The equipment's resistance can be

regarded as a constant value, while the charged electrolyte's resistance relates to the size of the polishing area.

[0027] There will be several cells 202 constituting in the polishing area, and all of them are connected in parallel. To simplify the model of the polishing area, the boundary effect of charged electrolyte 105 is neglected, the current (i.e. ions concentration) and liquid resistance in the charged electrolyte 105 are the same and uniformly distributed in the charged electrolyte 105. Further, for a particular cell 202, the resistance of the cell 202 is determined by the structure of the cell 202 itself.

[0028] Referring to Figure 4 to Figure 7, a typical structure of cell 202 is shown. The cell 202 consists of lines 401 and spaces 402 which are buried under the metal before the polishing process. Both the lines 401 and the spaces 402 are distributed at intervals from each other. In one embodiment, the metal may be copper. Referring to the cross-sectional view A of the cell 202, it can be seen that the cell 202 comprises the first copper layer 403, the second copper layer 404, the barrier layer 405 and the dielectric layer 406 from top to bottom. The first copper layer 403 is on top of the barrier layer 405, and the second copper layer 404 is in the line 401. Figure 6 illustrates another cross-sectional view A of the cell 202, in which the first copper layer 403 has been removed in the polishing process.

[0029] Based on previous estimation, the resistance of the cell 202 can be obtained according to the following equation:

$$\text{[0030]} \quad R = \rho L/A = \rho L/(T*W) \quad (1)$$

[0031] Wherein ρ represents resistivity of material; L represents length, more specifically, the length of the cell's side; A represents the cross-sectional area of the first copper layer 403 and the barrier layer 405, which is equal to T multiply W; T represents the thickness of the first copper layer 403 and the barrier layer 405; W represent the cell's side width.

[0032] In some cases, if the cell 202 is defined as a square, then L will be equal to the W, so the equation (1) can be converted to:

$$\text{[0033]} \quad R = \rho /T \quad (2)$$

[0034] The copper's resistivity is much lower than barrier's resistivity, so the resistance of the copper layers is much lower than the resistance of the barrier layer 405. Moreover, according to the equation (1), the resistance of the first copper layer 403 and the barrier layer 405 is inversely proportional to the cross-sectional area A, and which is also inversely proportional to the thickness T as described in the equation (2). Therefore, as the first copper

layer 403 is removed gradually in the polishing process, the resistance of the polishing area will become higher and higher. Thus, if the constant voltage mode is applied to the electrochemical polish, the current will be automatically reduced, by this means, the removal rate will be well controlled to achieve a good polishing result. This phenomenon can be defined as self-ending effect of constant voltage mode.

[0035] Figures 8-11 illustrate one embodiment of the present invention. In the embodiment, a method for electrochemical polish in constant voltage mode is provided. The method comprises:

[0036] Step 901: presetting a constant current recipe with a current distribution which comprises multiple positions with different radius on a wafer and a predetermined current for each position;

[0037] Step 902: applying the constant current recipe to polish a first wafer;

[0038] Step 903: detecting and recording the voltage of each position during the polish;

[0039] Step 904: generating a constant voltage recipe with a voltage distribution which comprises the multiple positions and the recorded voltage of each position;

[0040] Step 905: applying the constant voltage recipe to polish a second wafer.

[0041] As the constant voltage mode is applied in this method, a good polishing result is obtained. Referring to Figure 8, a post-process dishing of electrochemical polish in the constant voltage mode is given. Wherein 35 μ m and 5 μ m represent different line widths in a polishing area, C (Center), M (Middle) and E (Edge) represent different position on the processed wafer. Because of the self-ending effect of constant voltage mode, it can be seen, in the same position, the dishings between different line widths are very close. And in the same line width, the dishings between different positions are very close too. On contrary, if the constant current mode is applied in this method, even in the same position, the dishings between different line widths will vary widely. And in the same line width, the dishings between different positions will also vary widely.

[0042] Referring to Figure 10, Table 1 is a constant current recipe which is applied to the present method. It can be seen that each position has a corresponding current value in this constant current recipe. Further, a constant voltage recipe is generated as shown in Figure 11. According to Table 1, the corresponding voltage value of each position is given in Table 2.

[0043] Table 2 is only suitable for fixed process conditions, which implies that the process conditions should be stable. The process conditions in the constant voltage recipe are as same

as process conditions in the constant current recipe. Said process conditions including but not limited to electrolyte flow rate, electrolyte temperature and wafer spin speed. If the process conditions vary over the designated scope, Table 2 should be regenerated according to Step 901-Step 903.

[0044] In order to achieve a uniform removal profile after the electrochemical polish of the present method, the predetermined current of the position is proportional to the radius of the position. Optionally, the constant current recipe is operated in pulse mode and the constant voltage recipe is operated in pulse mode. Combined with the pulse mode, the removal rate can be reduced without any side effect for metal surface roughness of the wafer. The pulse mode is conducive to improving metal surface roughness of the wafer because the pulse mode can shorten the polishing time and the metal surface roughness is inversely proportional to the polishing time.

[0045] In one embodiment, the first wafer comprises a bare wafer, and a metal blanket disposed on the bare wafer. The metal blanket can be a copper blanket, a stannum blanket, a nickel blanket, an argentum blanket or an aurum blanket.

[0046] In one embodiment, the second wafer comprises a wafer with a plurality of patterned trenches or vias; and a metal layer disposed on the wafer. The patterned trenches or vias are filled by the metal layer. The metal layer is a copper layer, a stannum layer, a nickel layer, an argentum layer or an aurum layer.

[0047] According to the present invention, a relatively uniform Cu line can be obtained, so the dishing difference will be optimized.

[0048] Although the present invention has been disclosed in preferable embodiments as above, the present invention is not limited thereto. Those skilled in the art may make possible variations and modifications without deviating from the spirit and scope of the present invention. Accordingly, the scope of the present invention should be defined by the claims.

CLAIMS

What is claimed is:

1. A method for electrochemical polish in constant voltage mode, comprising:
presetting a constant current recipe with a current distribution which comprises multiple positions with different radius on a wafer and a predetermined current for each position;
applying the constant current recipe to polish a first wafer;
detecting and recording the voltage of each position during the polish;
generating a constant voltage recipe with a voltage distribution which comprises the multiple positions and the recorded voltage of each position; and
applying the constant voltage recipe to polish a second wafer.
2. The method of claim 1, wherein the predetermined current of the position is proportional to the radius of the position.
3. The method of claim 1, wherein the first wafer comprises:
a bare wafer; and
a metal blanket disposed on the bare wafer.
4. The method of claim 3, wherein the metal blanket is a copper blanket, a stannum blanket, a nickel blanket, an argentum blanket or an aurum blanket.
5. The method of claim 1, wherein the second wafer comprises:
a wafer with a plurality of patterned trenches or vias; and
a metal layer disposed on the wafer, wherein the patterned trenches or vias are filled by the metal layer.

6. The method of claim 5, wherein the metal layer is a copper layer, a stannum layer, a nickel layer, an argentum layer or an aurum layer.
7. The method of claim 1, wherein the constant current recipe is operated in pulse mode.
8. The method of claim 1, wherein the constant voltage recipe is operated in pulse mode.
9. The method of claim 1, wherein process conditions in the constant voltage recipe are as same as process conditions in the constant current recipe.
10. The method of claim 9, wherein the process conditions comprise: electrolyte flow rate, electrolyte temperature and wafer spin speed.

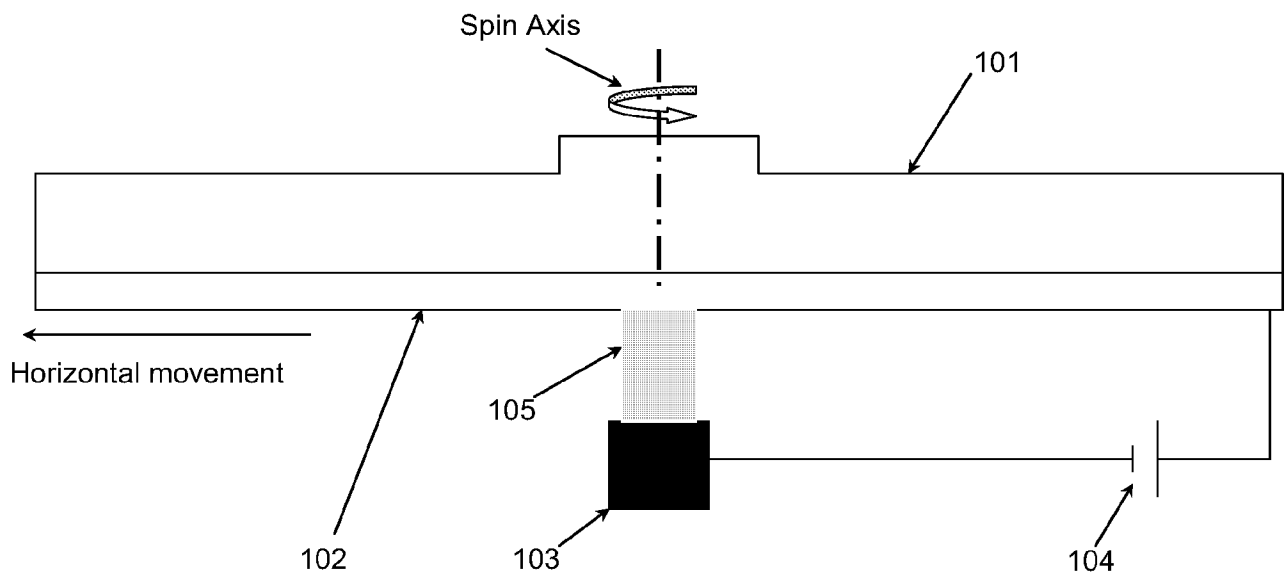


Figure 1

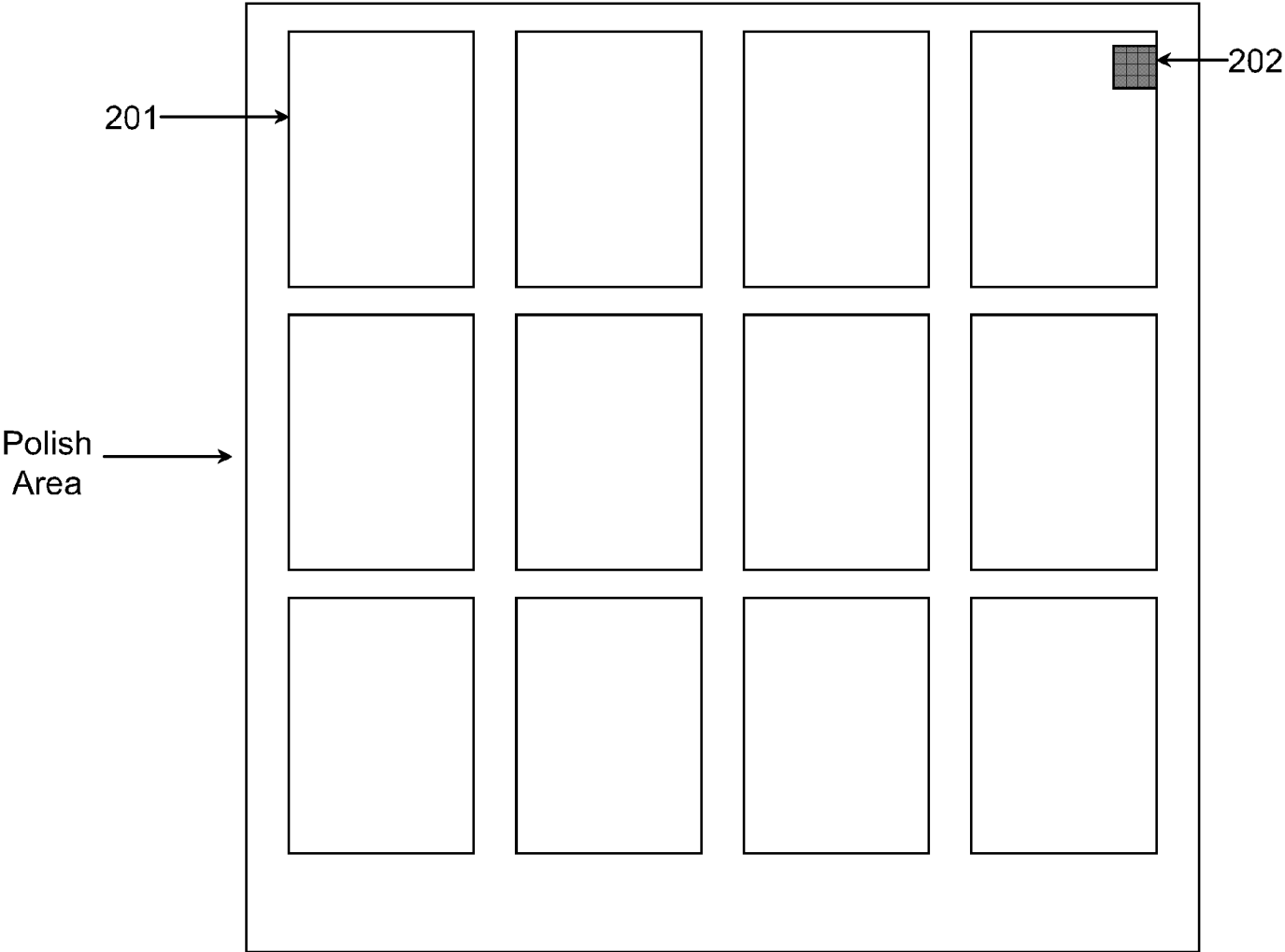


Figure 2

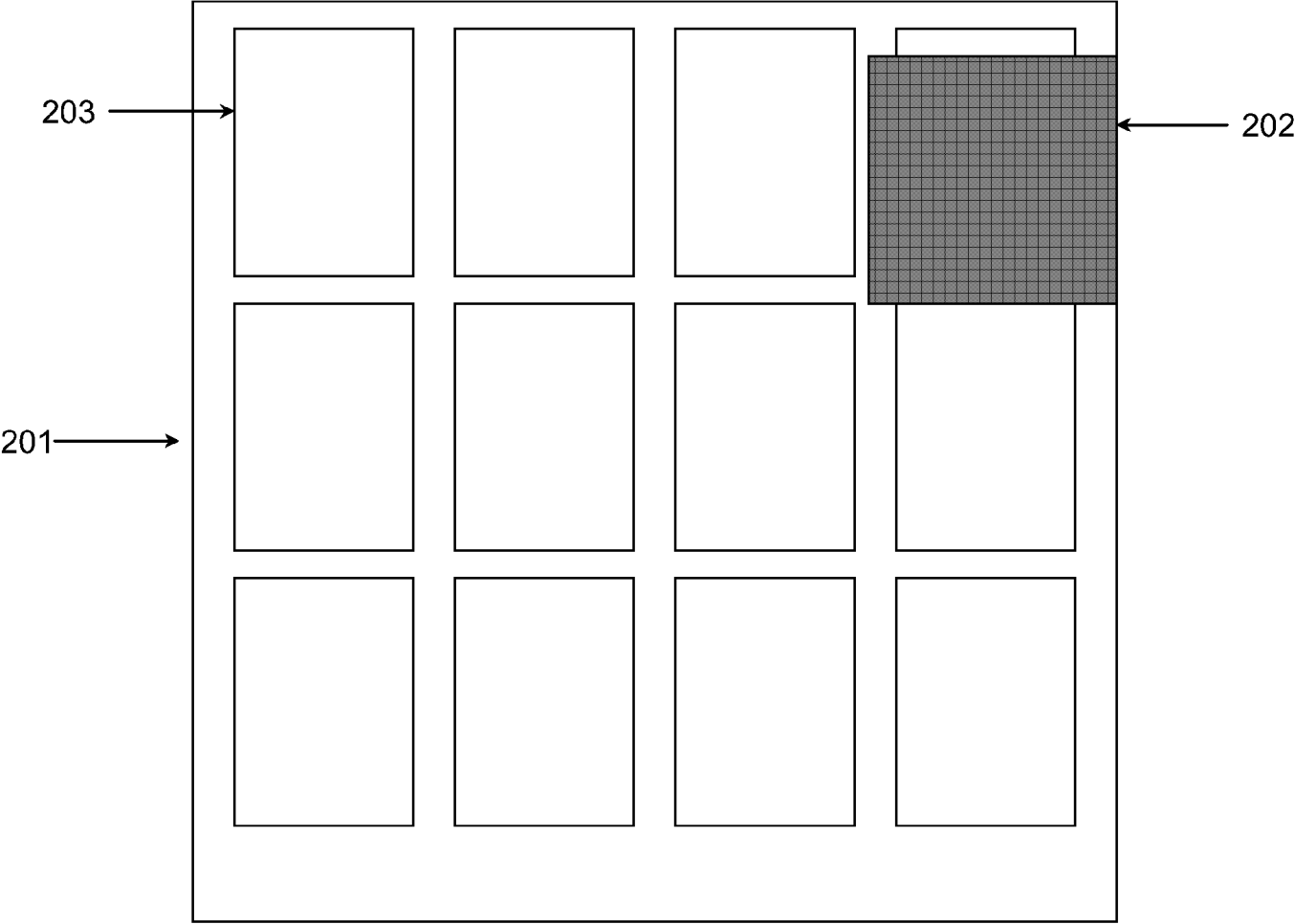
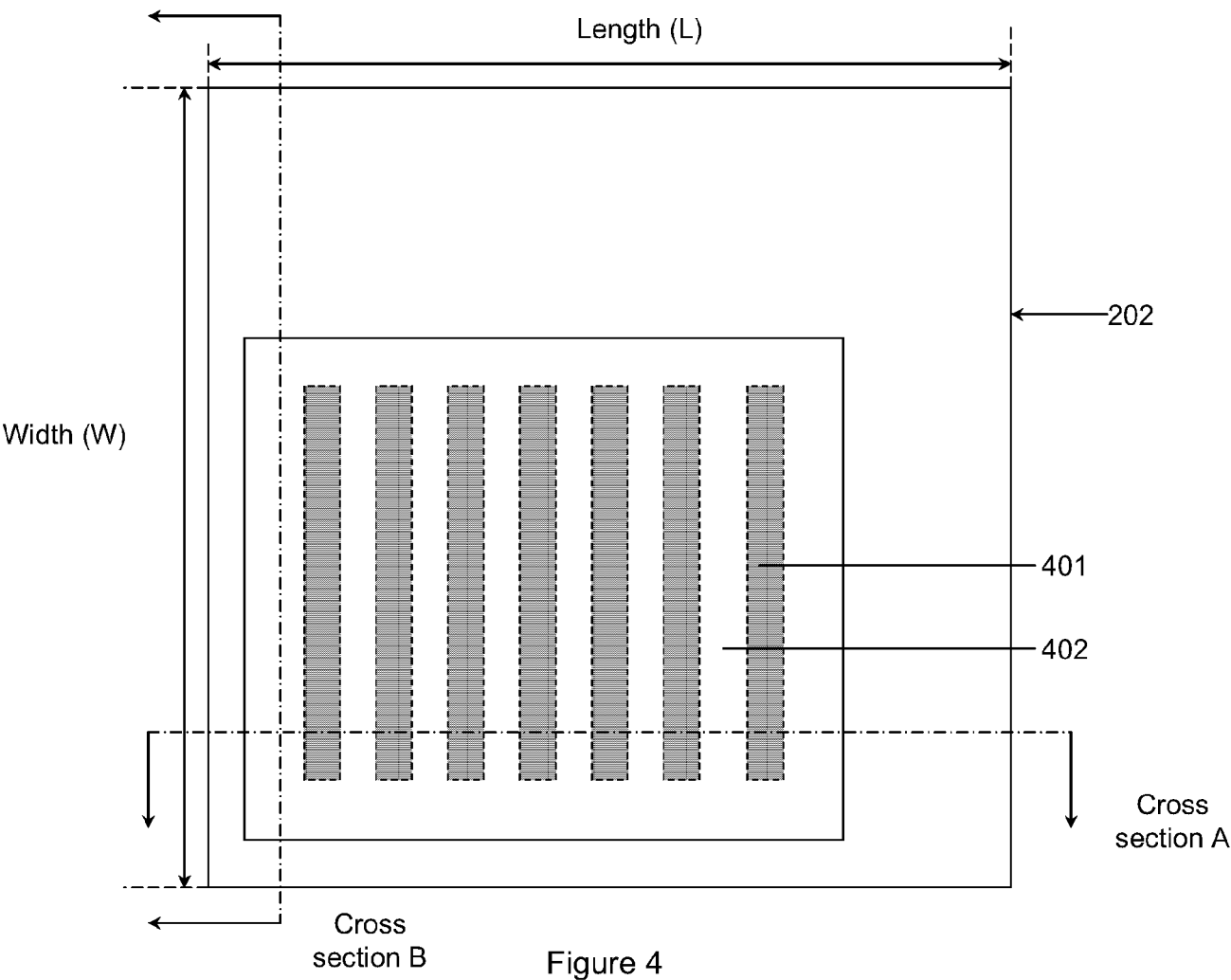


Figure 3



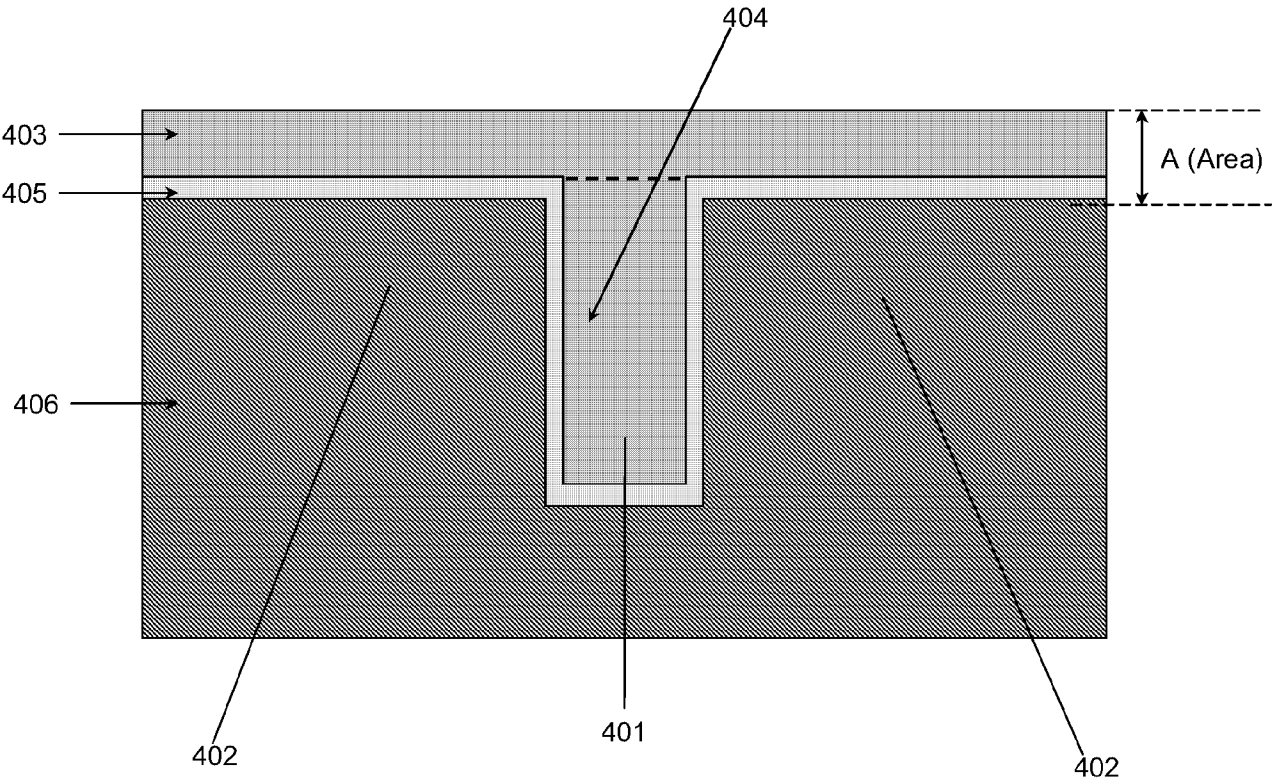


Figure 5

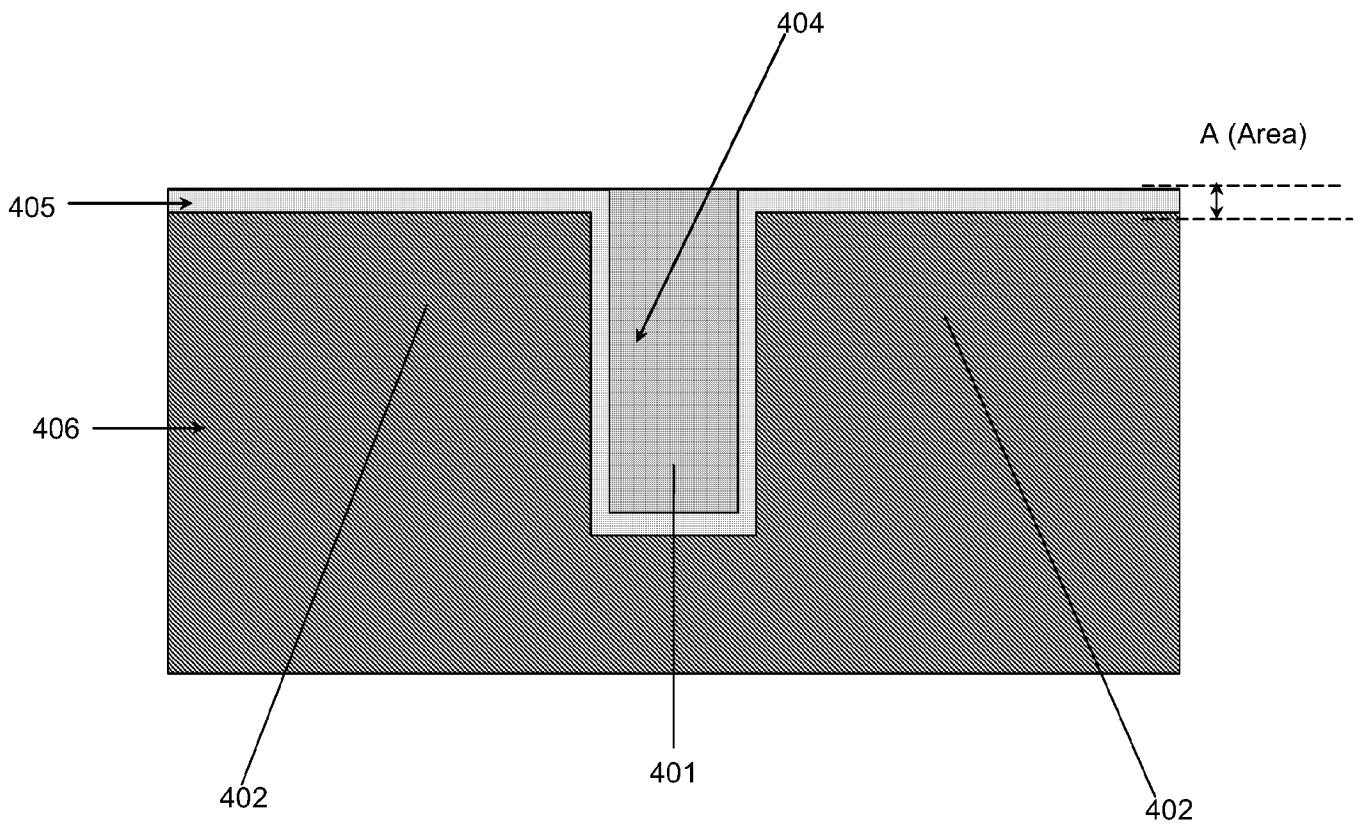


Figure 6

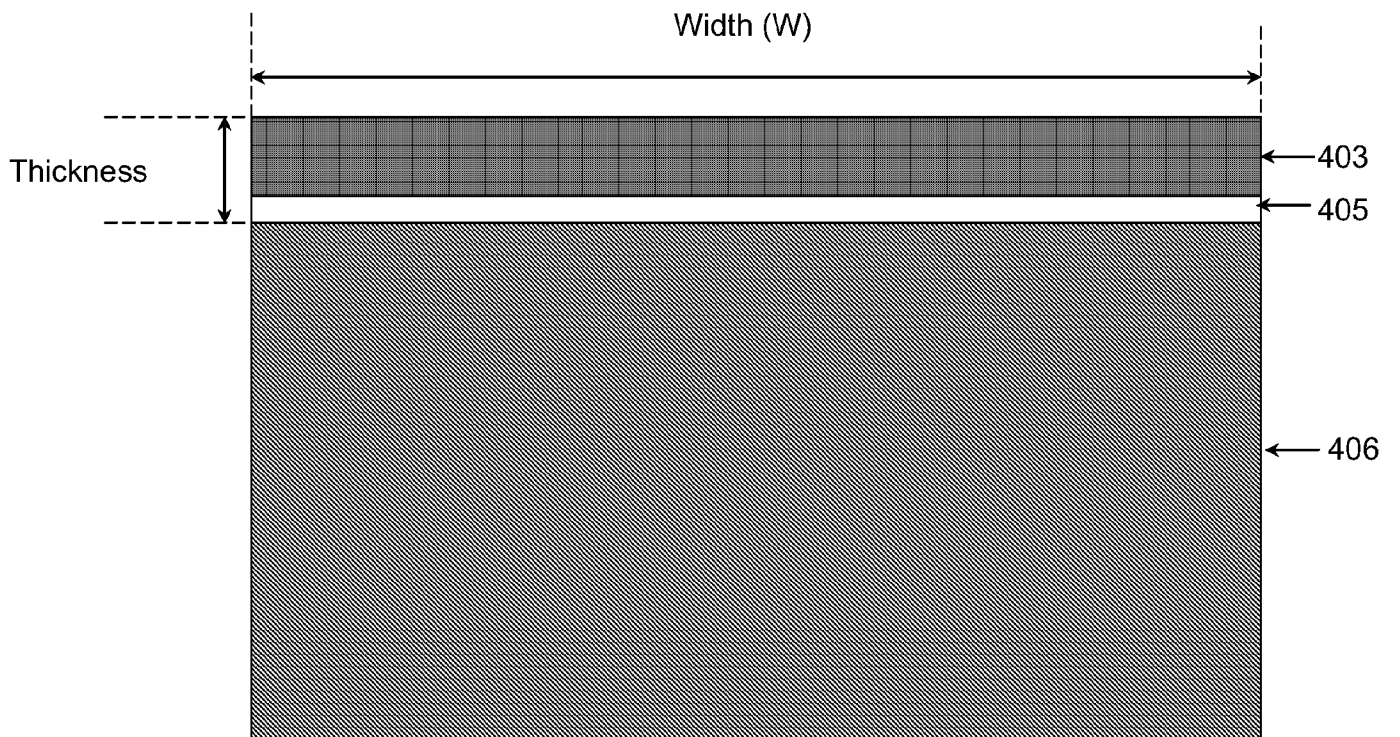


Figure 7

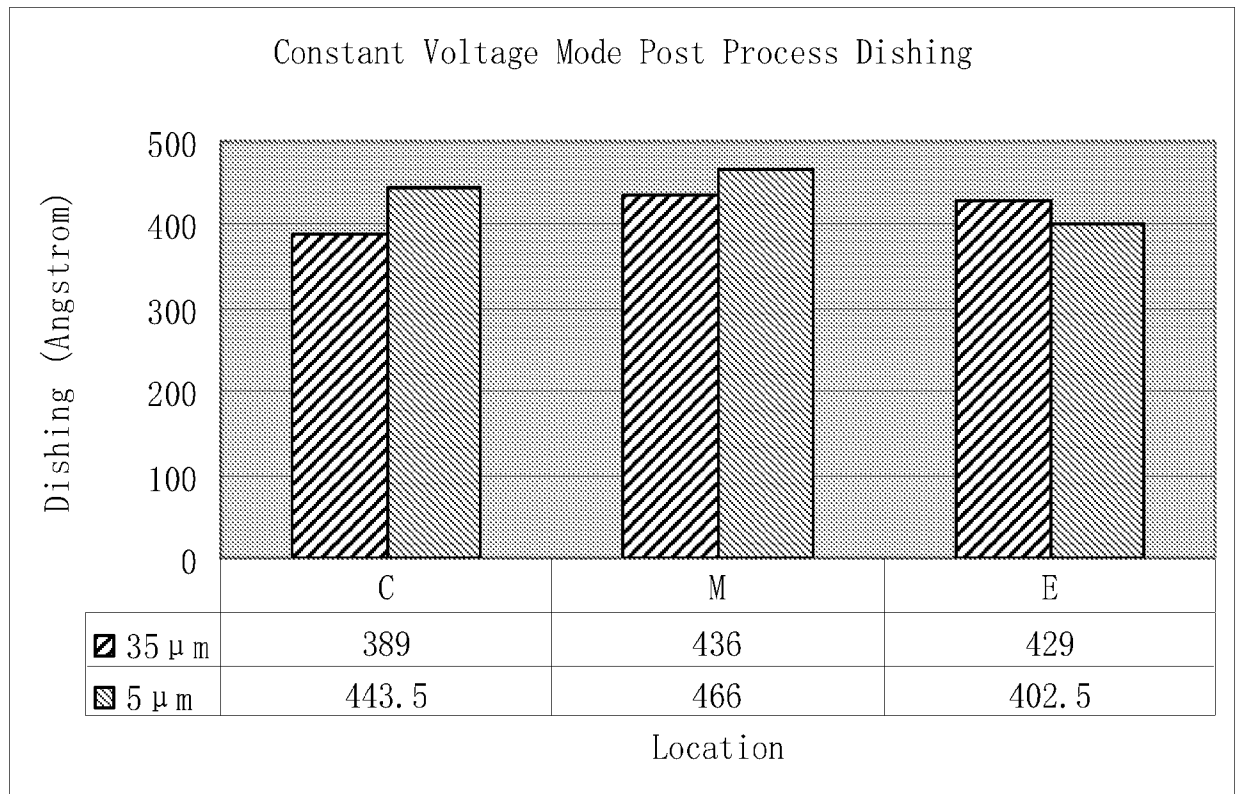


Figure 8

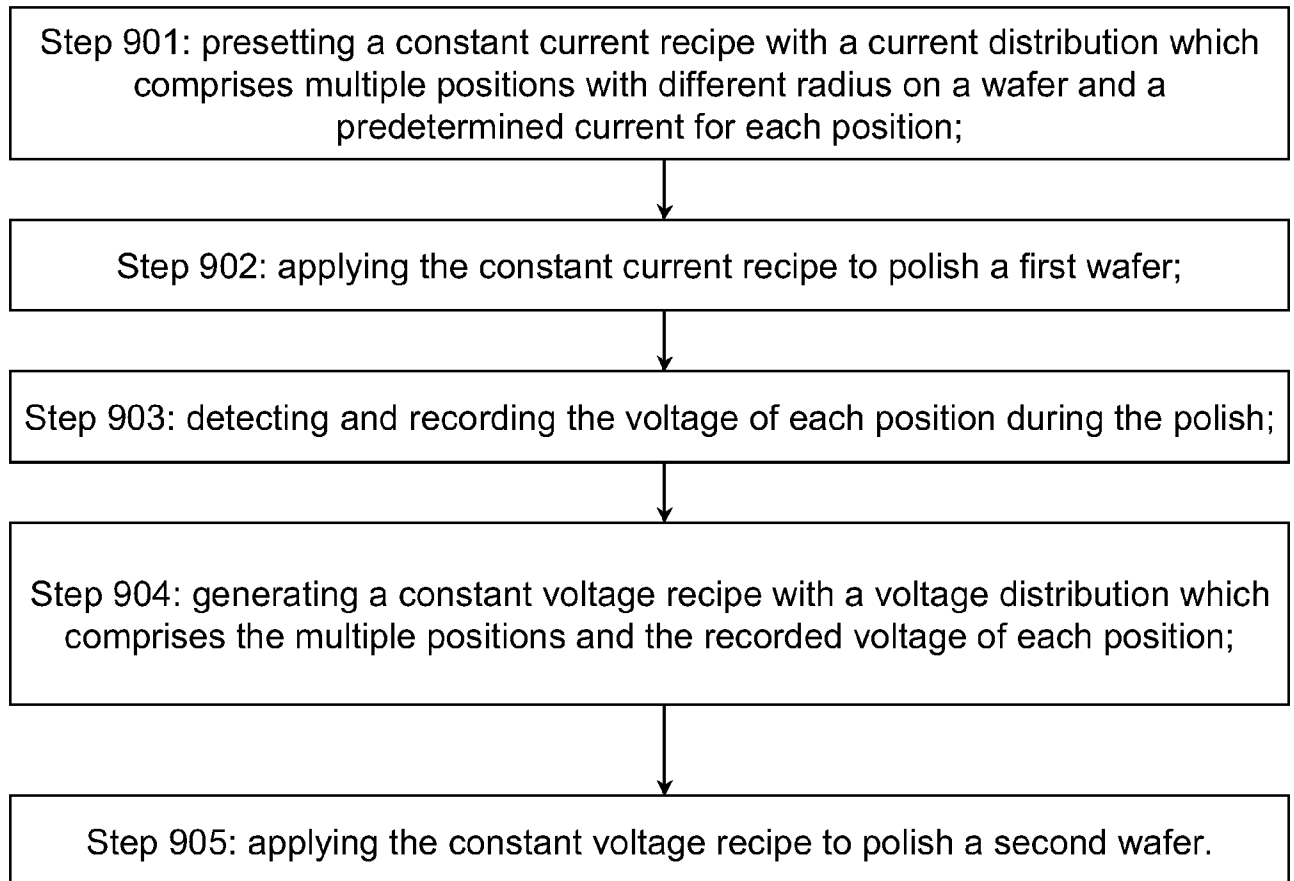


Figure 9

Table 1

Position	Current (A)
1	1.50
2	1.43
3	1.71
4	1.90
5	2.12
6	2.33
7	2.53
8	2.73
9	2.92
10	3.11
11	3.30
12	3.48
13	.
14	.
15	.

Figure 10

Table 2

Position	Voltage (A)
1	30.00
2	32.55
3	32.80
4	34.65
5	36.13
6	37.63
7	39.15
8	40.70
9	42.28
10	43.88
11	45.50
12	47.15
13	.
14	.
15	.

Figure 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/093343

A. CLASSIFICATION OF SUBJECT MATTER

C25F 3/22(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C25F 3/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: electrochemical polish+, ECP, constant voltage, CV control, constant current, CC control, uniform+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5139624 A (STANFORD RES INST INT) 18 August 1992 (1992-08-18) description, column 3, lines 56-61, column 4, lines 11-29	1-10
A	CN 104838480 A (ACM RES SHANGHAI INC) 12 August 2015 (2015-08-12) the whole document	1-10
A	TW 200809014 A (APPLIED MATERIALS INC) 16 February 2008 (2008-02-16) the whole document	1-10
A	US 2004129576 A1 (EBARA CORP) 08 July 2004 (2004-07-08) the whole document	1-10

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2015/093343

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	5139624	A	18 August 1992	None			
CN	104838480	A	12 August 2015	WO	2014089731	A1	19 June 2014
TW	200809014	A	16 February 2008	US	2007243709	A1	18 October 2007
				WO	2007121177	A2	25 October 2007
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				JP	2004197220	A	15 July 2004