ABSTRACT
A semiconductor chip package is fabricated including providing a compliant layer over a contact bearing face of a semiconductor chip, with a bottom surface of the compliant layer adjacent that chip face, a top surface facing away from the bottom surface, and at least one sloping surface extending between the top and bottom surfaces. Bond ribbons can be formed atop the compliant layer, each bond ribbon electrically coupling one of the contacts with an associated conductive terminal at the top surface of the compliant layer. A bond ribbon can include a strip extending along the sloping surface. The strip may have a substantially constant thickness in a direction away from the sloping surface.
METHODS OF MAKING COMPLIANT SEMICONDUCTOR CHIP PACKAGES

CROSS REFERENCE TO RELATED APPLICATIONS


BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention
[0003] The present invention relates to semiconductor chip packaging. More particularly, the present invention relates to an improved compliant semiconductor package structure and methods for making the same.

[0004] 2. Description of the Related Art
[0005] Complex microelectronic devices such as modern semiconductor chips require numerous connections to other electronic components. For example, a complex microprocessor chip may require many hundreds of connections to external devices.

[0006] Semiconductor chips commonly have been connected to electrical traces on mounting substrates by one of three methods: wire bonding, tape automated bonding, and flip-chip bonding. In wire bonding, the chip is positioned on a substrate with a bottom or back surface of the chip abutting the substrate and with the contact-bearing front or top surface of the chip facing upward, away from the substrate. Individual gold or aluminum wires are connected between the contacts on the chip and pads on the substrate. In tape automated bonding a flexible dielectric tape with a prefabricated array of leads thereon is positioned over the chip and substrate and the individual leads are bonded to the contacts on the chip and to pads on the substrate. In both wire bonding and conventional tape automated bonding, the pads on the substrate are arranged outside of the area covered by the chip, so that the wires or leads fan out from the chip to the surrounding pads. The area covered by the subassembly as a whole is considerably larger than the area covered by the chip. This makes the entire assembly substantially larger than it otherwise would be. Because the speed with which a microelectronic assembly can be inversely related to its size, this presents a serious drawback. Moreover, the wire bonding and tape automated bonding approaches are generally more workable with chips having contacts disposed in rows extending along the periphery of the chip. They generally do not lend themselves to use with chips having contacts disposed in a so-called area array, i.e., a grid-like pattern covering all or a substantial portion of the chip front surface.

[0007] In the flip-chip mounting technique, the contact bearing surface of the chip faces towards the substrate. Each contact on the chip is joined by a solder bond to the corresponding pad on the substrate, as by positioning solder balls on the substrate or chip, juxtaposing the chip with the substrate in the front-face-down orientation and momentarily melting or reflowing the solder. The flip-chip technique yields a compact assembly, which occupies an area of the substrate no larger than the area of the chip itself. However, flip-chip assemblies suffer from significant problems with thermal stress. The solder bonds between the chip contacts and substrate are substantially rigid. Changes in the size of the chip and of the substrate due to thermal expansion and contraction in service create substantial stresses in these rigid bonds, which in turn can lead to fatigue failure of the bonds. Moreover, it is difficult to test the chip before attaching it to the substrate, and hence difficult to maintain the required outgassing quality level in the finished assembly, particularly where the assembly includes numerous chips.

[0008] Numerous attempts have been made to solve the foregoing problem. Useful solutions are disclosed in commonly assigned U.S. Pat. Nos. 5,148,265 and 5,148,266. Preferred embodiments of the structures disclosed in these patents incorporate flexible, sheet-like structures referred to as "interposers" or "chip carriers". The preferred chip carriers have a plurality of terminals disposed on a flexible, sheet-like top layer. In use, the interposer is disposed on the front or contact bearing surface of the chip with the terminals facing upwardly, away from the chip. The terminals are then connected to the contacts of the chip. Most preferably, this connection is made by bonding prefabricated leads on the interposer to the chip contacts, using a tool engaged with the lead. The completed assembly is then connected to a substrate, as by bonding the terminals of the chip carrier to the substrate. Because the leads and the dielectric layer of the chip carrier are flexible, the terminals on the chip carrier can move relative to the contacts on the chip without imposing significant stresses on the bonds between the leads and the chip, or on the bonds between the terminals and the substrate. Thus, the assembly can compensate for thermal effects. Moreover, the assembly most preferably includes a compliant layer disposed between the terminals on the chip carrier and the face of the chip itself as, for example, an elastomeric layer incorporated in the chip carrier and disposed between the dielectric layer of the chip carrier and the chip. Such a compliant structure permits displacement of the individual terminals independently towards the chip. This permits effective engagement between the subassembly and a test fixture. Thus, a test fixture incorporating numerous electrical contacts can be engaged with all of the terminals in the subassembly despite minor variations in the height of the terminals. The subassembly can be tested before it is bonded to a substrate so as to provide a tested, known, good part to the substrate assembly operation. This in turn provides very substantial economic and quality advantages.

[0009] Commonly owned U.S. Pat. No. 5,455,390 describes a further improvement. Components according to preferred embodiments of the '390 patent use a flexible, dielectric top sheet having top and bottom surfaces. A plurality of terminals are mounted on the top sheet. A support layer is disposed underneath the top sheet, the support layer having a bottom surface remote from the top sheet. A plurality of electrically conductive, elongated leads are connected to the terminals on the top sheet and extend generally side by side downwardly from the terminals through the support layer. Each lead has a lower end at the bottom surface of the support layer. The lower ends of the leads have conductive bonding materials as, for example, eutectic bonding metals. The support layer surrounds and supports the leads.

[0010] Components of this type can be connected to microelectronic elements such as semiconductor chips or wafers by juxtaposing the bottom surface of the support layer with the
contact-bearing surface of the chip so as to bring the lower ends of the leads into engagement with the contacts on the chip, and then subjecting the assembly to elevated temperature and pressure conditions. All of the lower ends of the leads bond to the contacts on the chip substantially simultaneously. The bonded leads connect the terminals of the top sheet with the contacts on the chip. The support layer desirably is either formed from a relatively low-modulus, compliant material, or else is removed and replaced after the lead bonding step with such a compliant material. In the finished assembly, the terminals desirably are movable with respect to the chip to permit testing and to compensate for thermal effects. However, the components and methods of the '390 patent provide further advantages, including the ability to make all of the bonds to the chip or other component in a single laminating process step. The components and methods of the '390 application are especially advantageous when used with chips or other microelectronic elements having contacts disposed in an area array.

Additionally, the method described above may further include the optional step of providing for an encapsulant layer above the bond ribbons. If this optional step is performed, it is performed after the step of selectively electroplating the bond ribbons. Like the first dielectric layer, the encapsulant layer is fabricated with a set of apertures so that the terminal positions are exposed. The encapsulant layer material consists preferably of either a curable liquid, such as silicone, a flexibilized epoxy or a gel. This optional step may also be performed just prior to the optional step of providing for a second dielectric protective layer.

The method above can be applied simultaneously to a multiplicity of undiced semiconductor chips on a wafer or an array of diced semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages.

The present invention also claims the structure of a unique compliant semiconductor chip package having fan-in type leads. The compliant semiconductor chip package is comprised of (1) a semiconductor chip having a plurality of peripheral bonding pads on a face surface thereof and a central region bound by the peripheral bonding pads; (2) a first dielectric protective layer having a first surface, a second surface and apertures, wherein the first surface of the first dielectric layer is joined to the face surface of the semiconductor chip and the peripheral bonding pads are exposed through the apertures; (3) a compliant layer having a top surface and a bottom surface, wherein the bottom surface of the compliant layer is joined to the second surface of the first dielectric layer within the central region of the semiconductor chip package; and (4) a plurality of electrically conductive bond ribbons, each bond ribbon having a first end that electrically couples to a respective peripheral bonding pad of the semiconductor chips and a second end that joins to the top surface of the compliant layer to form a package terminal.

The package terminals of the completed package are configured in an array that has an area smaller than the area bound by the peripheral bonding pads on the face of the semiconductor chip. In other words, the package has fan-in leads that permits minimization of the overall package size.

For increased reliability, the compliant layer has sloped peripheral edges so that the overlying bond ribbons are curved rather than kinked.

The compliant semiconductor chip package may also have a compliant layer characterized by an array of bumped protrusions. The bumped protrusions support the overlying conductive terminal position ends of the bond ribbons and function as conductive balls that join to a substrate thus forming a ball grid array type interconnection. Alternate to the bumped protrusions, the compliant layer may have an array of concavities that are useful for placement of solder balls into each concavity. This arrangement is also useful for a ball grid array type interconnect.

The foregoing and other objects and advantages of the present invention will be better understood from the following Detailed Description of a Preferred Embodiment, taken together with the attached figures.

**BRIEF DESCRIPTION OF THE DRAWINGS**

**FIG. 1A** is a cross-sectional view of a semiconductor chip assembly at the beginning of a fabrication process.

**FIG. 1B** is a cross-sectional view of the semiconductor chip assembly after a first step of the fabrication process, showing a deposited or laminated dielectric passivation layer.
FIG. 1C is a cross-sectional view of the semiconductor chip assembly after a second step of the fabrication process, showing a deposited or laminated compliant layer within the central region of the semiconductor chip contact-bearing surface.

FIG. 1D is a cross-sectional view of the semiconductor chip assembly after a third step of the fabrication process, showing a conductive seed layer that has been sputtered over the assembly.

FIG. 1E is a cross-sectional view of the semiconductor chip assembly after a fourth step of the fabrication process, illustrating how a photolithographic step conductive bond ribbons can be formed over the assembly.

FIG. 1F is a cross-sectional view of the semiconductor chip assembly after a fifth step of the fabrication process, showing how the assembly is coated with a second dielectric protective layer.

FIG. 2 is a perspective view of the semiconductor chip assembly after the bond ribbons have been formed over the compliant layer, but before the second dielectric protective layer is coated.

FIG. 3 is a plan view of a wafer having a multiplicity of semiconductor chips, illustrating how said multiplicity of semiconductor chips can be simultaneously packaged using the semiconductor chip assembly process depicted in FIGS. 1A-1F.

FIG. 4 is a cross-sectional view of an alternate embodiment of the present invention, illustrating the use of a low modulus encapsulant material to provide further support and stress relief to the bond ribbons.

FIG. 5A is a cross-sectional view of an alternate embodiment of the present invention, illustrating the formation of bumped protrusions in the compliant layer that raise the overlying terminals such that the terminals form an array over the top surface of the compliant layer.

FIG. 5B is a perspective view of the embodiment shown in FIG. 5A.

FIG. 6A is a cross-sectional view of an alternate embodiment of the present invention, illustrating the formation of concave areas in the compliant layer such that the overlying terminals have cup-like depressions useful for accurate placement of solder balls.

FIG. 6B is a perspective view of the embodiment shown in FIG. 6A.

### DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

FIGS. 1A-1F illustrate a side view of the process of creating the compliant chip package of the present invention on the face surface of a single die, on the face surfaces of multiple dies arranged in a coplanar array or on the face surface of an undiced silicon wafer which may be subsequently diced into individual packaged chips or multi-chip modules.

FIG. 1A shows a single semiconductor chip 100 with a contact bearing face surface 120. The contacts 110 on the face surface 120 are typically aligned in a peripheral region 112 and further define a central region 115 therein. In FIG. 1B, a dielectric passivation layer is deposited or adhered onto the face surface 120 of the chip 100. The passivation layer may simply be the SiO₂ passivation layer (not shown) commonly found on the contact bearing surface of semiconductor chips, or a separate dielectric passivation layer 130 may be used, such as an epoxy resin, a polyimide resin, photo-imagable dielectric, etc. If the separate passivation layer 130 is used, the passivation layer 130 may be spun onto and built up to a planar sheet-like form on the face surface 120 or a dielectric sheet may be laminated to the face surface 120 using any of a number of electronic grade adhesives commonly known and used by those skilled in the art. The passivation layer 130 covers the face surface 120 of the chip 100 while leaving the chip contacts 110 exposed so that a bond ribbon may be placed thereon in a later step, as described below. Typically, this will be done by depositing or adhering the passivation layer 130 in a continuous sheet on the face surface 120 of the chip 100. A registering system, such as an automatic vision system, is used to locate the contacts 110. If a photo-imagable dielectric is used, the passivation layer 130 may be exposed and developed without exposing the area above the contacts 110, that unexposed area may then be removed. Another removal process which can be used is to use a pulse of directed energy, such as an excimer laser, to selectively remove the passivation layer 130 above the contacts 110. Alternately, a continuous dielectric sheet already having set contact holes may be registered and laminated to the chip 100.

In the next step, as illustrated in FIG. 1C, a compliant layer 140 is deposited or laminated onto the exposed surface of the passivation layer 130. The compliant layer 140 may be stenciled, screened or transfer molded onto the passivation layer 130 using a curable liquid which, when cured, adheres to the passivation layer 130. Alternately, the compliant layer 140 may be adhered to the exposed surface of the passivation layer 130 in the form of cured compliant pads using the aforementioned electronic grade adhesives. The compliant layer 140 has a substantially flat top surface 147 which further typically has a gradual, sloping transition 145 between the face surface 120 of the chip 100 and the top surface 147. This transition 145 may follow a line of curvature from the passivation layer 130 to a substantially flat top surface 147 or may simply be casted at an angle such that the transition 145 is not too vertically oriented in relation to the passivation layer 130 and the top surface 147. The compliant layer 140 itself may be formed from a wide variety of materials; however, preferably, a low modulus of elasticity material is used as the compliant layer 140. Compliant interposers typically are fabricated from polymeric and other materials such as silicones, flexibilized epoxy, polyimides and other thermosetting polymers, fluoropolymers and thermoplastic polymers. Also, the interposer may be a composite incorporating plural materials. The interposer may consist of, or incorporate, a foam or mesh layer. The flexibility of the interposer depends on the thickness and configuration of the interposer, as well as on the properties of the materials used therein. Thus, a flexible interposer, capable of buckling or wrinkling to accommodate relative movement, can be fabricated from high elastic modulus materials, normally considered as “rigid” provided that these materials are present in thin layers. Relatively soft materials and foams can be used in greater thicknesses and still provide a highly flexible interposer. Moreover, such soft materials and foams provide a highly compliant interposer, i.e., an interposer which is readily compressible in the directions perpendicular its surfaces and which therefore permits movement of the terminals in these directions.

FIG. 1D is then deposited atop the aforementioned assembly, as shown in FIG. 1D, typically using a sputtering operation. Typical plating seed layer materials include palladium (for electroless plating), titanium,
tungsten, nickel, chromium; however, primarily copper seed layers are used. FIG. 1E shows the next step in which photoresist 160 is applied to the exposed top surfaces of the assembly and then exposed and developed such that bond ribbons 170 may be plated within defined areas to form conductive paths electrically connecting thechip contacts 110 near a first end region of the ribbons 170 to terminals 175 comprising the second end region of the ribbons 170. This is perhaps more easily seen in the perspective view shown in FIG. 2. As shown, the ribbons 170 are plated directly onto the contacts 110 and extend in a “fan-in” arrangement from the peripheral region 112 to the central region 115 of the face surface 120 of the chip 100 atop the compliant layer 140. The elongated bond ribbons 170 extend along the sloping edges 145 of compliant layer 140. As seen in FIGS. 1C, 1A, and 2, the compliant layer can be spaced apart in a direction along the contact bearing face 120 from at least one contact 110 of the chip adjacent to the sloping surface 145. Possible bond ribbon materials include copper, gold, nickel, and alloys, combinations and composites thereof, among others. As seen in FIG. 1E, a bond ribbon may include a strip that extends along at least one of the sloping surfaces 145 of the compliant layer 140. As illustrated in FIG. 1E, the strip can have a thickness D3 in a direction extending away from the sloping surface 145. As further shown in FIG. 2, the strip can be formed to have a first dimension D1 or length extending in a lengthwise direction of the bond ribbon between the top and bottom surfaces, and a second dimension D2 or width extending in a widthwise direction of the bond ribbon transverse to the first dimension D1. Since the bond ribbons 170 are plated directly onto the chip contact/compliant layer themselves, there is no need to develop a process for bonding the ribbons 170 to the contacts, as is necessary with most other approaches such as TAB, beam lead or wire bonding. This provides a significant cost savings because specialized thermocompression or ultrasonic bonders and their bonding tools need not be purchased or maintained. It is important, however, that the material selected for the bond ribbon 170 be compatible with the chip contact 110 material, which is typically aluminum. Otherwise, a phenomenon called Kirkendahl Voiding (voids created at the boundary of two metals having different interdiffusion coefficients) may cause voiding along the boundary of the two metals (ribbon/contact) leading to intermetallic degradation and embrittlement of the bond ribbon 170 itself making the lead/bond susceptible to failure during thermal cycling. Alternatively, one or more barrier metals may be plated atop the chip contacts 110 prior to the bond ribbon plating step to thereby ensure the compatibility of materials.

As shown in FIG. 1F, preferably, a dielectric layer 180 is deposited or laminated over the top of the assembly so that only the terminals 175 are exposed. The dielectric layer may be comprised of a screened, exposed and developed or laminated sheet photo resist material or may be comprised of pyrane, epoxy resin, polyimide resin, fluoropolymer, etc. which is deposited or laminated on to the assembly, as described above in relation to the passivation layer 130. The terminals 175 may then be electrically connected to a circuitized substrate, such as a printed wiring board.

Typically, a solder ball or a solid-core solder ball will be used to create this electrical connection. The dielectric layer 180 is thus used as a solder mask to ensure that the solder does not electrically short between adjacent bond ribbons 170. Oxide layers and other surface contaminates typically build up on the surface of many types of metal (copper, nickel, etc.). Although not shown in FIG. 1F, the terminals 175 are typically flash plated with a thin layer of gold (approximately 0.25 to 0.5 microns) to inhibit the formation of these oxide layers. The gold layer is kept very thin so that it does not appreciably affect the aforementioned solder joint by dissolving into the solder to an amount which would embrittle the resulting solder joint between the terminal and a circuitized substrate.

The configuration of the above described chip package allows the package to mechanically decouple the chip 100 from an attached circuitized substrate (not shown). Typically, solder connections between the chip and the circuitized substrate are woefully inadequate to compensate for the thermal mismatch problem during temperature cycling of the chip. The combination of the compliant layer 140 and the flexible bond ribbons plated thereon allow the package to compensate for much of the TCE mismatch problem by giving limited movement of the terminals in the X, Y and Z directions with respect to the chip contacts 110 thereby minimizing the stress placed on the solder connections themselves, without imposing substantial forces on the bond between the ribbons 170 and the chip contacts 110. Further, because the compliant layer 140 is compressible, it also has the effect of compensating for any terminals 175 which are not perfectly planar with respect to its adjacent terminals when the terminals 175 are abutted against and coupled to the circuitized substrate. However, the top surface 147 of the compliant layer 140 should be made as flat and planar as possible so that the terminals 175 all lie in or near the same plane in order to minimize the amount of pressure needed to be placed on the bottom surface 125 of the chip 100 to ensure that all of the terminals/solder balls are electrically connected to a circuitized substrate.

As illustrated in FIG. 3, the chip package described above in relation to FIGS. 1 and 2 may also be provided in the form of a multiplicity of packages on a wafer incorporating a plurality of individual, diced chips, all of the same design or of differing designs. As shown, an array of individual passivation layers 230 may be deposited or laminated onto the face surface 220 of the wafer 200 leaving the chip contacts 210 of the various individual chips exposed, as described above. This arrangement is shown to better define the individual chips within the wafer. Preferably, however, a single passivation layer 230 is deposited or laminated onto the face surface 220 leaving the contacts 210 exposed. Individual compliant layers 240, as described above, are deposited or laminated onto the central regions of each of the individual chips within the wafer 200. The steps found in FIG. 1A-F are then performed, as described above, to create a plurality of connected individually packaged chips on the face surface 220 of the wafer 200. Each packaged chip having bond ribbons 270 which are connected at one end to contacts 210 and extending into to a central region of the respective chip in a fan-in fashion atop a respective compliant layer 240 and ending with a terminal 275 on the top surface 247 of the compliant layer 240. After the individual packages are completed, the individual chips may be separated from the wafer 200 and from one another, as by cutting the wafer 200 using conventional wafer severing or “dicing” equipment commonly utilized to sever wafers into individual chips. This procedure yields a plurality of packaged chip subassemblies, each of which may be secured to an individual circuitized substrate. Alternatively, the chips may be separated from the wafer 200 in multi-chip arrangements of multiples of the
same or different operational chips. The wafer level embodiment shown in FIG. 3 could be simulated using a panel of individual chips spaced apart from one another in a processing boat. The face surfaces of the individual chips would be coplanar with respect to one another to simulate the face surface 220 of the wafer 200. The chips above described steps would be performed and the chips would be separated if desired.

[0045] In the alternate embodiment shown in FIG. 4, a low modulus encapsulant material 290 may be deposited around the exposed surfaces of the bond ribbons 170 leads prior to the step shown in FIG. 1F of depositing or laminating the assembly with the dielectric layer 180. The encapsulant material 290 may have properties similar to those of rubber, gum or gel. Typical encapsulation materials include curable liquid or cured pads comprised of silicone, flexibilized epoxy, gels, thermoplastics, etc. If the encapsulant 290 is applied as a curable liquid, a fixture may be made such that the liquid flows around the bond ribbons 170 but does not flow on top of the terminals 175 to ensure that solder balls may be subsequently electrically connected to the terminals 175, as described above. Alternately, a machine such as a Camalot 1818 manufactured by Camalot Systems, Inc. of Havermill, MA may be used to flow the liquid encapsulant into the desired areas. After the liquid is deposited, it may be cured by any number of ways depending on the encapsulant material 290 used, e.g., heat, infrared energy, etc. The encapsulant 290 gives each of the bond ribbons 170 more support and further spreads some of the stress away from the ribbons 170 thus allowing a larger TCE mismatch between the chip and a circuitized substrate, as described above. After curing of the encapsulant 290, the dielectric layer 180 may be deposited or laminated thereto.

[0046] In another alternate embodiment, a conductive material such as beryllium copper, or a super plastic or shape memory alloy (such as Nitinol), is sputtered or otherwise deposited across the entire exposed surface of the chip/passivation layer/compliant layer (100/130/140) combination, shown in FIG. 1C. The conductive material may then be etched using industry standard photolithographic techniques resulting in a multiplicity of bond ribbons positioned and configured much like the bond ribbons 170 shown in FIG. 1E and FIG. 2. In this embodiment, as described above, a barrier metal, such as a flash plated layer of gold, may first be plated to the chip contacts to ensure compatibility of the electrical connection between the chip contact and the bond ribbon. Likewise, a flash plated layer of gold may be plated atop the exposed surface of the terminal. Also, the entire exposed surface of the bond ribbon could be plated with a thin layer of gold to increase the overall conductivity of such super plastic leads. A dielectric layer is next deposited or laminated as shown in FIG. 1E.

[0047] FIG. 5A shows a side view and FIG. 5B a perspective view of another embodiment, according to the present invention. In this embodiment, the compliant layer 140 has protrusions 300 on its top surface 147. These protrusions 300 may be integral with the compliant layer 140 or may be deposited or laminated onto the top surface 147 subsequent to the formation of the compliant layer 140. The protrusions 300 may be formed of compliant, elastomeric material, such as the material comprising the compliant layer 140, or may be comprised of a semi-rigid or rigid material. The bond ribbon terminals 175 are plated on top of the protrusions 300 thereby providing raised surfaces which may be connected to a circuitized substrate. This technique allows for connection to such a substrate using less solder and without the need to accurately position solid-core solder balls.

[0048] FIG. 6A shows a side view and FIG. 6B a perspective view of another embodiment, according to the present invention. In this embodiment, concave areas 310 are created in the compliant layer 140. These concave areas 310 may be created in the formation of the compliant layer 140 or may be created subsequent to the formation of the compliant layer 140. The bond ribbon terminals 175 are plated within the concave areas 310 creating conductive "cup-like" areas on the top surface 147 of the compliant layer 140. Solder or solid-core solder balls are then placed within these areas 310 and reflowed to attach the package to a circuitized substrate, as described earlier. This technique allows for the accurate placement of solder or solid-core solder balls by allowing them to be deposited and retained within the cup-like areas.

[0049] As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention as defined by the claims, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention set forth in the claims.

1. (canceled)

2. A compliant semiconductor chip package comprising: a semiconductor chip having a major surface and plurality of chip contacts at said major surface; a compliant layer having a bottom surface adjacent to said major surface, a top surface raised above and remote from said major surface and a sloped surface between said top and bottom surfaces and adjacent at least one of the chip contacts, wherein the bottom surface of the compliant layer is fully spaced apart from each of the chip contacts in a lateral direction parallel to said major surface; and a bond ribbon formed of electrically conductive material deposited to overlie and extend along said sloped surface from said bottom surface to said top surface of said compliant layer, said bond ribbon electrically coupled to said at least one chip contact.

3. The assembly as claimed in claim 2, wherein the bond ribbon is a strip of electrically conductive material overlying and extending along the sloped surface from the bottom surface to the top surface.

4. The assembly as claimed in claim 2, further comprising an electrically conductive terminal overlying said semiconductor chip, wherein said compliant layer supports said terminal over said semiconductor chip.

5. The assembly as claimed in claim 2, wherein said compliant layer has a second sloped surface extending from said bottom surface to said top surface, and said assembly includes a second bond ribbon deposited to overlie and extend along said second sloped surface from said bottom surface to said top surface, said second bond ribbon electrically coupled to a second chip contact of said plurality of chip contacts, wherein at least a portion of said second sloped surface adjacent said bottom surface and adjacent said second bond ribbon is uncovered by said second bond ribbon.

6. The assembly as claimed in claim 2, wherein said contacts are provided on a surface of said semiconductor chip.

7. The assembly as claimed in claim 6, wherein at least some of said contacts are provided in peripheral regions of said semiconductor chip.
8. The assembly as claimed in claim 2, further comprising an encapsulant layer overlying a top surface of said bond ribbon.

9. The assembly as claimed in claim 8, wherein said encapsulant layer is selected from the group consisting of a curable liquid, silicone, flexibilized epoxy, thermoplastic and gel.

10. The assembly as claimed in claim 2, wherein said compliant layer is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting epoxy, fluoropolymer, thermoplastic polymer and polynime.

11. The assembly as claimed in claim 5, further comprising a dielectric cover layer over the top surface of said compliant layer and said bond ribbon, wherein said dielectric cover layer has a plurality of apertures therein so that said terminal is accessible through the apertures.

12. The assembly as claimed in claim 2, wherein said sloped surface of said compliant layer extends in both vertical and horizontal directions.

13. The assembly as claimed in claim 12, wherein said sloped surface has a first transition region near the top surface of said compliant layer and a second transition region near the bottom surface of said compliant layer, and wherein both the first and second transition regions have respective radii of curvature.

14. The assembly as claimed in claim 2, wherein said compliant layer is readily compressible in directions perpendicular to the top and bottom surfaces.

15. The assembly as claimed in claim 13, wherein the assembly includes a second terminal atop said compliant layer, and the terminals of said assembly are bonded to corresponding contacts of a substrate, wherein said compliant layer permits movement of the terminals so as to relieve stress on electrical connections between the terminals and the substrate.

16. A compliant semiconductor chip package assembly comprising:

- a semiconductor chip having a major surface and plurality of chip contacts at said major surface;
- a compliant layer having a bottom surface adjacent to said major surface, a top surface raised above and remote from said major surface and a sloped surface between said top and bottom surfaces and adjacent at least one of the chip contacts; and
- a bond ribbon deposited to overlie and extend along said sloped surface to said top surface, said bond ribbon electrically coupled to said at least one chip contact, wherein at least a portion of the sloped surface adjacent the bottom surface and adjacent said bond ribbon is uncovered by said bond ribbon.

17. The assembly as claimed in claim 16, wherein the bond ribbon is a strip of electrically conductive material overlying and extending along the sloped surface from the bottom surface to the top surface.

18. The assembly as claimed in claim 16, further comprising an electrically conductive terminal overlying said semiconductor chip, wherein said compliant layer supports said terminal over said semiconductor chip.

19. The assembly as claimed in claim 16, wherein said compliant layer has a second sloped surface extending from said bottom surface to said top surface, and said assembly includes a second bond ribbon deposited to overlie and extend along said second sloped surface from said bottom surface to said top surface, said second bond ribbon electrically coupled to a second chip contact of said plurality of chip contacts, wherein at least a portion of said second sloped surface adjacent said bottom surface and adjacent said second bond ribbon is uncovered by said second bond ribbon.

20. The assembly as claimed in claim 16, wherein at least some of said contacts are provided in peripheral regions of said semiconductor chip.

21. The assembly as claimed in claim 16, further comprising a dielectric cover layer over the top surface of said compliant layer and said bond ribbon, wherein said dielectric cover layer has a plurality of apertures therein so that said terminal is accessible through the apertures.