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(71) Applicant
Mitsubishi Denki Kabushiki Kaisha

(Incorporated in Japan)

2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan

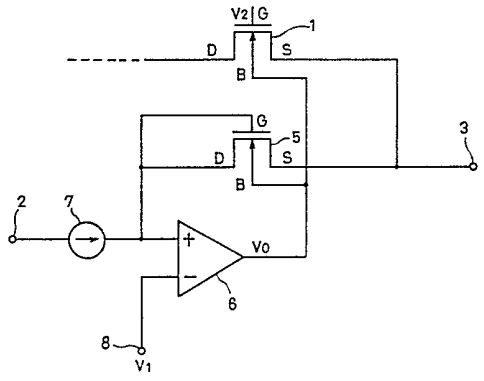
(72) Inventors
Takahiro Miki
Shiro Hosotani
Toshio Kumamoto

(74) Agent and/or Address for Service
Beresford & Co
2-5 Warwick Court, High Holborn, London, WC1R 5DJ, United Kingdom

(54) A controlled threshold device

(57) In a controlled threshold type electric device, a control voltage (V_0) from a differential amplifier (6) is inputted to a backgate (B) of a MOS transistor and the gate (G) and drain (D) of the MOS transistor (5, 11) are commonly connected to one input terminal of the differential amplifier (6), whereby a feed back loop including the MOS transistor (5, 11) is formed for the differential amplifier (6). A reference input voltage is inputted to the other input terminal of the differential amplifier (6), and a control voltage (V_0) which makes the threshold of the said MOS transistor (5, 11) converge to a value which is equal to the reference input voltage is outputted from the said differential amplifier (6) by means of the feed back loop. Since the said control voltage (V_0) is also inputted the gackgate (B) of a MOS transistor (1, 10) which is to be controlled, the threshold of the MOS transistor (1, 10) to be controlled is adjusted to be equal to the reference input voltage. Consequently, the threshold of the MOS transistor (1, 10) which is the object of control can be adjusted to an aimed value. A comparator employing the controlled threshold type electric device in which the threshold can be controlled to have the aimed value determines magnitude of the external input voltage (V_2) with the threshold being a reference.

FIG.1



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FIG.1

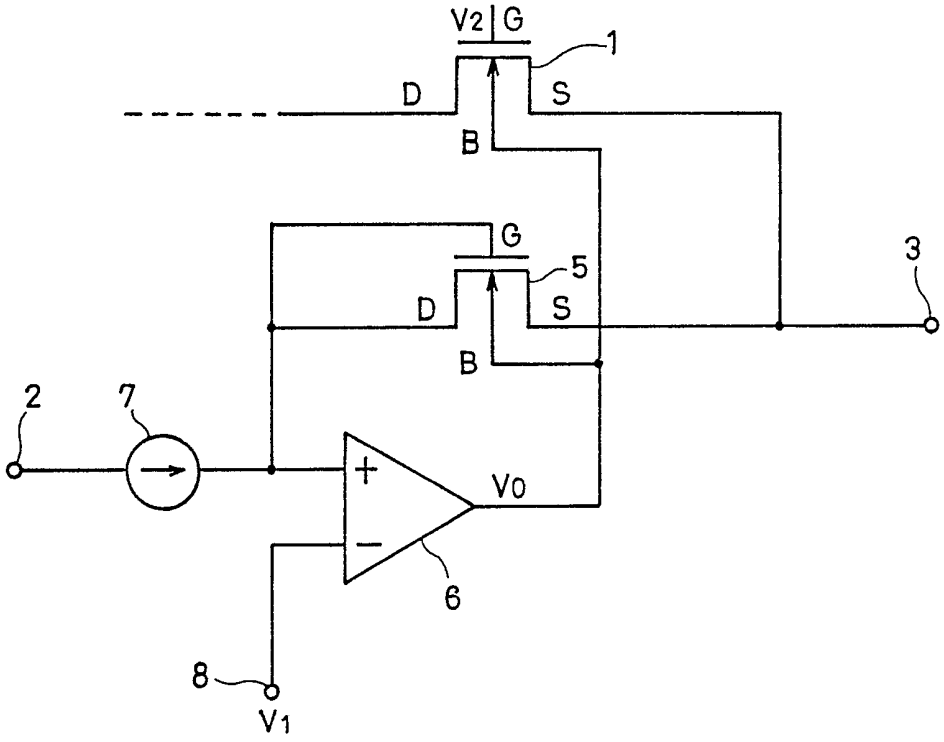


FIG.2A

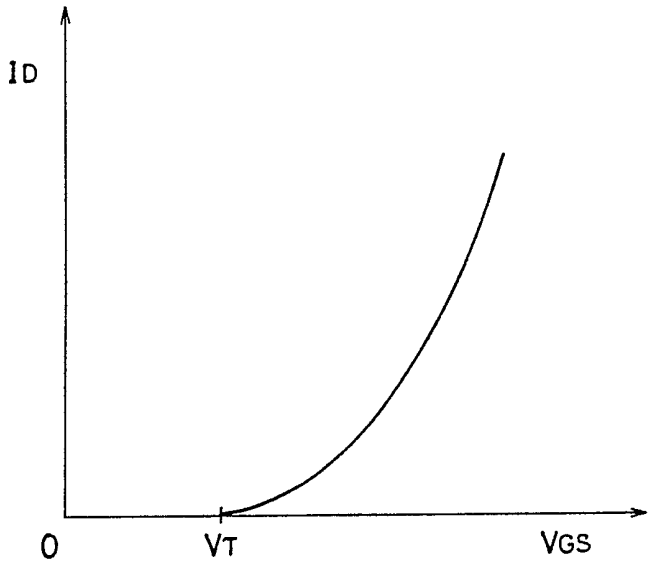
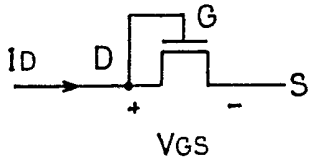


FIG.2B



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FIG.3

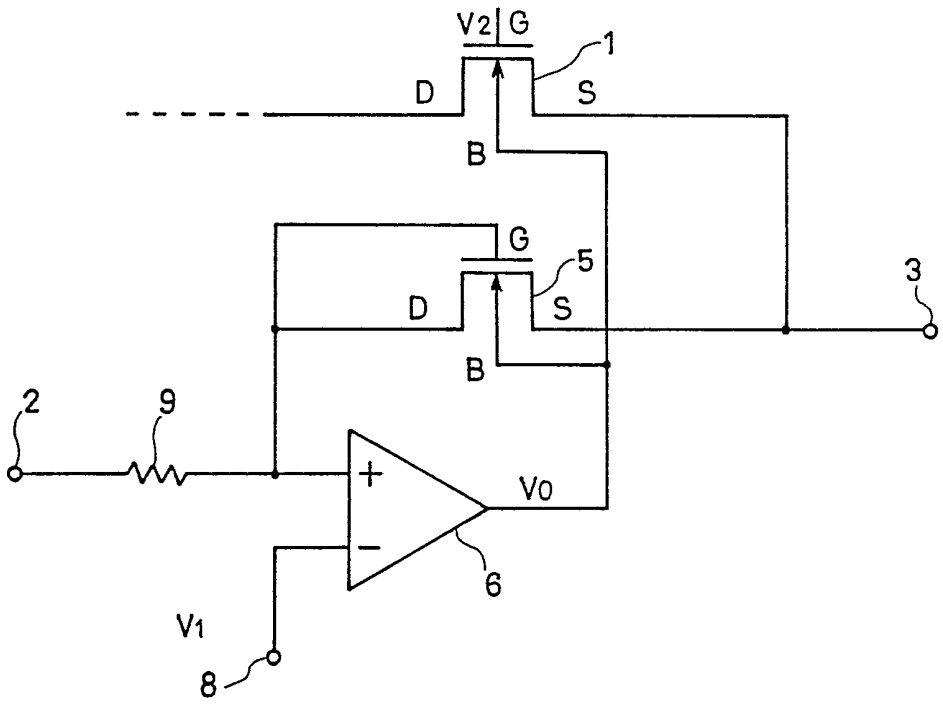
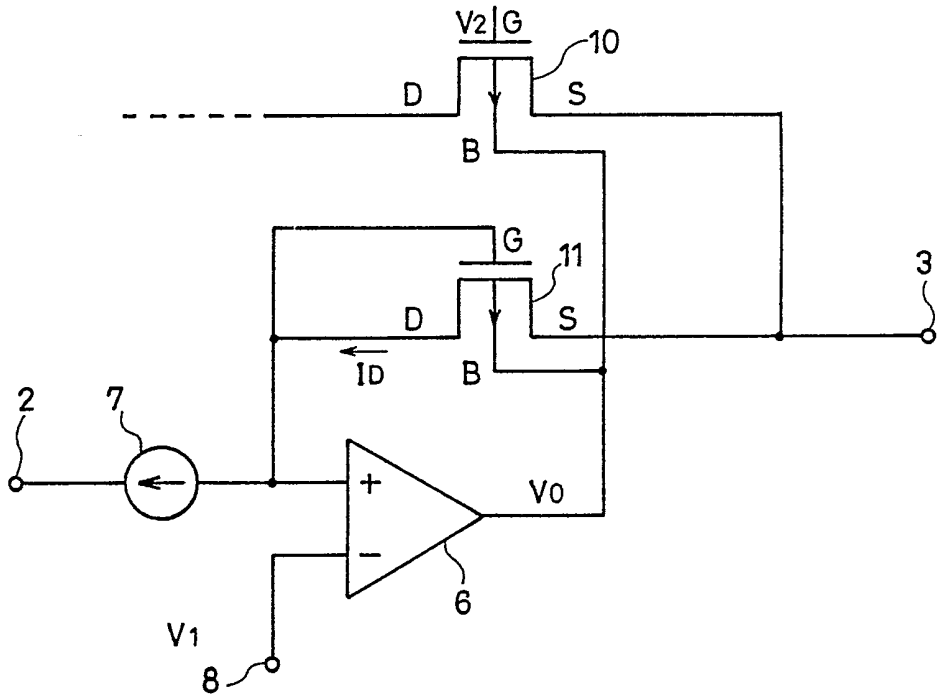


FIG.4



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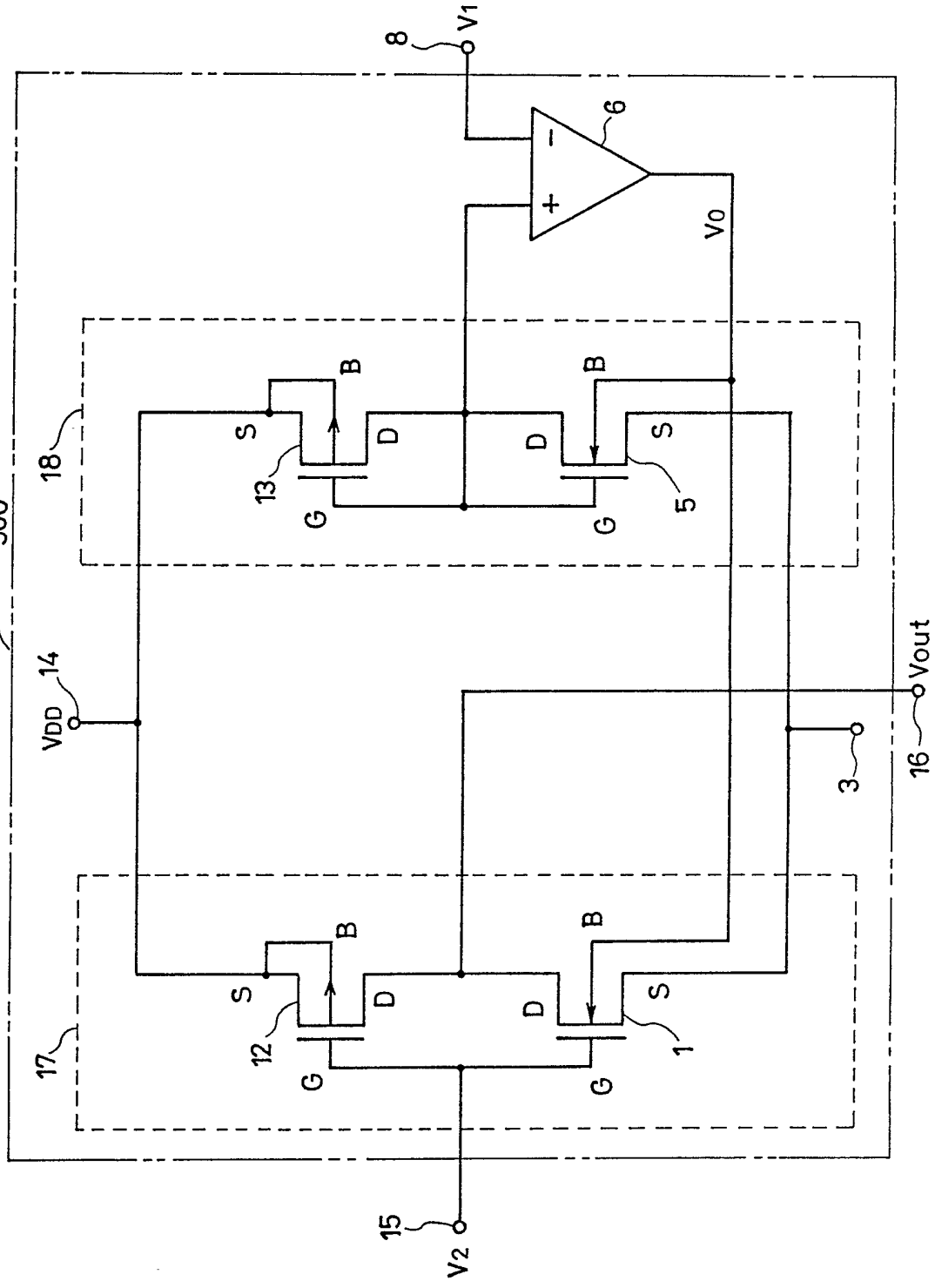


FIG.5

FIG.7

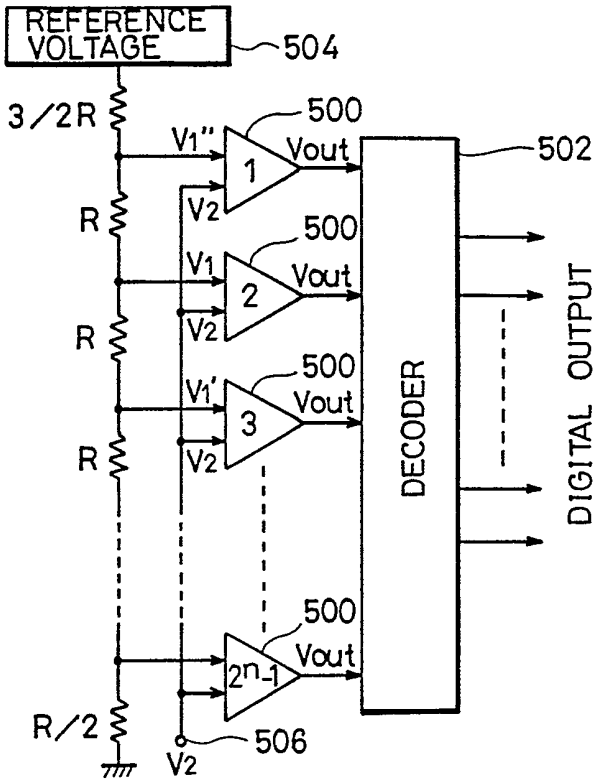

REFERENCE VOLTAGE
504
3/2R
R
R
R
R/2
V1"
V1
V1'
V2
500
Vout
1
2
3
2n-1
502
DECODER
DIGITAL OUTPUT
506

FIG.6

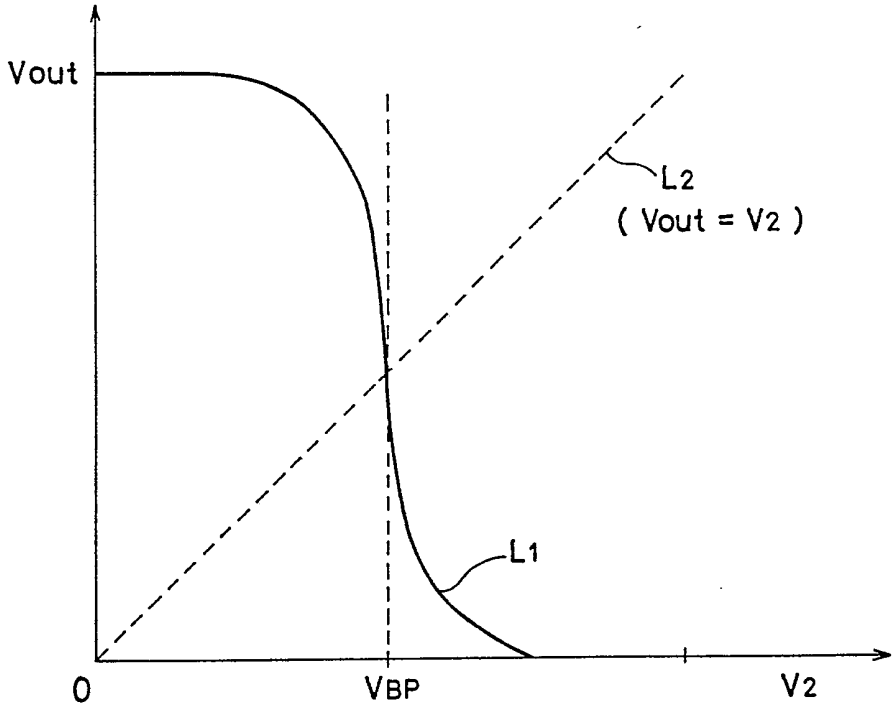

Vout
L2
(Vout = V2)
L1
0
VBP
V2

FIG.8

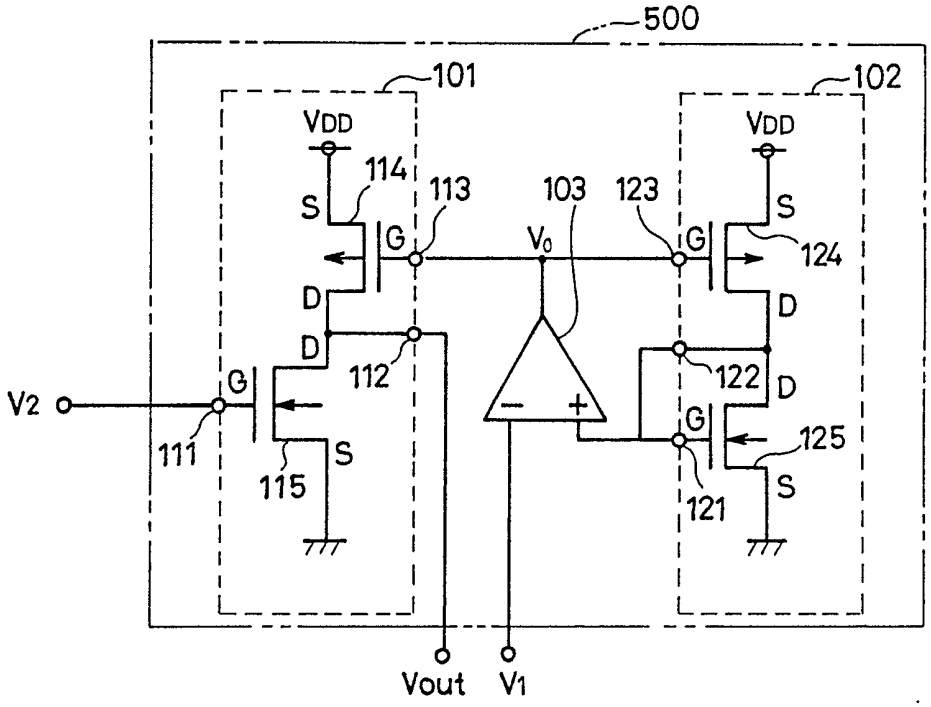

500
101
102
VDD
VDD
114
113
103
123
S
G
V_0
G
S
124
D
D
D
112
122
D
V2
G
G
111
S
115
125
S
121
Vout
V1

FIG.9

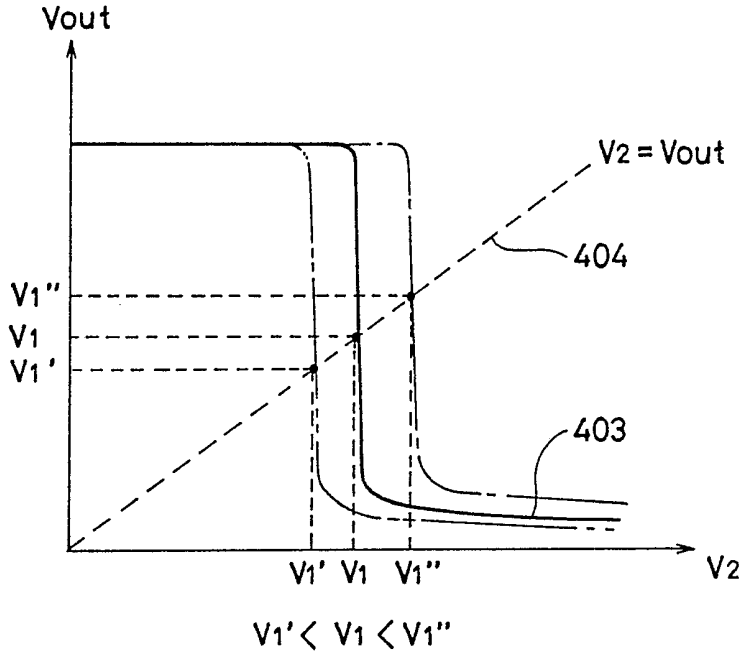

Vout
V2 = Vout
404
V1"
V1
V1'
403
V1'
V1
V1"
V2
V1' < V1 < V1"

FIG.10

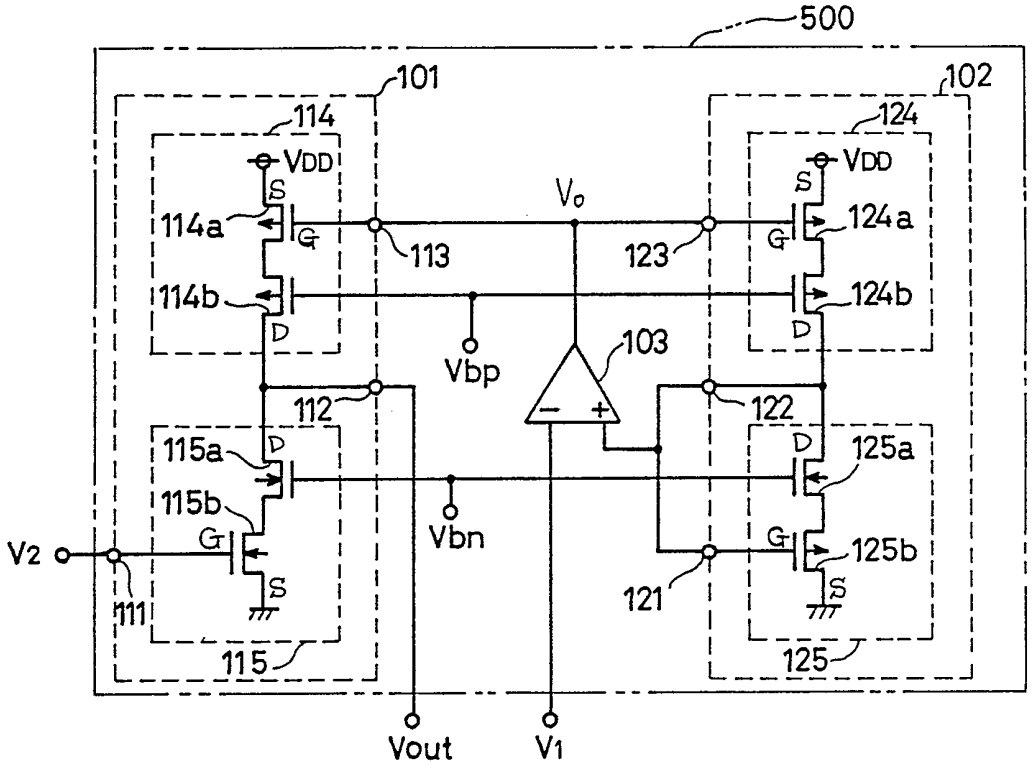


FIG.11A

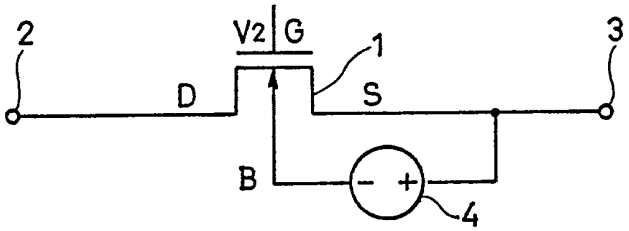


FIG.11B

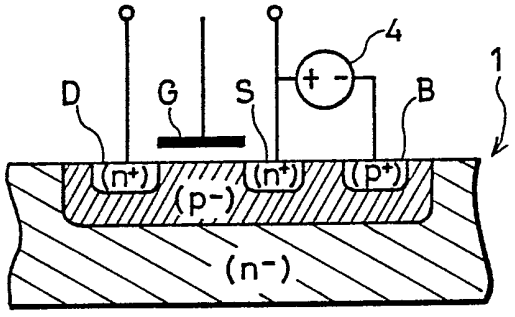
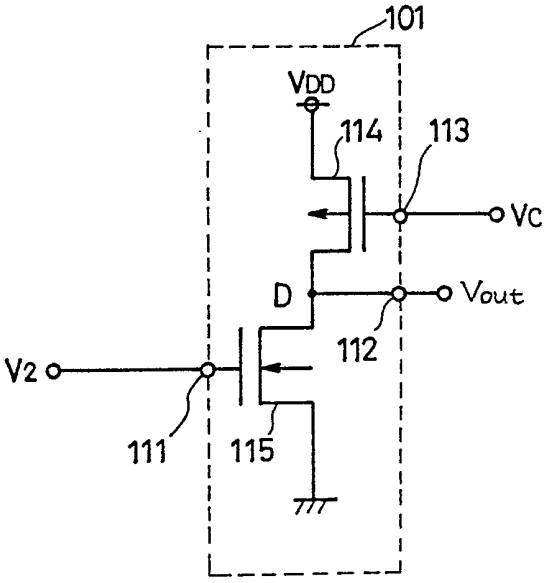


FIG.12



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FIG.13

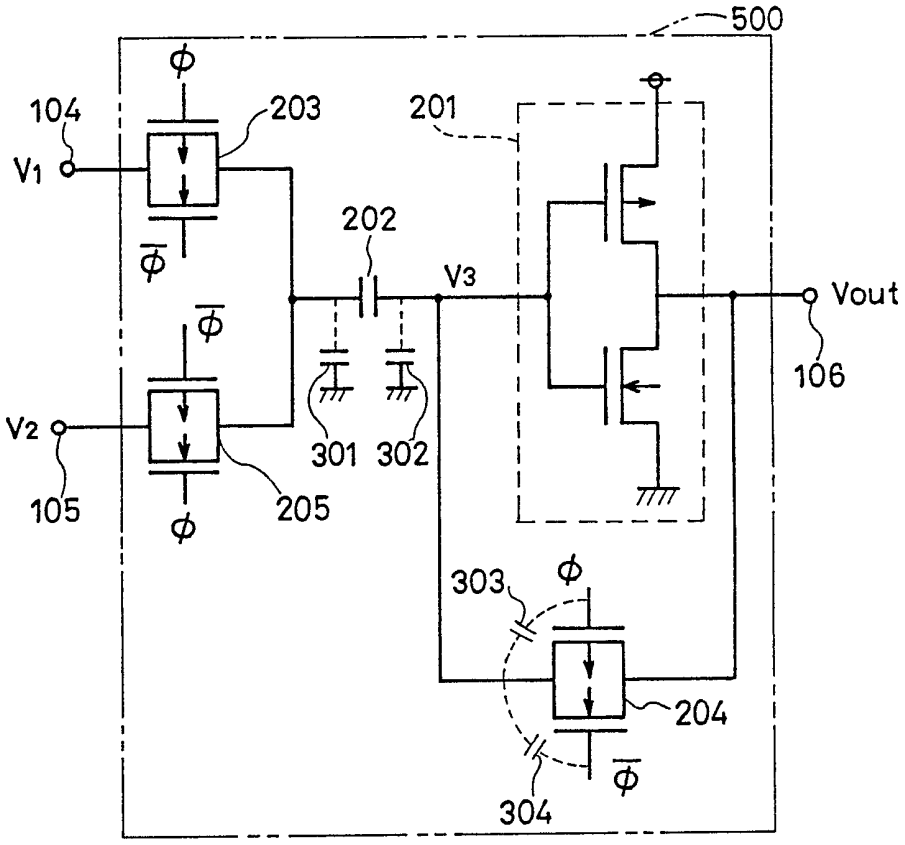


FIG.14

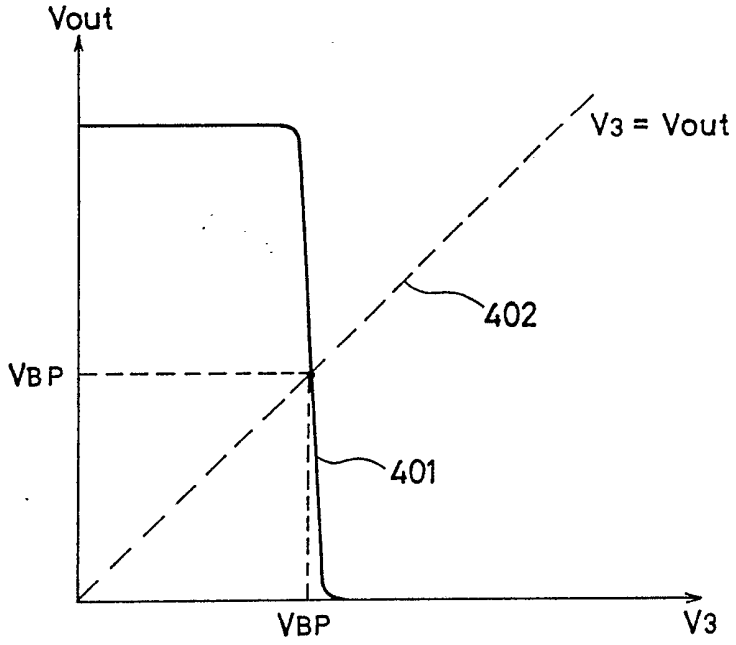
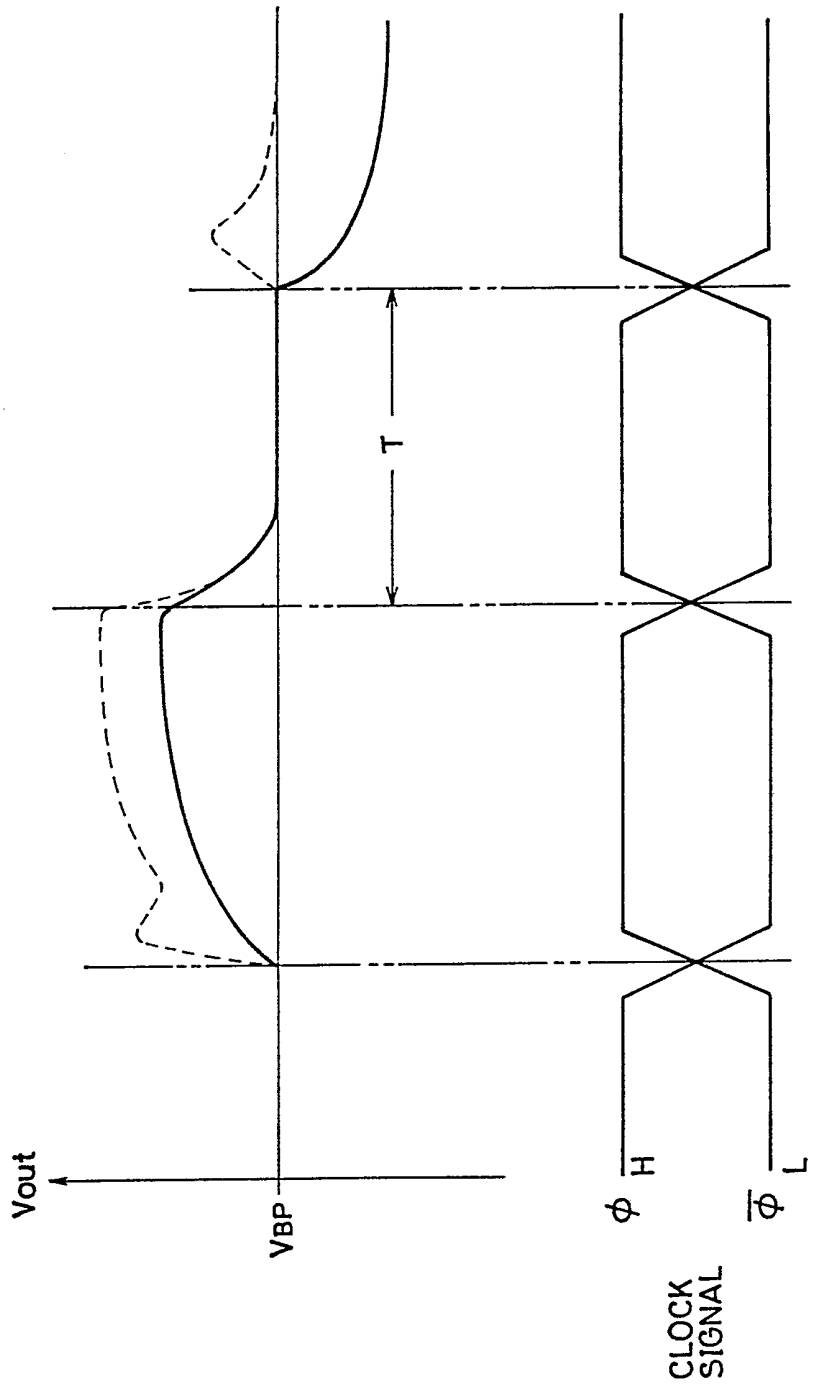


FIG.15



TITLE OF THE INVENTION

A Controlled Threshold Device Comparator Employing the Same

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a controlled threshold type electric device and a comparator employing the same. More specifically, the present invention relates to a controlled threshold type electric device comprising voltage responding means having a prescribed threshold, receiving and responding an external input voltage inputted thereto, with the state of the voltage responding means changed in accordance with a relation of magnitude between the said threshold and the said external input voltage, the said threshold controlled by a control voltage, and to a comparator employing such a controlled threshold type electric device for determining the magnitude of the inputted external input voltage based on an inputted reference input voltage to output the result of determination.

Description of the Background Art

A threshold voltage V_T of a MOS transistor and the like generally fluctuates due to differences of various parameters such as an initial threshold voltage V_{TO} and a substrate effect constant γ. For example, the initial

threshold voltage V_{TO} may differ from a desired value by about 100 mV to several 100 mV due to delicate difference of manufacturing conditions. Since accurate control of the said various parameters during manufacturing of the transistors is difficult, the threshold voltage V_T must be controlled based on measurements after the manufacturing to provide a desired threshold voltage V_T.

Fig. 11A shows an electric device proposed to meet the above described necessity. It is a circuit diagram of a controlled threshold type electric device for electrically controlling the threshold voltage V_T of MOS transistors after fabrication. Fig. 11B is a schematic cross sectional view for illustrating the structure of the electric device which will be shown later in Fig. 11A. A drain D of an N channel MOS transistor 1 is connected to an input terminal 2 and a source S is connected to a terminal 3, respectively. A gate G is connected to a control circuit, not shown, and an external input voltage V_2 is inputted thereto as a gate voltage. A positive potential side of a voltage source 4 is connected to the source S and the negative potential side thereof is connected to a backgate B. In Fig. 11B, the reference characters "p" and "n" in brackets represent conductivity types of semiconductors in the n channel MOS transistor, while the signs "+" and "-" respectively represent higher

and lower concentrations of impurities. In Fig. 11B, a gate oxide film and a field oxide film are omitted.

The operation will be described in the following. A voltage between the source and backgate (a source-backgate voltage) V_{SB} of the N channel MOS transistor 1 is a potential of the source S with the backgate B being a reference. The source-backgate voltage V_{SB} is controlled by the voltage source 4. It is known that the relation between the source-backgate voltage V_{SB} and the threshold voltage V_T can be represented by the following equation (1) (more specifically, (1a) and (1b)). The threshold voltage V_T of a N channel MOS transistor is represented by the following equation (see "Analysis and Design of Analog Integrated Circuits (Second Edition)", P. R. Gray et al., published by John Wiley and Sons p. 63).

$$V_T = V_{TO} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}) \quad \ldots(1a)$$

The threshold voltage V_T of a P channel MOS transistor is represented by the following equation.

$$V_T = V_{TO} - \gamma(\sqrt{2|\phi_f| - V_{SB}} - \sqrt{2|\phi_f|}) \quad \ldots(1b)$$

In the equations (1a) and (1b), the reference character V_{TO} represents the initial threshold voltage when the source-backgate voltage $V_{SB}=0$, the reference character ϕ_f represents a Fermi level of a substrate or a well corresponding to the backgate region (more accurately, a difference between an intrinsic Fermi level and the Fermi level), and the reference character γ

represents a positive constant which is called a substrate effect constant.

In an N channel MOS transistor, the threshold voltage V_T is a potential of the gate G with the source S being the reference at the start of the flow of the drain current I_D. If the N channel MOS transistor is an enhancement type, the said threshold voltage V_T will be a positive value. When the potential of the backgate B becomes low and the source-backgate voltage V_{SB} becomes large, the threshold voltage V_T becomes large in accordance with the equation (1a). In case of a P channel MOS transistor, the threshold voltage V_T is a potential of the gate G with the source S being the reference at the start of the flow of the drain current I_D. This will be a negative value when the transistor is an enhancement type. When the potential of the backgate B lowers and the source-backgate voltage V_{SB} becomes large (i.e. $|V_{SB}|$ becomes small), the threshold voltage V_T becomes large in accordance with the equation (1b) (as it is a negative value, the absolute value thereof becomes small). Namely, referring to Figs. 11A and 11B, the threshold voltage V_T of the N channel MOS transistor 1 can be changed by changing the source-backgate voltage V_{SB} by the voltage source 4. The control of the threshold of the N channel MOS transistor 1 can be carried out in this manner.

Fig. 12 is a circuit diagram showing another example of a conventional controlled threshold type electric device. A drain of an N channel MOS transistor 115, which is an example of a first voltage controlled type current source, and a drain of a P channel MOS transistor 114, which is an example of a second voltage controlled type current source, are connected to each other, constituting an inverting amplifier 101. An input terminal 111 of the inverting amplifier 101 is formed of a terminal connected to a gate of the said N channel MOS transistor 115, and an external input voltage V_2, which is an analog voltage, is applied to the input terminal 111. Meanwhile, a bias voltage input terminal 113 of the inverting amplifier 101 is formed of a terminal connected to the gate of the said P channel MOS transistor 114, and a control voltage V_C having a prescribed voltage value is applied to the bias voltage input terminal.

The operation of the conventional controlled threshold type electric device shown in Fig. 12 will be described in the following.

Generally, when a MOS transistor is operating in a saturated state, the drain current changes as the voltage between the gate and source changes. However, the drain current do not change so much, even when the voltage between the drain and the source changes. Namely, the MOS

transistor is widely known as a voltage controlled type current source in which the drain current can be controlled by the gate voltage.

When the drains D of the P channel MOS transistor 114 and the N channel MOS transistor 115 are connected to each other and a bias voltage is applied to the P channel MOS transistor 114, the inverting amplifier 101 is formed by the said transistors 114 and 115 with an output terminal 112 being a terminal connected to said drains D and an input terminal 111 being a terminal connected to the gate of the N channel MOS transistor 115. More specifically, when a drive current flowing into the N channel MOS transistor 115 approximately coincides with a bias current flowing from the P channel MOS transistor 114, the output of the inverting amplifier 101 will be an intermediate potential between the supply voltage V_{DD} and the ground voltage and the balance is kept. Meanwhile, when the input voltage of the inverting amplifier 101 slightly changes and the balance is lost, either one of the MOS transistors will be out of the saturated state, and the output voltage changes until the function as a current source is lost. These are well known facts which are also disclosed in pages 726 to 729 of the above mentioned article. Therefore, by changing the control voltage V_C, which is the bias voltage, a critical point can be

controlled at which the output voltage V_{OUT} changes largely in response to a small change of the external input voltage V_2. The critical point at which the output voltage V_{OUT} changes largely in response to a small change of the external voltage is called a threshold, and more specifically an input threshold in this case, and the output voltage V_{OUT} changes to and from a first logic state (low level) and a second logic state (high level) dependent on whether the external input voltage V_2 is larger than or smaller than the input threshold.

In short, a conventional controlled threshold type electric device comprises voltage responding means formed of, for example a transistor 1 shown in Figs. 11A and 11B or of an inverting amplifier 101 shown in Fig. 12. An output voltage of the voltage responding means changes to and from a first logic state and a second logic state in response to a magnitude of the external input voltage with a threshold being the reference. In the conventional controlled threshold type electric device, the said threshold in the voltage responding means is adjusted to be a desired value by inputting a control voltage of a constant magnitude.

Meanwhile, Fig. 7 is schematic diagram showing a typical A/D converter. The A/D converter comprises a plurality of comparators 500 for determining the magnitude

of the inputted external input voltage based on the inputted reference input voltage to output the result of determination. Fig. 13 is a diagram showing one of the plurality of comparators 500.

Referring to Fig. 13, the reference numeral 201 represents an inverting amplifier which is a CMOS inverter in this example. The reference numeral 204 represents a transmission gate incorporated in a wiring connecting an input portion and an output portion of the inverting amplifier 201. The reference numeral 202 represents a capacitor having one electrode coupled to the input portion of the inverting amplifier 201 and the other electrode coupled to transmission gates 203 and 205. The transmission gates 203 and 205 are respectively coupled to comparing voltage input terminals 104 and 105.

The operation will be described in the following. The operation of the comparator 500 comprises two cycles. First, when a clock signal ϕ is at a low level (L), the transmission gates 203 and 204 turn on. Accordingly, a voltage on an input side of the capacitor 202 is charged to V_1. Since the input and output portions of the inverting amplifier 201 are coupled to each other through the transmission gate 204, an output side of the said capacitor 202 is charged to a voltage V_{BP}, which is provided at an intersection of a curve 401 representing a

transfer function of the circuit (hereinafter referred to as a transfer curve) and a line 402 on which the input voltage V_3 is equal to the output voltage V_{out} of the inverting amplifier 201 shown in Fig. 14.

When the clock signal ϕ becomes high level, the transmission gates 203 and 204 are turned off, and the transmission gate 205 is turned on, the potential on the input side of the capacitor 202 changes from V_1 to V_2. On this occasion, a node on the output side of the capacitor 202 is simultaneously brought to a floating state, and therefore the voltage change of the input side of the capacitor 202 is transmitted to the inverting amplifier 201. Therefore, when $V_2 > V_1$, V_3 changes in a positive direction, and the output of the inverting amplifier sways from V_{BP} to a negative direction. When $V_2 < V_1$, V_3 changes to the negative direction and the output of the inverting amplifier 201 sways from V_{BP} to the positive direction. Now, the reference character V_1 represents a reference input voltage from the side of the reference voltage 504 shown in Fig. 7, and the reference character V_2 represents an external input voltage whose magnitude is to be determined, as shown in Fig. 7.

In this manner, when the voltage on the input side of the capacitor 202 becomes smaller, the output voltage V_{out} is amplified on the output side of the inverting amplifier

201, and the output voltage V_{out} changes in an amplitude approximately the same as the supply voltage, with V_{BP} being the center.

Fig. 15 illustrates the change of the said output voltage V_{out}. A graph shown in the upper half of Fig. 15 shows how the output voltage V_{out} changes as the time passes with the ordinate representing the output voltage V_{out} and the abscissa representing the time t.

The lower half of Fig. 15 shows how the said clock signals change as the time t passes, in which the reference character H means that the clock signal is at the high level, while the reference character L means that the clock signal is at the low level. When the clock signal ϕ is at the high level, the clock signal $\overline{\phi}$ is at the low level. While the clock signal ϕ is at the high level, the voltage on the input side of the capacitor 202 is charged to V_1 as described above, and the output voltage from the inverting amplifier 201 is maintained at V_{BP}. When the relation between the input voltages is $V_1 > V_2$, the output voltage V_{out} gradually becomes larger from a moment when said clock signals ϕ and $\overline{\phi}$ are switched. From the next point of switching of the clock signals, the output voltage of the inverting amplifier 201 is reduced to return to the voltage V_{BP}. When the relation between the input voltages is changed to $V_1 < V_2$, the output

voltage of the inverting amplifier 201 gradually decreases from the next switching point of the clock signals. The output voltage of the inverting amplifier 201 changes in accordance with the switching of the clock signals as shown by the solid line, enabling comparison of the magnitude of the input voltage V_1 with that of the voltage V_2. If the output amplitude of the said output voltage V_{out} is too small, an additional inverting amplifier having the same structure as that inverting amplifier 201 is cascaded connected in common practice.

However, in the conventional controlled threshold type electric device shown in Figs. 11A, 11B and 12, the initially set threshold may possibly be changed during use by the influence of heat and so on. Since the control voltage of the device is constant and not changeable, it can not dynamically cope with the fluctuation of the threshold during use. Therefore, the conventional device could not accurately respond the magnitude of the external input voltage, due to the change of the threshold during use.

The conventional comparator shown in Fig. 13 has following disadvantages.

(1) As is apparent from the foregoing description of the operation and from Fig. 15, a time period (represented by T in Fig. 15) for charging the voltage of the output

side of the capacitor to V_{BP} is necessary before actually amplifying the difference between the input voltages, increasing the whole operation period of the comparator.

(2) On a signal path from the comparing voltage input terminal 104 or 105 to the inverting amplifier 201, there are ON resistances of the transmission gates 203 and 205 and capacitances formed of the capacitor 202 and the stray capacitances 301 and 302 thereof, causing a RC delay, further lowering the responding operation of the inverting amplifier.

(3) If the time period for charging the said capacitor is shortened in order to shorten the operation period of the comparator, the output voltage may possibly be fluctuated since the capacitor is not fully charged.

(4) A noise of the clock signal is generated in the input side of the inverting amplifier 201 through parasitic capacitances 303 and 304 at the moment when the transmission gate 204 is turned off. The noise charges are shut in between the transmission gate 204 and the input side of the inverting amplifier 201 as the transmission gate 204 is turned off, affecting the circuit operation. Fig. 15 illustrates the bad influences on the output voltage V_{out} from the noise. The actual output voltage affected by the said noise is represented by a broken line in Fig. 15. Since the said noise charges are

added to the input side of the said inverting amplifier 201, the output voltage of the inverting amplifier 201 becomes higher by that amount and therefore, the actual output voltage is considerably different from the ideal output voltage free from the influences of the said noise represented by the solid line. Therefore, a serious disadvantage affecting the essential performance of the comparator is generated that the relation between the magnitude of the input voltage V_1 and that of V_2 can not be accurately compared.

SUMMARY OF THE INVENTION

The present invention was made in view of the foregoing and an object of the present invention is to provide a controlled threshold type electric device capable of preventing fluctuation of the threshold of the voltage responding means which is caused not only by difference of various parameters in manufacturing but also by influences after fabrication such as heat during use to appropriately control the threshold.

Another object of the present invention is to provide a controlled threshold type electric device capable of preventing fluctuation of the threshold of a transistor caused not only by differences of various parameters in manufacturing but also by influences after fabrication

such as heat during use to appropriately control the threshold.

A further object of the present invention is to provide a highly precise comparator capable of preventing fluctuation of outputs.

A controlled threshold type electric device in accordance with the present invention comprises comparing means, voltage responding means and threshold corresponding voltage outputting means, wherein said comparing means receives a reference input voltage and a feedback input voltage inputted thereto, compares the both input voltages to output a prescribed control voltage with the control voltage and an external input voltage being inputted to the voltage responding means; the said voltage responding means has a predetermined first threshold, and receives said control voltage from said comparing means and an external input voltage, said first threshold controlled by said control voltage, the state of said voltage responding means changed in accordance with a relation of magnitude between said first threshold and said external input voltage; and the threshold corresponding voltage outputting means having a predetermined second threshold, receiving said control voltage outputted from said comparing means for outputting a threshold corresponding voltage whose value corresponds

to said second threshold, said second threshold being controlled by said control voltage while maintaining a prescribed relation with said first threshold of said voltage responding means, said threshold corresponding voltage fed back as said feed back voltage to said comparing means; whereby a feed back loop toward said comparing means is formed by said threshold corresponding voltage outputting means, and said control voltage is controlled such that said first threshold of said voltage responding means converges to an aimed value.

In the controlled threshold type electric device in accordance with the present invention, the reference input voltage is compared with a feedback input voltage by means of the comparing means to provide a prescribed control voltage. The control voltage and an external input voltage are inputted to the voltage responding means, the voltage responding means has a first threshold which is controlled by said control voltage and responds to the external input voltage, with the state of the responding means changed in accordance with a relation of magnitude between the external input voltage and the first threshold.

The control voltage outputted from the said comparing means is also inputted to the threshold corresponding voltage output means, a threshold corresponding voltage

which is controlled by the control voltage while maintaining a prescribed relation with the said first threshold is outputted from the said threshold corresponding voltage output means and the threshold corresponding voltage is fed back to the said comparing means as a feed back voltage. A feed back loop for the said threshold corresponding voltage output means is formed by the said comparing means, and the said control voltage is controlled such that the said first threshold of the said voltage responding means converges to an aimed value.

Namely, by the function of the feed back loop including the comparing means, the magnitude of the said control voltage, that is, the said control operation signal is controlled such that the amount of control of the object of control, that is, the threshold corresponding voltage outputted from the threshold corresponding voltage output means, converges to a prescribed magnitude. Since the control voltage is also inputted to the voltage responding means having the first threshold being controlled while maintaining a constant relation with said second threshold voltage, the first threshold of the said voltage responding means is adjusted to converge to an aimed value. Consequently, even if the first threshold of the voltage responding means is changed

by the influences after fabrication such as heat, the said influence after fabrication is also on the threshold corresponding voltage output means and the threshold value, that is, the control amount, is changed, whereby a control voltage, that is, the control operation signal making the amount of change of the threshold corresponding voltage, that is, the control deflection to be 0 is outputted from the comparing means, and therefore the first threshold of the voltage responding means is modified and maintained at the aimed value.

According to a preferred embodiment, the said threshold corresponding voltage output means has a threshold which is controlled by said control voltage while maintaining the same value as the first threshold of the said voltage responding means.

Since the threshold corresponding voltage output means is structured as described above, the said first threshold and said second threshold are controlled maintaining a relation of one to one correspondence, a threshold according to said threshold is fed back to the comparing means, and the said first threshold can be controlled easily based on the threshold corresponding voltage.

In accordance with a more preferred embodiment, the threshold corresponding voltage output means comprises

first and second voltage controlled current sources each comprising a control voltage input portion and an output portion for outputting a current whose magnitude is controlled by a voltage applied to the control voltage input portion; a threshold corresponding voltage output terminal connected to said control voltage input portion of said first voltage controlled current source and to respective said output portions of said first and second voltage controlled current sources for outputting said threshold corresponding voltage; and a bias voltage input terminal connected to the said control voltage input portion of the said second voltage controlled current source for inputting a control voltage from the said comparing means as a bias voltage.

According to a more preferred embodiment of the present invention, the voltage responding means comprises, first and second voltage controlled current sources each comprising a control voltage input portion and an output portion for outputting a current whose magnitude is controlled by a voltage applied to the control voltage input portion; an input terminal connected to the said control voltage input portion of the said first voltage controlled current source to receive the said external input voltage; an output terminal connected to respective output portions of the said first and second voltage

controlled current sources for outputting, in response to said external input voltage, the said output voltage having the first or second logic state determined in association with said first threshold; and a bias voltage input terminal connected to the said control voltage input portion of the said second voltage controlled current source for inputting the control voltage from the said comparing means as a bias voltage.

According to a more preferred embodiment of the present invention, the said first voltage controlled current source comprises a first transistor of a certain conductivity type, and the said second voltage controlled current source comprises a second transistor of an opposite conductivity type to the said first transistor.

A controlled threshold type electric device in accordance with a still further preferred embodiment of the present invention comprises a first transistor, a second transistor and differential amplifying means, wherein said first transistor comprises first and second control electrodes and first and second conductive terminals, the said first control electrode being connected to the said first conductive terminal, the said first conductive terminal supplied with a current from current supplying means and said second conductive terminal applied with a prescribed voltage; the said

second transistor comprises first and second control electrodes and first and second conductive terminals, the said second conductive terminal applied with a prescribed voltage, the said second control electrode being connected to the second control electrode of the said first transistor; and the said differential amplifying means comprises a first input terminal connected to the said first conductive terminal of the said first transistor and a second input terminal to which a reference input voltage is inputted, and the said differential amplifying means apply outputs to the second control electrodes of the said first and second transistors; whereby a negative feed back loop toward said differential amplifying means is formed by said first transistor.

In accordance with a the more preferred embodiment, the first control electrode and the first conductive terminal of the first transistor are connected to each other and a current is supplied to the first conductive terminal, whereby the threshold corresponding voltage is applied to the first input terminal of the differential amplifying means. The differential amplifying means in which the negative feed back loop is formed provides an output voltage adapted to equalize the said threshold corresponding voltage applied to the first input terminal thereof with the reference input voltage applied to the

second input terminal. The output voltage is applied to the second control electrode of the first transistor, whereby the first transistor is controlled such that the threshold voltage thereof converges to the reference input voltage. Since the same output voltage as the output voltage inputted to the second control electrode of the first transistor is also applied to the second control electrode of the said second transistor, the said second transistor is controlled such that the threshold thereof converges to an aimed value corresponding to the said reference to input voltage.

In another aspect, the present invention is a comparator receiving a reference input voltage and an external input voltage for determining the magnitude of the said external input voltage based on the said reference input voltage to output the result of determination, comprising: comparing means; means for determining magnification of the external input voltage; and threshold corresponding voltage output means; wherein said comparing means receives said reference input voltage and a feed back input voltage, compares the both input voltages and outputs a prescribed the control voltage, with the control voltage and the external input voltage inputted to the said means for determining magnitude of the external input voltage; the means for determining

magnitude of the external input voltage having a predetermined logic determining threshold outputs a result of determination of the magnitude of the said external input voltage with the said logic determining threshold being a reference, said logic determining threshold being controlled by said inputted control voltage; and said threshold corresponding voltage output means having a predetermined threshold value receives said control voltage outputted from the said comparing means and outputs a threshold corresponding voltage corresponding to the said threshold, said threshold being controlled by said control voltage while maintaining a prescribed relation with the said logic determining threshold of the said means for determining magnitude of the external input voltage, said threshold corresponding voltage output means feeds back said threshold corresponding voltage to the said comparing means as the said feed back voltage; whereby a feed back loop toward said comparing means is formed by said threshold corresponding voltage output means and said control voltage is controlled such that the said logic determining threshold of the said means for determining magnitude of the external input voltage converges to an aimed value by the said feed back loop.

In the comparator in accordance with another aspect of the present invention, the determination of the

magnitude of the external input voltage inputted to the means for determining magnitude of the external input voltage is carried out using the said controlled logic determining threshold as a reference, and the result of determination is outputted from the said means for determining magnitude of the external input voltage. The said control voltage is inputted also to the said threshold corresponding voltage output means, the said threshold is controlled by the control voltage while maintaining a prescribed relation with said logic determining threshold, and a threshold corresponding voltage whose value corresponds to the threshold is outputted to be fed back to said comparing means as a feed back voltage. By means of the feed back loop including the said threshold corresponding voltage output means, the said control voltage is controlled such that the said logic determining threshold of the said means for determining magnitude of the external input voltage converges to an aimed value.

Namely, by means of the feed back loop including the threshold corresponding voltage output means, the said control voltage, that is, the magnitude of the control operation signal is controlled such that the threshold corresponding voltage outputted from the threshold corresponding voltage output means, that is, the amount of

control of the object, converges to a prescribed magnitude. Since the control voltage is also inputted to the means for determining magnitude of the external input voltage having the logic determining threshold value controlled while maintaining a constant relation with said threshold corresponding voltage, the logic determining threshold of the said means for determining magnitude of the external input voltage is controlled to converge to an aimed value. When an external input voltage is inputted to the means for determining magnification of the external input voltage having the logic determining threshold converged to an aimed value, the determination of magnitude is carried out based on the appropriately controlled logic determining threshold and an accurate result of determination of the magnitude corresponding to the appropriate logic determining threshold is outputted.

According to a preferred embodiment of the present invention, the said threshold corresponding value output means has a threshold being controlled by the said control voltage while maintained at a same value as the logic determining threshold of the said means for determining magnification of the external input voltage.

Since the threshold corresponding voltage output means is structured as described above, the said logic determining threshold and the said threshold are

controlled by the control voltage while maintaining one to one correspondence, a threshold corresponding voltage corresponding to the said threshold is fed back, and the said logic determining threshold can be controlled easily based on the threshold voltage.

According to a further more preferred embodiment of the present invention, the said comparing means comprises differential amplifying means for amplifying and outputting a difference between two input voltages.

According to a still further more preferred embodiment of the present invention, the said threshold corresponding voltage output means comprises first and second voltage controlled current sources each comprising a control corresponding voltage input portion and an output portion for outputting a current whose magnitude is controlled by the voltage applied to the control voltage input portion; a threshold corresponding voltage output terminal connected to the said control voltage input portion of the said first voltage controlled current source and to respective said output portions of the said first and second voltage controlled current sources for outputting the said threshold corresponding voltage; and a bias voltage input terminal connected to the said control voltage input portion of the said second voltage

controlled current source for inputting the control voltage from the said comparing means as a bias voltage.

According to a still further more preferred embodiment of the present invention, the said means for determining magnitude of the external input voltage comprises first and second voltage controlled current sources each comprising a control voltage input portion and an output portion for outputting a current whose magnitude is controlled by the voltage applied to the control voltage input portion; an input terminal connected to the said control voltage input portion of the said first voltage controlled current source to receive the said external input voltage; an output terminal connected to the respective output portions of the said first and second voltage controlled current sources for outputting the said output voltage of the first or second logic state; and a bias voltage input terminal connected to the said control voltage input portion of the said second voltage controlled current source for inputting the control voltage from the said comparing means as a bias voltage.

According to a still further more preferred embodiment of the present invention, the said first voltage controlled current source comprises a first transistor of a certain conductivity type and the said

second voltage controlled current source comprises a second transistor of an opposite conductivity type to the said first transistor.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram showing an example of a controlled threshold type electric device in accordance with the present invention;

Fig. 2A is a graph showing characteristics of a MOS transistor and Fig. 2B is a schematic diagram of a diode connected MOS transistors;

Figs. 3 and 4 are schematic diagrams showing other examples of the controlled threshold type electric devices in accordance with the present invention;

Fig. 5 is a schematic diagram showing the controlled threshold type electric device in accordance with the present invention and a comparator employing the same;

Fig. 6 is a graph showing an input/output characteristic of an inverting amplifier of Fig. 5;

Fig. 7 is a block diagram showing one application of the comparator in accordance with the present invention;

Fig. 8 is a schematic diagram showing another example of a controlled threshold type electric device in accordance with the present invention and a comparator employing the same;

Fig. 9 is a graph showing the input/output characteristics of the inverting amplifiers shown in Fig. 8;

Fig. 10 is a schematic diagram showing a further example of the controlled threshold type electric device in accordance with the present invention and a comparator employing the same;

Fig. 11A is a schematic diagram showing a conventional controlled threshold type electric device;

Fig. 11B is a schematic cross sectional view for illustrating the structure of the controlled threshold type electric device shown in Fig. 11A;

Fig. 12 is a schematic diagram showing another example of the conventional controlled threshold type electric device;

Fig. 13 is a schematic diagram showing a conventional comparator;

Fig. 14 is a graph showing the input/output characteristics of the inverting amplifier shown in Fig. 13; and

Fig. 15 is a graph showing a change of the output of the comparator shown in Fig. 13 on a time basis.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a schematic diagram showing one example of a controlled threshold type electric device of the present invention. Respective sources S of an N channel MOS transistor 1, which is an example of a first transistor, and of an N channel MOS transistor 5, which is an example of a second transistor, are each connected to a terminal 3 to have the same potential. The sources S of the transistors 1 and 5 constitute second conductive terminals, respectively. A control voltage V_0 from a differential amplifier 6 which is an example of differential amplifying means is inputted to each of the backgates B, which is an example of a second control electrode. The gate G which is an example of a first control electrode and the drain D which is an example of a first conductive terminal of the N channel MOS transistor 5 are commonly connected to a positive input terminal of the differential amplifier 6. A current source 7 which is an example of current supplying means has its input connected to an input terminal and its output connected to the positive input terminal of the differential amplifier 6. A reference input voltage V_1 is inputted from a terminal 8 to a negative input terminal of the

differential amplifier 6. The gate G which is an example of the first control electrode of the N channel MOS transistor 1 and the drain D which is an example of the first conductive terminal are connected to a circuit, not shown, and an external input voltage V_2 is inputted to the gate G.

The operation will be described in the following. Each voltage value is a potential difference from the source S which is a positive or negative value, unless specially mentioned. A drain current from a current source 7 flows through the N channel MOS transistor 5 having its gate G and drain D connected to each other (hereinafter referred to as "diode connection"), and a voltage dependent on a threshold voltage V_T of the N channel MOS transistor 5 is generated at the drain D of the N channel MOS transistor 5. Description will be given of a case in which the n channel MOS transistor 5 is an enhancement type. Fig. 2a is a graph showing a relation between a drain current I_D and a gate-source voltage V_{GS} of a diode connected enhancement type transistor shown in Fig. 2b. The relation is represented by the following equation (2).

$$I_D = \begin{cases} 0 & (V_{GS} < V_T) \\ \frac{\beta}{2}(V_{GS} - V_T)^2 & (V_{GS} \geqq V_T) \end{cases} \quad \cdots (2)$$

In the equation (2), the reference character β represents a coefficient. The equation (2) is modified to provide the following equation (3).

$$V_{GS} = V_T + \sqrt{2I_D/\beta} \quad \ldots (3)$$

In the equation (3), when the drain current I_D is very small, the gate-source voltage V_{GS} which is the potential of the gate G with the source S being the reference becomes approximately equal to the threshold voltage V_T. Since the gate G and the drain D of the N channel MOS transistor 5 are connected to each other, the drain-source voltage V_{DS} which is the potential of the drain D with the source S being the reference becomes equal to the threshold voltage V_D, whereby the threshold voltage V_D is generated at the drain D.

The threshold voltage V_T generated as the drain-source voltage V_{DS} of the N channel MOS transistor 5 is also inputted to the positive input terminal of the differential amplifier 6. The reference input voltage V_1 is applied from the terminal 8 to the negative input terminal of the differential amplifier 6. Therefore, a control voltage V_0 outputted from the differential amplifier 6 will be represented by the following equation (4) where the gain of the differential amplifier 6 is represented by a reference character A.

$$V_0 = A\ (V_T - V_1) + V_{00} \quad \ldots (4)$$

where the reference character V_{00} is an output of the differential amplifier when $V_T=V_1$.

The output V_0 is applied to the backgate B of the N channel MOS transistor 5. In the equations (1a) and (1b) described in the foregoing, the source-backgate voltage V_{SB} is considered as the potential of the source S with the backgate B being the reference, so that $V_0= -V_{SB}$. Accordingly, the equation (4) is transformed to provide the following equation (5).

$$V_{SB} = - A (V_T-V_1) - V_{00} \quad \ldots(5)$$

The operation will be described when the threshold voltage V_T is higher than the reference input voltage V_1 in the equations (1a) and (5). In the equation (5) the gain A is a positive value and $V_T > V_1$, therefore V_{SB} will be smaller than in the case where $V_T = V_1$. In an N channel MOS transistor, when the source-backgate voltage V_{SB} is reduced, the threshold voltage V_T tends to be lower according to the equation (1a). On the contrary, when the threshold voltage V_T is lower than the reference input voltage V_1, the threshold voltage V_T tends to be higher in the similar manner. In this manner, a negative feed back loop is formed by a closed loop including the differential amplifier 6 and the N channel MOS transistor 5, with the amount of control being the threshold voltage V_T and the aimed value being the reference input voltage V_1, and the

circuit is balanced when the voltage of the positive and negative input terminals of the differential amplifier 6 are equal to each other. The operation is well known as a virtual grounding function of the differential amplifier. The fact that the voltages of the positive and negative input terminals of the differential amplifier 6 become equal to each other can be described by the following equations.

When the equation (1a) is transformed by employing the equation (5), the following equation (6) is provided.

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_f - A\,(V_T - V_1) - V_{00}} - \sqrt{2\phi_f})$$

Thus,

$$\frac{V_T}{\sqrt{A}} = \frac{V_{\gamma 0}}{\sqrt{A}} + \gamma\left(\sqrt{\frac{2\phi_f}{A} - (V_T - V_1) - \frac{V_{00}}{A}} - \sqrt{\frac{2\phi_f}{A}}\right) \cdots (6)$$

In the equation (6), when the gain A of the differential amplifier 6 is very large and considered as $A \to \infty$, the following equation (7) is provided.

$$0 = \gamma\sqrt{-(V_T - V_1)} \qquad \cdots (7)$$

Consequently, $V_T = V_1$.

As described above, in the circuit comprising the N channel MOS transistor 5, the differential amplifier 6 and the current source 7, a source-backgate voltage V_{SB} which makes the threshold voltage V_T of the transistor 5 to be equal to the reference input voltage V_1 is inputted from the differential amplifier 6 to the backgate B of the N

channel MOS transistor 5 as a control voltage V_0. The control voltage V_0 is also inputted to the backgate B of the N channel MOS transistor 1, the threshold voltage V_T of the N channel MOS transistor 1 will be equal to the reference input voltage V_1 provided that the characteristics of the N channel MOS transistors 1 and 5 on the same substrate are the same. In this manner, the threshold voltage V_T of any desired transistor on the same substrate can be made equal to the reference input voltage V_1 constantly. When the threshold of the N channel MOS transistor 1 is controlled such that it is equal to the reference input voltage V_1 and an external input voltage V_2 is inputted to the gate G of the N channel MOS transistor 1, the N channel MOS transistor 1 becomes conductive when the control input voltage V_2 is larger, and the N channel MOS transistor 1 becomes non-conductive when the external input voltage V_2 is smaller. Voltage responding means is formed by the N channel MOS transistor 1, which means has a predetermined first threshold, and receives said control voltage from comparing means, which will be later, and an external input voltage, said first threshold controlled by said control voltage. The state of said voltage responding means is changed in accordance with a relation of magnitude between said first threshold and said external input voltage.

Comparing means is formed by the said differential amplifier 6 which receives a reference input voltage and a feedback input voltage and compares the both input voltages to output a prescribed control voltage. Threshold corresponding voltage output means is formed by said N channel MOS transistor 5, which has a predetermined second threshold, receiving said control voltage outputted from said comparing means for outputting a threshold corresponding voltage whose value corresponds to said second threshold, said second threshold being controlled by said control voltage while maintaining a prescribed relation with said first threshold of said voltage responding means. Further, a feed back loop is formed by a closed loop including the N channel MOS transistor 5 which feeds back the threshold corresponding voltage outputted from the said threshold corresponding voltage output means as a feed back voltage to the said comparing means and controls the said control voltage such that the said fist threshold of the said voltage responding means converges to an aimed value.

Fig. 3 is a schematic diagram showing another embodiment of the controlled threshold type electric device in which a resistance 9 is employed instead of the current source 7 shown in Fig. 1. In Fig. 3, the same reference characters as Fig. 1 represent the same

components having the same functions, and therefore detailed descriptions thereof are omitted. The controlled threshold type electric device shown in Fig. 3 operates in the similar manner as the controlled threshold type electric device shown in Fig. 1 by converting a voltage applied to the input terminal 2 to a small current by the resistance 9. An element having the same function as the resistance 9, for example a diode connected the transistor may be used instead of the resistance 9.

Fig. 4 is a schematic diagram showing one embodiment of the controlled threshold type electric device employing a P channel MOS transistors. In Fig. 4, the same reference characters as Fig. 1 represent the same components having the same functions, so that detailed descriptions thereof are omitted. Instead of the N channel MOS transistors 1 and 5 shown in Fig. 1, P channel MOS transistors 10 and 11 are connected. An input of the current source 7 which is an example of the current supplying means is connected to the positive input terminal of the differential amplifier 6 which is an example of the comparing means, and the output is connected to the input terminal 2. Except these points, the structure is the same as the controlled threshold type electric device employing N channel MOS transistors shown in Fig. 1.

The operation will be described in the following. It is assumed that the drain current I_D of the current source 7 is very small. As in the case of the above described N channel MOS transistor, the drain-source voltage V_{DS} of the P channel MOS transistor 11 becomes the threshold voltage V_T. In the case of the P channel MOS transistor, the threshold voltage V_T is the potential of the gate G with the source S being a reference, and the said threshold voltage V_T becomes a negative value when the P channel MOS transistor is an enhancement type.

When the threshold voltage V_T of the P channel MOS transistor 11 is higher than the reference input voltage V_1, the control voltage V_0 becomes larger than when $V_T=V_1$ as in the case of the above described N channel MOS transistor, and the source-backgate voltage V_{SB} becomes smaller than when $V_T=V_1$. When the source-backgate voltage V_{SB} decreases, the threshold voltage V_t tends to be lowered according to the equation (1b). On the contrary, when the threshold voltage V_T is lower than the reference input voltage V_1, the threshold voltage V_T tends to be raised. In this manner, the threshold voltage V_T and the reference input voltage V_1 become equal to each other by the function of the negative feed back loop.

Namely, in the controlled threshold type electric device shown in Fig. 4, voltage responding means is formed

by the P channel MOS transistor 10 as an example of the second transistor, the voltage responding means having a predetermined first threshold, receiving said control voltage from said comparing means and an external input voltage, said first threshold controlled by said control voltage. The state of said voltage responding means is changed in accordance with a relation of magnitude between said first threshold and said external input voltage. Threshold corresponding voltage output means is formed by the P channel MOS transistor 11 as an example of the first transistor, the said threshold corresponding voltage outputting means having a predetermined second threshold, receiving said control voltage outputted from said comparing means for outputting a threshold corresponding voltage whose value corresponds to said second threshold, said second threshold being controlled by said control voltage while maintaining a prescribed relation with said first threshold of said voltage responding means, said threshold corresponding voltage fed back as said feed back voltage to said comparing means. Further, a feed back loop toward said comparing means is formed by said threshold corresponding voltage outputting means, and said control voltage is controlled such that said first threshold of said voltage responding means converges to an aimed value.

Meanwhile, in the controlled threshold type electric devices shown in Figs. 1 to 4, the first transistor is formed of one MOS transistor 1 or 10. However, the first transistor may be formed of a plurality of MOS transistors, with the control voltage V_0 from the differential amplifier 6 inputted to the respective backgates. Although MOS transistors are shown in Fig. 1 to 4, MIS transistors may be employed.

Fig. 5 is a schematic diagram showing a further example of the controlled threshold type electric device in accordance with the present invention. Referring to the figure, the sources S of the N channel MOS transistors 1 and 5, which are in turn examples of the first voltage controlled current source, are commonly connected to a terminal 3 to have the same potential. The backgates B which are examples of the second driving voltage input portions, of the N channel MOS transistors 1 and 5 are commonly connected to an output portion of a differential amplifier 6 which is an example of the differential amplifying means to receive a control voltage V_0. The source S which is an example of the input portion of the P channel MOS transistors 12 and 13 which are in turn examples of the second voltage controlled current sources and the backgate B which is an example of the driving voltage input portion are connected commonly to the

terminal 14 to receive a supplied voltage V_{DD}. The gate G which is an example of the first driving voltage input portion of the N channel MOS transistor 1 and the gate G which is an example of the first driving voltage input portion of the P channel MOS transistor 12 are commonly connected to the input terminal 15 to receive the external input voltage V_2. The drain D which is an example of an output portion of the N channel MOS transistor 1 and the drain D which is an example of the output portion of the P channel MOS transistor 12 are commonly connected to the output terminal 16, and an output voltage V_{out} is outputted. The N channel MOS transistor 1 and the P channel MOS transistor 12 constitute an inverting amplifier 17. The gates G which are examples of the first driving voltage input portions of the transistors 5 and 13 and the drains which are the examples of the output portions are commonly connected to the positive input terminal of the differential amplifier 6 which is an example of the differential applying means. The N channel MOS transistor 5 and the P channel MOS transistor 13 constitute an inverting amplifier. The reference input voltage V_1 is applied from the terminal 8 to the negative input terminal of the differential amplifier 6.

The operation will be described in the following. Fig. 6 is a graph showing a general input/output

characteristics of the said inverting amplifier. At an intersection of a transfer curve L_1 and a line L_2 ($V_2=V_{out}$), the transfer curve L_1 inclines steeply. The value of this intersection is defined as an input threshold V_{BP}. It is well known that the input threshold V_{BP} has a close relation with the threshold of each transistor, which is represented by the following equation (8) (see, for example, "Principles of CMOS VLSI Design", Neil H. E. Weste et al, published by Addison-Wesley Publishing Company, p. 47).

$$V_{BP} = \frac{V_{DD} + V_{tP} + V_{tn}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \quad \ldots(8)$$

In the equation (8), the reference character V_{DD} represents a supply voltage, which corresponds to the potential of the terminal 14 with the terminal 3 being the reference in Fig. 5. The reference character V_{tn} represents the threshold voltage of the N channel MOS transistor, the reference character V_{tp} represents the threshold voltage of the P channel MOS transistor, and the reference characters β_n and β_p are constants.

In the case of the inverting amplifier 18 having the input portion and the output portion connected to each other as shown in Fig. 5, a balanced point of the circuit is given as the intersection of the transfer curve L_1 and the line L_2. Namely, the output of the inverting

amplifier 18 becomes the input threshold V_{BP} and it is inputted to the positive input terminal of the differential amplifier 6. If the input threshold V_{BP} is higher than the reference input voltage V_1, the control voltage V_0 outputted from the differential amplifier 6 becomes higher than when $V_{BP}=V_1$, and the threshold V_T of the N channel MOS transistor 5 becomes lower. Since the threshold V_{tn} of the N channel MOS transistor becomes lower in the equation (8), the input threshold V_{BP} also tends to be lower. On the contrary, if the input threshold V_{BP} is lower than the reference input voltage V_1, the control voltage V_0 outputted from the differential amplifier 6 becomes lower than when $V_{BP}=V_1$, and the input threshold V_{BP} becomes higher.

Since the differential amplifier 6 and the N channel MOS transistor 5 constitute a negative feed back loop as described above, the input threshold V_{BP} and the reference input voltage V_1 become equal to each other by the virtual grounding function.

If the N channel MOS transistors 1 and 5 and the P channel MOS transistors 12 and 13 have the same size, and if the inverting amplifiers 17 and 18 are designed to have the same input/output characteristics, the N channel MOS transistors 1 and 5 have the same source-backgate voltage V_{SB}, so that the inverting amplifiers 17 and 18 have the

same input threshold V_{BP}. More specifically, the input threshold V_{BP} determining whether the output V_{out} of the inverting amplifier 17 is at the "H" level or at the "L" level will be equal to the reference input voltage V_1 and the transfer curve L_1 of Fig. 6 corresponds to the reference input voltage V_1. An input threshold V_{BP} corresponding to the reference input voltage V_1 is set, the external input voltage V_2 is distinguished from the prescribed input threshold V_{BP}, and a signal of high level or low level is outputted from the output terminal 16 dependent on whether the external input voltage V_2 is larger than or smaller than the prescribed input threshold V_{BP}. Namely, the state of the inverting amplifier 17 is changed to output an "H" level signal or to output an "L" level signal, in accordance with a relation of magnitude between said input threshold and said external input voltage V_2.

The comparing means is formed by the said differential amplifier 6 shown in Fig. 5, which receives the reference input voltage and the feed back input voltage and compares the both input voltages to output a prescribed control voltage. Voltage responding means is formed by the said inverting amplifier 17 which has a predetermined first threshold, receives said control voltage from said comparing means and an external input

voltage, said first threshold controlled by said control voltage. The state of said voltage responding means is changed in accordance with a relation of magnitude between said first threshold and said external input voltage.

Threshold corresponding voltage output means is constituted by the said inverting amplifier 18 which has a predetermined second threshold, receiving said control voltage outputted from said comparing means for outputting a threshold corresponding voltage whose value corresponds to said second threshold, said second threshold being controlled by said control voltage while maintaining a prescribed relation with said first threshold of said voltage responding means. A feed back loop is formed by a closed loop including the said inverting amplifier 18, which feeds back the threshold corresponding voltage outputted from the said threshold corresponding voltage output means to the said comparing means as the feedback voltage for controlling the said control voltage such that the said fist threshold of the said voltage responding means converges to an aimed value.

The controlled threshold type electric device shown in Fig. 5 may be applied to a comparator which determines the magnitude of an inputted external input voltage based on an inputted reference input voltage to output the result of determination.

Fig. 7 is a circuit diagram showing an A/D converter. The parallel type A/D converter shown in Fig. 7 comprises a plurality of comparators 500 which receive reference input voltages $V"_1$, V_1, V'_1... from a reference voltage 504 and an external input voltage V_2 from an analog input portion 506 and compare the magnitude of the inputted voltages. The comparator 500 is formed by the said controlled threshold type electric device shown in Fig. 5. The parallel type A/D converter shown in Fig. 7 converts analog signals to digital signals. Namely, it takes an input analog signal at a certain timing and converts the voltage (current) value at that time into a digital value by a predetermined bit number. The parallel type A/D converter employs 2^{n-1} comparators for N bit quantization, as shown in Fig. 7. In case of 8 bit quantization, a voltage provided by dividing the reference voltage by means of $8^n - 1 = 255$ comparators in 1LSB unit is compared with the external input voltage V_2, and the result of comparison is converted into a 8 bit digital output by a decoder 502.

When the controlled threshold type electric device shown in Fig. 5 is used as a comparator as shown in Fig. 7, means for determining magnitude of the external input voltage is formed by the inverting amplifier 17 shown in Fig. 5, which has a predetermined logic determining

threshold, receives the said control voltage from the said comparing means and the external input voltage, and outputs the result of determination of the magnitude of the said external input voltage with the said logic determining threshold being a reference, with the said logic determining threshold being controlled by the said inputted control voltage.

Fig. 8 is a schematic diagram showing a further example of the controlled threshold type electric device in accordance with the present invention.

Referring to Fig. 8, the reference numeral 114 represents a P channel MOS transistor which is an example of a second voltage controlled current source and the reference numeral 115 represents an N channel MOS transistor which is an example of a first voltage controlled current source. The drains D of these transistors which are examples of the output portions thereof are connected to each other to provide an output terminal 112 of an inverting amplifier 101. The gate G which is an example of a driving control voltage input portion of the N channel MOS transistor 115 constitutes an input terminal 111 of the inverting amplifier 101, and the gate G which is an example of the driving voltage input portion of the P channel MOS transistor 114 constitutes a bias voltage input terminal 113 of the inverting amplifier

101. Similarly, a P channel MOS transistor 124 which is an example of the second voltage controlled current source and an N channel MOS transistor 125 which is an example of the first voltage controlled current source constitute an inverting amplifier 102, and the input terminal, the output terminal and the bias voltage input terminal are respectively formed of the terminals 121, 122 and 123.

The bias voltage input terminals 113 and 123 of the inverting amplifiers 101 and 102 are coupled together to an output portion of a differential amplifier 103 which is an example of the differential amplifying means. The input and output terminals 121 and 122 of the inverting amplifier 102 are coupled to a positive input terminal of the differential amplifier 103, and a signal from the inverting amplifier 102 is inputted to the said differential amplifier 103 as a feedback signal.

The reference input voltage V1 is inputted to a negative input terminal of the differential amplifier 103, and the external input voltage V_2 is inputted to the input terminal 111 of the said inverting amplifier 101.

The operation will be described in the following.

When the reference input voltage V_1 is inputted to the negative input terminal side of the differential amplifier 103, a signal provided by amplifying a difference between the reference input voltage V_1 and the

input voltage inputted to the positive input terminal side of the differential amplifier is inputted to the bias voltage input terminals of the said inverting amplifiers 101 and 102 as a control voltage V_0. In the both inverting amplifiers 101 and 102, the point at which the output voltage V_{out} changes largely in accordance with a slight change of the external input voltage V_2, that is, the input threshold, can be controlled by the magnitude of the said control voltage V_0, as described above.

A curve 403 shown in Fig. 9 shows the transfer curve of the inverting amplifiers 101 and 102. Since the P channel MOS transistors 114 and 124 are always conductive, the output voltage V_{out} is slightly higher than the ground voltage even if the external input voltage V_2 is high. Since the input and output terminals 121 and 122 of the inverting amplifier 102 are connected to each other, the potentials on the output terminal 122 and the input terminal 121 are provided at the intersection of the transfer curve 403 and the line on which the reference input voltage V_1= output voltage V_{out}, shown in Fig. 9. Therefore, the threshold voltage representing the input threshold of the inverting amplifier 102 is inputted to the positive input terminal of the differential amplifier 103. Meanwhile, since the bias voltage input terminal 123 of the inverting amplifier 102 is connected to the output

portion of the differential amplifier 103, a negative feed back loop is formed by the closed loop including the inverting amplifier 102. Therefore, the control voltage V_0 is controlled such that the voltages applied to the positive and negative input terminals of the differential amplifier 103 become equal to each other, by the virtual grounding function. More specifically, when the potential of the output terminal 122 is higher than the reference input voltage V_1, the control voltage V_0 is controlled such that the potential of the control voltage V_0 rises to reduce the bias current. Consequently, the potential of the output terminal 122 is lowered. If the potential of the output terminal 122 is lower than the reference input voltage V_1, the potential of the control voltage V_0 inputted to the bias voltage input terminal 123 decreases to increase the bias current. Consequently, the potential of the output terminal 122 is raised. Through these operations, the input threshold of the inverting amplifier 102 becomes equal to the reference input voltage V_1 inputted to the negative input terminal of the differential amplifier 103. Namely, as shown in Fig. 9, the coordinate of the intersection of the transfer curve 403 of the inverting amplifier 102 and the line on which $V_2 = V_{out}$ is represented by (V_1, V_1). As is apparent from Fig. 7, if the reference input voltage is V'_1 which is a

little smaller than V_1, the transfer curve of the inverting amplifier 102 will be the curve represented by two dotted lines in Fig. 9, and the threshold voltage from the inverting amplifier 102 converges to V'_1. If the reference input voltage is V''_1 which is a little larger than V_1, the transfer curve will be the curve represented by a chain dotted line of Fig. 9, and the threshold voltage from the inverting amplifier 102 converges to V''_1.

If the inverting amplifier 101 has the same transfer curve as the inverting amplifier 102, the input threshold of the inverting amplifier 101 converges to the same value as the reference input voltage V_1. Therefore, when the external input voltage V_2 applied to the input terminal 111 of the inverting amplifier 101 is larger than V_1 ($V_2 > V_1$), the output voltage V_{out} from the output terminal 112 sways from V1 to the negative direction in Fig. 9, and when $V_2 < V_1$, the output voltage V_{out} sways from V_1 to the positive direction in Fig. 9. In other words, the threshold which is the reference for determining the magnitude of the external input voltage V_2 can be controlled by the magnitude of the reference input voltage V_1, and therefore, the output voltage V_{out} of the inverting amplifier 101 is the result of comparison of V_1 with V_2 represented by a digital value.

By the said differential amplifier 103, the comparing means is formed which receives the reference input voltage and a feed back input voltage, compares the both input voltages to output a prescribed control voltage. Voltage responding means is formed by the said inverting amplifier 101 which has a predetermined first threshold and receives said control voltage from said comparing means and an external input voltage, said first threshold controlled by said control voltage. The state of said voltage responding means is changed in accordance with a relation of magnitude between said first threshold and said external input voltage. Threshold corresponding voltage output means is formed by the said inverting amplifier 102 which has a predetermined second threshold and receives said control voltage outputted from said comparing means for outputting threshold corresponding voltage whose value corresponds to said second threshold, said second threshold being controlled by said control voltage while maintaining a prescribed relation with said first threshold of said voltage responding means. In addition, a feed back loop is formed by the closed loop including the inverting amplifier 102 which feeds back the said threshold corresponding voltage outputted from the said threshold corresponding voltage output means to the said comparing means as the feed back voltage for controlling

the said control voltage such that the said first threshold of the said voltage responding logic state determining means converges to an aimed value.

The controlled threshold type electric device shown in Fig. 8 may be applied to a comparator 500 employing the A/D converter shown in Fig. 7 and the like. More specifically, each of the plurality of comparators 500 shown in Fig. 7 is formed by the controlled threshold type electric device shown in Fig. 8. The reference input voltage from the reference voltage 504 is inputted to the negative input terminal of the differential amplifier 103, and the external input voltage, which is an analog voltage inputted from an analog input portion 506 is inputted to the input terminal 111. Then, the output voltage V_{out} representing the result of determination of the magnitude of the external input voltage V_2 based on the input threshold is outputted from the output terminal 112. When the circuit shown in Fig. 8 is used as the comparator 500, the external input voltage magnitude determining means is formed by the inverting amplifier 101, which has a predetermined logic determining threshold, receives the said control voltage from the said comparing means and the external input voltage, and outputs the result of determination of the magnitude of the said external input voltage with the said logic determining threshold being

the reference, the said logic determining threshold being controlled by the said inputted control voltage.

Fig. 10 is a schematic diagram showing an improvement of the controlled threshold type electric device shown in Fig. 8. The circuit of Fig. 10 is capable of enlarging the gain of the inverting amplifier (101) shown in Fig. 8. In that controlled threshold type electric device shown in Fig. 10, inverting amplifiers 101 and 102 respectively comprise first voltage controlled current sources 115 and 125 and second voltage controlled current sources 114 and 124. The first voltage controlled current sources 115 and 125 respectively comprise N channel MOS transistors 115a and 125a and P channel MOS transistors 115b and 125b. The second voltage controlled current sources 114 and 124 respectively comprise P channel MOS transistors 114a and 124a and 114b and 124b. The structure of Fig. 10 is the same as that of Fig. 8 except that the voltage controlled current source is formed by a single transistor in the circuit of Fig. 8 while the voltage controlled current source of Fig. 10 is formed by a plurality of transistors. Therefore, the detailed description thereof will be omitted. The controlled threshold type electric device shown in Fig. 10 may be employed as the comparator 500 for the A/D converter shown in Fig. 7, and the like.

Although the voltage responding means or the means for determining magnitude of the external input voltage and the threshold voltage output means have the same response characteristics in the present embodiment, the present invention is not limited to this, and it is effective provided that the said first threshold and the said second threshold are controlled while maintaining a prescribed relation by the control voltage. Although the bias current generating side are formed of P channel MOS transistors and the driving current generating side are formed of N channel MOS transistors in Figs. 8 and 10, the transistors of opposite conductivities may be employed for respective sides, and transistors other than MOS transistors, such as bipolar transistors and JFETs may be employed. In addition, passive elements may be included in the voltage controlled current source in Figs. 8 and 10.

As described above, in the present invention, even if the first threshold of the voltage responding means is changed by influences such as heat after fabrication, the threshold corresponding voltage output means also receives the same influences and therefore the threshold corresponding voltage, that is, the amount of control is changed. Therefore, a control voltage, that is, a control operation signal which makes the amount of change of the

threshold corresponding voltage, namely, the control deflection to be 0 is outputted from the comparing means, so that the first threshold of the voltage responding means is modified and maintained at the aimed value. Therefore, the fluctuation of the first threshold of the voltage responding means caused not only by the differences of various parameters in manufacturing but also by influences after fabrication such as heat during use can be prevented, whereby a controlled threshold type electric device capable of appropriately controlling the first threshold can be provided.

According to a preferred embodiment of the present invention, even if the threshold of the second transistor is changed by the influence such as heat after fabrication, the first transistor is also influenced and the threshold corresponding voltage, that is, the amount of control, is changed, the negative feed back loop functions such that the amount of change of the threshold corresponding voltage, that is, the control deflection becomes 0, whereby the threshold of the second transistor is modified and maintained at the aimed value. Therefore a controlled threshold type electric device can be provided which is capable of preventing fluctuation of the threshold of transistors caused not only by differences of various parameters during manufacturing but by influences

after fabrication such as heat during used and capable of appropriately controlling the threshold.

According to the comparator of the present invention, if an external input voltage is inputted to means for determining the magnitude of the external input voltage having the logic determining threshold converged to an aimed value, an accurate result of determination is outputted based on the logic determining threshold which is adjusted at the appropriate value, whereby a comparator capable of providing precise results of determination can be provided.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A controlled threshold type electric device comprising:

comparing means (6, 103) for receiving a reference input voltage (V_1) and a feed back input voltage and for comparing the both input voltages to output a prescribed control voltage (V_0);

voltage responding means (1, 10, 17, 101) having a predetermined first threshold for receiving said control voltage (V_0) from said comparing means (6, 103) and an external input voltage (V_2), said first threshold controlled by said control voltage (V_0), the state of said voltage responding means (1, 10, 17, 101) changed in accordance with a relation of magnitude between said first threshold and said external input voltage (V_2), and

threshold corresponding voltage outputting means (5, 11, 18, 102) having a predetermined second threshold, receiving said control voltage (V_0) outputted from said comparing means (6, 103) for outputting a threshold corresponding voltage whose value corresponds to said second threshold, said second threshold being controlled by said control voltage (V_0) while maintaining a prescribed relation with said first threshold of said voltage responding means (1, 10, 17, 101), said threshold

corresponding voltage fed back as said feed back voltage to said comparing means (6, 103), whereby a feed back loop toward said comparing means is formed by said threshold corresponding voltage outputting means (6, 103), and said control voltage (V_0) is controlled such that said first threshold of said voltage responding means (1, 10, 17, 101) converges to an aimed value.

2. A controlled threshold type electric device according to claim 1, wherein

said threshold corresponding voltage output means (5, 11, 18, 102) has a second threshold which is controlled by said control voltage (V_0) while maintaining the same value as the first threshold of said voltage responding means (1, 10, 17, 101).

3. A controlled threshold type electric device according to claim 1, wherein said comparing means (6, 103) comprises differential amplifying means (6, 103) for amplifying a difference between two input voltages to output the same.

4. A controlled threshold type electric device according to claim 1, wherein

said threshold corresponding voltage output means (102) comprises:

first and second voltage controlled current sources (125, 124) each comprising a control voltage input portion and an output portion (D) for outputting a current whose magnitude is controlled by a voltage applied to said control voltage input portion (G);

a threshold corresponding voltage output terminal (122) connected to said control voltage input portion (G) of said first voltage controlled current source (125) and to respective said output portions (D) of said first and second voltage controlled current sources (125, 124) for outputting said threshold corresponding voltage; and

a bias voltage input terminal (125) connected to said control voltage input portion (G) of said second voltage controlled current source (124) for inputting said control voltage (V_0) from said comparing means (103) as a bias voltage.

5. A controlled threshold type electric device according to claim 1, wherein said voltage responding means (101) comprises:

first and second voltage controlled current sources (115, 114) each comprising a control voltage input portion (G) and an output portion (D) for outputting a current

whose magnitude is controlled by a voltage applied to said control voltage input portion (G);

an input terminal (111) connected to said control voltage input portion (G) of said first voltage controlled current source (111) for receiving said external input voltage;

an output terminal (112) connected to respective said output portions (D) of said first and second voltage controlled current sources (115, 114) for outputting, in response to said external input voltage (V_2), an output voltage (V_{out}) having a first or second logic state determined in association with said first threshold; and

a bias voltage input terminal (113) connected to said control voltage input portion (G) of said second voltage controlled current source (114) for inputting said control voltage V_0 from said comparing means (103) as a bias voltage.

6. A controlled threshold type electric device according to claim 5, wherein

said first voltage controlled current source (115) comprises a first transistor (115) of a certain conductivity type and said second voltage controlled current source (114) comprises a second transistor (114) of an opposite conductivity type to said first transistor.

7. A controlled threshold type electric device comprising:

a first transistor (5, 11) having first and second control electrodes (G, B) and first and second conductive terminals (D, S) said first control electrode (G) connected to said first conductive terminal (D) and said second conductive terminal (S) supplied with a prescribed voltage;

a second transistor (1, 10) having first and second control electrodes (G, B) and first and second conductive terminals (D, S), said second conductive terminal (S) supplied with a prescribed voltage, said second control electrode (B) connected to the second control electrode (B) of said first transistor (5, 11);

current supplying means (7) for supplying current to the first conductive terminal (G) of said first transistor (5, 11); and

differential amplifying means (6) having a first input terminal connected to said first conductive terminal (G) of said first transistor (5, 11) and a second input terminal receiving a reference input voltage, for applying an output to the second control electrode (B) of said first and second transistors (5, 11, 1, 10) ;

whereby a negative feed back loop toward said differential amplifying means (6) is formed by said first transistor (5, 11).

8. A comparator receiving a reference input voltage (V_1) and an external input voltage (V_2) for determining magnitude of said external input voltage (V_2) based on said reference input voltage (V_1) to output a result of determination, comprising:

comparing means (6, 103) receiving said reference input voltage (V_1) and a feed back input voltage, for comparing the both input voltages to output a prescribed control voltage;

means for determining magnitude of the external input voltage (17, 101) having a predetermined logic determining threshold, for receiving said control voltage (V_0) from said comparing means (6, 103) and the external input voltage (V_2) and for outputting a result of determination of the magnitude of said external input voltage (V_2) with said logic determining threshold being a reference, with said logic determining threshold being controlled by said inputted control voltage (V_2); and

threshold corresponding voltage output means (18, 102) having a predetermined threshold, receiving said control voltage (V_0) outputted from said comparing means

(6, 103) for outputting a threshold corresponding voltage whose value corresponds to said threshold, said threshold being controlled by said control voltage (V_0) while maintaining a prescribed relation with said logic determining threshold of said means for determining magnitude of said external input voltage (17, 101), and for feeding back said threshold corresponding voltage to said comparing means (6, 103) as said feed back voltage; whereby said feed back loop toward said comparing means (6, 103) is formed by said threshold corresponding voltage output means (18, 102) and said control voltage is controlled such that said logic determining threshold of said means for determining magnitude of said external input voltage (17, 101) converges to an aimed value.

9. A comparator according to claim 8, wherein said threshold corresponding voltage output means (18, 102) has a threshold which is controlled by said control voltage (V_0) while maintaining the same value as the logic determining threshold of said means for determining magnitude of the external input voltage (17, 101).

10. A comparator according to claim 8, wherein said comparing means (6, 103) comprises differential amplifying

means (6, 103) for amplifying a difference between two input voltages to output the same.

11. A comparator according to claim 8, wherein said threshold corresponding voltage output means (102) comprises:

first and second voltage controlled current sources (125, 124) each having a control voltage input portion (G) and an output portion (D) for outputting a current whose magnitude is controlled by a voltage applied to said control voltage input portion (G);

a threshold corresponding voltage output terminal (122) connected to said control voltage input portion (G) of said first voltage controlled current source (125) and to respective said output portions (D) of said first and second voltage controlled current sources (125, 124) for outputting said threshold corresponding voltage; and

a bias voltage input terminal (123) connected to said control voltage input portion (G) of said second voltage controlled current source (124) for inputting said control voltage from said comparing means (103) as a bias voltage.

12. A comparator according to claim 8, wherein said means for determining magnitude of the external input voltage (101) comprises:

first and second voltage controlled current sources (115, 114) each comprising a control voltage input portion (G) and an output portion (D) for outputting a current whose magnitude is controlled by a voltage applied to said control voltage input portion (G);

an input terminal (111) connected to said control voltage input portion (G) of said first voltage controlled current source (115) to receive said external input voltage (V_2);

an output terminal (112) connected to respective said output portions (D) of said first and second voltage controlled current sources (115, 114) for outputting an output voltage of said first or second logic state; and

a bias voltage input terminal (113) connected to said control voltage input portion (G) of said second voltage controlled current source (114) for inputting said control voltage (V_0) from said comparing means (103) as a bias voltage.

13. A comparator according to claim 12, wherein

said first voltage controlled current source (115) comprises a first transistor (115) of a certain conductivity type, and said second voltage controlled current source (114) comprises a second transistor (114) of an opposite conductivity type to said first transistor.

14. A controlled threshold device having:

a first means which receives an input signal and a first control signal, and provides an output signal in accordance with the relationship between the input signal and a threshold value, the said threshold value of the first means being determined in accordance with the first control signal;

a second means, which receives the first control signal and provides a feedback signal in accordance with a threshold value, the said threshold value of the second means being determined in accordance with the first control signal; and

a third means, which receives the feedback signal and a second control signal and provides the first control signal in accordance with the feedback signal and the second control signal.

15. A controlled threshold device substantially as herein described with reference to Figures 1 to 6, 8 and 9 of the accompanying drawings.

16. A comparison device substantially as herein described with reference to Figures 1 to 6, 8, 9, and 13 to 15 of the accompanying drawings.

17. An analogue-to-digital converter

substantially as herein described with reference to Figures 1 to 9 and 13 to 15 of the accompanying drawings.

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