

[54] ALARM SYSTEM HAVING PULSE PAIR CODING

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[22] Filed: May 26, 1972

[21] Appl. No.: 257,307

[52] U.S. Cl. 340/164 R, 340/167 A, 340/167 B, 340/167 R

[51] Int. Cl. H04q 5/14

[58] Field of Search 340/168 R, 167 R, 167 A, 340/167 B, 147 PC, 171 R, 164 R; 325/41, 42; 328/109, 110, 111

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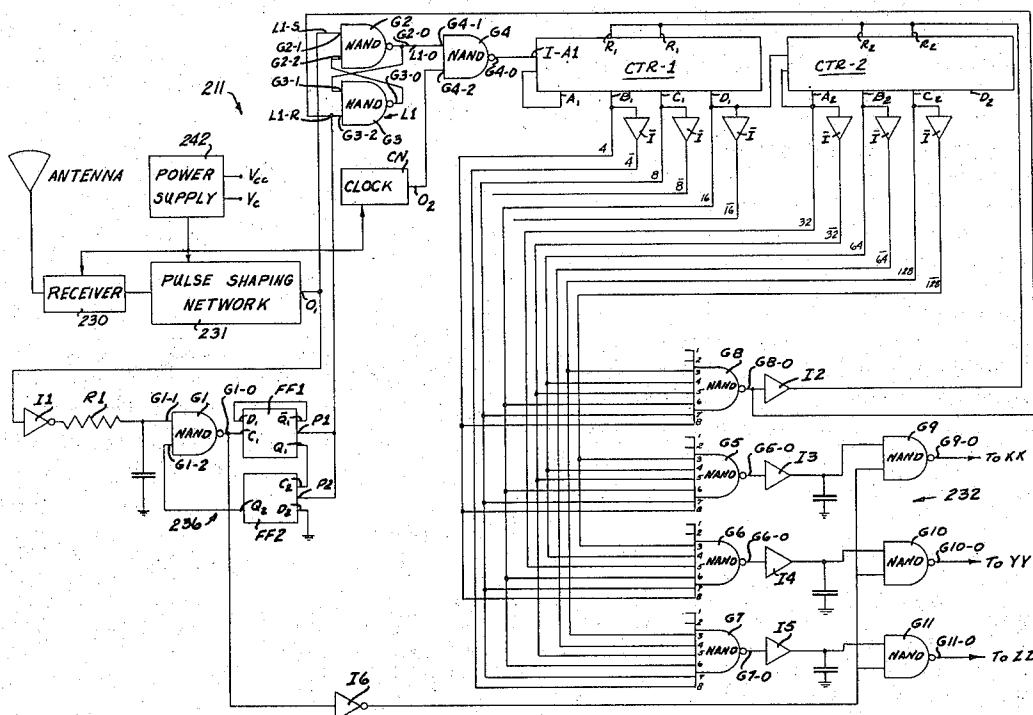
Attorney, Agent, or Firm—B. J. Powell

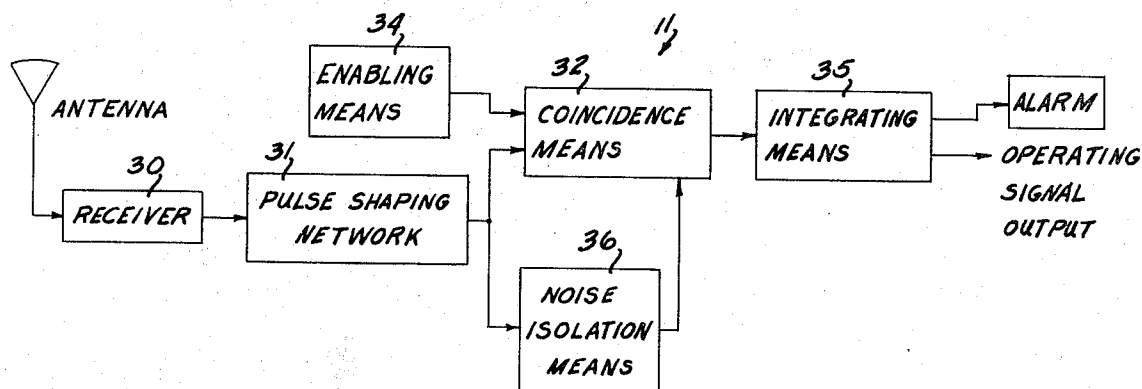
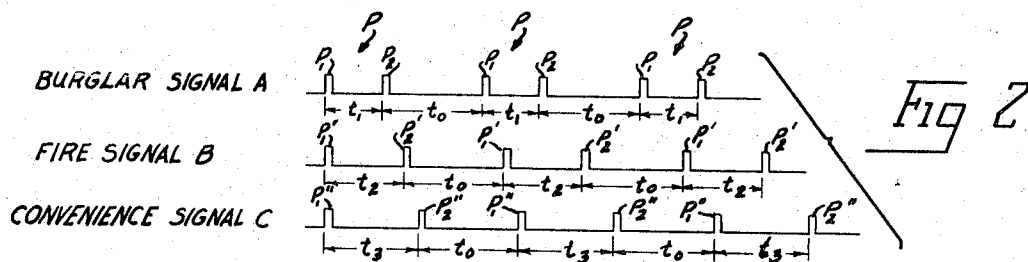
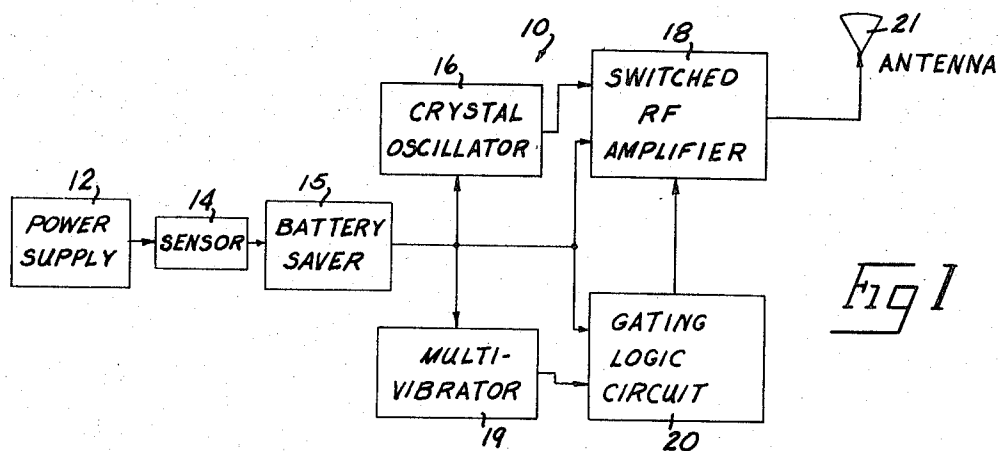
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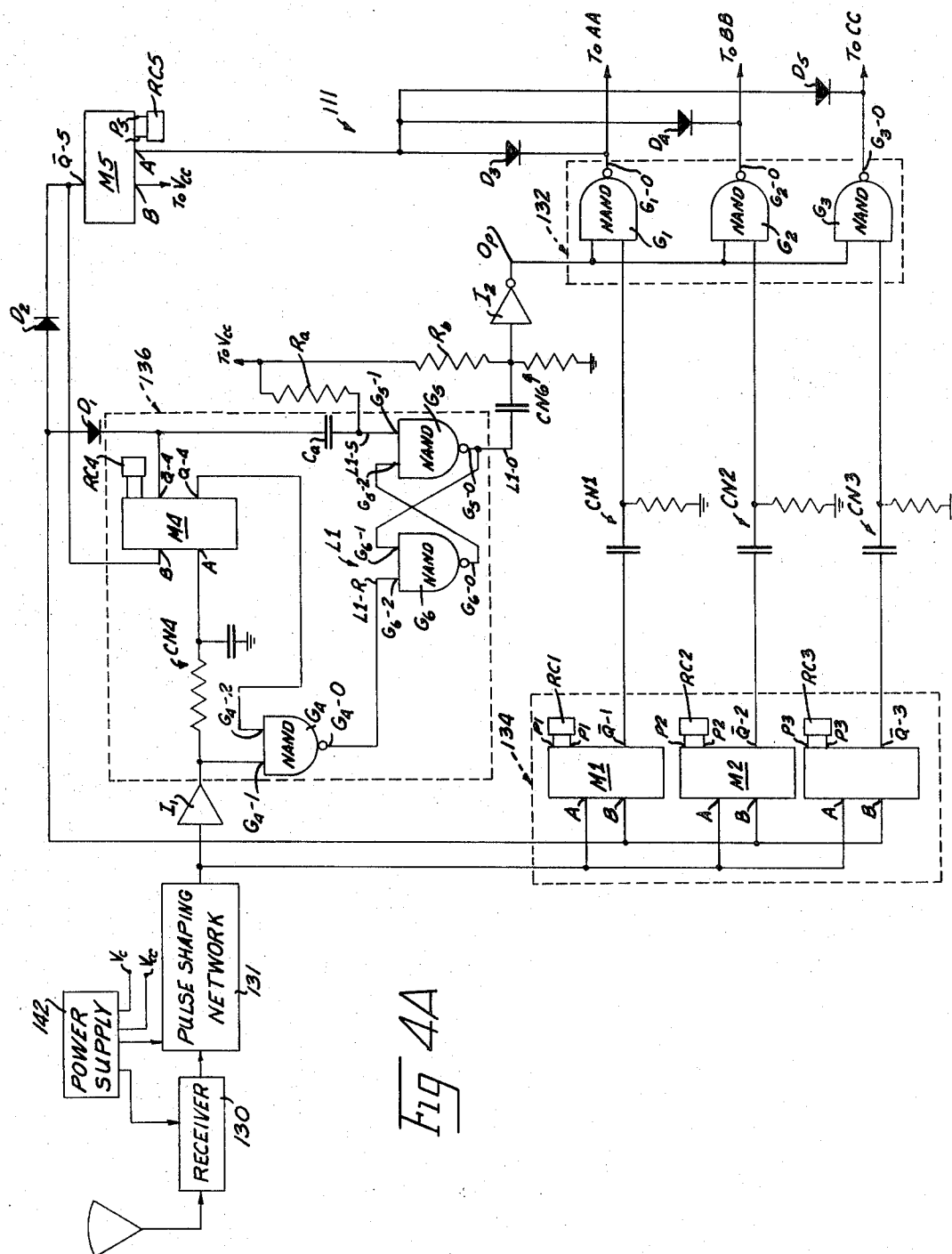
ABSTRACT

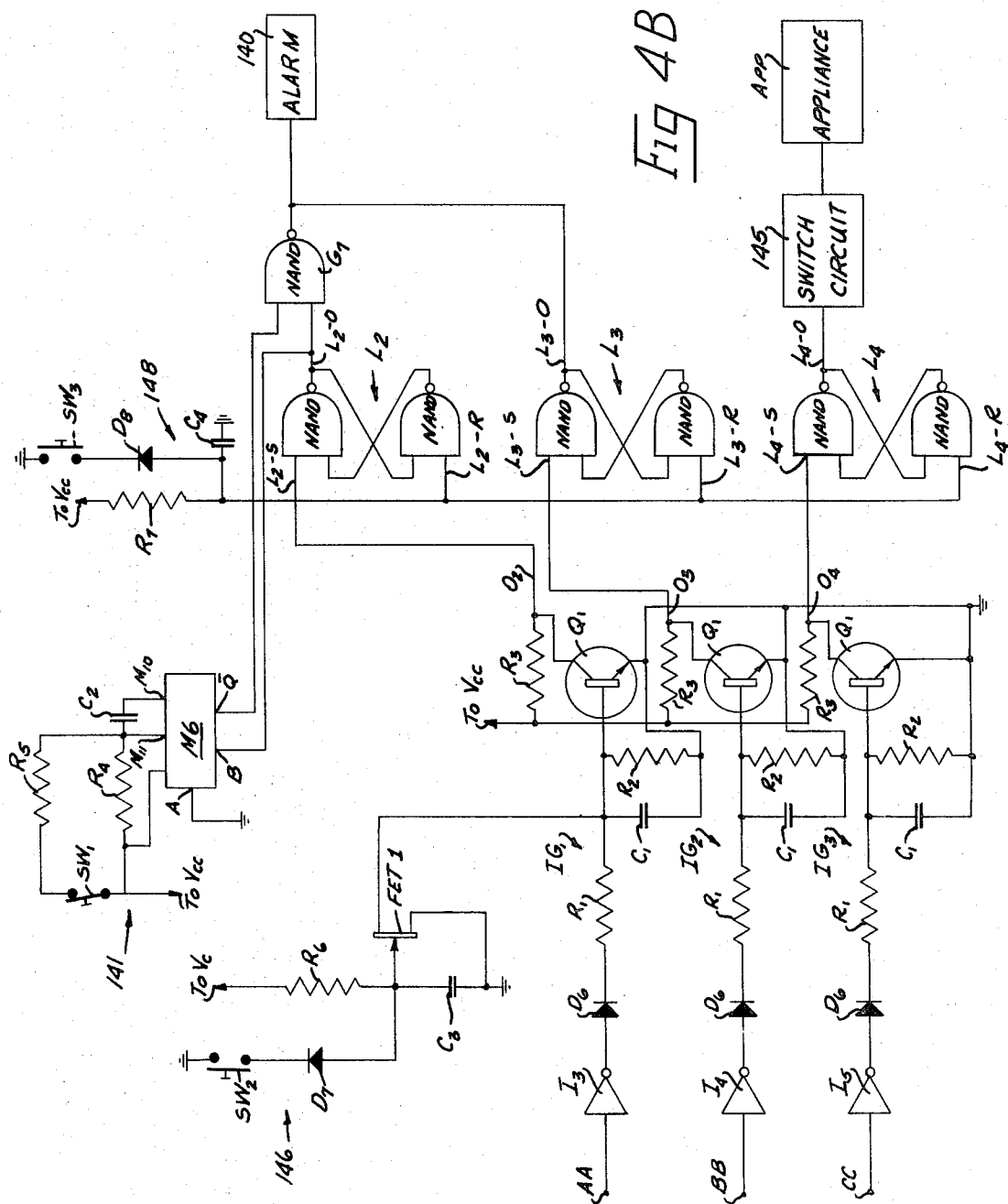
An alarm system including generally a transmitter for generating a predetermined signal of pulse pairs in response to the occurrence of a preconceived condition; and a receiver for receiving the signal generated by the transmitter. The receiver detects the pulsed RF signal from the transmitter, generates the proper pulse signal in response thereto, compares the generated signal to a standard reference signal generated by the receiver and generates an alarm or operating signal when a predetermined number of coincidences between the received signal and the standard reference signal occur. In both the analog and digital embodiments, the receiver includes a radio frequency receiver for detecting an RF signal and generating a corresponding signal output, a pulse shaping network for shaping the signal output from the receiver, coincidence means for receiving the pulse signal output from the pulse shaping network, enabling means for selectively enabling the coincidence means to generate an output in response to the receipt of the pulse signal from the pulse shaping network, integrating means for generating an alarm or operating signal output in response to receipt of a predetermined number of outputs within a predetermined time interval from the coincidence means, and noise isolation means for preventing the generation of an alarm signal as the result of a noise signal.

12 Claims, 10 Drawing Figures









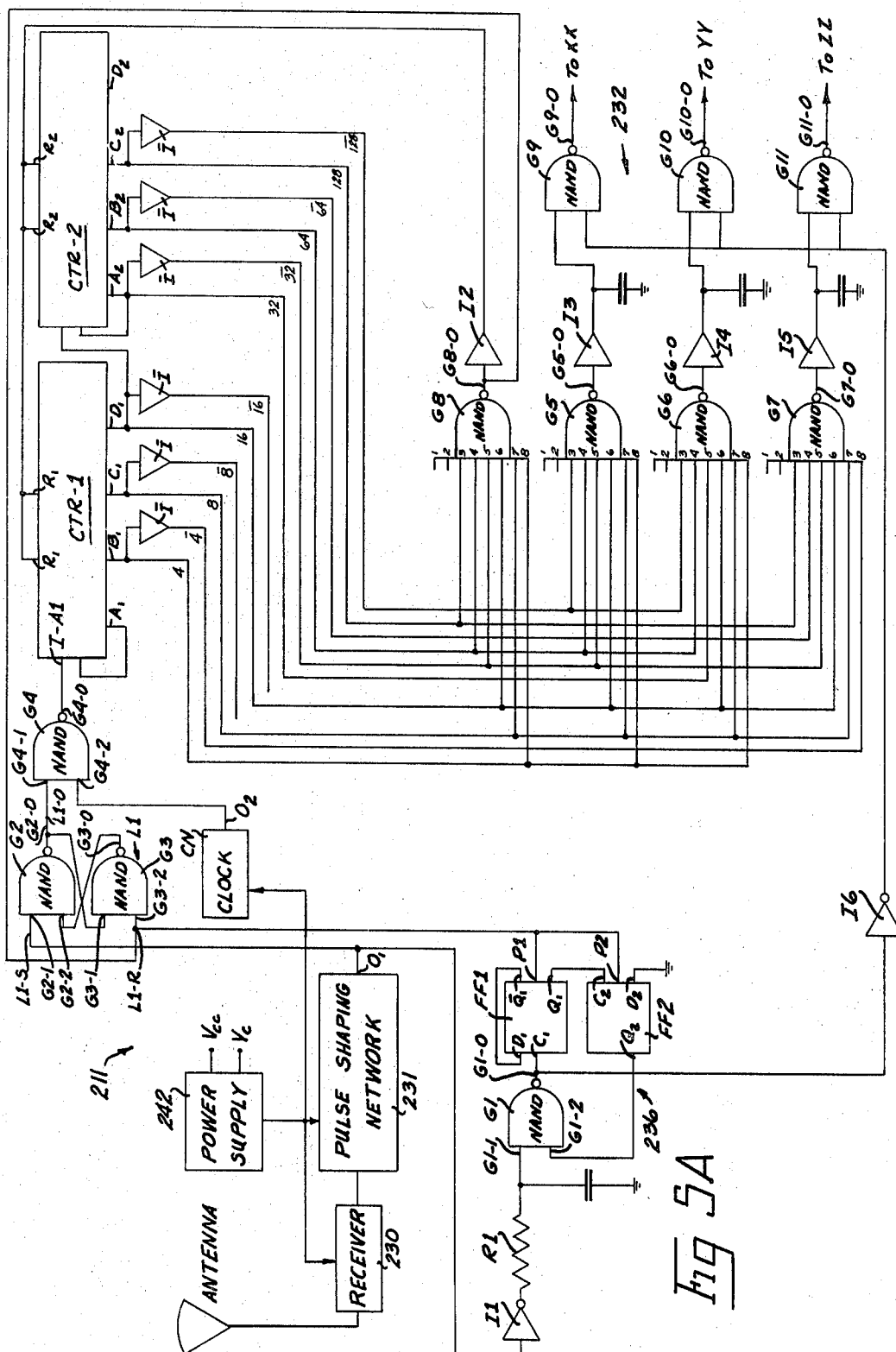
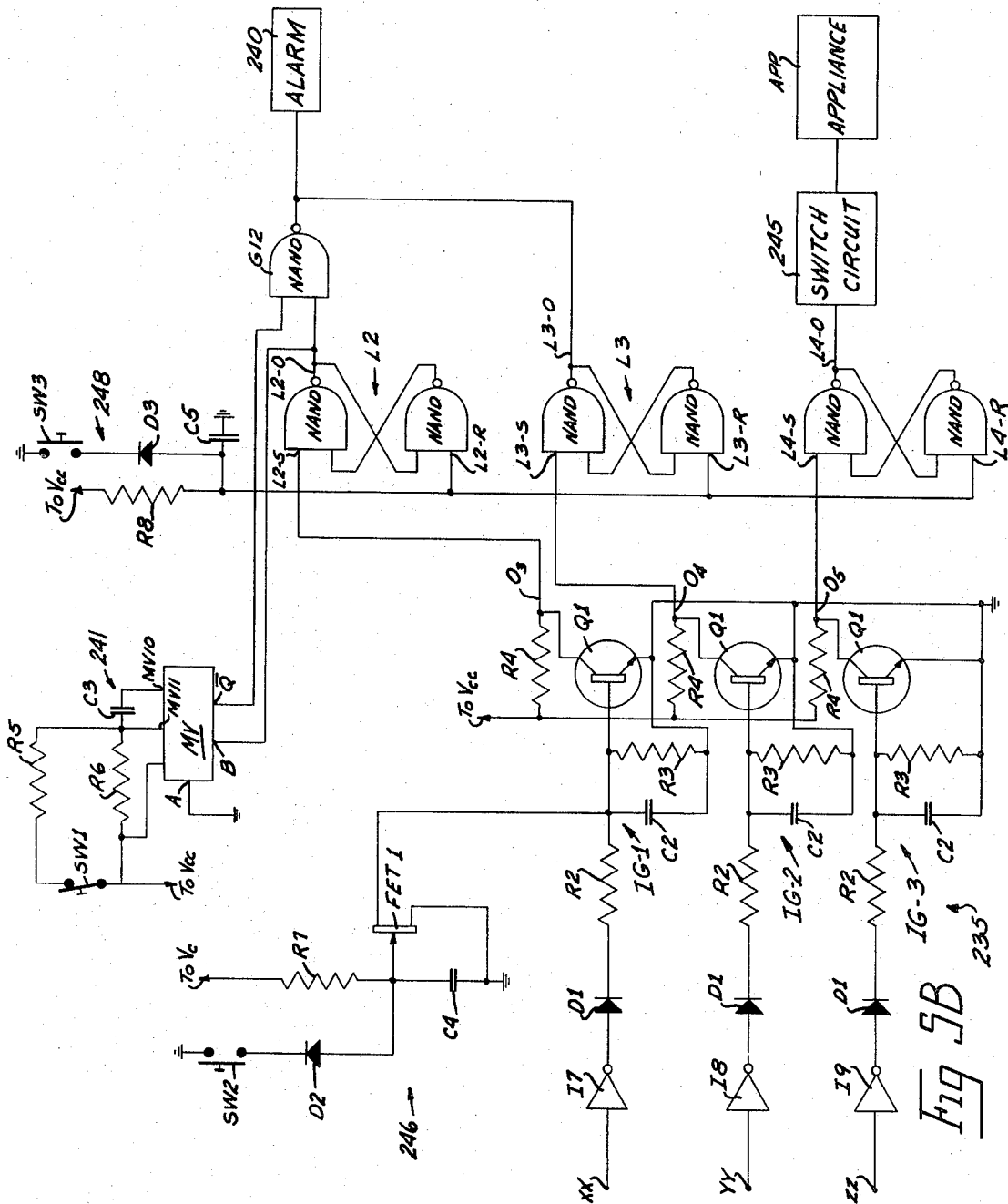
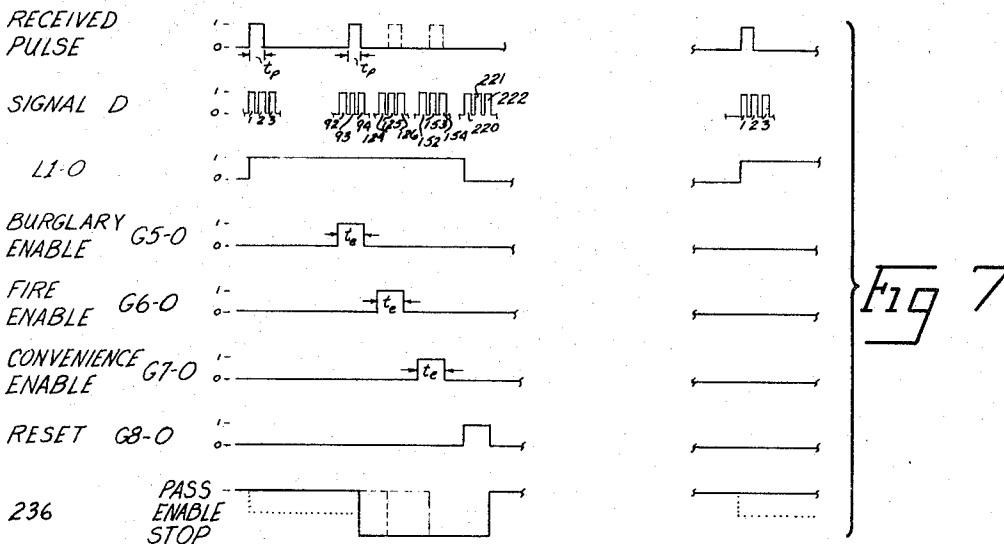
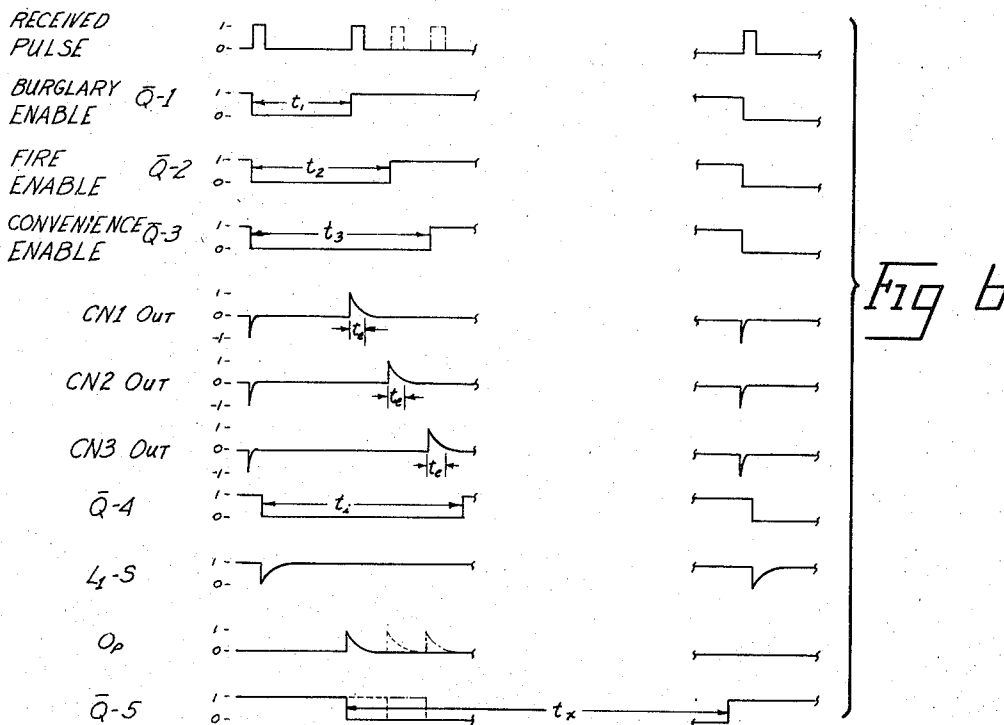
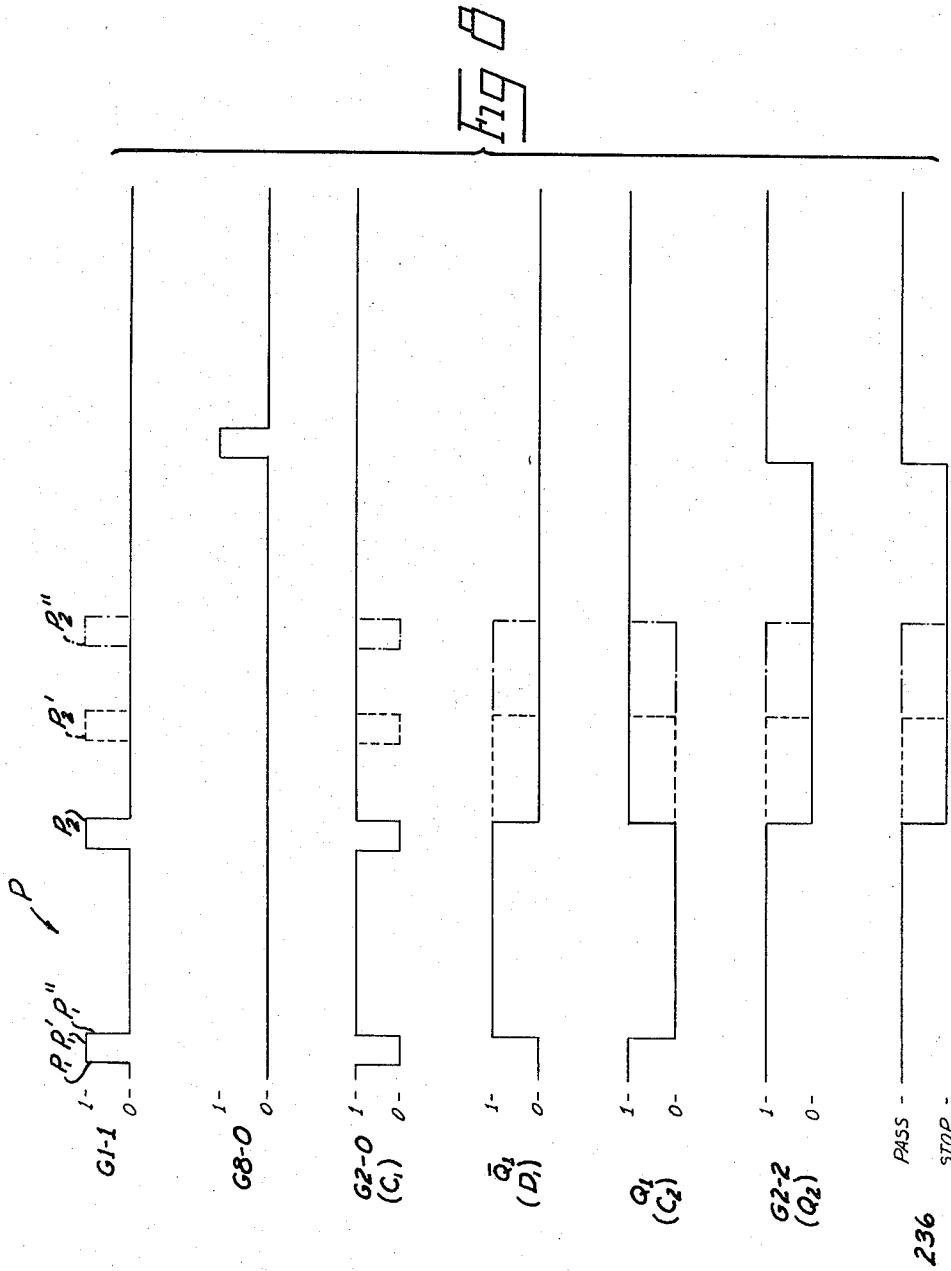


Fig 5A







ALARM SYSTEM HAVING PULSE PAIR CODING

BACKGROUND OF THE INVENTION

Various alarm systems to detect intruders, fire and other conditions are on the market today. Such systems are generally of the wired or wireless type. The major disadvantages of the wired type system is that installation cost of the wiring for the system is prohibitive, especially for small users, and that the system can be rendered useless by severing the wires. While the wireless systems have eliminated the wiring problem, such systems have been subject to frequent false alarms because of the normally encountered noise signals received by the receiver.

SUMMARY OF THE INVENTION

These and other problems associated with the prior art alarm systems are overcome by the invention disclosed herein by providing a wireless alarm system that virtually eliminates the false alarms normally associated with prior art systems. Moreover, the system is responsive to different signals to distinguish as to the particular condition detected. The system also tends to search for the particular alarm signal once the signal is detected.

The apparatus of the invention includes generally a transmitter for generating a predetermined signal of pulse pairs in response to the occurrence of a preceived condition; and a receiver for receiving the signal generated by the transmitter, comparing this signal to a standard signal generated within the receiver and generating an alarm signal in response to a predetermined number of matches between the received signal and the standard signal. The system also includes noise reject means that prevents activation of the system by signals other than the signals from the transmitters.

The transmitter includes a power supply, a sensing device for generating a signal in response to the occurrence of a certain condition such as the opening of a door or window by a burglar or the occurrence of a certain temperature indicating a fire or the closing of a switch manually to remotely operate a piece of equipment, a battery saver device for deactivating the power supply after a predetermined period of time, a crystal oscillator circuit for generating an RF carrier wave, a switched RF amplifier for generating a radio frequency output signal, a multivibrator for generating a predetermined amplitude signal, a gating logic circuit for connecting the output of the multivibrator to the switched RF amplifier to generate an RF output signal having pulse pairs with a predetermined time interval between the first generated pulse and the second generated pulse.

The receiver detects the pulsed RF signals from the transmitter, generates the proper pulse signal in response thereto, compares the generated signal to a standard reference signal generated by the receiver and generates an alarm or operating signal when a predetermined number of coincidences between the received signal and the standard reference signal occur. In both the analog and digital embodiments, the receiver includes a radio frequency receiver for detecting an RF signal and generating a corresponding signal output, a pulse shaping network for shaping the signal output from the receiver, coincidence means for receiving the pulse signal output from the pulse shaping network, en-

abling means for selectively enabling the coincidence means to generate an output in response to the receipt of the pulse signal from the pulse shaping network, integrating means for generating an alarm or operating signal output in response to receipt of a predetermined number of outputs within a predetermined time interval from the coincidence means, and noise isolation means for preventing the generation of an alarm signal as the result of a noise signal.

These and other features and advantages of the invention disclosed herein will become more apparent upon consideration of the following specification and accompanying drawings wherein like characters of reference designate corresponding parts throughout the several views and in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the transmitter of the invention;

FIG. 2 is a chart showing the relationship between the coded pulse pair signals generated by the transmitters;

FIG. 3 is a schematic diagram for the receiver of the invention;

FIGS. 4A and 4B are detailed schematic diagrams of the analog embodiment of the receiver;

FIGS. 5A and 5B are detailed schematic diagrams of the digital embodiment of the receiver;

FIG. 6 shows the output waveforms of the various components of the analog embodiment of the invention;

FIG. 7 shows the output waveforms of the various components of the digital embodiment of the invention; and,

FIG. 8 shows the output waveforms of the various components of the noise isolation means of the digital embodiment of the invention.

These figures and the following detailed description disclose specific embodiments of the invention, however, it is to be understood that the inventive concept is not limited thereto since it may be embodied in other forms.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Referring to the figures, it will be seen that the invention includes a transmitter 10 and receiver 11. The system is designed to operate on a separate code for each particular type of occurrence that is to be sensed. The system shown has three separate codes, one for fire, one for burglary, and one for convenience. The transmitters 10 generate a radio frequency signal having pulse pairs with a prescribed time interval between the first generated pulse and the second generated pulse and a prescribed time interval between pulse pairs. To generate a different code, the time interval between the pulses of the pairs is changed while the time interval between pulse pairs remains the same so that sensing of the particular code can be easily achieved. FIG. 2 illustrates the different signals for the codes and compares these signals to show that the time interval between the first generated pulse and the second generated pulse is different for each particular code.

Referring to FIG. 2, it will be seen that the first coded signal is a burglary code and is identified as signal A, the second coded signal is a fire code and is identified as signal B, and the third coded signal is a convenience

code identified as signal C. Each of the signals uses pulse pairs P to generate the code. The coding is accomplished by varying the time interval between the pulses of each pulse pair while the time intervals between pulse pairs remains the same. The first generated pulse of each pulse pair is designated P_1 for signal A, P_1' for signal B and P_1'' for signal C and the second generated pulse of each pulse pair is designated P_2 for signal A, P_2' for signal B and P_2'' for signal C. The time interval between the first generated pulse P_1 and the second generated pulse P_2 for the signal A is designated t_1 , t_2 for signal B, and t_3 for signal C. It will be noted that time t_2 is greater than time t_1 and time t_3 is greater than time t_2 . The time intervals t_1 , t_2 , and t_3 can be selectively varied to match the particular coding requirements for each particular location and prevent alarm signal generation in response to a similar system in the vicinity. The time interval t_0 between the pulse pairs P of each signal remains the same. It will also be noted that the time interval t_0 is always greater than time intervals t_1 , t_2 or t_3 but less than 2 times the time intervals t_1 , t_2 or t_3 to facilitate encoding as will be apparent.

The transmitter 10 as seen in FIG. 1 includes a power source 12, usually a battery, a sensing switch 14, a battery saver circuit 15 connected to the power source 12 through sensing switch 14, a crystal oscillator 16 connected to the battery saver circuit 15, a switched RF amplifier 18 connected to the output of the oscillator 16 and battery saver circuit 15, a multivibrator 19 connected to battery saver circuit 15, a gating logic circuit 20 connected to the output of multivibrator 19 and battery saver circuit 15 and having its output connected to the amplifier 18, and a transmitting antenna 21 connected to the output of amplifier 18 for transmitting the pulsed RF signal. The sensing switch 14 may be any of a number of commercially available switches that are activated in response to a preconceived condition such as entry to the premises or fire or a standard manually operable switch. The particular kind of switch 14 selected, of course, depends on the particular condition to be detected.

Closing of the sensing switch 14 connects the power source 12 to the other components of the transmitter to energize same. This causes the oscillator 16 to generate an RF carrier wave in known manner and the multivibrator to generate a pulse signal. This causes the amplifier 18 to transmit a pulsed RF signal to receiver 11. The RF signal is coded according to one of the signals A, B or C shown in FIG. 2 in known manner for the proper detection of the condition at the transmitter to take place as will become apparent.

After a predetermined period of time, the battery saver circuit 15 automatically disconnects the power source 12 from the other components of the transmitter. The predetermined period of time is sufficient to cause the receiver to set off an alarm, however.

The receiver 11 as seen in FIG. 3 detects the pulsed RF signal from the transmitter 10, generates the proper pulse signal A, B or C in response thereto, compares the generated signal A, B or C to a standard reference signal generated by the receiver 11 and generates an alarm or operating signal when a predetermined number of coincidences between the received signal and the standard reference signal occur. Generally, the receiver 11 includes a radio frequency receiver 30 for detecting an RF signal and generating a corresponding signal output, a pulse shaping network 31 for shaping

the signal output from the receiver 30, coincidence means 32 for receiving the pulse signal output from the network 31, enabling means 34 for selectively enabling the coincidence means 32 to generate an output in response to the receipt of the pulse signal from network 31, integrating means 35 for generating an alarm or operating signal output in response to receipt of a predetermined number of outputs within a predetermined time interval from the coincidence means, and noise isolation means 36 for preventing the generation of an alarm signal as the result of a noise signal.

The analog embodiment of the receiver is illustrated in FIGS. 4A and 4B and designated 111 while the digital embodiment of the receiver is illustrated in FIGS. 5A and 5B and designated 211. The components of receiver 111 corresponding to receiver 11 have the reference numerals of receiver 11 applied thereto displaced by 100 and the components of receiver 211 corresponding to receiver 11 have the reference numerals of receiver 11 applied thereto displaced by 200.

ANALOG EMBODIMENT

Referring generally to FIGS. 4A and 4B, the receiver 111 of the analog version of the invention includes the conventional radio frequency receiver 130 for detecting an RF signal and generating a corresponding signal output, and the conventional pulse shaping network 131 for shaping the signal output from receiver 130 as previously described. If one of the signals A, B or C is received by the receiver 130, corresponding signals A, B or C will be generated at the output O_1 of the network 131.

The output O_1 is connected three monolithic transistor-transistor logic multivibrators M1, M2 and M3 with d-c triggering and inhibit capabilities. Such multivibrators are commercially available under part number SN 74121 manufactured by Texas Instruments, Inc. of Dallas, Texas. The output O_1 is connected to the logic inputs A of each multivibrator M1, M2 and M3. These multivibrators M1-M3 form the enabling means 134 of the receiver 111.

The timing pins P1 of multivibrator M1 are connected to the external timing circuit RC1 of known construction to cause the activated time of multivibrator M1 to correspond to time interval t_1 of the signal A. In like manner, the timing pins P2 of multivibrator M2 are connected to the external timing circuit RC2 to cause the activated time of multivibrator M2 to correspond to the time interval t_2 of signal B. Also, the timing pins P3 of multivibrator M3 are connected to the external timing circuit RC3 to cause the activated time of multivibrator M3 to correspond to time interval t_3 of signal C.

The output $\bar{Q}-1$ of multivibrator M1 is connected to one input of a burglary NAND gate G_1 in the coincidence means 132 through an RC coupling network CN1 of known construction. The output $\bar{Q}-2$ of multivibrator M2 is likewise connected to one input of a fire NAND gate G_2 in the coincidence means 132 through an RC coupling network CN2. Also, the output $\bar{Q}-3$ of multivibrator M3 is connected to one input of a convenience NAND gate G_3 in the coincidence means 132 through an RC coupling network CN3.

The output O_1 is also connected to the logic inputs A of a multivibrator M4 like multivibrator M1 through an inverter I_1 and the RC coupling network CN4 of known construction and also to one input G_4-1 of a noise isola-

tion NAND gate G_4 in the noise isolation means 136 through the inverter I_1 . The output $\bar{Q}$ -4 of multivibrator M4 is connected to the inhibit inputs B of each multivibrator M1, M2 and M3 through diode D_1 and to the set input L₁-S of a two gate latch L_1 of known construction using two NAND gates G_5 and G_6 through the coupling capacitor C_n of known construction. The Q-4 output is connected to the other input G_4 -2 of gate G_4 . The timing pins P4 of multivibrator M4 are connected to an external timing circuit RC4 of known construction designed to cause the multivibrator M4 to time out in a time interval greater than the time interval between any pair of pulses in signals A, B or C, here shown as time interval t_3 yet less than the time interval t_0 between pulse pairs.

Input L₁-S of latch L_1 is also connected to voltage source V_{cc} of power supply 142 through resistor R_n . Input L₁-S is the input G_5 -1 of gate G_5 and its output G_5 -0 is connected to the input G_6 -1 of gate G_6 . The output G_5 -0 is the latch output L₁-0. The reset input L₁-R which is input G_6 -2 of gate G_6 is connected to output G_4 -0 of gate G_4 . The output L₁-0 of latch L_1 is connected to the enabling inputs of gates G_1 - G_3 through an RC coupling network CN6 of known construction and an inverter I_2 . The enabling inputs G_1 -1, G_2 -1 and G_3 -1 of gates G_1 - G_3 are also connected to the voltage source V_{cc} through resistor R_n and inverter I_2 . The outputs Q-1, Q-2, and Q-3 selectively enable gates G_1 - G_3 so that they will change state if coincidence occurs between output L₁-0 and outputs Q-1, Q-2, and Q-3 as will become apparent.

The outputs G_1 -0, G_2 -0 and G_3 -0 are connected to the logic inputs A of the disabling multivibrator M5 like multivibrator M1 respectively through diodes D_3 , D_4 and D_5 . The inhibit input B of multivibrator M5 is connected to the voltage source V_{cc} of power supply 142 and output Q-5 is connected directly to the inhibit input B of multivibrator M4 and to the inhibit inputs B of multivibrators M1-M3 through diode D_2 . Each output G_1 -0, G_2 -0 and G_3 -0 is also connected respectively to an integrator network IG₁, IG₂ and IG₃ through inverters I_3 , I_4 and I_5 . The networks IG₁, IG₂ and IG₃ are identical with each having a diode D_6 , a charging rate control resistor R_1 , a capacitor C_1 , a discharge rate control resistor R_2 , a transistor Q_1 and a voltage drop resistor R_3 arranged in known manner to integrate the outputs G_1 -0, G_2 -0 and G_3 -0 to render transistor Q_1 conductive upon a certain number of pulses at a particular rate as will become apparent.

The output O₂ of the integrator network IG₁ is connected to the set input L₂-S of a two gate latch L_2 like latch L_1 and the output L₂-0 thereof is connected to one input of the burglary alarm control NAND gate G_7 . The output of gate G_7 is connected to an alarm device 140 of known construction. The other input of the gate G_7 is also connected to the latch output L₂-0 but through an entry time delay means 141. The time delay means 141 includes the multivibrator M6. The output L₂-0 is connected to input B of multivibrator M6 like multivibrator M1, the inputs A thereof are connected to ground, and the output Q thereof is connected to the other input of gate G_7 . Resistors R_4 and R_5 are connected in parallel to the appropriate timing pin M6₁₁ and the voltage source V_{cc} from the power supply 142 of known construction. A shunt switch SW₁ selectively connects resistor R_4 to the source V_{cc} and the values of resistors R_4 and R_5 are selected so that when switch

SW₁ is open, a second predetermined time will elapse before output Q returns to its original state upon receipt of a signal at input B but when switch SW₁ is closed a first predetermined time much less than the second predetermined time will elapse before output Q returns to its original state as will become more apparent. A capacitor C_2 connects timing pins M6₁₁ and M6₁₀ to complete the timing circuit of multivibrator M6.

The common point between resistor R_1 and capacitor C_1 in the integrator network IG₁ is connected to an exit delay means 146. Means 146 includes a field effect transistor FET₁, a diode D_7 , a resistor R_6 , a capacitor C_3 and a switch SW₂. The drain of transistor FET₁ is connected to the common point between resistor R_6 and capacitor C_3 connected in series between the voltage source V_c of power supply 142 and ground. The gate of transistor FET₁ is also connected to ground through diode D_7 and switch SW₂ so that when switch SW₂ is closed, transistor FET₁ will conduct as will become more apparent.

The output O₃ of the integrator network IG₂ is connected to the set input L₃-S of a two gate latch L_3 like latch L_1 . Its output L₃-0 is connected to a convenience switching device 145 of known construction to activate an appliance APP as will become apparent.

The reset inputs L₂-R, L₃-R and L₄-R of latches L_2 - L_4 are connected to a reset circuit 148 of known construction. The circuit 148 includes resistor R_7 and capacitor C_4 in series between the voltage source V_{cc} and ground. The common point between resistor R_7 and capacitor C_4 is connected to the inputs L₂-R, L₃-R and L₄-R and to ground through diode D_8 and switch SW₃. Thus, when switch SW₃ is closed latches L_2 - L_4 will be reset as will become more apparent.

DIGITAL EMBODIMENT

Referring generally to FIGS. 5A and 5B, the receiver 211 of the digital version of the invention includes the conventional radio frequency receiver 230 for detecting an RF signal and generating a corresponding signal output, and the conventional pulse shaping network 231 for shaping the signal output from the receiver 230 as previously described. If one of the signals A, B or C is received by the receiver 230, corresponding signals A, B or C will be generated at the output O₁ of the network 231.

The output O₁ is connected through an inverter I_1 and resistor R_1 to input G1-1 of NAND gate G1. The common point between resistor R_1 and input G1-1 is connected to ground through capacitor C_1 . The output G1-0 of gate G1 is connected to the clock input C₁ of a monolithic, D-type, positive edge triggered flip-flop FF1. The output Q-1 of the flip-flop FF1 is connected to the data input D₁ of flip-flop FF1 and its output Q1 is connected to the clock input C₂ of a like flip-flop FF2. The data input D₂ of flip-flop FF2 is connected to ground while the output Q2 thereof is connected back to the input G1-2 of gate G1. The gate G1 and flip-flops FF1 and FF2 define the noise isolation means 236.

The output O₁ is also connected to the set input L1-S of a two gate latch L1. The latch L1 is a pair of NAND gates G2 and G3 with the output G2-0 of gate G2 connected to the input G3-1 of gate G3 and the output G3-0 of gate G3 connected to the input G2-2 of gate G2. The input G2-1 of gate G2 is the set input to the latch while input G3-2 is the reset input L1-R to latch L1. The output G2-0 is the output L1-0 of latch L1 and

is connected to the input G4-1 of the count start NAND gate G4. The other input G4-2 of gate G4 is connected to the output Q2 of a binary clock network CN of known arrangement and which produces an incrementally variable pulsed signal output identified as signal D in FIG. 7.

The output G4-0 of gate G4 is connected to a pair of high-speed, monolithic 4-bit binary counters CTR-1 and CTR-2. The counters CTR-1 and CTR-2 are identical and each consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter with a gated direct reset line which inhibits the count inputs and simultaneously returns the flip-flop outputs to a logical 0. Such counters are commercially available in transistor-transistor logic and one such commercial type is designated SN 7493 TTL 4-bit binary counter manufactured by Texas Instruments, Inc. of Dallas, Texas. The output G4-0 of gate G4 is connected to the input I-A1 of counter CTR-1. Each counter has four outputs A, B, C and D. The counters CTR-1 and CTR-2 are connected so that output A₁ corresponds to the binary 2, output B₁ to binary 4, output C₁ to binary 8, and output D₁ to binary 16 on the counter CTR-1 while output A₂ corresponds to binary 32, output B₂ corresponds to the binary 64, output C₂ corresponds to the binary 128, and output D₂ corresponds to the binary 256 on the counter CTR-2. Each of the outputs is also connected through an inverter $\bar{I}$ to give a NOT output corresponding to each of the above outputs as will become apparent.

The outputs of the counters CTR-1 and CTR-2 are connected to six of the inputs of eight-input positive NAND gates G5-G8. Two of the inputs of each gate G5-G8 are left open so that the gates will remain transferred for three clock pulses in the signal D instead of one as will become apparent.

The outputs of the counters CTR-1 and CTR-2 are connected to the inputs of gate G5 so that the proper number of clock pulses in signal D corresponding to the time interval t_1 in signal A will trigger gate 5. Likewise, it will be seen that gate G6 will be triggered corresponding to time interval t_2 in signal B and gate G7 will be triggered corresponding to time interval t_3 in signal C. The gate G8 serves to reset the systems and corresponds to a time interval which is less than interval t_0 between pulse pairs but greater than any of intervals t_1 , t_2 , or t_3 .

The output G8-0 of gate G8 is connected directly to the resetting input L1-R of the latch L1, this being input G3-2 of gate G3 and also to the preset input P1 of the flip-flop FF1 as well as the preset input P2 of the flip-flop FF2. The output G8-0 is also connected to the reset inputs R₁ of counter CTR-1 and reset inputs R₂ of counter CTR-2 through inverter I2 since reset of counters CTR-1 and CTR-2 takes place when inputs R₁ and R₂ go to logical 1.

The output G5-0 of gate G5, which is adapted to change state in accordance with time t_1 of the burglary signal A, is connected to one input of NAND gate G9 in the coincidence means 232 through an inverter I3. Likewise, output G6-0 of gate G6, which is adapted to change state in accordance with time t_2 of the fire signal B is connected to one input of NAND gate G10 in the coincidence means 232 through inverter I4. Output G7-0 of gate G7, which is adapted to change state in accordance with time t_3 of the coincidence signal C, is connected to one input of NAND gate G11 in the coin-

cidence means 232 through inverter I5. The other inputs of gates G9, G10, and G11 are connected to the output G1-0 of gate G1 in the noise isolation means 236 through inverter I6 so that the outputs thereof will change state upon coincidence between output G1-0 and one of the outputs G5-0, G6-0, or G7-0.

Each output G9-0, G10-0, and G11-0 is connected respectively to an integrator network IG-1, IG-2, and IG-3 through interconnectors I7, I8, and I9. The networks IG-1, IG-2 and IG-3 form the integrating means 235 and are identical with each having a diode D1, a charging rate control resistor R2, a capacitor C2, a discharge rate control resistor R3, a transistor Q1 and a voltage drop resistor R4 arranged in known manner to integrate the outputs G9-0, G10-0 and G11-0 to render transistor Q1 conductive upon receipt of a certain number of pulses at a particular rate as will become apparent.

The output O₃ of the integrator network IG-1 is connected to the set input L2-S of a two gate latch L2 like latch L1 and the output L2-0 thereof is connected to one input of the burglary alarm control NAND gate G12. The output of gate G12 is connected to a burglary alarm device 240 of known construction. The other input of the gate G12 is also connected to the latch output L2-0 but through an entry time delay means 241. The time delay means 241 includes a monolithic transistor-transistor logic monostable multi-vibrator MV with d-c triggering. The multivibrator MV is commercially available under part number SN 74121 manufactured by Texas Instruments, Inc. of Dallas, Texas. The output L2-0 is connected to input B of multivibrator MV, the inputs A thereof are connected to ground, and the output $\bar{Q}$ thereof is connected to the other input of gate G12. Resistors R5 and R6 are connected in parallel to the appropriate timing pin MV11 and the voltage source V_{cc} from the power supply 242 of known construction. A shunt switch SW1 selectively connects resistor R5 to the source V_{cc} and the values of resistors R5 and R6 are selected so that when switch SW1 is open, a second predetermined time will elapse before output $\bar{Q}$ returns to its original state upon receipt of a signal at input B but, when switch SW1 is closed, a first predetermined time much less than the second predetermined time will elapse before output $\bar{Q}$ returns to its original state as will become more apparent. A capacitor C3 connects timing pins MV₁₁ and MV₁₀ to complete the timing circuit of multivibrator MV.

The common point between resistor R2 and capacitor C2 in the integrator network IG-1 is connected to an exit delay means 246. Means 246 includes a field effect transistor FET 1, a diode D2, a resistor R7, a capacitor C4 and a switch SW2. The drain of transistor FET 1 is connected to the common point between resistor R1 and capacitor C1 and its drain is connected to ground. Its gate is connected to the common point between resistor R6 and capacitor C3 connected in series between the voltage source V_c of power supply 242 and ground. The gate of transistor FET 1 is also connected to ground through diode D2 and switch SW2 so that when switch SW2 is closed, transistor FET 1 will conduct as will become more apparent.

The output O₄ of the integrator network IG-2 is connected to the set input L3-S of a two gate latch L3 like latch L1 and its output L3-0 is connected to the alarm

device 240 of known construction. The operation thereof will become more apparent.

The output O_3 of the integrator network IG-3 is connected to the set input L4-S of a two gate latch L4 like latch L1. Its output L4-0 is connected to a convenience switching device 245 of known construction to activate an appliance APP as will become more apparent.

The reset inputs L2-R, L3-R, and L4-R of latches L2-L4 are connected to a reset circuit 248 of known construction. The circuit 248 includes resistor R8 and capacitor C5 in series between the voltage source V_{cc} and ground. The common point between resistor R8 and capacitor C5 is connected to the inputs L2-R, L3-R and L4-R and to ground through diode D3 and switch SW3. Thus, when switch SW3 is closed, latches L2-L4 will be reset as will become more apparent.

THE OPERATION OF ANALOG EMBODIMENT

Referring to FIG. 6, the received signal A, B or C received by the radio frequency receiver 130 is transmitted through the pulse shaping network 131 to multivibrators M1-M3 and through inverter I₁ to multivibrator M4. Since the multivibrators are all triggered by the negative going edge of the received pulses P of the signal A, B, or C, it will be seen that the first pulse P_1 , P_1' or P_1'' activates the multivibrators as illustrated in FIG. 6. Because any one of the three signals can be received, the signals are superimposed over each other with the second pulse P_2 of the signal A appearing in solid lines, the second pulse P_2' of the signal B appearing in dashed lines, and the second pulse P_2'' of the signal C appearing in phantom lines in FIG. 6.

Because the leading edge of the pulses P are negative going when they emerge from the pulse shaping network 131 at output O_1 as seen in FIG. 4A, the leading edge of the first pulse P_1 , P_1' or P_1'' triggers each of the multivibrators M1-M3 to cause the outputs $\bar{Q}-1$, $\bar{Q}-2$ and $\bar{Q}-3$ thereof to go low. The output $\bar{Q}-1$ of multivibrator M1 remains low until it times out through the timing circuit RC1 in known manner. The timing circuit RC1 is selected so that the output $\bar{Q}-1$ goes high again after a time interval equal to the time interval t_1 of the signal A. This will enable the coincidence NAND gate at the same time the second pulse P_2 of a burglar signal A should be received at the coincidence means 132. Likewise, the output $\bar{Q}-2$ of the multivibrator M2 goes low with the leading edge of the pulse P_1 , P_1' or P_1'' and times out through the timing circuit RC2 after a time interval equal to the time interval t_2 of fire signal B. Thus, the coincidence NAND gate G_2 is enabled at the same time the pulse P_2' should be received at the coincidence means 132. The output $\bar{Q}-3$ goes low on the leading edge of the pulse P_1 , P_1' or P_1'' and remains low until the multivibrator M3 times out through the timing circuit RC3 which is equal to the time interval t_3 of the convenience signal C. This enables the coincidence NAND gate G_3 at the time the second pulse P_2'' of signal C should be received at the coincidence means 132. The coupling networks CN1-CN3 serve to spread the positive going edge of the outputs $\bar{Q}-1$, $\bar{Q}-2$, and $\bar{Q}-3$ so as to maintain the time interval t_e as seen in FIG. 6 so that the coincidence gates G_1 - G_3 are enabled when the outputs of multivibrators M1-M3 go high.

The trailing edge of the first pulse P_1 , P_1' or P_1'' triggers the multivibrator M4 since the pulse has been inverted in the inverter I₁. This causes its output $\bar{Q}-4$ to

go high and its output $\bar{Q}-4$ to go low until the multivibrator M4 times out through the timing circuit RC4. As was indicated, the circuit RC4 is designed to time out and cause output $\bar{Q}-4$ to go low with output $\bar{Q}-4$ going high at a time interval t_i greater than time interval t_3 but less than time interval t_6 between pulse pairs. Time interval t_i is usually just greater than time interval t_3 . When output $\bar{Q}-4$ goes low, the set input L₁-S of latch L₁ momentarily goes low to set the latch L₁ and cause its output L₁-0 to go high. Because the input L₁-S is tied to voltage source V_{cc} through resistor R_n , this input floats high again even though output $\bar{Q}-4$ remains low. This is best seen in FIG. 6. Thus, the output L₁-0 will remain high until its reset input L₁-R goes low. The value of the resistor R_n is selected such that input L₁-S will float high before any of the second pulses P_2 , P_2' or P_2'' are received as will become apparent.

Because of inverter I₂, the pulse inputs G_1-1 , G_2-1 , and G_3-1 of the coincidence gates G_1 - G_3 remain low as seen in FIG. 6 for point Op. On the other hand, when output $\bar{Q}-4$ went high, the input G_4-2 of noise isolation NAND gate G_4 went high so that when the input G_4-1 thereof goes high as the second pulse P_2 , P_2' or P_2'' is received at input G_4-1 , the output G_4-0 goes low to cause the reset input L₁-R to go low and the output of gate G_6-0 in latch L₁ to go high. This causes the cross-coupled input G_5-2 of gate G_5 in latch L₁ to go high. When input G_5-2 goes high, the output G_5-0 thereof goes low to lock the latch L₁ in that condition until the set input L₁-S again goes low. Thus, latch L₁ is locked with its output L₁-0 low.

When output L₁-0 goes low, this causes the pulse inputs G_1-1 , G_2-1 and G_3-1 to go high because of inverter I₂. Because the inputs G_1-1 , G_2-1 and G_3-1 are tied to voltage source V_{cc} through resistor R_b and inverter I₂, these inputs float low again after a prescribed period of time even though output L₁-0 remains low as seen in FIG. 6 for point Op. The value of resistor R_b is such that the inputs G_1-1 , G_2-1 and G_3-1 remain high just long enough to obtain coincidence if one of the enabling inputs G_1-2 , G_2-2 or G_3-2 is also high. Thus, if the pulse P_2 , P_2' or P_2'' is received in coincidence with the timing out of one of the multivibrators M1-M3, the correct output G_1-0 , G_2-0 or G_3-0 will go low and pass through associated inverter I₃, I₄ or I₅ to the integrator IG₁, IG₂ or IG₃.

It will also be noted that the output $\bar{Q}-4$ of the multivibrator M4 is connected to the inhibit inputs B of each of the multivibrators M1-M3 to prevent re-activation of the multivibrators until multivibrator M4 times out. Multivibrator M4 times out just after the longest time interval t_3 of the received signals. This prevents re-activation of the multivibrators M1-M3 during the time the first and second pulses of a signal is received.

When the output G_1-0 , G_2-0 or G_3-0 goes low, the negative going edge of the output pulses causes the multivibrator M5 to trigger and its output $\bar{Q}-5$ to go low. Since output $\bar{Q}-5$ is connected to the inhibit input B of the multivibrator M4 and to the inhibit inputs B of the multivibrators M1-M3, all of the multivibrators M1-M4 are disabled to prevent re-activation until multivibrator M5 times out. The time interval t_2 for multivibrator M5 to time out is such that multivibrator M5 times out just before the next pulse pair P of the signals A, B or C should be received. Thus, once a pulse pair is received, the system is disabled until just prior

to the probable receipt of the next pulse pair. This renders the system self-searching for the particular signals A, B or C once the first pulse pair of signals has been received.

When a sufficient number of pulses has been received by the integrator network IG₁, IG₂, or IG₃, its output 0₂, 0₃ or 0₄ goes low to trigger and lock its associated latch L₂, L₃ or L₄ to energize the associated alarm device or a convenient switching network until the locked latch L₂, L₃ or L₄ is reset. The integrator networks IG₁, IG₂ and IG₃ are designed so that the signals A, B or C must be received for a predetermined period of time and a predetermined percentage of coincidences versus received pulse pairs P between the signals A, B or C and the enabling signals from multivibrators M1-M3. While the values of resistor R₁ and capacitor C₁ may be varied to provide any convenient predetermined signal receiving time, and the values of resistor R₂ and capacitor C₁ may be varied to provide any convenient predetermined percentage of coincidence, one satisfactory receiving time is 0.5 seconds and one satisfactory coincidence rate is 90 percent of the pulses at which coincidence should occur to obtain an output 0₂, 0₃ or 0₄.

Once the latch L₂, L₃ or L₄ has been locked, it will remain in that state to operate the alarm device 140 or the appliance APP. The latches L₂, L₃ and L₄ are reset to turn off the alarm device 140 or appliance APP by closing switch SW₃. This connects the reset inputs L₂-R, L₃-R and L₄-R to ground so that the outputs thereof are changed. When switch SW₃ is released, the inputs L₂-R, L₃-R and L₄-R again go high to render the latches operable.

When the user wants to leave the premises without setting off the alarm, he simply momentarily closes the exit switch SW₂ which would preferably be of the normally open pushbutton type. When he closes switch SW₂, he allows the capacitor C₃ to be discharged to ground to allow the field effect transistor FET₁ to conduct. The value of capacitor C₃ and resistor R₆ is selected to provide a predetermined period of time before the capacitor C₃ is recharged from the voltage source V_c after the switch SW₂ is again open. This predetermined elapsed time is sufficient to allow the user to exit the premises and stop the transmission of the burglar signal A from the appropriately located transmitter on the door through which he exits. As long as the transistor FET₁ is conducting while the capacitor C₃ is being recharged, any pulses received by the integrator network IG₁ will be discharged through the transistor FET₁ to prevent the capacitor C₁ from being charged and operating the integrator network IG₁ and thus prevent the device from alarming. Once the capacitor C₃ has been recharged, the receiver 111 operates in its aforementioned manner.

Since the user must be able to re-enter the premises once he has left without the alarm sounding, the multivibrator M6 is triggered when the latch L₂ is transferred by the output of the integrator circuit IG₁ to cause the output Q thereof to go low for the predetermined period of time depending on the position of the shunt switch SW₁. Therefore, in order to make this component of the circuit operative, the shunt switch SW₁ should be open before the user leaves the premises and when he closes the switch SW₂. This places the larger value of the resistor R4 is the timing circuit of the multivibrator M6 so that the longer predetermined time

lapse will be in effect before the gate G₇ is transferred to give the alarm signal. Thus, if switch SW₁ is open, the user can enter the premises and go to the receiver 111 and reset same by closing switch SW₃ before the multivibrator M6 is timed out to enable the gate G₇. If the user is in the premises, however, he may close switch SW₁ which places the lesser value of the resistor R₅ in parallel across resistor R₄ and reduces the time delay of the time delay means 141 to a negligible amount to provide substantially instantaneous alarm generating capability.

OPERATION OF DIGITAL EMBODIMENT

Referring now to FIGS. 7 and 8, the receiver 230 receives a signal from one of the transmitters and generates a like signal A, B or C from the pulse shaping network 231. The signal generated at output 0₁ is directed to the start input L1-S of the latch L1 to enable the gate G4 and allow the output 0₂ from the clock CN to be received by the counters CTR1 and CTR2 to start the generation of the enabling pulses. The outputs of the counters are appropriately connected to the gates G5-G8 so as to enable the gate G9 at the time the second pulse P₂ of the burglar alarm signal A should be received thereat. The gate G6 enables the gate G10 at the time the second pulse P₂' of the fire signal B should be received and the gate G7 enables the gate G11 at the same time the second pulse P₂'' of the convenience signal C should be received. With the particular frequency generated by the clock CN and because two of the eight inputs of each of the gates G5-G8 are open and therefore high, gate G5 is transferred from the 92nd to the 94th pulses P_c of the clock generated signal D as seen in FIG. 7. Gate G6 is enabled from the 124th to 126th pulses P_c of the clock signal D and gate G7 is transferred from the 152nd to 154th pulses P_c of the clock signal D. The reset pulse from gate G8 is generated from the 220th to 222nd pulses P_c of the clock signal D. By enabling gate G5-G7 on more than one clock pulse P_c, the enabled time interval t_e of each of the gates is slightly greater than the pulse interval t_p of signals A, B or C to facilitate adjustment of the system.

The output 0₁ of the pulse shaping network 31, at the same time that it turns on the latch L1, passes through inverter I1 to gate G1 to transfer the first flip-flop FF1 as seen in FIG. 8. Since output G1-0 is pulsed low when input G1-1 is pulsed high, the output Q̄1 of flip-flop FF1 goes high because it was preset low and the output Q1 thereof goes low because it was preset high on the positive going or trailing edge of the pulse from output G1-0. Because the flip-flops FF1 and FF2 are triggered only on the positive going edges of the input pulse, flip-flop FF2 is not transferred on the first pulse from output G1-0 even though output Q1 is connected thereto. When the second pulse is received from output G1-0, the output Q̄-1 goes low and output Q1 goes high since the input D1 was high. Since input D2 is tied low, the positive going edge of the output Q1 as it goes high transfers the output Q2 low. This causes the input G1-2 to go low to prevent it from being triggered until the flip-flops FF1 and FF2 are again preset. Thus, after two pulses have been received through gate G1, the flip-flops FF1 and FF2 disable it to prevent transmission of any more pulses to the coincidence gates G9-G11 until the flip-flops are again preset by the output of gate G8 going low. When the output of gate G8 goes low, the

latch L1 and counters CTR-1 and CTR-2 are also reset for a repeat operation.

When a sufficient number of pulses has been received by the integrator network IG-1, IG-2 or IG-3, its output 0₃, 0₄ or 0₅ goes low to trigger and lock its associated latch L2, L3 or L4 to energize the associated alarm device or a convenient switching network until the locked latch L2, L3 or L4 is reset. The integrator networks IG-1, IG-2 and IG-3 are designed so that the signals A, B or C must be received for a predetermined period of time and a predetermined percentage of coincidence versus received pulse pairs P between the signals A, B or C and the enabling signals from gates G5-G7. While the value of resistor R3 and capacitor C2 may be varied to provide any convenient predetermined signal receiving time and the values of resistor R3 and capacitor C2 may be varied to provide any convenient predetermined percentage of coincidence, one satisfactory receiving time is 0.5 seconds and one satisfactory coincidence rate is 90 percent of the pulses at which coincidence should occur to obtain an output 0₃, 0₄ or 0₅.

Once the latch L2, L3 or L4 has been locked, it will remain in that state to operate the alarm device 240 or the appliance APP. The latches L2, L3 and L4 are reset to turn off the alarm device 240 or appliance APP by closing switch SW3. This connects the reset inputs L2-R, L3-R and L4-R to ground so that the outputs thereof are changed. When switch SW3 is released, the inputs L2-R, L3-R and L4-R again go high to render the latches operable.

When the user wants to leave the premises without setting off the alarm, he simply momentarily closes the exit switch SW2 which would preferably be of the normally open pushbutton type. When he closes switch SW2, he allows the capacitor C4 to be discharged to ground to allow the field effect transistor FET 1 to conduct. The value of the capacitor C4 and resistor R7 is selected to provide a predetermined period of time before the capacitor C4 is recharged from the voltage source V_c after the switch SW2 is again open. This predetermined elapsed time is sufficient to allow the user to exit the premises and stop transmission of the burglar signal A from the appropriately located transmitter on the door through which he exits. As long as the transistor FET 1 is conducting while the capacitor C4 is being recharged, any pulses received by the integrator network IG-1 will be discharged through the transistor FET 1 to prevent the capacitor C2 from being charged and operating the integrator network IG-1 and thus prevent the device from alarming. Once the capacitor C4 has been recharged, the receiver 211 operates in its aforementioned manner.

Since the user must be able to re-enter the premises once he has left without the alarm sounding, the multivibrator MV is triggered when the latch L2 is transferred by the output of the integrator circuit IG-1 to cause the output Q thereof to go low for the predetermined period of time depending on the position of the shunt switch SW1. Therefore, in order to make this component of the circuit operative, the shunt switch SW1 should be open before the user leaves the premises and when he closes the switch SW2. This places the larger value of the resistor R6 in the timing circuit of the multivibrator MV so that the longer predetermined time lapse will be in effect before the gate G12 is transferred to give the alarm signal. Thus, if switch SW1 is

open, the user can enter the premises and go to the receiver 211 and reset same by closing switch SW 3 before the multivibrator MV is times out to enable the gate G12. If the user is in the premises, however, he may close switch SW1 which places the lesser value of the resistor R5 in parallel across resistor R6 and reduces the time delay of the time delay means 241 to a negligible amount to provide substantially instantaneous alarm generating capability.

In both embodiments of the invention, the noise rejection or isolation means 36 automatically disables the coincidence means 32 is an extraneous pulse signal is received by the receiver 11 which has a time interval between pulses less than the smallest time interval between the pulses of each pulse pair of signals A, B or C. This gives maximum noise rejection for extraneous pulse signals of high frequency. Also, extraneous pulse signals having a time interval between pulses greater than twice the smallest time interval between the pulses of each pulse pair of signals A, B or C are inherently rejected since there will be no coincidence.

This leaves extraneous pulse signals which have a time interval between pulses equal to or greater than the smallest time interval between the pulses of the pulse pair of signals A, B or C but less than twice the smallest time interval between pulses of the pulse pairs of signals A, B or C. Coincidence may occur for such extraneous signals, however, the integrating means 35 of both embodiments of receiver 11 is adjusted so as to cause an alarm signal not to be generated unless a prescribed percentage of coincidences with the received pulses takes place. Because the total energy level of both the extraneous pulses and signals A, B or C is approximately the same, it will be seen that coincidence will occur with only one out of every three pulses rather than one of every two pulses as is the case with signals A, B or C. Thus, the charging rate to the firing capacitor in the integrating means 35 is adjusted so that it takes more coincidences than one out of every three pulses to charge the capacitor to firing level within the prescribed time interval while one out of every two pulses will charge same to firing potential within a prescribed interval. Because there are generally a few pulses within a signal A, B or C that may not create coincidence within the prescribed time interval, the integrating means is adjusted so that an average coincidence of less than one out of every two received pulses will generate an alarm signal but an average coincidence of one out of three received pulses will not generate an alarm signal. Thus, a pure tone having a time interval equal to that of signals A, B or C will not generate an alarm signal.

While it is understood that the carrier frequency and time intervals between pulses may be varied, one set of values is as follows:

Carrier Frequency: 250 megacycles/sec.

Time Interval t_1 : 350 microseconds

Time Interval t_2 : 400 microseconds

Time Interval t_3 : 450 microseconds

Time Interval t_0 : 600 microseconds

While specific embodiments of the invention have been disclosed herein, it is to be understood that full use may be made of modifications, substitutions, and equivalents without departing from the scope of the inventive concept.

We claim:

1. An alarm system responsive to certain preconceived conditions to produce an alarm signal comprising:

transmitter means for generating a signal having pulse pairs with a prescribed time interval between said pulses of each said pulse pair upon occurrence of the preconceived conditions;

receiver means for detecting said generated signal and producing a corresponding operating signal output;

enabling means operatively connected to said receiver means for generating a reference enabling pulse a predetermined time interval after receipt of said first pulse of said pulse pair equal to said prescribed time interval between said pulses of each said pulse pair;

coincidence means operatively connected to said receiver means and said enabling means for generating an output signal pulse upon coincidingly receiving said reference enabling pulse and said second pulse of said pulse pair; and,

noise isolation means for preventing further receipt of pulses by said coincidence means from said receiver means after receipt of a second generated pulse from said receiver means after said first generated pulse for a second prescribed period of time.

2. The alarm system of claim 1 further including integrating means operatively connected to said coincidence means for generating the alarm signal upon receipt of a prescribed number of said output signal pulses from said coincidence means within a prescribed period of time.

3. The alarm system of claim 1 wherein said noise isolation means includes latch means operatively connecting said receiver means to said coincidence means, said first generated pulse of said operating signal output from said receiver means corresponding to said first generated pulse of said pulse pair rendering said latch means operative and second generated pulse of said operating signal output from said receiver means corresponding to said second generated pulse of said pulse pair rendering said latch means inoperative while generating a pulse output from said latch means to said coincidence means.

4. The alarm system of claim 1 wherein said noise isolation means includes flip-flop means operatively connecting said receiver means to said coincidence means, said first generated pulse of said operating signal output from said receiver means corresponding to said first generated pulse of said pulse pair rendering said flip-flop means operative and second generated pulse of said operating signal output from said receiver means corresponding to said second generated pulse of said pulse pair rendering said flip-flop means inoperative while generating a pulse output from said flip-flop means to said coincidence means.

5. In an alarm system for generating an alarm signal upon receipt of a pulsed radio frequency signal having pulse pairs with a prescribed time interval between the first and second pulses of each pulse pair, detection means comprising:

tuned radio frequency receiver means for receiving pulsed radio signals and generating a pulsed signal output corresponding to the received radio frequency signal;

coincidence means having a first input operatively connected to said output of said receiver and a second input;

enabling means operatively connected to said output of said receiver for generating an output pulse a reference prescribed time interval after receipt of a pulse from said output of said receiver, said reference prescribed time interval corresponding to said time interval of between the first and second pulses of each of pulse pair of the radio frequency signal to be detected, and said output of said enabling means connected to said second input of said coincidence means;

said coincidence means generating an alarm output upon coincidence between said output pulse of said enabling means and a pulse of said pulsed signal output of said receiver means; and,

noise isolation means operatively connecting said receiver means and said coincidence means, said noise isolation means responsive to the receipt of the next generated pulse from said receiver means after activation of said enabling means to prevent receipt of additional pulses from said receiver means by said coincidence means until said noise isolation means is reset.

6. In the alarm system as set forth in claim 5 wherein said noise isolation means includes a latch circuit means; first monostable multivibrator means having its input connected to said output of said receiver means and its normally high output connected to the set input of said latch circuit means; gating means having one of its inputs connected to said output of said receiver means, the other of its inputs connected to the normally low output of said multivibrator means, and its output connected to the reset input of said latch circuit means; the output of said latch circuit means connected to one input of said coincidence means so that said latch circuit means is locked in a prescribed state upon the change in output of said gating means until retriggering of said multivibrator means.

7. In the alarm system as set forth in claim 5 wherein said noise isolation means includes gating means having one of its inputs connected to the output of said receiver means; first flip-flop means having its input connected to the output of said gating means; and second flip-flop means having its input connected to the normally high input of said first flip-flop means and its normally high output connected to the other input of said gating means; the output of said gating means also connected to one input of said coincidence means, and said first and second flip-flop means rendering said gating means inoperative upon passage of any second pulse from said receiver means until said first and second flip-flop means are preset to their normal states.

8. In the alarm system as set forth in claim 5 further including integrating means operatively connected to said coincidence means for generating the alarm signal upon receipt of a prescribed number of said alarm output pulses from said coincidence means within a prescribed period of time.

9. In an alarm system as set forth in claim 6 wherein said enabling means includes second monostable multivibrator means and a first RC coupling network, said second multivibrator means having its logic input connected to said output of said receiver, its inhibit input connected to the normally high output of said first monostable multivibrator means, and its normally high

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output operatively connected to another input of said coincidence means through said first RC coupling network so that an enabling pulse is supplied to said coincidence means when the normally high output of said second multivibrator means changes from its low state to its high state. 5

10. In an alarm system as set forth in claim 9 wherein said noise isolation means further includes a second RC coupling network operatively connecting the output of said latch circuit means to the one input of said coincidence means for returning the one input of said coincidence means back to a low state a prescribed period of time after the one input of said coincidence means is moved to a high state, said second RC coupling network operating independently of the output of said latch circuit means. 15

11. In an alarm system as set forth in claim 9 wherein said enabling means further includes third monostable multivibrator means having its logic input operatively connected to the alarm output of said coincidence means and its normally high output operatively connected to the inhibit input of said first monostable multivibrator means for disabling said first multivibrator means for a predetermined period of time upon generation of an alarm signal output from said coincidence means. 20 25

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12. A method of decoding received multi-pulsed signals having pulse pairs using a two input coincidence system comprising the steps of:

generating a reference signal in response to the receipt of the first pulse of the received signal, the reference signal being a pulsed signal having a time interval between initiation of the reference signal and its pulse corresponding to the time interval between pulses of the pulse pairs of the received signal to be decoded;

connecting the reference signal to one of the inputs of the coincidence system to enable the coincidence system;

connecting the received signal to the other of the inputs of the coincidence system;

disconnecting the received signal from the other of the inputs of the coincidence system immediately after receipt of the second pulse of the received signal for a prescribed period of time; and,

generating an alarm signal upon the pulse from the reference signal being received at the coincidence system simultaneously with the receipt of the second pulse of the received signal at the coincidence system.

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