PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :

H04N 5/63

(11) International Publication Number:

WO 98/21887

(43) International Publication Date:

22 May 1998 (22.05.98)

(21) International Application Number:

PCT/US97/21011

A₁

(22) International Filing Date:

12 November 1997 (12.11.97)

(30) Priority Data:

08/749,714

15 November 1996 (15.11.96) US

(71) Applicant: THOMSON CONSUMER ELECTRONICS, INC. [US/US]; 10330 North Meridian Street, Indianapolis, IN 46290-1024 (US).

(72) Inventor: WILLIAMS, Kevin, Michael; 6101 North Primrose Avenue, Indianapolis, IN 46220 (US).

(74) Agents: TRIPOLI, Joseph, S. et al.; GE & RCA Licensing Management Operation, Inc., P.O. Box 5312, Princeton, NJ 08543 (US).

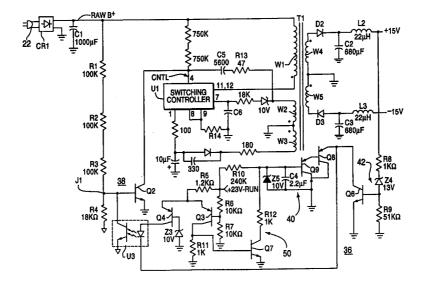
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: QUICK-RESET CIRCUIT FOR AUXILIARY POWER SUPPLY



(57) Abstract

Run/standby switching including switching to standby upon excessive current loading is provided in a switched mode power supply useful as an auxiliary power supply in a television. A switching controller IC (U1) is coupled between a primary transformer winding (W1) on the rectified raw B+ (RAW B+) input voltage and ground. A switching transistor (Q2) is coupled to the control input of the controller and is biased by the raw B+ input voltage for pulling down the control input (CNTL). A run/standby control circuit (R5, R6, R7, Q3, Q4, Z3, U3) and an overcurrent protective circuit disable the switching transistor during run mode operation and enable the switching transistor upon an overcurrent fault. The switched—mode power supply is further provided with a quick—reset capability (Q7, R11, R12) to enable the power supply to consistently provide output voltages which are within nominal output voltage levels despite rapidly repeated dislocations in the operational mode of the apparatus.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

nia		Spain	LS	Lesotho	SI	Slovenia
	FI	Finland	LT	Lithuania	SK	Slovakia
ia	FR	France	LU	Luxembourg	SN	Senegal
alia	GA	Gabon	LV	Latvia	SZ	Swaziland
paijan	GB	United Kingdom	MC	Monaco	TD	Chad
a and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
idos	GH	Ghana	MG	Madagascar	TJ	Tajikistan
um	GN	Guinea	MK	The former Yugoslav	TM	Turkmenistan
na Faso	GR	Greece		Republic of Macedonia	TR	Turkey
ıria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
 1	ΙE	Ireland	MN	Mongolia	UA	Ukraine
1	IL	Israel	MR	Mauritania	\mathbf{UG}	Uganda
us	IS	Iceland	MW	Malawi	US	United States of America
da	IT	Italy	MX	Mexico	UZ	Uzbekistan
al African Republic	JP	Japan	NE	Niger	VN	Viet Nam
0	KE	Kenya	NL	Netherlands	YU	Yugoslavia
erland	KG	Kyrgyzstan	NO	Norway	$\mathbf{z}\mathbf{w}$	Zimbabwe
d'Ivoire	KP	Democratic People's	NZ	New Zealand		
roon		Republic of Korea	PL	Poland		
1	KR	Republic of Korea	PT	Portugal		
	KZ	Kazakstan	RO	Romania		
1 Republic	LC	Saint Lucia	RU	Russian Federation		
•	LI	Liechtenstein	SD	Sudan		
•	LK	Sri Lanka	SE	Sweden		
	LR	Liberia	\mathbf{SG}	Singapore		
n Repu any nark ia	blic	LI LK	LI Liechtenstein LK Sri Lanka	LI Liechtenstein SD LK Sri Lanka SE	LI Liechtenstein SD Sudan LK Sri Lanka SE Sweden	LI Liechtenstein SD Sudan LK Sri Lanka SE Sweden

QUICK-RESET CIRCUIT FOR AUXILIARY POWER SUPPLY

This invention relates to the field of switched mode power supplies for apparatus having a run mode and a standby mode of operation, such as a television receiver. In particular, the invention relates to the field of resetting switched mode power supplies, for example an auxiliary power supply, in such apparatus when changing between the run and standby modes of operation.

5

10

15

20

2.5

30

35

In a typical run/standby power supply, for example as used in television receivers, a bridge rectifier and a filter capacitor provide a raw DC voltage (called the B+ voltage, or raw B+), whenever the power supply is coupled to the domestic mains. Standby mode loads can be powered directly from the B+ voltage or from another voltage that is always present. Many run mode loads, however, are powered through a voltage regulating supply such as a switched mode supply, that operates only in the run mode. The run mode power supply for certain loads, such as the deflection circuits and high voltage screen loads, typically employ the flyback transformer that powers beam deflection. A separate or auxiliary power supply also can be operated as a switched mode supply and may provide a regulated B+ voltage for the flyback transformer as well as other auxiliary supply voltages.

Projection televisions, for example, have particularly demanding power needs because they have three high power cathode ray tubes (CRTs). An auxiliary power supply is useful to power the convergence amplifiers for the tubes, two such amplifiers generally being required for each CRT. These amplifiers require positive and negative polarity voltages and can dissipate substantial power.

In a switched mode supply, an input DC voltage (such as the B+ voltage in a television) is coupled to one terminal of a primary winding of a transformer and the other terminal of the primary winding is coupled to a switching device, such that current is

2

coupled to the transformer when the switching device conducts. The switching device is alternately turned on and off during the run mode of operation, providing alternating currents in secondary windings of the transformer, which are rectified and filtered to provide run mode supply voltages.

5

10

15

20

25

30

35

Regulation of the output voltages is achieved by feedback control provided by, for example, a feedback winding of the The respective secondary windings are closely transformer. coupled, so that load variations on any of the secondary windings are reflected on the feedback winding. The feedback control compares a voltage on the feedback winding with a standard or threshold voltage level, which may be provided by the switching device, and modulates the frequency and/or pulse width at which the switching circuit is turned on and off. The switching device is compensated to render it insensitive to variation of the raw B+ input voltage, while maintaining accurate output voltage levels as current loading varies over a nominal range of power consumption.

The switching device for a power supply as described can be an integrated circuit (IC) power supply controller from the Sanyo This controller includes a FET power switching STK730 series. transistor, an error amplifier and driver, and an over-current protection circuit in a single package. When coupled into a switched mode supply and first turned on, current from the B+ voltage flows to ground through the primary winding of the transformer, the FET and a current sensing resistor. increases until the over-current protection circuit in the controller IC is triggered, whereupon the IC controller turns off its FET power transistor. Energy is transferred to the secondary windings of the transformer, where the induced AC current is rectified and After a starting interval of several charges filter capacitors. cycles, the output voltage reaches its regulated level. A threshold comparison circuit provided by the IC controller is coupled to a feedback winding of the transformer and controls the timing of switching by the control IC to maintain the regulated output

3

voltage level. Oscillation stabilizes at a frequency and duty cycle that accommodate the loads coupled to the secondary windings. Many other power supply controllers operate in a similar fashion and may be used instead of the Sanyo STK730 series.

5

10

15

20

25

30

35

Such an IC controller will attempt to start whenever the raw B+ voltage is present. Other switched circuits control switching between the standby mode and the run mode. In a situation wherein the apparatus is switched quickly and repeatedly between the run and standby modes of operation, it is necessary for the auxiliary power supply to reset quickly so that its output voltages may be approximately equal to their nominal output voltage levels when the apparatus is switched from a standby If, for example, the apparatus is shifted mode to a run mode. from the run mode to the standby mode and then back to the run mode in rapid succession, the run mode output voltages of the auxiliary power supply may be prevented from coming up and attaining their nominal output voltage levels. This would hinder proper operation of the apparatus.

It would be advantageous to control switching between the standby and run modes of the apparatus in a manner that enables the auxiliary power supply to reset quickly, so as not to prevent completion of the startup phase of the auxiliary power supply when the apparatus is shifted from a standby mode to a run mode following a rapid succession of changes in its operational mode.

A switched power supply according to inventive arrangements taught herein provides a quick-reset capability when an apparatus containing the power supply is rapidly switched between run and standby modes of operation. The quick-reset capability enables the power supply to consistently provide output voltages which are within nominal output voltage levels despite rapidly repeated dislocations in the operational mode of the apparatus.

In such a switched power supply, an on/off switch control turns the power supply on and off as the apparatus changes between the standby and run modes of operation. The quick-

4

reset circuit is coupled to the on/off switch control and to a delay circuit which contains a startup delay capacitor that charges when the apparatus is switched from standby mode to run mode. The quick-reset circuit is energized by a transition from the run mode to the standby mode and rapidly discharges the startup delay capacitor upon such transition.

5

10

15

20

25

30

A switched power supply according to the inventive arrangements described herein comprises: a voltage source, a transformer and a switching controller coupled for switched-mode generation of an output supply voltage; a feedback circuit for regulating the switched-mode operation responsive to loading on the output supply voltage; a switching circuit responsive to an on/off signal for turning the power supply on and off by controlling conduction in a conduction path, the power supply being turned on by a conductive condition in the conduction path; a delay circuit responsive to the on/off signal and continuously energized by current after the power supply is turned on; and, a reset circuit responsive to the switching circuit for discharging energy from the delay circuit.

The on/off signal may be a run mode supply voltage generated by another power supply in the apparatus. The voltage source may be an unregulated, rectified mains voltage source.

A voltage provided by the delay circuit may be limited. The delay circuit may comprise: a capacitor; a Zener diode coupled in parallel with the capacitor; and, a resistance coupling the on/off signal to a cathode of the diode. A delay time provided by the delay circuit may be established by the capacitor and the resistance.

The reset circuit may complete discharging of the delay circuit before the on/off signal reaches a minimum level. The reset circuit may comprise a semiconductor switch responsive to the switching circuit for discharging the capacitor.

The above, and other features and advantages of the present invention will become apparent from the following description

5

read in conjunction with the accompanying drawings, in which like reference numerals designate the same elements.

FIGURE 1 is a block diagram of an auxiliary power supply having control circuitry in accordance with inventive arrangements.

5

10

15

20

25

30

FIGURE 2 is a schematic diagram of the auxiliary power supply having control circuitry in accordance with inventive arrangements and illustrating on/off control in more detail.

FIGURE 3 is a schematic diagram of an auxiliary power supply having control circuitry in accordance with inventive arrangements and illustrating start up and fault detection circuitry in more detail.

FIGURE 4 is a schematic diagram of an auxiliary power supply having a current overload detection circuit in accordance with inventive arrangements.

FIGURE 5 is a schematic diagram of an auxiliary power supply having a quick-reset circuit in accordance with inventive arrangements.

FIGURE 1 generally shows an inventive switched mode power supply 10 having a switching controller U1 operable periodically to apply current from a voltage input, for example a raw B+ voltage, to a primary winding W1 of a transformer T1 for variably coupling power to one or more secondary windings W2, W3, W4 and W5 of transformer T1. The switching controller U1 can comprise, for example, a Sanyo STK730 series controller. Switching controller U1 conducts when a driving voltage, for example the raw B+ voltage, is available on its control input CNTL at pin 4.

The raw B⁺ input supply voltage is a direct current voltage obtained from the output of a bridge rectifier CR1 filtered by a capacitor C1. The raw B⁺ voltage is present whenever the power supply 10 is coupled to the domestic mains 22 (i.e., plugged in). However, the power supply 10 only operates in a run mode, and is disabled in a quiescent or standby mode.

When power supply 10 is plugged in and is also in the run mode, the raw B+ voltage is present at the control input CNTL of switching controller U1, thus enabling switching controller U1 to conduct a current through the primary winding W1 of transformer T1. The current flow through winding W1 induces a voltage across winding W2 of transformer T1, which voltage is applied to the control input CNTL through resistor R13 and capacitor C5. The polarity of winding W2 is such that the voltage induced across winding W2 keeps switching controller U1 conducting.

Switching controller U1 ceases conducting current through primary winding W1, or turns off, when the current conducted by switching controller U1 reaches a current limit threshold that is set by the combination of resistor R14 and capacitor C6. When switching controller U1 ceases conducting, the magnetic field of primary winding W1 collapses, its polarity reverses and the energy contained in primary winding W1 is transferred to windings W4 and W5, which supply power to the +15 V and -15 V, respectively, outputs.

As the energy from windings W4 and W5 becomes exhausted, their magnetic fields collapse and their polarities reverse. In accordance with the polarities of windings W2, W4 and W5, winding W2 provides a positive voltage to pin 4 of switching controller U1, thereby enabling switching controller U1 to once again conduct current through primary winding W1 until the current limit threshold of switching controller U1 has been reached and switching controller U1 ceases conducting current. Energy is then again transferred from primary winding W1 to windings W4 and W5. This process repeats for several cycles, until the operation of power supply 10 has stabilized.

Feedback winding W3 controls the duty cycle of switching controller U1 after the operation of power supply 10 has stabilized. The voltage developed across feedback winding W3 is compared with an internal reference, equal to approximately -40.5 V, developed by switching controller U1. The duty cycle of switching controller U1 is modulated such that the voltage

7

developed across feedback winding W3 is maintained approximately equal to -40.5 V. Feedback winding W3 is coupled to the secondary windings W4 and W5 so that load changes are reflected in the voltage developed across feedback winding W3. Thus, feedback winding W3 is also used to regulate the output voltages developed by windings W4 and W5.

5

10

15

25

30

35

Normally, switching from the standby mode to the run mode or vice versa is accomplished under user control via control inputs (not shown) such as an infrared receiver, panel switches or the like. According to an inventive aspect, additional run/standby switching circuits 36 are provided to shift the power supply 10 between the operational run mode and the non-operational standby mode. Switching controller U1 requires a large start-up current. For dependable starting and assistance in developing this drive current, the run/standby switching circuits 36 include a first circuit 38 coupled between the raw B+ voltage input and the control input CNTL, for providing a voltage bias to enable conduction by the switching controller whenever the raw B+ voltage input is present.

In accordance with an inventive arrangement, the drive current bias provided from first circuit 38 can be shunted away to reduce the available drive current to disable the switching controller U1. The drive current can be shunted to a source of reference potential, for example ground.

The run/standby switching circuits 36 further comprise a fault condition detection circuit 42 coupled to at least one of the transformer secondary windings W4 and W5. The circuit 42 senses a fault condition, such as current overloading on the auxiliary power supply, for example by sensing a low voltage threshold on the output coupled to the same or another secondary winding W4 or W5. The circuit 42 generates an output 41 indicative of a fault condition to disable conduction of switching controller U1 by pulling control input CNTL of switching controller U1 to a ground potential, as a means for switching the auxiliary power supply off, as though the apparatus had been changed to

8

the standby mode of operation. In order to make certain that the startup phase of the auxiliary power supply is not prevented by a false detection of a fault condition, due to initial low voltage output levels, a delay circuit 40 inhibits the effect of the output of the fault condition detection circuit 42 for a sufficient period of time for the nominal output voltage levels of the auxiliary power supply to be established.

5

10

15

20

25

30

3 5

FIGURES 2 and 3 illustrate in detail different aspect of the inventive arrangements shown generally in FIGURE 1. reference numbers are used throughout the drawings to refer to the same or comparable elements. Referring to FIGURE 2. switching controller U1 is coupled in series with primary winding W1 of transformer T1. Switching controller U1 alternately conducts and turns off, for transferring power to the secondary windings W4 and W5, where the resulting AC signal is rectified by diodes D2 and D3 and filtered by capacitors C2 and C3, The filtered voltages provided on windings W4 and W5 are further filtered by chokes L2 and L3, respectively, to provide operational supply voltages +15 V and -15 respectively, for powering loads in the run mode.

The polarities of secondary windings W4 and W5 are opposite that of the primary winding W1, as shown in FIGURE 2, such that capacitors C2 and C3 are charged when switching controller U1 turns off and the energy stored in the primary winding W1 of transformer T1 is transferred to windings W4 and W5.

According to an inventive aspect, the power supply 10 as shown is arranged to further control the voltage at control input CNTL of switching controller U1 for controlling shifts between run and standby modes. When the device is in standby mode and switching controller U1 is not conducting periodically, the only power going into the power supply 10 is the raw B+ voltage, which is present because the device is coupled to domestic mains 22. It would be possible in controlling run/standby operation to couple and decouple the raw B+ voltage to the switching elements of the

9

power supply 10 using a relay or other switching device powered from a supplemental low power supply (not shown). However, according to the invention a more cost effective solution is obtained by using a signal derived in part from the raw B+ voltage and in part from the run mode voltages, to reduce the bias on control input CNTL to switching controller U1, namely to bring the voltage on the control input to near ground to hold switching controller U1 off until normal bias is restored.

5

10

15

20

25

30

3 5

Thus, a voltage divider comprising resistors R1, R2, R3 and R4 is coupled between the raw B+ voltage and ground, and the junction J1 of the voltage divider is coupled to the base of a switching transistor Q2, having its collector coupled to the control input and its emitter grounded. When the raw B+ voltage is present, control input CNTL is pulled to near ground by conduction of transistor Q2. When the power supply 10 is first coupled to the mains, it is held in standby mode.

The invention is advantageously applied to an auxiliary power supply such as the auxiliary supply of a television for powering run mode loads such as convergence amplifiers. For switching into the run mode, the inventive power supply senses the presence of a run mode supply voltage developed from a source other than the secondary windings of transformer T1. This run mode supply voltage is compared to a threshold level, and when the threshold level is passed, transistor Q2 is turned off, permitting the bias on control input CNTL of switching controller U1 to return to normal and permit operation of the auxiliary power supply in the run mode, namely under feedback control by feedback winding W3 of transformer T1. For example, the +23 V supply that is developed by the run mode operation of the deflection and other circuits in a television can be used for this purpose.

Referring to FIGURE 2, a differential pair of PNP transistors Q3 and Q4 have their emitters coupled to the run mode supply voltage by resistor R5, and differentially compare the level of the run mode supply voltage, via the voltage divider of resistors R6

10

and R7 on the base of transistor Q3, with a reference voltage of +8.2 V provided by Zener diode Z3 on the base of transistor Q4. When the run mode supply exceeds a level determined by the ratio of resistances in the voltage divider, transistor Q4 conducts and switches on optocoupler U3. The phototransistor of optocoupler U3 grounds the base of transistor Q2, which ceases conducting, thereby permitting normal bias on control input CNTL of switching controller U1. Operation of the power supply 10 then commences in the run mode responsive to the voltages on the secondary windings W2 and W3 of transformer T1.

5

10

15

20

25

Another inventive embodiment is shown in FIGURE 3, and includes a latching circuit that has the additional function of detecting current overload conditions, when in the run mode, for switching the power supply 10 into the standby mode. overloading causes the output voltage level to drop below nominal, because in overcurrent conditions the overcurrent protection circuits of switching controller U1 turn switching controller U1 off before sufficient power has been coupled through the power supply 10 to maintain the nominal output voltage level. This method of current limiting is less than optimal for powering loads such as the digital convergence amplifiers of a projection television. For such loads, it is advantageous if the power supply 10 can be turned off when an overcurrent condition occurs, instead of attempting to supply current to the loads at reduced voltage. According to the invention, this function is achieved in a manner that interfaces with the circuits controlling switching between the run and standby modes as in FIGURE 2.

In FIGURE 3, control for switching from standby to run mode is provided in part by the run mode supply voltage, such as the +23 V run supply, passing a predetermined voltage as determined by the differential transistor pair Q3 and Q4, which provide current to the LED of optocoupler U3. The phototransistor of optocoupler U3 then turns off transistor Q2 and permits operation of switching controller U1. Resistors R1, R2, R3 and R4 provide 35 bias to transistor Q2 at junction J1 from the raw B+ supply voltage.

11

In comparison to the embodiment of FIGURE 2, in which the cathode of the LED in optocoupler U3 is grounded, according to FIGURE 3, the current through the LED charges a capacitor C4, through the base of a PNP transistor Q5.

5

10

15

20

25

30

Capacitor C4 provides for a delay upon first switching from the standby mode into the run mode, in which the power supply 10 can start up. When the supply 10 is running and the regulated voltage, in this case nominally +15 V, exceeds approximately +10 V, Zener diode Z4 conducts through resistors R8 and R9, and turns on transistor Q6. The current from optocoupler U3 is then shunted to ground through transistor Q6 and capacitor C4 stops charging. Transistor Q5 is then off and capacitor C4 cannot discharge through either transistor Q5 or through diode D6, which is coupled to the +23 V run mode supply and is reverse biased.

In the event that the +15 V output voltage falls below the level needed to cause Zener diode Z4 to conduct, especially in the case of a current overload on secondary winding W4, transistor Q6 turns off due to insufficient base drive. With transistor Q6 off, capacitor C4 can charge from the current through optocoupler U3. When the charge on capacitor C4 reaches approximately +10 V, transistor Q5 turns off, and there is no path for the current In that case, although differential through optocoupler U3. transistors Q3 and Q4 still detect the presence of the +23 V run supply, no current is conducted by the phototransistor of optocoupler U3. The raw B+ supply turns on transistor Q2 due to the voltage divider formed at junction J1 by resistors R1, R2, R3 The control input CNTL of switching controller U1 is The power supply 10 shuts off, protecting the loads pulled low. coupled to the outputs. Thus, unlike a power limiting solution wherein the current limiting circuits of the switching controller reduce the output voltage below nominal but continue to supply power, the inventive circuit as described switches off the power supply 10 in overcurrent conditions. This is accomplished using the run/standby circuits driven from the raw B+ power supply,

1 2

providing a current overload protective function with a minimum of parts and complexity.

As illustrated in FIGURES 1 and 3, fault condition detection circuit 42 is utilized to detect current overload conditions on the +15 V output of power supply 10. Detection of overload conditions on the -15 V output is complicated by the fact that exclusively positive-polarity biasing voltages, for example raw B+, are used in power supply 10.

An additional inventive arrangement, shown in FIGURE 4, advantageously and elegantly provides for detection of current 10 overload conditions on the -15 V output in the absence of negative-polarity bias voltages. Detection of a current overload condition on the -15 V output, when in the run mode, causes the power supply 10 to be switched into the standby mode. FIGURE 4, the negative supply voltage overload detection circuit 43 is coupled between the +15 V and -15 V outputs of power supply 10. The Zener diode Z6 is biased between the +15 V and -15 V outputs of the power supply 10, such that the base of transistor Q8 has a bias voltage that is equal to approximately -2 V when the -15 V output is nominally loaded. The Zener diode Z6 thus provides a level-shifting mechanism, or a dc offset, that enables the -15 V output to be compared against a positive reference voltage, which in this embodiment is the turn-on voltage of the base-emitter junction of transistor Q8, for detecting 25 a current overload condition.

15

20

30

35

If, in response to a current overload condition, the -15 V output begins to drop toward a ground potential, the voltage at the base of transistor Q8 will also tend to move toward ground. Eventually, if the current overload condition persists and the -15 V output consequently reaches a predetermined threshold voltage level, the voltage at the base of transistor Q8 will become positive and will eventually become high enough, for example approximately 0.7 V, to turn on transistor Q8 to signal a current overload condition. Unlike fault condition detection circuit 42, where a current overload condition is signaled by a change in the

13

conductive state of Zener diode Z4, Zener diode Z6 remains in a conductive state when a current overload condition is signaled by transistor Q8. The desired threshold level can be selected by an appropriate choice of the breakdown voltage of Zener diode Z6.

5

10

15

20

25

30

35

When transistor Q8 turns on, current is drawn from the base of transistor Q6, thereby turning transistor Q6 off. Thus, similarly to the detection of an overcurrent condition on the +15 V output, with transistor Q6 off, capacitor C4 can charge from the current through optocoupler U3. When the charge on capacitor C4 reaches approximately +10 V, transistor Q5 turns off, and there is no path for the current through optocoupler U3. In that case, although differential transistors Q3 and Q4 still detect the presence of the +23 V run supply, no current is conducted by the phototransistor of optocoupler U3. The raw B+ supply turns on transistor Q2 due to the voltage divider formed at junction J1 by resistors R1, R2, R3 and R4. The control input CNTL of switching controller U1 is pulled low. The power supply 10 shuts off, protecting the loads coupled to the outputs.

When the +23 V run supply voltage drops, capacitor C4 is discharged through diode D6, which otherwise would be reverse biased by the presence of the +23 V run supply. Once capacitor C4 has discharged, the power supply 10 can be restarted unless there is still an overload condition on the output that prevents development of a sufficient output voltage to turn on transistor Q6 during the delay time in which the charge on capacitor C4 can rise to a sufficient voltage to turn off transistor Q5.

If capacitor C4 is not allowed enough time to fully discharge, for example if switched mode power supply 10 is shifted from the run mode to the standby mode and then back to the run mode in rapid succession, transistor Q5 will remain off. The run mode output voltages will thus be prevented from coming up and attaining their nominal output voltage levels.

A further inventive embodiment shown in FIGURE 5 provides a quick-reset circuit 50 for rapidly discharging capacitor C4 when the +23 V run supply voltage drops. According to the

14

invention, this function is achieved in a manner that interfaces with the circuits controlling switching between the run and standby modes as in FIGURE 2.

In FIGURE 5, the delay circuit 40 has a Zener diode Z5 in parallel with capacitor C4. When the +23 V run supply voltage comes up, capacitor C4 charges through resistor R10 to provide the delay time for the run mode output voltages to stabilize at approximately their nominal output voltage levels. Zener diode Z5 clamps the voltage across capacitor C4 to approximately +10 V to prevent damage to the base-emitter junctions of transistors Q8 and Q9, which are arranged in a Darlington configuration.

5

10

15

20

25

30

Once power supply 10 is in the run mode, transistor Q4 and the diode of optocoupler U3 conduct current, in a manner similar to the embodiment shown in FIGURE 3. Unlike the embodiment in FIGURE 3, however, this current is not used to charge capacitor C4. The arrangement of transistors Q8 and Q9 in a Darlington configuration results in only a minimal current flow in the base of transistor Q9. Thus, the charging rate of capacitor C4, and the delay time caused thereby, is determined exclusively by the time constant formed by resistor R10 and capacitor C4. This advantageously eliminates any variation in the charging rate of capacitor C4 due to the current amplification factor, or beta, of transistor Q5 in FIGURE 3 or the Darlington arrangement of transistors Q8 and Q9 in FIGURE 5.

Referring to FIGURE 5, when power supply 10 is shifted into the standby mode, the +23 V run supply voltage starts to drop. As the run supply voltage drops below a level determined by the ratio of resistances in the voltage divider of resistances R6 and R7, current flow is redirected from transistor Q4 to transistor Q3. The current flowing through transistor Q3 establishes a voltage across resistor R11, which voltage biases reset transistor Q7 on. Capacitor C4 is thereby rapidly discharged to ground through resistor R12 and reset transistor Q7 before the +23 V run voltage has completely decayed.

1 5 CLAIMS

1. A switched power supply, comprising:

1

2

3

4

5

6

7

8

9

12

a voltage source (RAW B⁺), a transformer (T1) and a switching controller (U1) coupled for switched-mode generation of an output supply voltage;

a feedback circuit (W3) for regulating said switched-mode operation responsive to loading on said output supply voltage;

a switching circuit (R5, R6, R7, Q3, Q4, Z3, U3) responsive to an on/off signal (+23 V-RUN) for turning said power supply on and off by controlling conduction in a conduction path, said power supply being turned on by a conductive condition in said conduction path;

a delay circuit (40) responsive to said on/off signal and continuously energized by current after said power supply is turned on; and,

a reset circuit (50) responsive to said switching circuit for discharging energy from said delay circuit.

- 2. The switched power supply of claim 1, wherein said on/off signal (+23 V-RUN) is a run mode supply voltage generated by another power supply in said apparatus.
- 3. The switched power supply of claim 1, wherein said voltage source (RAW B⁺) is an unregulated, rectified mains voltage source.
- 4. The switched power supply of claim 1, wherein said voltage source (RAW B⁺) is an unregulated, rectified mains voltage source and said on/off signal (+23 V-RUN) is a run mode supply voltage generated by another power supply in said apparatus energized by said unregulated, rectified mains voltage source.
- 5. The switched power supply of claim 1, wherein a voltage provided by said delay circuit (40) is limited.

WO 98/21887

16

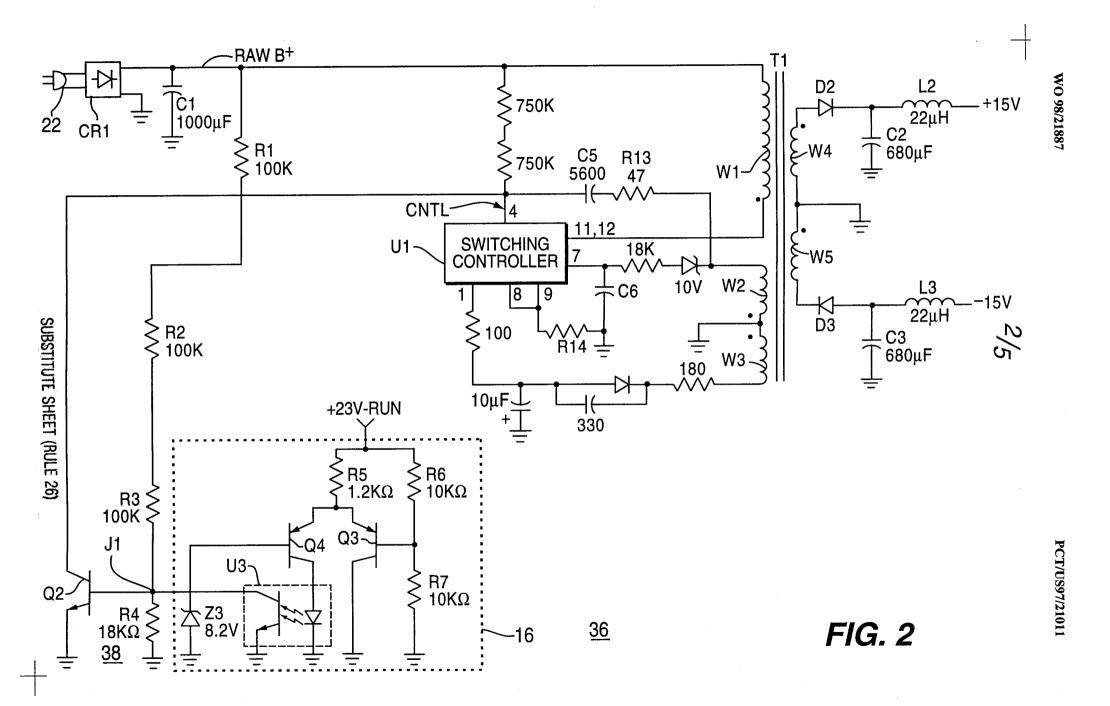
PCT/US97/21011

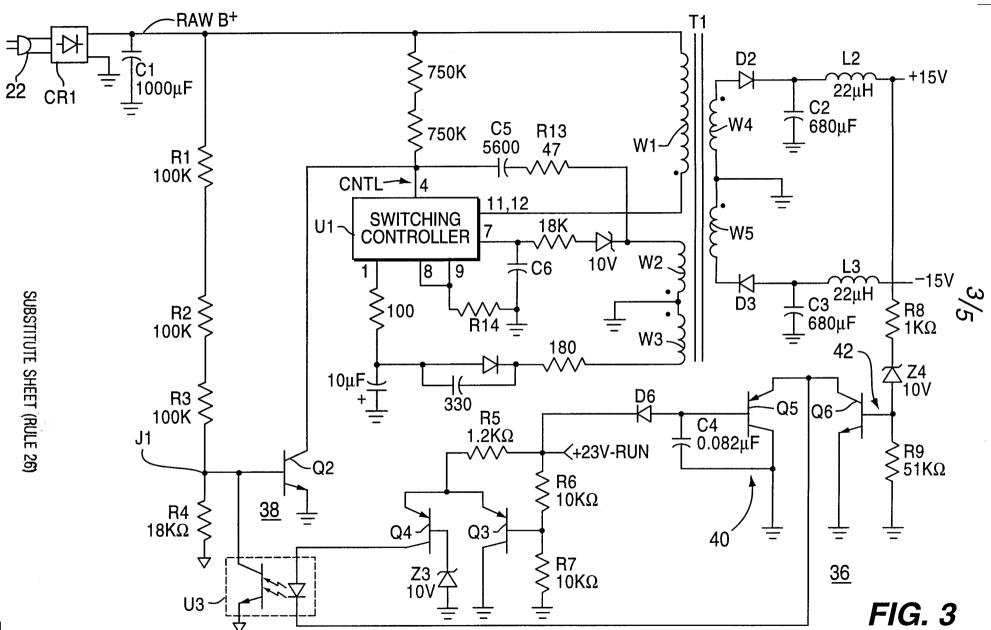
1	6.	The	switched	power	supply	of	claim	5,	wherein	said
2	delay circ									

- a capacitor (C4);
- a Zener diode (Z5) coupled in parallel with said capacitor; and,
- a resistance (R10) coupling said on/off signal (+23 V-RUN) to a cathode of said diode.
- 7. The switched power supply of claim 6, wherein a delay time provided by said delay circuit (40) is established by said capacitor (C4) and said resistance (R10).
- 8. The switched power supply of claim 6, wherein said reset circuit (50) completes discharging of said delay circuit (40) before said on/off signal (+23 V-RUN) reaches a minimum level.
- 9. The switched power supply of claim 8, wherein said reset circuit (50) comprises a semiconductor switch (Q7) responsive to said switching circuit (R5, R6, R7, Q3, Q4, Z3, U3) for discharging said capacitor (C4).

PCT/US97/21011

WO-98/21887





INTERNATIONAL SEARCH REPORT

Int. Lational Application No PCT/US 97/21011

		L	
A. CLASSI IPC 6	FICATION OF SUBJECT MATTER H04N5/63		
According to	o International Patent Classification(IPC) or to both national class	ification and IPC	**************************************
B. FIELDS	SEARCHED		
Minimum do IPC 6	ocumentation searched (classification system followed by classific H04N H02M	ation symbols)	
	tion searched other than minimumdocumentation to the extent tha		
Electronic d	lata base consulted during the international search (name of data	base and, where practical, search terms used	,
C. DOCUM	ENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the	relevant passages	Relevant to claim No.
A	US 4 761 702 A (PINARD JIM) 2 A see column 2, line 31 - line 47 see the whole document		1,3
А	PATENT ABSTRACTS OF JAPAN vol. 005, no. 163 (E-078), 20 0 & JP 56 091678 A (MATSUSHITA E CO LTD), 24 July 1981, see abstract		1
А	EP 0 588 168 A (RCA THOMSON LIC CORP) 23 March 1994 see abstract see column 8, line 29 - column figure 1		1
		-/	
X Furt	her documents are listed in the continuation of box C.	X Patent family members are listed	in annex.
° Special ca	ategories of cited documents :	"T" later document published after the inte	rnational filing data
consid	ent defining the general state of the art which is not dered to be of particular relevance document but published on or after the international	or priority date and not in conflict with cited to understand the principle or th invention	the application but leory underlying the
filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of posters.		 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the 	
"O" docum other i "P" docume	ent referring to an oral disclosure, use, exhibition or means ent published prior to the international filing date but	cannot be considered to involve an in document is combined with one or m- ments, such combination being obvio in the art.	ore other such docu-
later th	han the priority date claimed	"&" document member of the same patent	
	actual completion of theinternational search	Date of mailing of the international sea	arch report
1	2 March 1998	23/03/1998	
Name and r	mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk	Authorized officer	
	Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Fuchs, P	

1

INTERNATIONAL SEARCH REPORT

In. ational Application No
PCT/US 97/21011

Category Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. A US 4 751 580 A (FITZGERALD WILIAM V ET AL) 14 June 1988 see abstract; figure		Jation) DOCUMENTS CONSIDERED TO BE RELEVANT
AL) 14 June 1988	Relevant to claim No.	Citation of document, with indication, where appropriate, of the relevant passages
	1-4	AL) 14 June 1988
		·

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int .tional Application No PCT/US 97/21011

cited in search report	Publication date	Patent family member(s)	Publication date
US 4761702 A	02-08-88	CA 1287103 A DE 3713378 A FR 2599870 A GB 2191050 A,B JP 62250827 A	30-07-91 29-10-87 11-12-87 02-12-87 31-10-87
EP 0588168 A	23-03-94	CN 1085697 A EP 0588172 A EP 0588173 A JP 6225172 A US 5349515 A US 5351177 A US 5349516 A	20-04-94 23-03-94 23-03-94 12-08-94 20-09-94 27-09-94 20-09-94
US 4751580 A	14-06-88	NONE	