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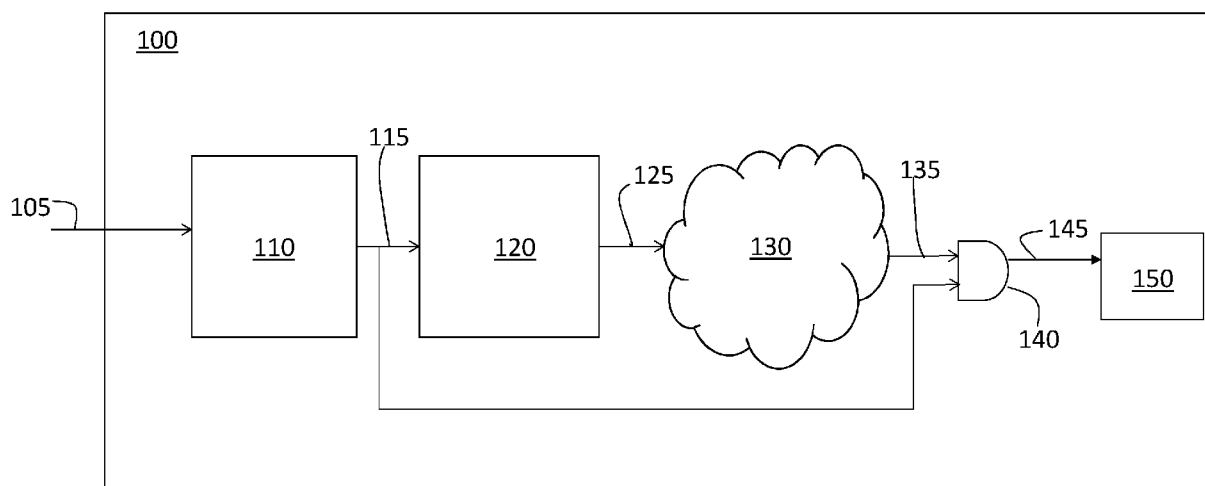


FIG. 1

(57) Abstract: An integrated circuit with a hardware-based controller enables a system for a set of clock cycles and selectively enables an aspect of the system for a subset of the set of clock cycles. The controller includes a clock cycle select circuit to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system, and a test start circuit to receive the test select signal and output a test signal to the system to enable the system for the set of clock cycles. The controller also includes an AND gate to output a gated signal to enable the aspect of the system for the subset of the set of clock cycles based on the test select signal.



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ON-CHIP HARDWARE-CONTROLLED WINDOW STROBING

BACKGROUND

[0001] The present invention relates to on-chip testing, and more specifically, to on-chip hardware-
5 controlled window strobing.

[0002] In an integrated circuit or chip, different components are triggered by clock signals. One example of a component that is triggered by a clock signal is a built-in self-test (BIST) engine. BIST refers to
10 hardware, software, or a combination of the two, which is built into an integrated circuit or chip and used to test the operation of the chip. For example, logic BIST (LBIST) tests the functional logic of the chip, and array BIST (ABIST) tests arrays or memory of the chip.
15 Typically, BIST runs over millions of clock cycles until testing is completed, and tests results are accumulated in a pass or fail format.

SUMMARY

[0003] According to an embodiment of the present
20 invention, a hardware-based controller in an integrated circuit enables a system for a set of clock cycles and selectively enables an aspect of the system for a subset of the set of clock cycles. The controller includes a clock cycle select circuit configured to output a test
25 select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system, and a test start circuit configured to receive the test select signal and output a test signal to the system to enable the system for the set of clock cycles.

The controller also includes an AND gate configured to output a gated signal to enable the aspect of the system for the subset of the set of clock cycles based on the test select signal.

5 **[0004]** According to another embodiment of the present invention, an integrated circuit includes a system, and a hardware-based controller configured to enable the system for a set of clock cycles and selectively enable an aspect of the system for a subset of the set of clock
10 cycles. The controller includes a clock cycle select circuit configured to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system, and a test start circuit configured to receive the test select
15 signal and output a test signal to the system to enable the system for the set of clock cycles. The controller also includes an AND gate configured to output a gated signal to enable the aspect of the system for the subset of the set of clock cycles based on the test select
20 signal.

[0005] According to yet another embodiment of the invention, a method of fabricating an integrated circuit to control a system in the integrated circuit to be enabled for a set of clock cycles and an aspect of the
25 system to be selectively enabled for a subset of the set of clock cycles includes fabricating a clock cycle select circuit to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system. The method also includes
30 fabricating a test start circuit to receive the test select signal and output a test signal to the system to

enable the system for the set of clock cycles, and arranging an AND gate to output a gated signal to enable the aspect of the system for the subset of the set of clock cycles based on the test select signal.

5 BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing and other features, and
10 advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0007] FIG. 1 is a block diagram of an integrated circuit with a system to perform on-chip hardware-
15 controlled window strobing according to one or more embodiments;

[0008] FIG. 2 details the system to perform on-chip hardware-controlled window strobing according to an exemplary embodiment;

20 [0009] FIG. 3 details the system to perform on-chip hardware-controlled window strobing according to another exemplary embodiment;

[0010] FIG. 4 details the system to perform on-chip hardware-controlled window strobing according to yet
25 another exemplary embodiment;

[0011] FIG. 5 shows exemplary strobe signals according to one or more embodiments to target or exclude specific clock cycles;

[0012] FIG. 6 shows exemplary strobe signals according to one or more embodiments to search for a fail;

[0013] FIG. 7 is a process flow of a method of performing targeted testing according to one or more
5 embodiments; and

[0014] FIG. 8 is a process flow of a method of performing failure identification according to one or more embodiments.

DETAILED DESCRIPTION

10 [0015] As previously noted, components of a chip are triggered by a clock signal. One example that is discussed herein for explanatory purposes is a BIST engine, also referred to as BIST logic. BIST can be used to test different aspects of chip operation. Exemplary
15 self-test engines include ABIST, LBIST, and architecture verification patterns (AVP). These tests are accomplished by functional code loaded into on-chip data and instruction storage. The tests typically run over millions of clock cycles. That is, the control signal
20 that triggers operation of the BIST is held at "1" (i.e., is high) over all the clock cycles of the tests.

[0016] Once the tests are completed, test results are provided in an accumulated pass/fail format. For example, the multiple-input signature register (MISR) is
25 used to convert output bits into a signature that can be compared with a fault-free signature to determine a pass or fail condition. A fault address register (FAR) holds the address at which a synchronous abort occurred, and AVP passcount values are obtained. Generally, the BIST

state machines store the output in an array and output a signal to a comparator to compare the data in the array with expected data. When a failure occurs during a BIST operation, the accumulated result does not provide
5 insight as to which section of the test sequence resulted in the failure. Thus, a separate control signal to control the comparison portion facilitates selecting particular clock cycles of the self-test for which the data array is compared with expected data or is omitted
10 from the comparison.

[0017] In this regard, embodiments of the systems and methods detailed herein relate to on-chip hardware controlled window strobing. That is, the embodiments pertain to controlling a component (e.g., BIST engine) to
15 run for a given number of clock cycles while additionally controlling an aspect of the component (e.g., stored data comparison) to be selectively on or off for a subset of the clock cycles. This selectively turning on and off is referred to as strobing. In the exemplary case of the
20 BIST engine, the strobing is provided by hardware elements that facilitate greater granularity (at the clock cycle level) of the at-speed test result observation or failure analysis. Specifically, one or more clock cycles can be isolated for test result
25 analysis or, if a known fault is to be masked, specific clock cycles can be omitted from test analysis. The testing itself, in terms of the setup or stimulation pattern, need not be modified and, according to some of the embodiments, already available test signal functions
30 may be reused for the strobing to avoid additional circuitry to obtain the additional diagnostic features.

[0018] FIG. 1 is a block diagram of an integrated circuit 100 with a system to perform on-chip hardware-controlled window strobing according to one or more embodiments. For explanatory purposes, window strobing of output from a BIST engine 130 is discussed with reference to FIG. 1. The BIST engine 130 can perform ABIST or LBIST or implement AVP, for example. As previously noted, the window strobing or enabling at selected clock cycles can be used to drive other components or aspects of components of the integrated circuit 100, as well. The system discussed with reference to FIG. 1 is a hardware-based controller that includes a clock cycle select circuit 110, test start circuit 120, and strobe application AND gate 140.

[0019] The clock cycle select circuit 110 can be implemented by different embodiments, as detailed with reference to FIGS. 2-4, and facilitates the window strobing or clock cycle selection. The test start circuit 120 ensures that the component (BIST engine 130 in the exemplary case) is operated as normal despite the strobing of an aspect of the BIST operation and is detailed with reference to FIG. 2. External signals from outside the integrated circuit 100 can be input to the clock cycle select circuit 110 according to one or more embodiments. The clock cycle select circuit 110 provides a test select signal 115 to the test start circuit 120 and also to the aspect controlled by the strobing, which is the comparator 150 in the exemplary case. The test start circuit 120 outputs a test signal 125 to the BIST engine 130 to facilitate normal operation of the BIST engine. The BIST engine 130 outputs a compare enable signal 135, which is controlled by the

strobing according to the test select signal 115 and the strobe application AND gate 140. The strobe application AND gate 140 applies the strobing to the compare enable signal 135 to output a gated compare enable signal 145
5 that ultimately drives the comparator 150 according to the embodiments detailed herein.

[0020] FIG. 2 details the system to perform on-chip hardware-controlled window strobing according to an exemplary embodiment. The clock cycle select circuit
10 110a according to the embodiment shown in FIG. 2 reuses existing clock signals as the external signals 105a from outside the integrated circuit 100. An alternate current (AC) clock signal 205 is supplied to an edge detector 210. The output of the edge detector 210 and a direct
15 current (DC) clock signal 215 are input to an AND gate 220. The output of the AND gate 220 is provided to an on-chip clock generator 225. Thus, the on-chip clock generator 225 only receives a "1" or start signal from the AND gate 220 when both the output of the edge
20 detector 210 of the AC clock signal 205 and the DC clock signal 215 are "1." The on-chip clock generator 225 is the component that enables the BIST engine 130 and maintains its operation throughout the testing. Specifically, the trigger signal 230 output by the on-
25 chip clock generator 225 is "1" for all the clock cycles associated with testing by the BIST engine 130.

[0021] The DC clock signal 215 is optionally also provided to latches 240 (e.g., flip flops) that provide a strobe (on/off) signal to AND gate 245. The latches 240
30 latch to the DC clock signal 215 and are needed for high-speed applications (e.g., on other order of gigahertz

(over 5 gigahertz)), for example. The AND gate 245 only outputs a "1" when the trigger signal 230 and the output of the latches 240 are both "1." This AND gate 245 provides the strobe.

5 **[0022]** As FIG. 2 indicates, the trigger signal 230 is provided to a multiplexer 265 and a rising edge detector 235, in addition to the AND gate 245. The rising edge detector 235, which detects the rising edge of the trigger signal 230, provides output to an OR gate 250.
10 The rising edge detector 235 being "1" indicates that the trigger signal 230 has transitioned to "1," which indicates a start of the BIST engine 130, as discussed with reference to the multiplexer 265.

[0023] The rising edge detector 235 output is "0" (i.e., is low) for the remainder of the testing duration. The output of the AND gate 245 is also provided to the OR gate 250. The output of the AND gate 245 is "1" only when both the trigger signal 230 and the output of the latches 240 (i.e., the latched DC clock signal 215) are
20 "1." As previously noted, the trigger signal 230 is "1" for the duration of testing by the BIST engine 130. The latches 240 output the window strobe signal and, thus, the AND gate 245 outputs the window strobe. Because, after the initial transition to "1" of the trigger signal
25 230 at the start of testing, the edge detector 235 outputs a "0," the OR gate 250 only outputs a "1" when the AND gate 245, which follows the strobing according to the DC input signal 215, is "1."

[0024] As previously described, when the AC clock
30 signal 205 goes to "1" to indicate the start of testing, the rising edge detector 235 outputs a "1", thereby

making the strobe enable signal 255 output by the OR gate 250 a value of "1" regardless of the DC clock signal 215. This leads to the multiplexer 265 outputting a "1" as the test select signal 115a for the first clock cycle of the testing by the BIST engine 130. That is, the rising edge detector 235 enable the initial value of the test select signal 115a to be "1" based solely on the AC clock signal 205 and regardless of the DC clock signal 215.

[0025] After the first clock cycle of testing by the BIST engine 130, the multiplexer 265 receives a "1" as the trigger signal 230 and a "1" or "0" as the strobe enable signal 255. The value of the strobe enable signal 255 is determined by the DC clock signal 215 and, consequently, the AND gate 245 and OR gate 250. Another input to the multiplexer 265 is a strobe override signal 260. The strobe override signal 260 is a control signal that can override the strobe enable signal 255 and is set for the duration of the testing.

[0026] When the strobe override signal 260 is "0," the normal operation of the BIST engine 130 is performed. In this case, both the signal provided to the BIST engine 130 (test signal 125) and the signal provided to the comparator 150 (gated compare enable signal 145) being "1" for the duration of testing. When the strobe override signal 260 is "1," then the window selection of clock cycles within the testing duration (the strobe window) is performed according to the DC clock signal 215. In this case, the signal provided to the BIST engine 130 (test signal 125) is "1" for the duration of testing, but the signal provided to the comparator 150 (gated compare enable signal 145) is controlled to be

either "1" or "0" based on the DC clock signal 215. The test select signal 115a that is output by the multiplexer 265 is "1" at the start of testing and is then either "1" or "0" according to the strobe window.

5 **[0027]** The test start circuit 120 receives the test select signal 115a from the clock cycle select circuit 110a and the strobe override signal 260. The test start circuit 120 ensures that the test signal 125 that is provided to the BIST engine 130 remains at "1" for the
10 entire duration of testing. The AND gate 270 receives the strobe override signal 260 and the test select signal 115a. Thus, the output signal 275 of the AND gate 270 is "1" only when the strobing is enabled for the testing duration (i.e., strobe override signal 260 is "1") and
15 the test signal 125 is "1." This output signal 275 and the test select signal 115a are provided to an OR gate 280. The OR gate 280 output 285 will be "1" when the test select signal 115a, the output signal 275, or both are "1."

20 **[0028]** During the duration of the test, the output 285 will remain "1." This is because either the test select signal 115a will remain at "1" (when the strobe override signal 260 is "0") or the output signal 275 of the AND gate 270 will remain "1" (when the strobe override signal
25 260 is "1"). The output signal 275 of the AND gate 270 will remain "1" when the strobe override signal 260 is "1" because the initial value of "1" for the test select signal 115a will be held by the latches 290, 295, which are in a master-slave configuration. As a result, the
30 test signal 125 that is fed back to the AND gate 270 will be "1." The result of the strobe override signal 260 and

the test signal 125 being "1" is that the output signal 275 of the AND gate 270 will be "1," as well.

[0029] As the BIST engine 130 operates, data is stored in memory arrays of the integrated circuit 100. The BIST engine 130 outputs a compare enable signal 135. In a prior system that does not include the strobing function, the compare enable signal 135 is provided directly to the comparator 150 and initiates a comparison of the data stored in the arrays by the BIST engine 130 with expected data for every clock cycle. According to the embodiments of the invention, the compare enable signal 135 of the BIST engine 130 is gated. Specifically, the test select signal 115a and the compare enable signal 135 are input to the strobe application AND gate 140. The compare enable signal 135 is always "1" but, when the strobe override signal 260 is "1" (i.e., window strobing is enabled), the test select signal 115a is either "1" or "0" based on the clock cycles that are of interest. Thus, when the strobe override signal 260 is "1" (i.e., window strobing is enabled), the gated compare enable signal 145 that drives the comparator 150 is either "1" or "0" based on the test select signal 115a. That is, the comparator 150 only compares data saved in the array by the BIST engine 130 when the test select signal 115a, which reflects the value of the DC clock signal 215, is "1."

[0030] FIG. 3 details the system to perform on-chip hardware-controlled window strobing according to another exemplary embodiment. The embodiment shown in FIG. 3 includes a simplified clock cycle select circuit 110b compared with the clock cycle select circuit 110a

according to the embodiment shown in FIG. 2. The test start circuit 120 and the operation of the strobe application AND gate 140 are the same for both embodiments. Thus, these components are not described again with reference to FIG. 3. The test start circuit 120 ensures that the test signal 125 provided to the BIST engine 130 is "1" for the duration of the testing. The strobe application AND gate 140 applies the window strobing to the compare enable signal 135 from the BIST engine 130 when the strobe override signal 260 is "1," thereby indicating that window strobing is enabled.

[0031] The clock cycle select circuit 110b shown in FIG. 3 does not receive the AC clock signal 205 and DC clock signal 215. As such, the clock cycle select circuit 110b does not include the edge detector 210, AND gate 220, and latches 240 that are shown in FIG. 2. The external signals 105b that are input to the clock cycle select circuit 110b include a start signal 305 and a tester pin input 325. The start signal 305 is provided to an on-chip clock generator 310. The start signal 305 stays at "1" for the duration of testing. As a result, the trigger signal 315 that is output by the on-chip clock generator stays at "1" for the duration of the testing by the BIST engine 130. Like the trigger signal 230 in the clock cycle select circuit 110a shown in FIG. 2, the trigger signal 315 is provided to a multiplexer 340, a rising edge detector 320, and an AND gate 330. The AND gate 330 also receives the tester pin input 325. Like the DC clock signal 215 in the embodiment shown in FIG. 2, the tester pin input 325 is the input of the strobing control.

[0032] The rising edge detector 320 outputs a "1" when the trigger signal 315 first goes to "1" but then remains at "0" for the remainder of the testing. After the initial clock cycle, during which the rising edge
5 detector 320 outputs a "1," the output of the OR gate 335, which is provided to the multiplexer 340 along with the trigger signal 315, is only "1" when the output of the AND gate 330 is "1." Because the trigger signal 315 is held at "1," the tester pin input 325 is determinative
10 of the output of the AND gate 330. That is, the AND gate 330 outputs a "1" (thereby making the output of the OR gate 335 a "1") when the tester pin input 325 is "1," and the AND gate 330 outputs a "0" (thereby making the output of the OR gate 335 a "0") when the tester pin input 325
15 is "0."

[0033] Because the initial output of the rising edge detector 320, at the start of testing, is a "1," the initial output of the OR gate 335 is "1." As a consequence, the test select signal 115b, which is output
20 by the multiplexer 340, is "1" when the testing by the BIST engine 130 is initiated. This is true regardless of the tester pin input 325. Subsequently, the test select signal 115b is either "1" or "0" according to the tester pin input 325 when strobing is enabled (i.e., the strobe
25 override signal 260 is "1"). This is because, as in the embodiment shown in FIG. 2, another input to the multiplexer 340 is the strobe override signal 260. Thus, the test select signal 115b follows the tester pin input 325 in the same way that the test select signal 115a
30 follows the DC clock signal 215 in the embodiment of FIG. 2 when strobing is enabled.

[0034] As previously noted, the remainder of the circuitry is the same in the embodiment of FIG. 3 as it is in FIG. 2. Accordingly, when the strobe override signal 260 is "0" (i.e., when strobing is disabled during testing), then the test select signal 115b value stays at "1" for the duration of the test, and when the strobe override signal 260 is "1" (i.e., when strobing is enabled), then the test select signal 115b value is either "0" or "1" based on the test select signal 115b. Ultimately, when the strobe override signal 260 is "1," the gated compare enable signal 145 that driver the comparator 150 follows the tester pin input 325. As such, controlling the tester pin input 325 facilitates controlling the clock cycles for which the comparison of BIST engine output data is compared with expected data.

[0035] FIG. 4 details the system to perform on-chip hardware-controlled window strobing according to yet another exemplary embodiment. The embodiment shown in FIG. 4 is further simplified from the embodiment shown in FIG. 3. Specifically, the clock cycle select circuit 110c is simplified in comparison to the clock cycle select circuits 110a and 110b. The test start circuit 120 and the operation of the strobe application AND gate 140 are again the same as in the embodiments described with reference to FIGS. 2 and 3. Thus, these components are not described again with reference to FIG. 4. The test start circuit 120 ensures that the test signal 125 provided to the BIST engine 130 is "1" for the duration of the testing. The strobe application AND gate 140 applies the window strobing to the compare enable signal 135 from the BIST engine 130 when the strobe override

signal 260 is "1," thereby indicating that window strobing is enabled.

[0036] The external signals 105c that are input to the clock cycle select circuit 110c include a start signal 405 and a tester pin input 420. The start signal 405 is provided to an on-chip clock generator 410. The start signal 405 remains at "1" for the duration of testing. As a result, the trigger signal 415 provided by the on-chip clock generator 410 remains at "1" for the duration of the testing by the BIST engine 130. The clock cycle select circuit 110c shown in FIG. 4 does not include the rising edge detector 235 shown in FIG. 2 or the rising edge detector 320 shown in FIG. 3. As a result, the tester pin input 420 must be "1" when the start signal 405 transitions to "1" in order to start the testing by the BIST engine 130. This is because, even though the trigger signal 415 that is provided to the multiplexer 430 and the AND gate 425 remains at "1" for the duration of testing, the output of the AND gate 425 that is also provided to the multiplexer 430 will only be "1" when the tester pin input 420 is also "1." Thus, for the test select signal 115c output by the multiplexer 430 to initially have the value of "1," the tester pin input 420 must be "1."

[0037] Following the first clock cycle of testing, the tester pin input 420 can be selected to control strobing by controlling the value output by the AND gate 425, because the trigger signal 415 value remains at "1." Consequently, when strobing is enabled (the strobe override signal 260 is "1"), the test select signal 115c follows the tester pin input 420. As previously noted,

the remainder of the circuitry is the same in the embodiment of FIG. 4 as it is in FIGS. 2 and 3. Accordingly, when the strobe override signal 260 is "0" (i.e., when strobing is disabled during testing), then the test select signal 115c value stays at "1" for the duration of the test, and when the strobe override signal 260 is "1" (i.e., when strobing is enabled), then the test select signal 115c value is either "0" or "1" based on the test select signal 115c. Ultimately, when the strobe override signal 260 is "1," the gated compare enable signal 145 that driver the comparator 150 follows the tester pin input 420. As such, controlling the tester pin input 420 facilitates controlling the clock cycles for which the comparison of BIST engine output data is compared with expected data.

[0038] FIG. 5 shows exemplary strobe signals according to one or more embodiments to target or exclude specific clock cycles. The BIST engine 130 is an ABIST in the exemplary case. As such, the exemplary test operations (op-1 through op-n) that are performed by the BIST engine 130 pertain to memory array operations. Four exemplary gated compare enable signals 145-W, 145-X, 145-Y, and 145-Z (referred to collectively as 145) are shown. These gated compare enable signals 145 result from the DC clock signal 215 according to the embodiment shown in FIG. 2, from the tester pin input 325 according to the embodiment shown in FIG. 3, or from the tester pin input 420 according to the embodiment shown in FIG. 4.

[0039] All of the gated compare enable signals 145 go to "1" during the start of the test. Thus, even according to the embodiment shown in FIG. 4, which does

not include a rising clock edge detector 235, 320, the test select signal 115a, 115b, 115c is "1" to start the testing by the BIST engine 130. The gated compare enable signals 145-W, 145-X, and 145-Y illustrate selective
5 comparisons for a subset of clock cycles (and associated operations), and the gated compare enable signal 145-Z illustrates selection exclusion of a subset of clock cycles (and associated operations) from comparison by the comparator 150.

10 [0040] The gated compare enable signals 145-W and 145-X are only "1" for one clock cycle. As such, a specific check can be accomplished. For example, the gated compare enable signal 145-W is only "1" for the "read 0" operation. Thus, by only checking the data stored by the
15 BIST engine 130 during the "read 0" operation with expected data, a check can be performed of a data=0 weakness (failure). The gated compare enable signal 145-X is only "1" for the "read ckb" operation. Thus, by only checking the data stored by the BIST engine 130 during
20 the "read ckb" operation with expected data, a check can be performed of checkerboard weakness (failure).

[0041] The gated compare enable signal 145-Y is "1" for more than one clock cycle. Specifically, the gated compare enable signal 145-Y is "1" for the "read0, write
25 1, read 1" operation. Thus, by only checking the data stored by the BIST engine 130 during the "read0, write 1, read 1" operation with expected data, a check can be performed for double address fails (fails related to specific address failing to write or read 0 or read 1).
30 Unlike the gated compare enable signals 145-W, 145-X, and 145-Y, which are only "1" for one or two clock cycles,

the gated compare enable signal 145-Z is "1" for every clock cycle except the ones associated with the "read ckb" and "read1" operations. This type of gated compare enable signal 145 can be used to exclude a known fail
5 from the comparisons made by the comparator 150. That is, if there were known errors in the "read ckb" and "read1" operations, for example, then the gated compare enable signal 145-Z would result in the comparator 150 indicating a pass, because the known errors are
10 explicitly excluded from being among the comparisons made by the comparator 150.

[0042] FIG. 6 shows exemplary strobe signals according to one or more embodiments to search for a fail. The first fail is identified according to the exemplary tests
15 discussed with reference to FIG. 6. The BIST engine 130 is an ABIST in the exemplary case. As such, the exemplary test operations (op-1 through op-n) that are performed by the BIST engine 130 pertain to memory array operations, as in the exemplary case shown in FIG. 5. A
20 sequence of five exemplary gated compare enable signals 145-A, 145-B, 145-C, 145-D, and 145-E (referred to collectively as 145) are shown. As noted with reference to FIG. 5, these gated compare enable signals 145 result from the DC clock signal 215 according to the embodiment
25 shown in FIG. 2, from the tester pin input 325 according to the embodiment shown in FIG. 3, or from the tester pin input 420 according to the embodiment shown in FIG. 4.

[0043] The sequence of gated compare enable signals 145 shown in FIG. 6 facilitate an expeditious approach to
30 finding an operation that fails. First, the gated compare enable signal 145-A is used to compare the

results of a first subset of operations with the expected results. As FIG. 6 indicates, this comparison results in a "pass" according to the example. The gated compare enable signal 145-B is then used to compare the results of a subsequent subset of operations with the expected results. As FIG. 6 indicates, this comparison, too, results in a "pass" according to the example. The gated compare enable signal 145-C is then used to compare the results of a subsequent subset of operations, specifically "writel, readl," with the expected results. As FIG. 6 indicates, this comparison results in a "fail" according to the example.

[0044] At this stage, to isolate the failure to one of the operations within the subset "writel, readl," the output of each of the operations is compared with expected results individually. That is, the gated compare enable signal 145-D enables a comparison of the results of only the "writel" operation with expected results. As FIG. 6 indicates, this comparison results in a "pass" according to the example. The gated compare enable signal 145-E enables a comparison of the results of only the "readl" operation with expected results. As FIG. 6 indicates, this comparison results in a "fail" according to the example. Thus, using a set of six gated compare enable signals 145, the "readl" operation could be isolated as the first failing operation.

[0045] FIG. 7 is a process flow of a method of performing targeted testing according to one or more embodiments. At block 710, calculating clock cycles to target operations of interest includes identifying the one or more clock cycles associated with the operation or

operations to be isolated or excluded. For example, as shown in FIG. 5, the clock cycle associated with the "read 0" operation is determined to generate the gated compare enable signal 145-W. Generating a pattern to isolate or exclude the calculated clock cycles, at block 720, refers to generating the pattern to be issued as the DC clock signal 215 according to the embodiment shown in FIG. 2, the tester pin input 325 according to the embodiment shown in FIG. 3, or the tester pin input 420 according to the embodiment shown in FIG. 4. Executing testing with the comparator 150 being controlled by the pattern, at block 730, refers to the fact that the pattern that is input as the DC clock signal 215 according to the embodiment shown in FIG. 2, the tester pin input 325 according to the embodiment shown in FIG. 3, or the tester pin input 420 according to the embodiment shown in FIG. 4 is that pattern that is ultimately input as the gated compare enable signal 145 to the comparator 150. Once the pattern is determined and used, it can be stored for subsequent testing as needed.

[0046] FIG. 8 is a process flow of a method of performing failure identification according to one or more embodiments. At block 810, identifying a clock cycle associated with a fail can include using a sequence of tests, as discussed with reference to FIG. 6 to identify the clock cycle associated with the "read1" operation. Generating a pattern to exclude clock cycles already associated with a fail, at block 820, refers to generating the gated compare enable signal 145 to exclude the clock cycle identified at block 810 for every iteration of the processes. As previously noted, the

gated compare enable signal 145 is generated according to a specific pattern based on the DC clock signal 215 according to the embodiment shown in FIG. 2, the tester pin input 325 according to the embodiment shown in FIG. 3, or the tester pin input 420 according to the embodiment shown in FIG. 4 being generated according to the specific pattern. Executing testing with the comparator 150 being controlled by the pattern, at block 830, refers to the comparator 150 comparing results stored by the BIST engine 130 with expected results according to the pattern defined by the gated compare enable signal 145.

[0047] At block 840, a check is done of whether the testing outputs a pass result based on all the known fails being excluded from comparison by the comparator 150. If the remainder (non-excluded portion) of the BIST engine 130 output does not match expected results (i.e., the result of the check is no), then another iteration of processes 810 through 840 is performed. If the remainder (non-excluded portion) of the BIST engine 130 output does match expected results (i.e., the result of the check is yes), then performing further testing, at block 850, can refer to several options. The pattern that excludes all the clock cycles associated with fails can be stored for use in subsequent testing. According to an alternate embodiment, a comparison for each of the operations associated with a fail can be run in isolation, according to the discussion with reference to FIG. 5, to further analyze the failing operation by changing test conditions, for example.

[0048] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are
5 intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps,
10 operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, element components, and/or groups thereof.

[0049] The corresponding structures, materials, acts, and equivalents of all means or step plus function
15 elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present
20 invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the
25 scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various
30 embodiments with various modifications as are suited to the particular use contemplated.

[0050] The flow diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the spirit of the invention. For
5 instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

[0051] While the preferred embodiment to the invention
10 had been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for
15 the invention first described.

[0052] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications
20 and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical
25 improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A hardware-based controller in an integrated circuit to enable a system for a set of clock cycles and selectively enable an aspect of the system for a subset
5 of the set of clock cycles, the controller comprising:

a clock cycle select circuit configured to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system;

10 a test start circuit configured to receive the test select signal and output a test signal to the system to enable the system for the set of clock cycles; and

an AND gate configured to output a gated signal to enable the aspect of the system for the subset of the set of
15 clock cycles based on the test select signal.
2. The controller according to claim 1, further comprising a multiplexer of the clock cycle select circuit, wherein the multiplexer is configured to output the test select signal.
- 20 3. The controller according to claim 2, further comprising an on-chip clock generator of the clock cycle select circuit, wherein the on-chip clock generator is configured to receive a clock signal from outside the integrated circuit and output a trigger signal to the
25 multiplexer that remains high for the set of clock cycles.
4. The controller according to claim 2, further comprising an OR gate of the clock cycle select circuit,

wherein the OR gate is configured to output a strobe-enable signal to the multiplexer that is high only for the subset of the set of clock cycles.

5 5. The controller according to claim 4, wherein the OR gate is controlled by a strobe signal from outside the integrated circuit and the strobe-enable signal output of the OR gate is configured to be high only when the strobe signal is high.

10 6. The controller according to claim 2, wherein the multiplexer is configured to receive a strobe override signal and output the test select signal that is high for the set of the clock cycles when the strobe override signal is low.

15 7. The controller according to claim 1, further comprising a set of latches of the test start circuit, the set of latches configured to output the test signal to the system that is high for the set of clock cycles.

20 8. The controller according to claim 1, wherein the system is a built-in self-test (BIST) and the aspect of the system is a comparator configured to compare data output by the BIST for the subset of the set of clock cycles respectively with expected data.

9. An integrated circuit, comprising:

a system; and

25 a hardware-based controller configured to enable the system for a set of clock cycles and selectively enable an aspect of the system for a subset of the set of clock cycles, the controller comprising:

a clock cycle select circuit configured to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the system;

- 5 a test start circuit configured to receive the test select signal and output a test signal to the system to enable the system for the set of clock cycles; and

an AND gate configured to output a gated signal to enable the aspect of the system for the subset of the set of
10 clock cycles based on the test select signal.

10. The integrated circuit according to claim 9, further comprising a multiplexer of the clock cycle select circuit, wherein the multiplexer is configured to output the test select signal.

- 15 11. The integrated circuit according to claim 10, further comprising an on-chip clock generator of the clock cycle select circuit, wherein the on-chip clock generator is configured to receive a clock signal from outside the integrated circuit and output a trigger signal to the
20 multiplexer that remains high for the set of clock cycles.

12. The integrated circuit according to claim 10, further comprising an OR gate of the clock cycle select circuit, wherein the OR gate is configured to output a strobe-
25 enable signal to the multiplexer that is high only for the subset of the set of clock cycles.

13. The integrated circuit according to claim 12, wherein the OR gate is controlled by a strobe signal from outside the integrated circuit and the strobe-enable signal

output of the OR gate is configured to be high only when the strobe signal is high.

14. The integrated circuit according to claim 10, wherein the multiplexer is configured to receive a strobe
5 override signal and output the test select signal that is high for the set of the clock cycles when the strobe override signal is low.

15. The integrated circuit according to claim 9, further comprising a set of latches of the test start circuit,
10 the set of latches configured to output the test signal to the system that is high for the set of clock cycles.

16. The integrated circuit according to claim 9, wherein the system is a built-in self-test (BIST) and the aspect of the system is a comparator configured to compare data
15 output by the BIST for the subset of the set of clock cycles respectively with expected data.

17. A method of fabricating an integrated circuit to control a system in the integrated circuit to be enabled for a set of clock cycles and an aspect of the system to
20 be selectively enabled for a subset of the set of clock cycles, the method comprising:

fabricating a clock cycle select circuit to output a test select signal that indicates the subset of the set of clock cycles during which to enable the aspect of the
25 system;

fabricating a test start circuit to receive the test select signal and output a test signal to the system to enable the system for the set of clock cycles; and

arranging an AND gate to output a gated signal to enable the aspect of the system for the subset of the set of clock cycles based on the test select signal.

18. The method according to claim 17, further comprising
5 arranging a multiplexer as part of the clock cycle select circuit, wherein the multiplexer is configured to output the test select signal.

19. The method according to claim 18, further comprising
10 arranging an on-chip clock generator as part of the clock cycle select circuit, wherein the on-chip clock generator is configured to receive a clock signal from outside the integrated circuit and output a trigger signal to the multiplexer that remains high for the set of clock cycles.

15 20. The method according to claim 18, further comprising arranging an OR gate as part of the clock cycle select circuit, wherein the OR gate is configured to output a strobe-enable signal to the multiplexer that is high only for the subset of the set of clock cycles.

20 21. The method according to claim 20, further comprising coupling a strobe signal from outside the integrated circuit to provide input to the clock cycle select circuit, wherein the OR gate is controlled by the strobe signal and the strobe-enable signal output of the OR gate
25 is configured to be high only when the strobe signal is high.

22. The method according to claim 18, further comprising coupling a strobe override signal to provide input to the clock cycle select circuit and the test start circuit,

wherein the multiplexer is configured to receive the strobe override signal and output the test select signal that is high for the set of the clock cycles when the strobe override signal is low.

5 23. The method according to claim 17, further comprising arranging a set of latches as part of the test start circuit, wherein the set of latches is configured to output the test signal to the system that is high for the set of clock cycles.

10 24. The method according to claim 17, wherein enabling the system includes enabling a built-in self-test (BIST) for the set of clock cycles.

25. The method according to claim 24, wherein enabling the aspect of the system includes enabling a comparator
15 configured to compare data output by the BIST for the subset of the set of clock cycles respectively with expected data.

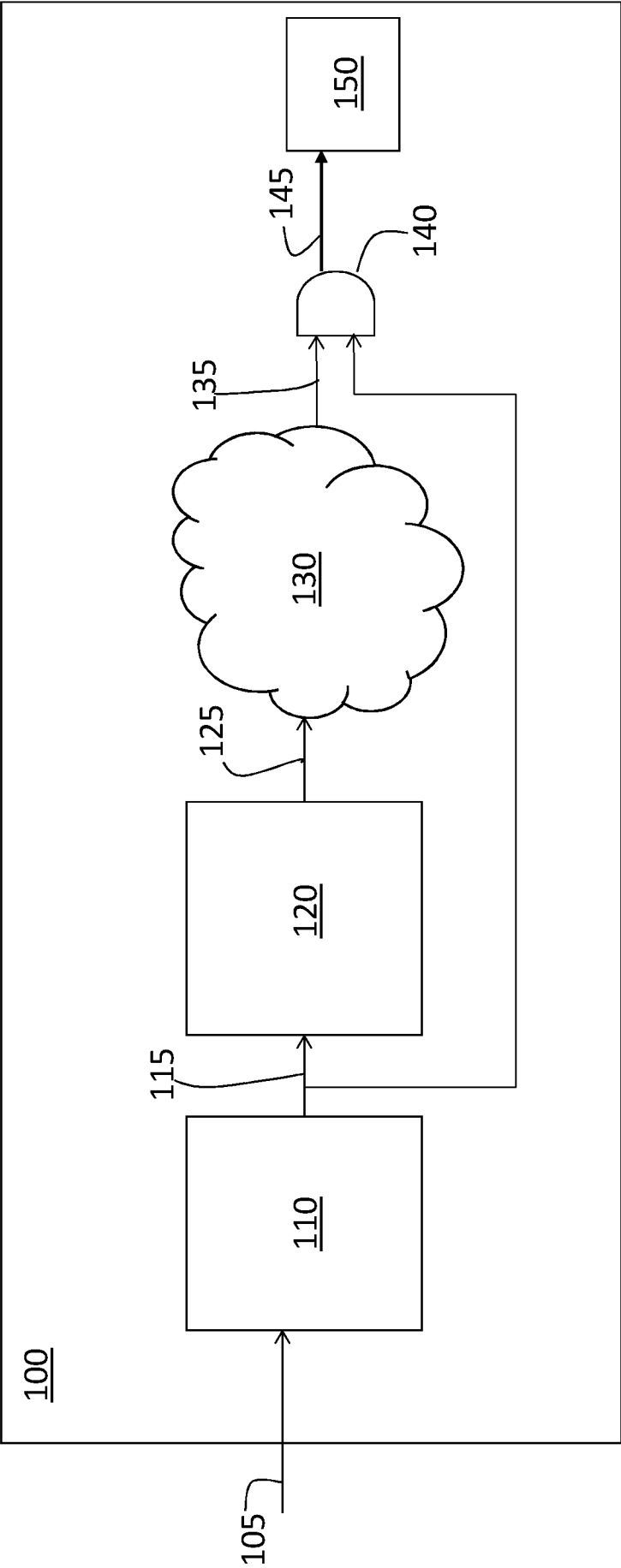


FIG. 1

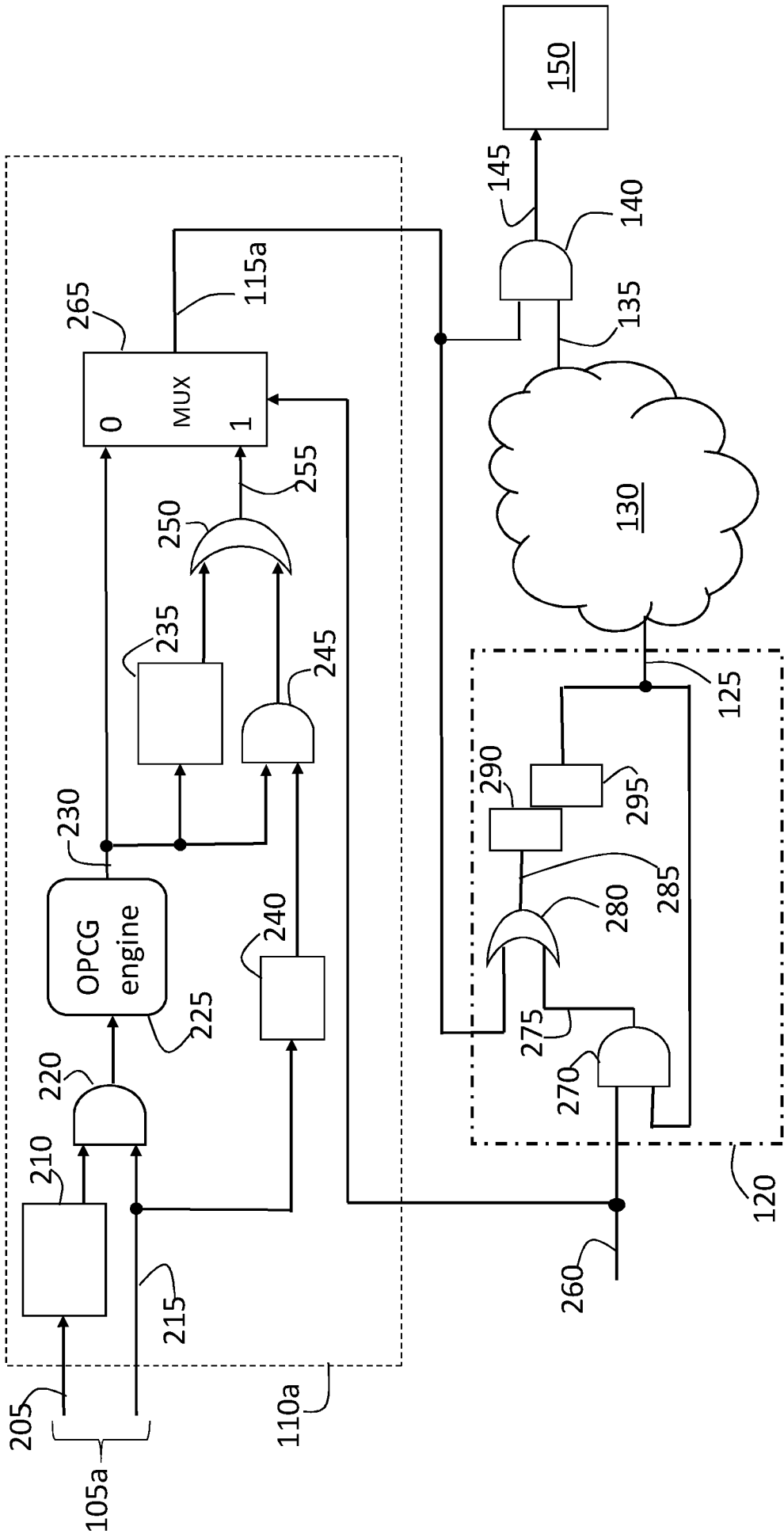


FIG. 2

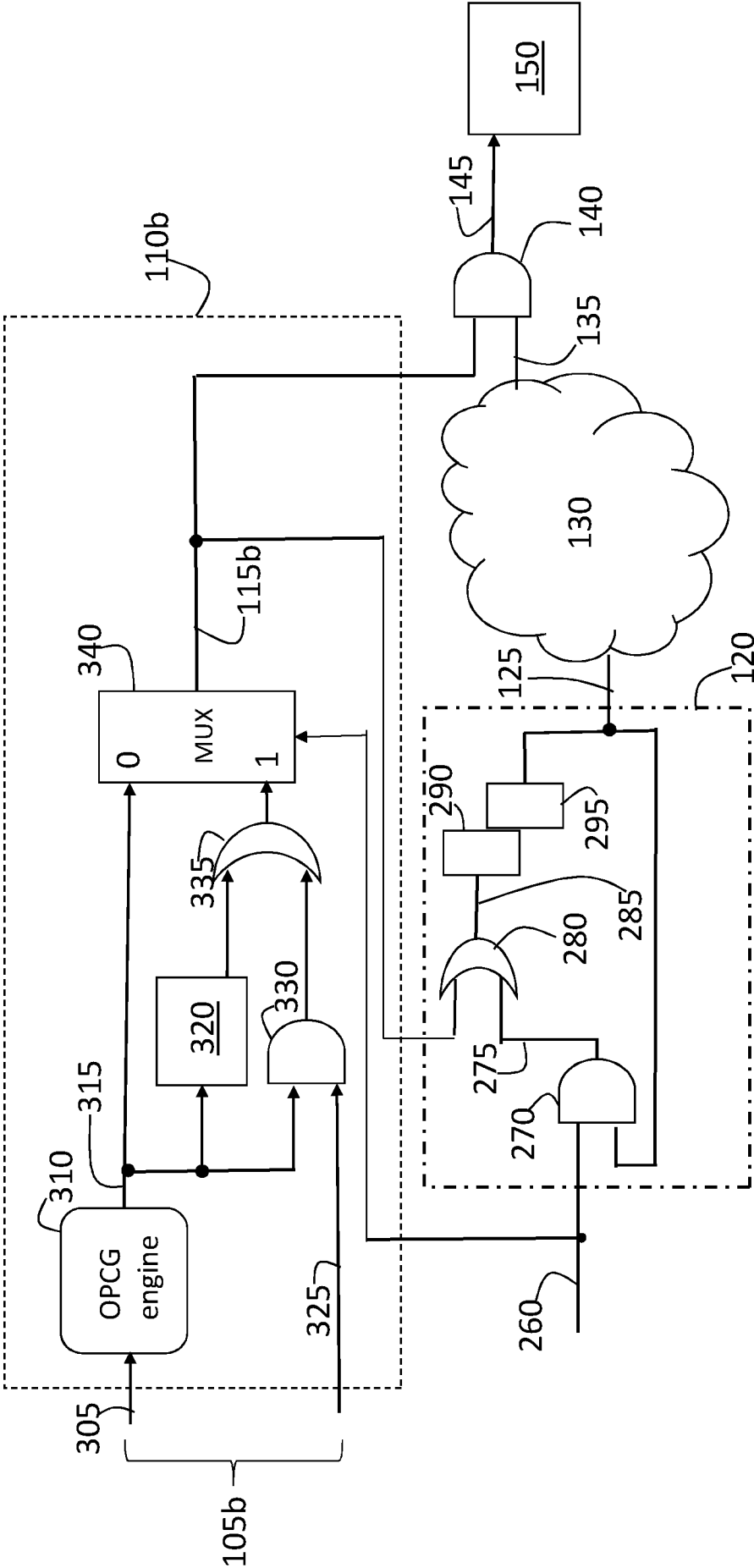


FIG. 3

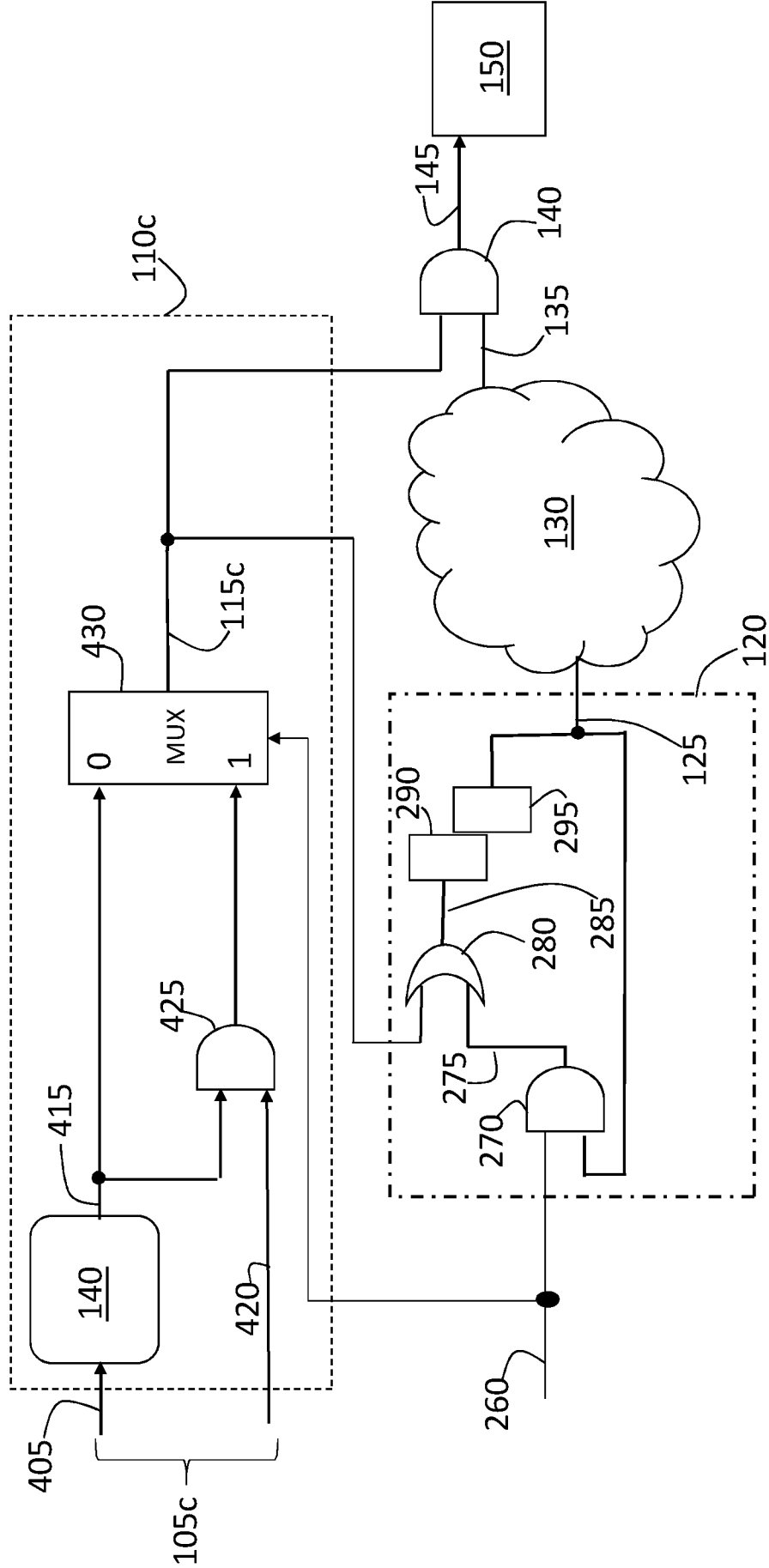


FIG. 4

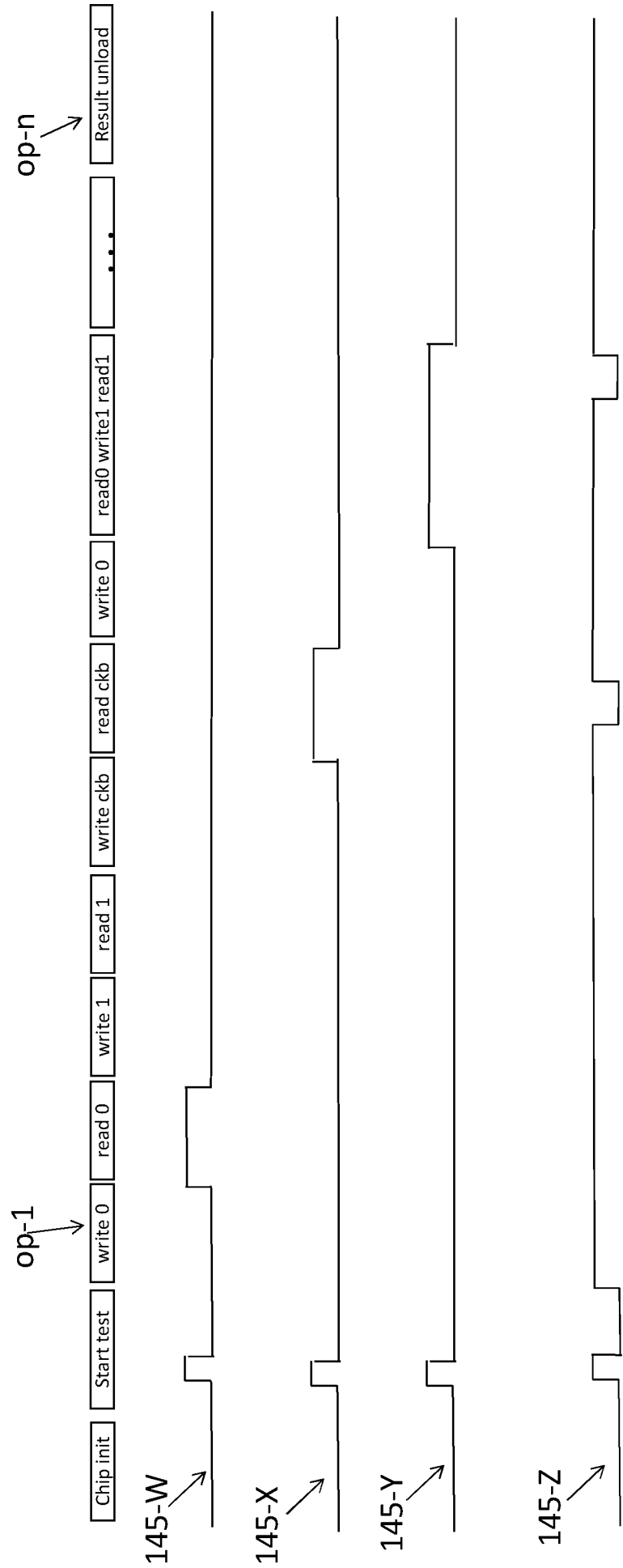


FIG. 5

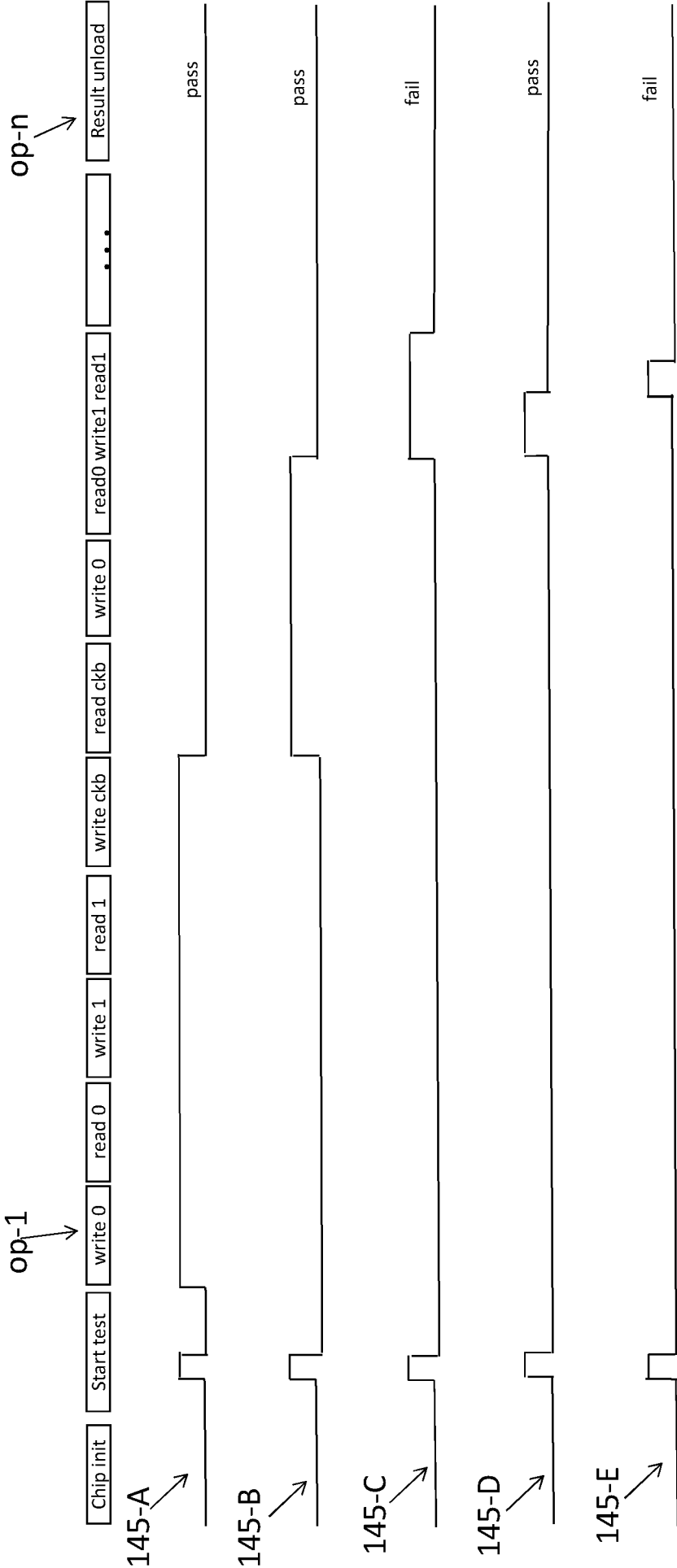


FIG. 6

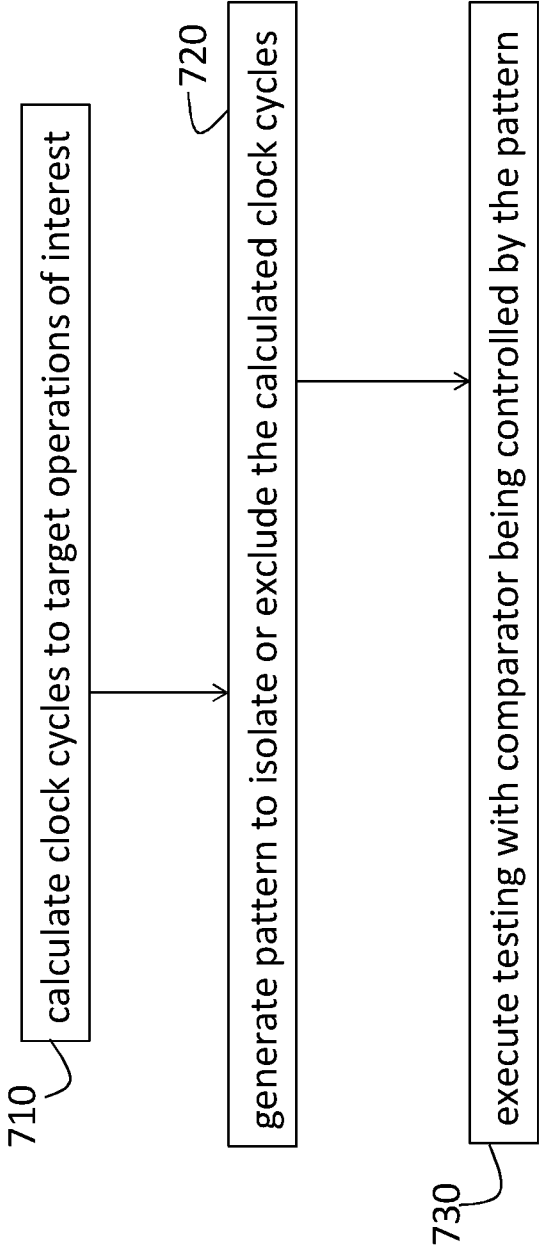


FIG. 7

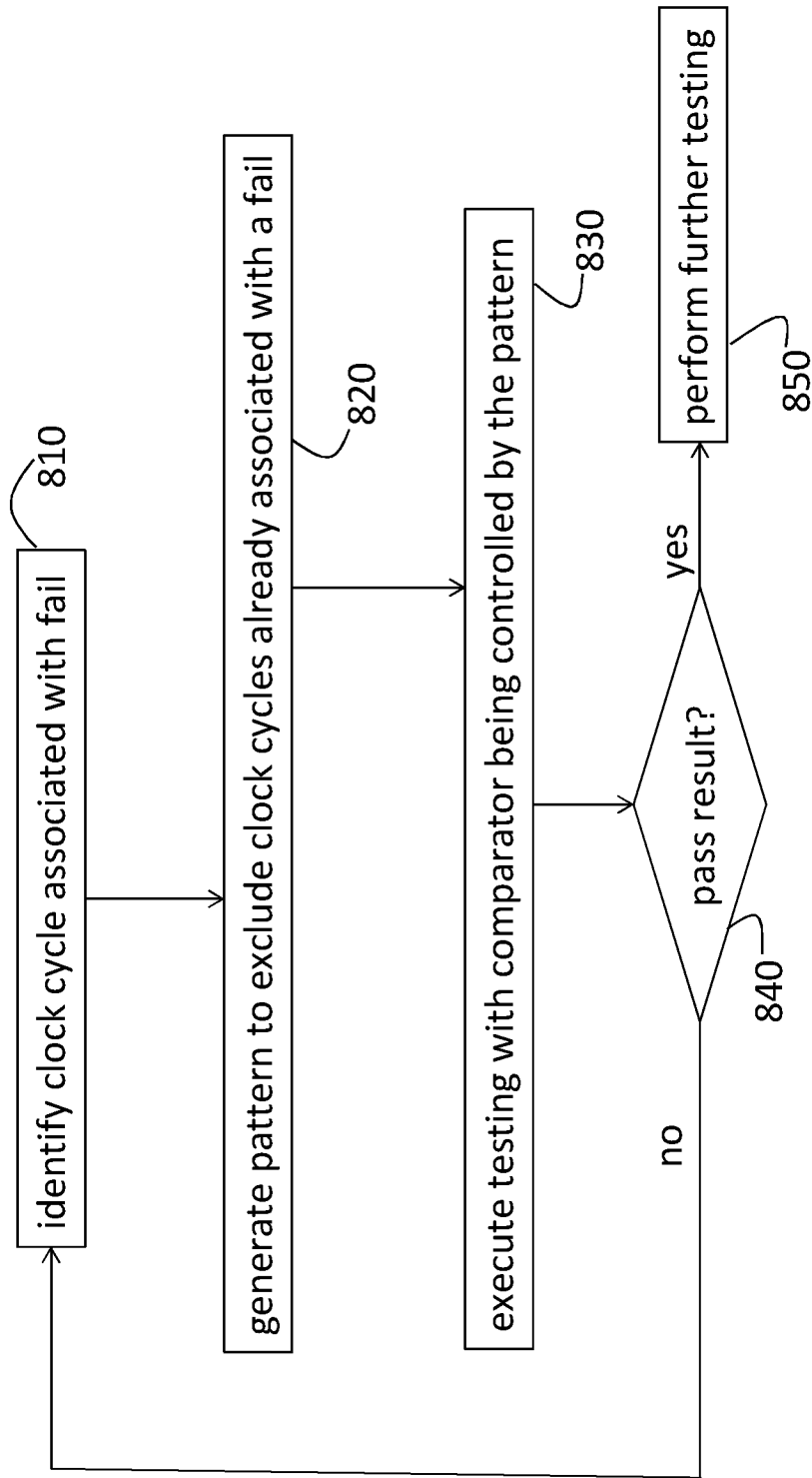


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2018/054354

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/3177(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R, G06F, G11C, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS;CNTXT;CNKI;DWPI;SIPOABS;USTXT;IEEE:TEST, CYCLE?, GAT+, SIGNAL, CONTROLL+, SELECT, ASPECT, CLOCK

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012054568 A1 (KUO MARK T ET AL.) 01 March 2012 (2012-03-01) see the whole document	1-25
A	US 2009232266 A1 (FUJITSU LTD) 17 September 2009 (2009-09-17) see the whole document	1-25
A	US 7630259 B1 (LATTICE SEMICONDUCTOR CORP) 08 December 2009 (2009-12-08) see the whole document	1-25

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

02 September 2018

Date of mailing of the international search report

19 September 2018

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/IB2018/054354

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2012054568	A1	01 March 2012	US	8356221	B2	15 January 2013
US	2009232266	A1	17 September 2009	JP	2009223472	A	01 October 2009
				JP	5082954	B2	28 November 2012
US	7630259	B1	08 December 2009	US	7944765	B1	17 May 2011