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McLeod, Jr. et al.

[11] **3,930,238**

[45] **Dec. 30, 1975**

[54] **DIGITAL APPARATUS**

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[52] **U.S. Cl.** ..... **340/173 R**; 340/172.5

[51] **Int. Cl.²** **G11C 13/00**

[58] **Field of Search** ..... 340/173 R, 172.5, 173 RC

[56] **References Cited**

UNITED STATES PATENTS

2,913,706	11/1959	Thorensen	340/172.5
2,989,731	6/1961	Albanes	340/172.5

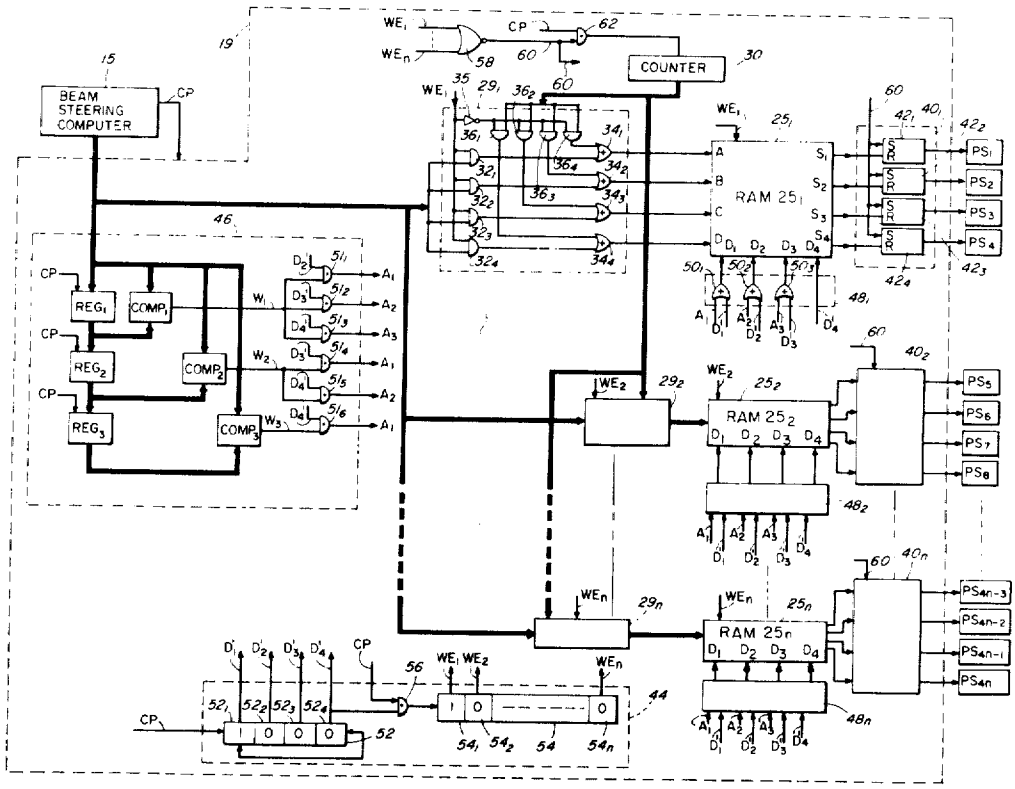
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[57] **ABSTRACT**

Digital apparatus adapted to produce an output pulse having a time duration controlled by a digital word is disclosed. Such apparatus includes an addressable memory for storing a control bit in an address defined by the digital word and means actuated after the storage of the control bit for reading the contents of contiguous addresses of the memory and for initiating the output pulse and means for terminating such output pulse in response to the reading of the control bit from the memory.

6 Claims, 3 Drawing Figures



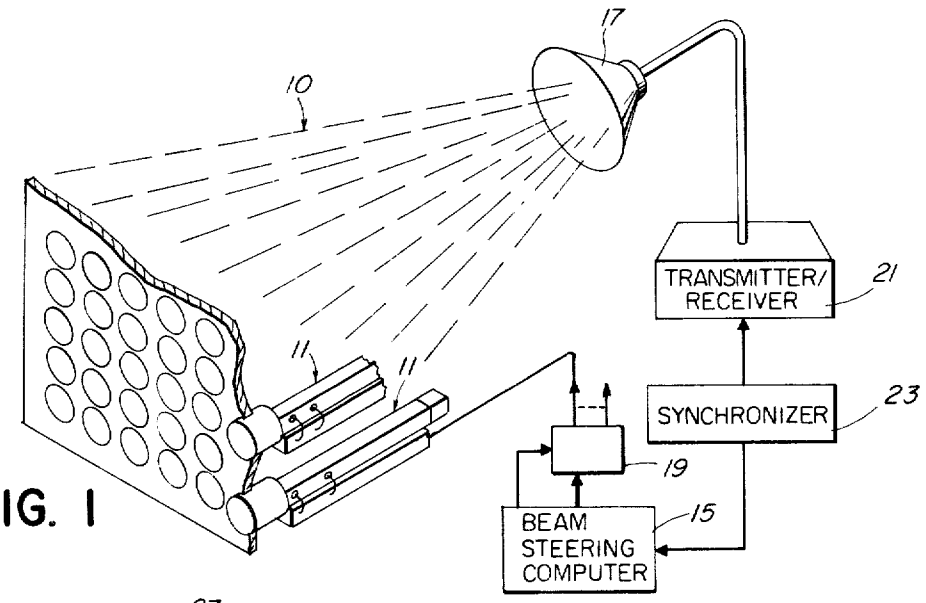


FIG. 1

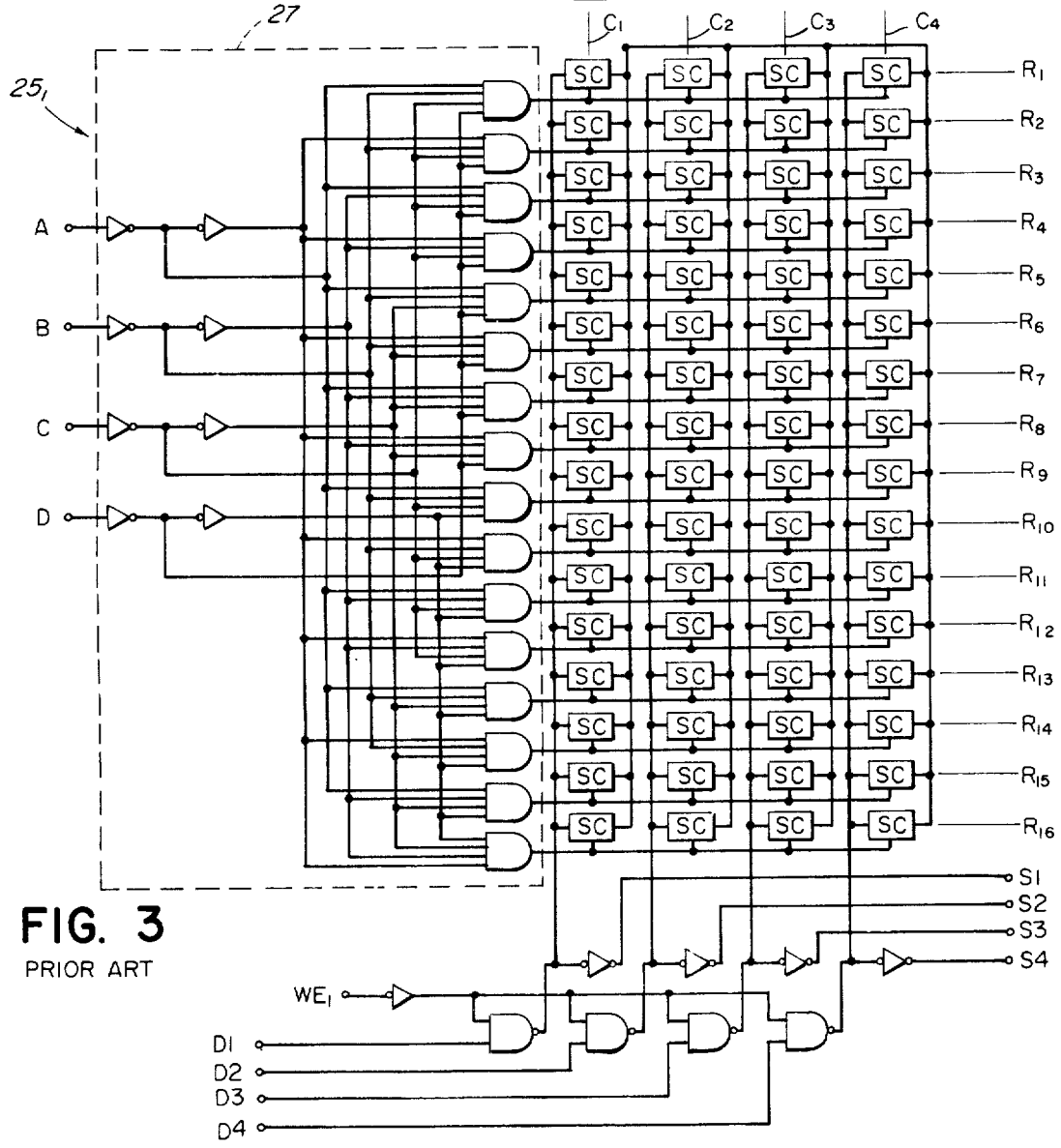


FIG. 3
PRIOR ART

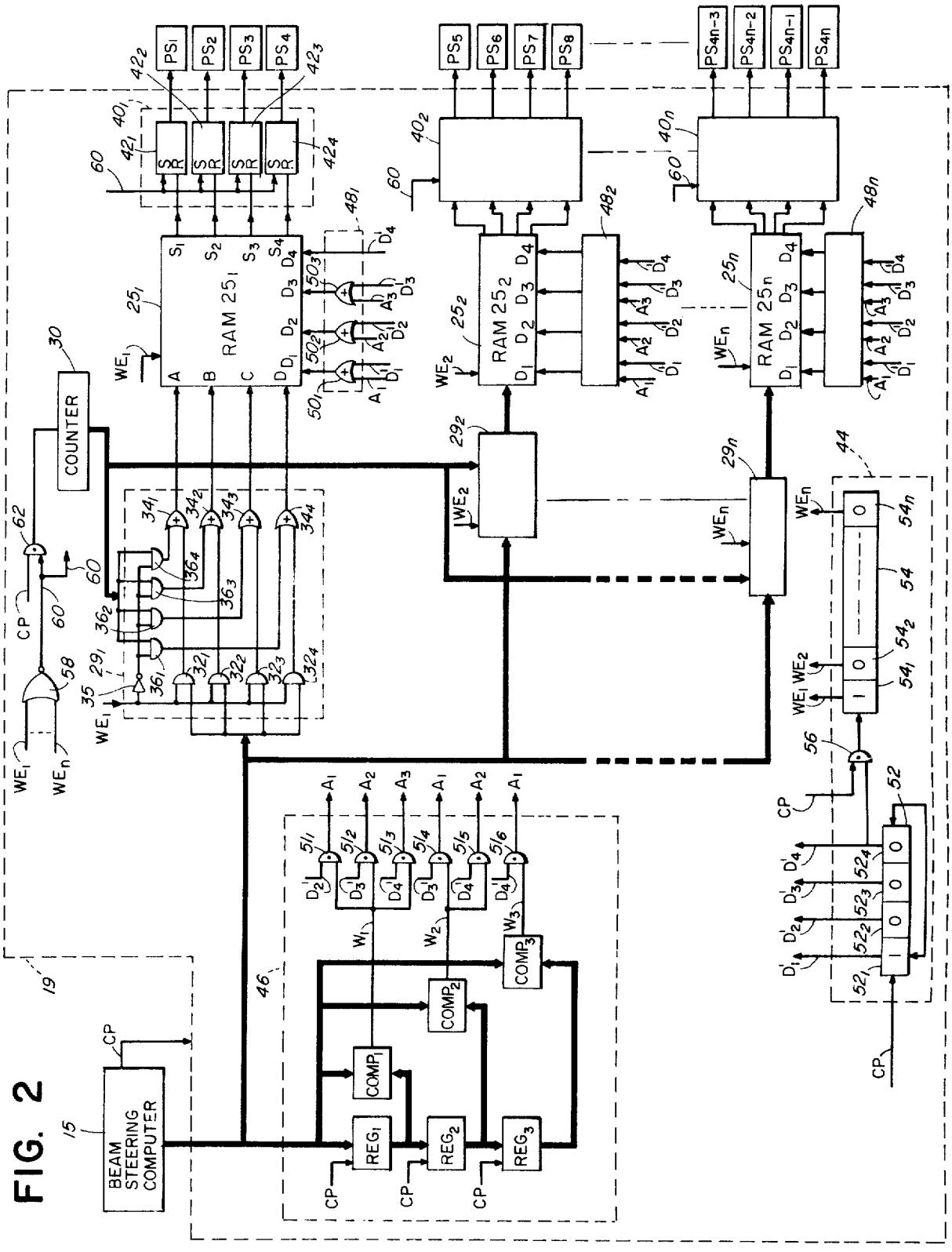

PS1
PS2
PS3
PS4
PS5
PS6
PS7
PS8
PS4n-3
PS4n-2
PS4n-1
PS4n
RAM 25 1
RAM 25 2
RAM 25n
COUNTER
BEAM STEERING COMPUTER
COMP1
COMP2
COMP3
REG1
REG2
REG3
WE1
WE2
WEn
CP

FIG. 2

DIGITAL APPARATUS

BACKGROUND OF THE INVENTION

This invention relates generally to digital apparatus adapted to produce an output pulse having a time duration controlled by a digital word applied to such apparatus and more particularly to digital apparatus of such type which is used to control "flux driven" phase shifters in phased array antennas.

As is known in the art, phased array antennas may include many thousands of antenna elements, each one including a phase shifter, to electronically steer a beam from such an antenna to a desired direction in response to predetermined electrical signals out of a beam steering computer. Various types of phase shifters for such antennas are described in detail in chapter 12, Phase Shifters for Arrays, of the book entitled "Radar Handbook," Editor-In-Chief Merrill I. Skolnik, published by McGraw-Hill Book Company, New York, New York, 1970. As described on pages 12–43 through 12–45 of such book, when an analog phase shifter (sometimes referred to herein as a "flux driven" phase shifter) is used in the phased array antenna, ferrimagnetic material of each phase shifter is first driven to a reference point on the hysteresis loop associated with such material, and then, in response to a control signal supplied by the beam steering computer, such material is driven to a desired flux level on such hysteresis loop. The flux drive technique generally uses the principle that the flux change in the ferrimagnetic material in each phase shifter is proportional to the time integral of a voltage applied to the phase shifter. Therefore, if the amplitude of the voltage applied to the ferrimagnetic material in each phase shifter is a constant, the resulting driven flux is proportional to the time duration of such voltage.

In one known technique used to provide a voltage pulse having a time duration in accordance with a digital word applied by the beam steering computer, the beam steering computer sequentially computes the digital word for each of the phase shifters in an antenna array. As each such digital word is computed, such word is used to initialize the "count" of a digital counter. The computer also provides a "set" signal to a flip-flop, thereby raising the voltage level at the output of such flip-flop at the time the counter is initialized. Clock pulses are coupled to the counter and when the counter is "full" a "reset" signal is applied to the flip-flop thereby to lower the voltage level at the output of the flip-flop. The time duration of the voltage pulse developed at the output of the flip-flop then is related to the number of clock pulses applied to the counter that are required to increase the "count" of the counter from the initialized "count" to the full "count."

While such technique may be found adequate in many applications, such technique generally requires a separate digital counter for each one of the phase shifters thereby adding to the weight, cost and complexity of the phased array antenna.

SUMMARY OF THE INVENTION

In accordance with this invention digital apparatus for producing a control pulse having a time duration in accordance with a digital word includes: An addressable memory means for storing a control bit in an address defined by the digital word; means, actuated after the storage of such control bit, for reading sequentially the contiguous addresses of the memory means and for initiating the control pulse; and, means for terminating such control pulse in response to the occurrence of reading the control bit from the memory means.

In a preferred embodiment the memory means includes a plurality of storage cells arranged in a matrix of rows and columns. The digital word out of the beam steering computer addresses a particular row of memory cells. The first control bit is written into the memory cell located at the addressed row and the first column. Succeeding digital words similarly address rows of the memory means, and control bits correspondingly are written into a memory cell located at each addressed row and each successive column. After a control bit has been written into the memory cell at the last column of the memory means, each row of storage cells is read sequentially and, concurrently with the reading of the first row of cells, a control pulse is initiated. Such control pulse then causes a flux drive signal to be initiated for each associated phase shifter, each such drive signal being terminated when the control bit stored in the column associated therewith is read from the memory means. The pulse time duration to any associated phase shifter then is equal to the time interval between the time the first row of cells is read and the time at which the control bit is read.

With such an arrangement a plurality of conventional random access memories and a single digital counter may be used to flux drive a plurality of phase shifters in a phased array antenna.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the invention, reference is now made to the following description of a preferred embodiment and to the drawings, in which:

FIG. **1** is a simplified sketch of a radar system using an array of antenna elements to radiate a collimated beam of radio frequency energy and to receive echo signals from targets illuminated by such radiated energy in accordance with this invention;

FIG. **2** is a block diagram of digital apparatus used in the radar system of FIG. **1** according to the invention; and

FIG. **3** is a block diagram of a random access memory used in the digital apparatus of FIG. **2** according to the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. **1**, it may be seen that a phased array antenna **10** includes a number of antenna elements **11**, each here including a conventional "flux driven" phase shifter (not shown) using a suitable ferrimagnetic material. The antenna elements **11** may be mounted in any conventional manner (not shown in detail) to form a space-fed planar array. Such an arrangement permits radio frequency energy from a feed horn **17** to be collimated and directed in a beam as desired and echo signals returning to the individual antenna elements **11** to be focused on such feed horn **17**, all in accordance with digital control signals from a beam steering computer **15**. Here such digital control signals, sometimes hereinafter referred to as digital words, are converted to voltage pulses of time durations in accordance with such digital words by digital apparatus **19**, the details of which will be discussed hereinafter. Suffice it to say here, however, that beam steering computer **15** produces, sequentially, digital

words for each of the phase shifters in the phased array antenna **10**. Such words produce control signals which, in turn, are converted into voltage pulses of different time durations. Here such voltage pulses are applied concurrently to the phase shifters, thereby appropriately changing the flux drive to such phase shifters to direct the beam to the desired direction.

Completing FIG. **1**, feed horn **17** is connected, in any convenient manner, as by waveguide (not numbered) to a transmitter/receiver **21**. The operation of the transmitter/receiver **21** and the beam steering computer **15** is controlled by a conventional synchronizer **23**.

Referring now to FIG. **2**, digital apparatus **19** is shown to include a plurality of, here n, identical read/write random access memories 25_1–25_n. Here such read/write random access memories 25_1–25_n are conventional T-T-L (Transistor-Transistor-Logic) semiconductor memories, each having 64 memory cells arranged in a matrix of 4 columns and 16 rows as described on page 9–232 of the book "The Integrated Circuits Catalog for Design Engineers," First Edition, published by Texas Instruments, Incorporated, (an exemplary one thereof, here random access memory 25_1, being shown, for convenience, in FIG. **3**). As shown in FIG. **3**, random access memory 25_1 includes: Four address terminals A, B, C, D; a write enable terminal, WE_1; four data input terminals D_1, D_2, D_3, D_4; and, four data output terminals S_1, S_2, S_3, S_4. In operation, when the level of the signal on the write enable terminal, WE_1, is "high," each bit of the data word applied to data input terminals D_1–D_4 becomes stored in a row of storage cells, SC, such storage cells being disposed in columns C_1–C_4, respectively, and in a row selected by the 4 bit digital word on address terminals A, B, C, D. Such row selection is accomplished in a conventional manner because the 4 bit digital word applied to address terminals A, B, C, D passes through a 4 to 16 decoder **27** (here made up, in a conventional way, of inverters and AND gates, not numbered,) to raise the level of one of the 16 output lines of such decoder in accordance with the 4 bits of such 4 bit digital word to thereby address the storage cells disposed in one of the 16 rows. Thus, when the write enable terminal, WE_1, is "high" the random access memory 25_1 is placed in a "write" condition and each one of the 4 bits of the data word applied to data input terminals D_1–D_4 becomes stored in the storage cells disposed in a different one of the columns C_1–C_4. When the write enable terminal, WE_1, is "low" the random access memory 25_1 is placed in a "read" condition and the storage cells disposed in a row addressed by the 4 bit digital word applied to address terminals A, B, C, D are read and the data stored in the storage cells disposed in columns C_1–C_4 of such selected row appear on output lines S_1–S_4, respectively. That is, output lines S_1–S_4 are, in effect, associated with columns C_1–C_4, respectively, during the "read" condition.

Referring now again to FIG. **2**, the random access memories 25_1–25_n have four address terminals A, B, C, D coupled to beam steering computer **15** and to a 4 bit counter **30** through read/write address selectors 29_1–29_n, respectively, as shown. An exemplary one of the read/write selectors 29_1–29_n, here read/write selector 29_1, is shown to include: (a) A first set of AND gates 32_1–32_4, such AND gates being enabled, when random access memory 25_1 is in a "write" condition, to pass the digital word supplied by beam steering computer **15** (via OR gates 34_1–34_4) to such random access memory; and, (b) a second set of AND gates 36_1–36_4, such second set of AND gates being enabled, when the random access memory 25_1 is in a "read" condition (because of inverter **35**), to pass the digital word supplied by counter **30** (via OR gates 34_1–34_4) to such random access memory. It follows then that when the random access memory 25_1 is in a "write" condition (i.e. when the signal on terminal WE_1 is "high") the digital word produced at the output of the beam steering computer **15** provides the write address for such random access memory and when such random access memory is in a "read" condition (i.e. when the signal on terminal WE_1 is "low") the digital word stored in counter **30** and produced at the output of such counter provides the read address for such random access memory.

Each one of the random access memories 25_1–25_n has its output terminals S_1–S_4 coupled to a different set of four phase shifters in the antenna array through pulse forming networks 40_1–40_n, as shown. An exemplary one of such pulse forming networks 40_1–40_n, here pulse forming network **40**, is shown to include four flip-flops 42_1–42_4, (each of conventional design) the set terminal (S) of each thereof being coupled to a read line **60** and the reset terminal (R) of each one thereof being coupled to a different one of the output terminals S_1–S_4, as shown. The output of each one of the flip-flops 42_1–42_n is coupled to a different one of a set of phase shifters PS_1–PS_4, as shown.

Random access memories 25_1–25_n have data input terminals D_1–D_4 coupled to a controller **44** and a comparator network **46** through logic networks 48_1–48_n, respectively, as shown.

Comparator network **46** includes three serially coupled, four stage registers, REG_1–REG_3, the first one thereof being coupled to the output of beam steering computer **15**, as shown. Each one of such registers REG_1–REG_3 stores the 4 bit binary word applied to its input in response to the trailing edge of each one of the clock pulses applied to line c.p. Comparators $COMP_1$–$COMP_3$ have one input coupled to the output of beam steering computer **15** and another input coupled to the output of registers REG_1–REG_3, respectively, as shown. Comparators $COMP_1$–$COMP_3$ are here of any conventional design and are adapted to produce a "high" or binary 1 signal at their output when the data applied to their inputs are equal and to produce a "low" or binary 0 signal when such inputs are not equal. The output of comparator $COMP_1$, (i.e. output W_1) is fed to three AND gates 51_1, 51_2, 51_3, as indicated. Likewise, the output of comparator $COMP_2$ (i.e. output W_2) is fed to two AND gates 51_4, 51_5, as indicated, and the output of comparator $COMP_3$ (i.e. output W_3) is fed to AND gate 51_6.

An exemplary one of the logic networks 48_1–48_n, here logic network 48_1, is shown to include three OR gates 50_1–50_3: OR gate 50_1 couples data input terminal D_1 of RAM 25_1 to the output of AND gates 51_1, 51_4 and 51_6 of comparator network **46** and to data output terminal D_1' of controller **44**; OR gate 50_2 couples data input terminal D_2 of RAM 25_1 to the output of gates 51_2 and 51_5 of comparator network **46** and to data output terminal D_2' of controller **44**; and, OR gate 50_3 couples data input terminal D_3 of RAM 25_1 to the output of gate 51_3 of comparator network **46** and data output terminal D_3' of controller **44**. Data input terminal D_4 of RAM 25_1 is directly coupled to data output terminal D_4' of controller **44**, as indicated.

Controller **44** includes two shift registers **52, 54.** Shift register **52** is here a four stage recirculating shift register of any conventional design, stages 52_1–52_4 being coupled to output terminals D_1'–D_4', respectively, as shown. Output terminals D_2', D_3' and D_4' (in addition to being connected to the logic networks $48_1 \ldots 48_n$ as just described) are also connected to the comparator network **46.** Thus, the output terminal D_2' is coupled to AND gate 51_1 of comparator network **46,** output terminal D_3' is coupled to AND gates 51_2 and 51_4 of such network and output terminal D_4' is coupled to AND gates 51_3, 51_5, 51_6 of such network, as shown. Shift register **54** here has "n" stages 54_1–54_n, such stages being coupled to terminals WE_1–WE_n, respectively, as shown. Shift register **52** is coupled to beam steering computer **15** through clock pulse line c.p. and shift register **54** is coupled to data output line D_4' of shift register **52** and clock pulse line c.p. through AND gate **56.** Shift registers **52, 54** are here constructed to shift a binary one from stage to stage in response to the trailing edge of each clock pulse applied to line c.p., all stages other than the stage containing a binary one containing a binary zero.

In operation, shift registers **52** and **54** are initialized, (by any convenient means, not shown,) so that a binary 1 is stored in stages 52_1 and 54_1, and a binary 0 is stored in each one of the other stages of such shift registers (i.e. stages 52_2–52_4 and 54_2–54_n). Such initialized condition is indicated in FIG. **2.** (It is here noted that a binary 1 is here defined as a "high" level signal, and a binary 0 as a "low" level signal.)

After such initialization, beam steering computer **15** produces at its output a sequence of digital words and, concurrently with each one of such produced digital words, a clock pulse on line c.p. Here such clock pulses and digital words are produced at regular time intervals. (As will become apparent hereinafter, each one of such digital words represents the time interval between the time a selected one of the flip flops 42_1–42_4 of pulse forming networks 40_1–40_n is "set" and the time such selected flip-flop is "reset." It follows then that each one of such digital words designates the desired time duration of a voltage pulse produced at the output of the selected flip-flop and applied to a selected one of the phase shifters PS_1–PS_{4n}.) Continuing then, because a binary **1** is initially stored in stages 52_1 and 54_1, only the random access memory 25_1 is placed in a "write" condition and the data applied to the data input terminals (D_1–D_4) thereof is binary 1000. Therefore, when the first digital word is produced at the output of beam steering computer **15,** such digital word passes through read/write address selector 29_1 to random access memory 25_1 and thereby provides a write address for such random access memory. Also, the data applied to input terminals D_1–D_4(i.e. binary 1000) becomes stored in the row of storage cells selected by the digital word produced at the output of beam steering computer **15** (i.e. the storage cell disposed in the first column, C_1, of such selected row has a binary **1** stored therein and the memory cells disposed in columns C_2–C_4 of such selected row having a binary 0 stored therein).

In response to the trailing edge of the first clock pulse: (a) the first digital word produced by beam steering computer also becomes stored in register REG_1; and (b) the binary 1 in register **52** is shifted from stage 52_1 to stage 52_2 (that is, the data at data output terminals D_1'–D_4' becomes binary 0100). It follows then that, if the first and second digital words out of the beam steering computer **15** are not equal, when the second digital word is produced at the output of the beam steering computer **15,** the data word binary 0100 becomes stored in random access memory 25_1 in the storage cells disposed in the row selected by such second digital word (the storage cell in the second column, C_2, having a binary 1 stored therein). If the first digital word produced by the beam steering computer is the same as the second digital word a binary 1 is produced on line W_1. Because data output terminal D_2' is "high," such binary 1 passes through AND gate 51_1 and OR gate 50_1 to data input terminal D_1 and becomes "restored" in the memory cell disposed in the column C_1 and in the row selected by the first digital word (because under this condition the first and second digital words are equal).

In response to the trailing edge of the second clock pulse: (a) the binary 1 in stage 52_2 shifts to stage 52_3 and the data applied to data output terminals D_1'–D_4' is binary 0010; and (b) the first digital word produced by the beam steering computer **15** becomes stored in register REG_3 and the second digital word becomes stored in register REG_2. It follows then that, if the third digital word is not equal to the first or second digital word when the third digital word is produced at the output of beam steering computer **15,** the data 0010 becomes stored in random access memory 25_1 at the storage cells disposed in the row selected by such third digital word; the storage cell in the third column, C_3, having a binary 1 stored therein. If the third digital word is equal to the first digital word a binary 1 is produced on line W_2 and, because the signal on output data terminal D_3' is "high," such binary 1 passes through AND gate 51_4 and OR gate 50_1 to data input terminal D_1 to become restored in the memory cell disposed in column C_1 and the row selected by the third digital word. Also, if the third digital word is equal to the second digital word a binary 1 is produced on line W_1, and, because the signal on output data terminal D_3' is "high," such binary 1 passes through AND gate 51_2 and OR gate 50_2 to data input terminal D_2 to become restored in the memory cell disposed in column C_2 and the row selected by the third digital word.

In response to the trailing edge of the third clock pulse: (a) the binary 1 in stage 52_3 shifts to stage 52_4 and the data applied to data output terminals D_1'–D_4' is binary 0001; and (b) the first digital word becomes stored in register REG_3, the second digital word becomes stored in register REG_2, and the third digital word becomes stored in REG_1. Therefore, if the fourth digital word is not equal to the first, second, nor third digital words, when the fourth digital word is produced at the output of the beam steering computer **15,** the data 0001 becomes stored in random access memory 25_1 at the storage cells disposed in the row selected by such digital word; the storage cell disposed in the fourth column, C_4, having a binary 1 stored therein. If the fourth digital word is equal to the first digital word a binary 1 is produced on line W_3 and, because the signal on output data terminal D_4' is "high," such binary 1 passes through AND gate 51_6 and OR gate 50_1 to data input terminal D_1 to become stored in the memory cell disposed in column C_1 and the row selected by the third digital word. If the fourth digital word is equal to the second digital word a binary 1 is produced on line W_2 and, because the signal on output terminal D_4' is "high," such binary 1 passes through AND gate 51_5 and OR gate 50_2 to data input terminal D_2 to become stored

in the memory cell disposed in column C_2 and the row selected by the fourth digital word. If the fourth digital word is equal to the third digital word a binary 1 is produced on line W_1 and passes to data input terminal D_3 to become stored in the memory cell disposed in column C_3 and the row selected by the fourth digital word. Further, the binary 1 now stored in stage 52_4 serves as an enabling signal for AND gate **56** so that in response to the trailing edge of fourth clock pulse the binary 1 in stage 54_1 shifts to stage 54_2.

Additionally, in response to the trailing edge of the fourth clock pulse the binary 1 stored in stage 52_4 shifts to stage 52_1 and the data applied to data output terminals D_1'–D_4' is binary 1000 thus allowing the above described process to continue for random access memories 25_2–25_n, successively.

It follows then that a binary 1 or control bit will be stored in random access memory 25_2 at the storage cells in the rows addressed by the fifth, sixth, seventh and eighth digital words produced by the beam steering computer **15**; a binary 1 being stored in the storage state in column C_1 and the row addressed by the fifth digital word, a binary 1 being stored in the storage cell in column C_2 and the row addressed by the sixth digital word, a binary 1 being stored in the storage cell in column C_3 and the row addressed by the seventh digital word, and a binary 1 being stored in the storage cell in column C_4 and the row addressed by the eighth digital word.

The process continues until a binary 1 is stored in the storage cell in random access memory 25*n* disposed at column C_4 and the row addressed by the 4*n*th digital word produced by beam steering computer **15**. Here in response to the next (i.e. the 4*n*+1) clock pulse, shift register **54** has a binary 0 stored in each one of the stages 54_1–54_n, the signals on terminals WE_1–WE_n become "low" thereby: (1) enabling NOR gate **58** to develop an enabling signal on line **60**; (2) placing random access memories 25_1–25_n in a "read" condition, and (3) enabling the contents of counter **30** to pass through read/write address selectors 29_1–29_n to random access memories 25_1–25_n respectively so that such contents serves as read addresses for such memories.

Line **60** is coupled to AND gate **62** and to the set terminals (S) of the flip-flops 42_1–42_4 of pulse forming networks 40_1–40_n. The enabling signal on line **60** serves to: (1) allow clock pulses on clock pulse line c.p. to pass through AND gate **62** to counter **30**, such counter **30** having been initially set to binary 0000 by any convenient means (not shown); and (2) set all flip-flops 42_1–42_4 in all networks 40_1–40_n.

Therefore, at the commencement of the "read" operation: all the random access memories 25_1–25_n are placed in a "read" condition thereby coupling the read address terminals A, B, C, D of random access memories 25_1–25_n to the output of the counter **30**, such counter addressing the random access members 25_1–25_n at location binary 0000; and all flip-flops in the pulse forming networks 40_1 . . . 40_n are placed in a set condition so that a voltage pulse is commenced, such being coupled to each one of the phase shifters, PS_1–PS_{4n}. It follows then that since the first row R_1 of all the random access memories 25_1–25_n are being read addressed simultaneously during the 4*n*+1st clock pulse, if a binary 1 is stored in the storage cell in the first row of any one of such memory, the flip-flop coupled to any such storage cell disposed in row R_1 will be reset thus terminating the voltage pulse coupled to the phase shifter fed by such flip-flop.

During the next clock pulse (i.e. 4*n*+2) the counter **30** counts up 1 c.p. and its contents change to 0001. Therefore, the second row (R_2) of all the random access memories 25_1–25_n are read simultaneously and if a binary 1 is stored in the storage cell in the second row (R_2) of any one of such memories, the flip-flop coupled to such storage cell will be reset thus terminating the voltage pulse coupled to the phase shifter fed by such flip-flop to produce a voltage pulse clock pulse in duration. The process continues until the memory cells in all **16** rows of all the random access memories have been read.

In summary then, each one of the digital words produced at the output of the beam steering computer by providing a write address for a particular row of storage cells in the random access memories 25_1–25_n where a binary 1, or control bit is to be stored, in effect represents the time duration (i.e. the number of clock pulses, 0 clock pulses to 16 clock pulses) between the commencement of the "read" operation (and hence the start of a voltage pulse) and the time at which such control bit is read. To put it another way, the voltage pulses produced at the output of the flip-flop 42_1–42_4 of pulse forming network 40_1–40_n are commenced simultaneously, i.e. when an enabling signal is developed on line **60**. Each one of the flip-flops 42_1–42_4 in each one of the pulse forming networks 40_1–40_n is associated with the storage cells in a different one of the columns C_1–C_4 of each one of the random access memories 25_1–25_n. Because the memory cells in each row are read sequentially at each clock pulse, each one of such flip-flops is reset at the time the control bit (or binary 1) stored in the column associated therewith is read, such reset time being related to the row in such column where the storage cell containing such control bit is disposed. The reset flip-flop thereby terminates the voltage pulse produced at its output.

Threfore, after the 4*n*+16th clock pulse all phase shifters are in their proper flux driven condition thereby enabling the beam of radiation to be directed in the desired direction.

Having described a preferred embodiment of this invention, it is evident that other embodiments incorporating its concepts may be used. For example, if random access memories 25_1–25_n were constructed so that, during the "write" operation, each one of the rows of storage cells could be independently selected for writing data, the comparator network **46** could be eliminated.

It is felt, therefore, that this invention should not be restricted to its disclosed embodiments but rather should be limited only by the spirit and scope of the appended claims.

What is claimed is:

1. Digital apparatus for producing a set of pulses having time durations in accordance with corresponding digital words applied sequentially to such digital apparatus comprising:

a. addressable memory means having storage cells arranged in rows and columns;

b. means for applying a control bit to a different one of the columns of storage cells synchronously as each one of the digital words is applied to the digital apparatus;

c. means for enabling storage of such control bit in the row addressed by such applied one of the digital words;

d. a plurality of pulse generating means, each one thereof being coupled to a common actuating line and having a terminating line connected to a corresponding one of the columns of storage cells, each one thereof initiating one of the set of pulses in response to a signal being applied to the actuating line and for terminating such one of the pulses in response to a signal being applied to the terminating line;

e. means, actuated in response to the last one of a predetermined number of applied digital words, for sequentially reading each one of the rows of storage cells and for applying a signal to the actuating line to initiate simultaneously each one of the set of pulses; and,

f. means for applying signals to a different one of the terminating lines in response to the reading of a different one of the stored control bits thereby to terminate a different one of such pulses at times corresponding to the successively applied digital words.

2. The apparatus recited in claim **1** wherein each one of the pulse generating means is a flip-flop having a set terminal coupled to the actuating line and a reset terminal coupled to the terminating line.

3. Digital apparatus for producing a set of pulses having time durations in accordance with corresponding digital words applied sequentially to such digital apparatus, comprising:

a. an addressable memory having storage cells arranged in a matrix of rows and columns;

b. a plurality of pulse generating means, each one thereof being coupled to a common actuating line and having a terminating line connected to a corresponding one of the columns of storage cells, each one thereof initiating one of the set of pulses in response to a signal being applied to the actuating line and for terminating such one of the pulses in response to a signal applied to the terminating line thereof;

c. means for write addressing the storage cells in the columns thereof sequentially as the digital words are sequentially applied to the digital apparatus and for writing a control bit into such ones of the storage cells located at both the write addressed columns and rows specified by the applied digital words; and,

d. means, actuated in response to the last one of a predetermined number of applied digital words, for sequentially reading each one of the rows of storage cells including means for applying a signal to the actuating line at commencement of such sequential reading to initiate simultaneously each one of the set of pulses, and for applying signals to the terminating lines in response to reading the stored control bits, thereby to terminate such pulses at times corresponding to the digital words.

4. The digital apparatus recited in claim **3,** wherein each one of the pulse generator means is a flip-flop having a set terminal coupled to the actuating line and a reset terminal coupled to the terminating line.

5. The digital apparatus recited in claim **1** wherein each one of the storage cells comprises an electrical circuit.

6. The digital apparatus recited in claim **3** wherein each one of the storage cells comprises an electrical circuit.

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