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(54) **INVERTER PRE-CHARGE CIRCUIT**

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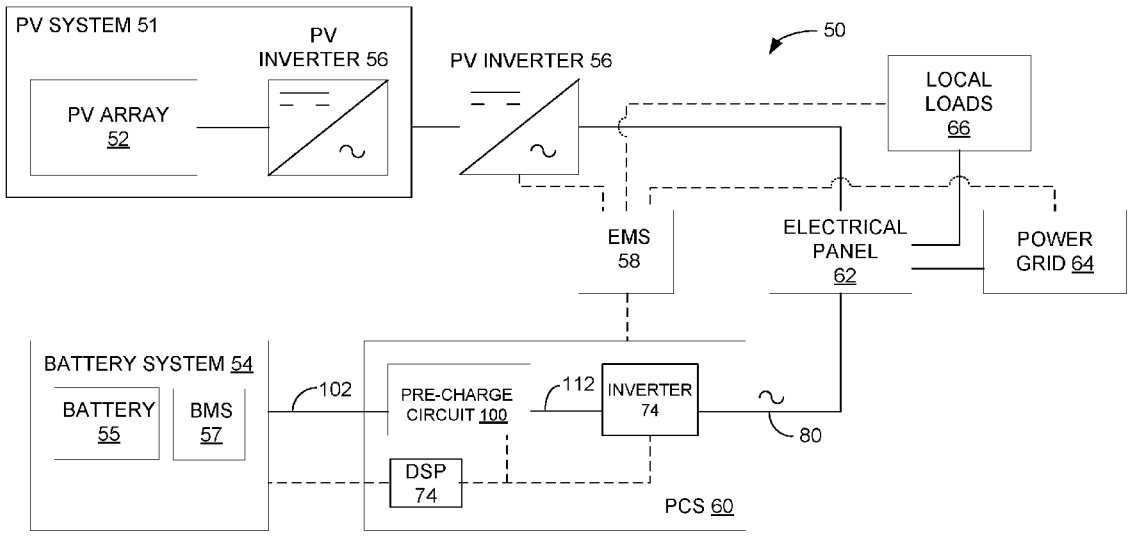
(52) **U.S. Cl.**

CPC ***H02J 3/383*** (2013.01); ***H02M 7/44*** (2013.01); ***H02J 7/0068*** (2013.01)

(57) **ABSTRACT**

A pre-charge circuit includes an input configured to connect to a DC power source, an output configured to connect to the input of an inverter, and a capacitor coupled to the output. A resistive branch in the pre-charge circuit includes a pre-charge switch and a limiting resistor coupled in series between the input and the output. A shunting branch in the pre-charge circuit is coupled in parallel with the resistive branch and includes one or more solid-state switches connected between the input and the output. A digital signal processor (DSP) controls the pre-charge switch enabling the DC power source to charge the capacitor through the resistive branch and activates the solid-state switches after charging the capacitor, shunting the output of the DC power source to the input of the inverter. Solid-state switching in the pre-charge circuit improves control and reliability compared to mechanical contact approaches.



DISTRIBUTED ENERGY RESOURCE (DER) SYSTEM WITH PRE-CHARGE CIRCUIT

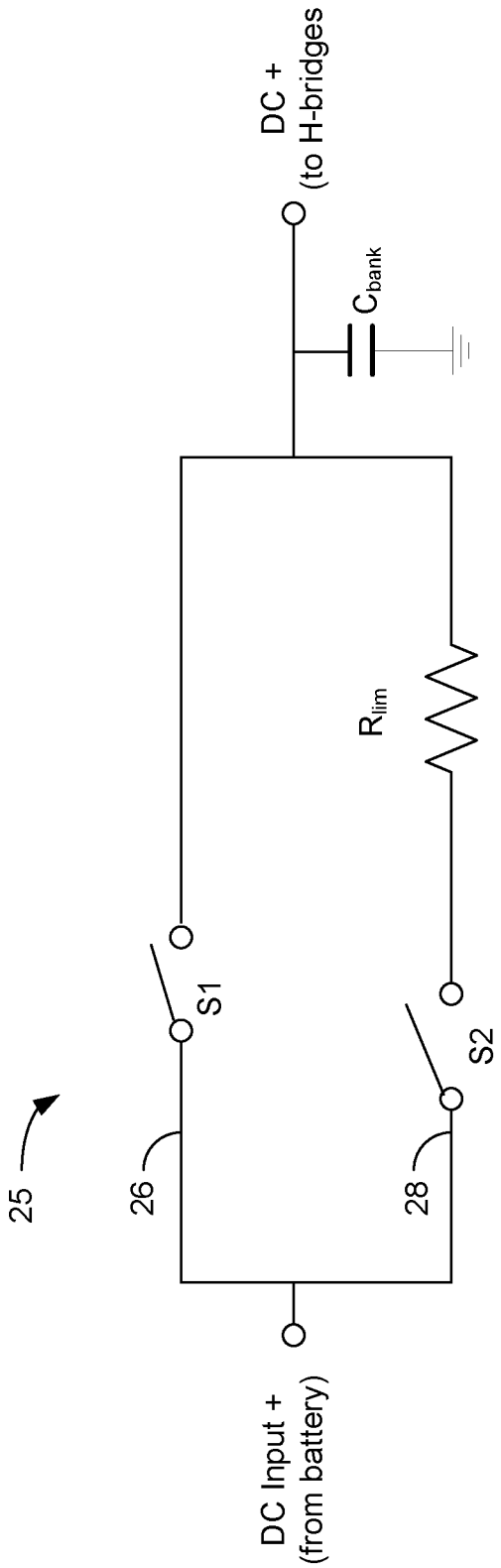
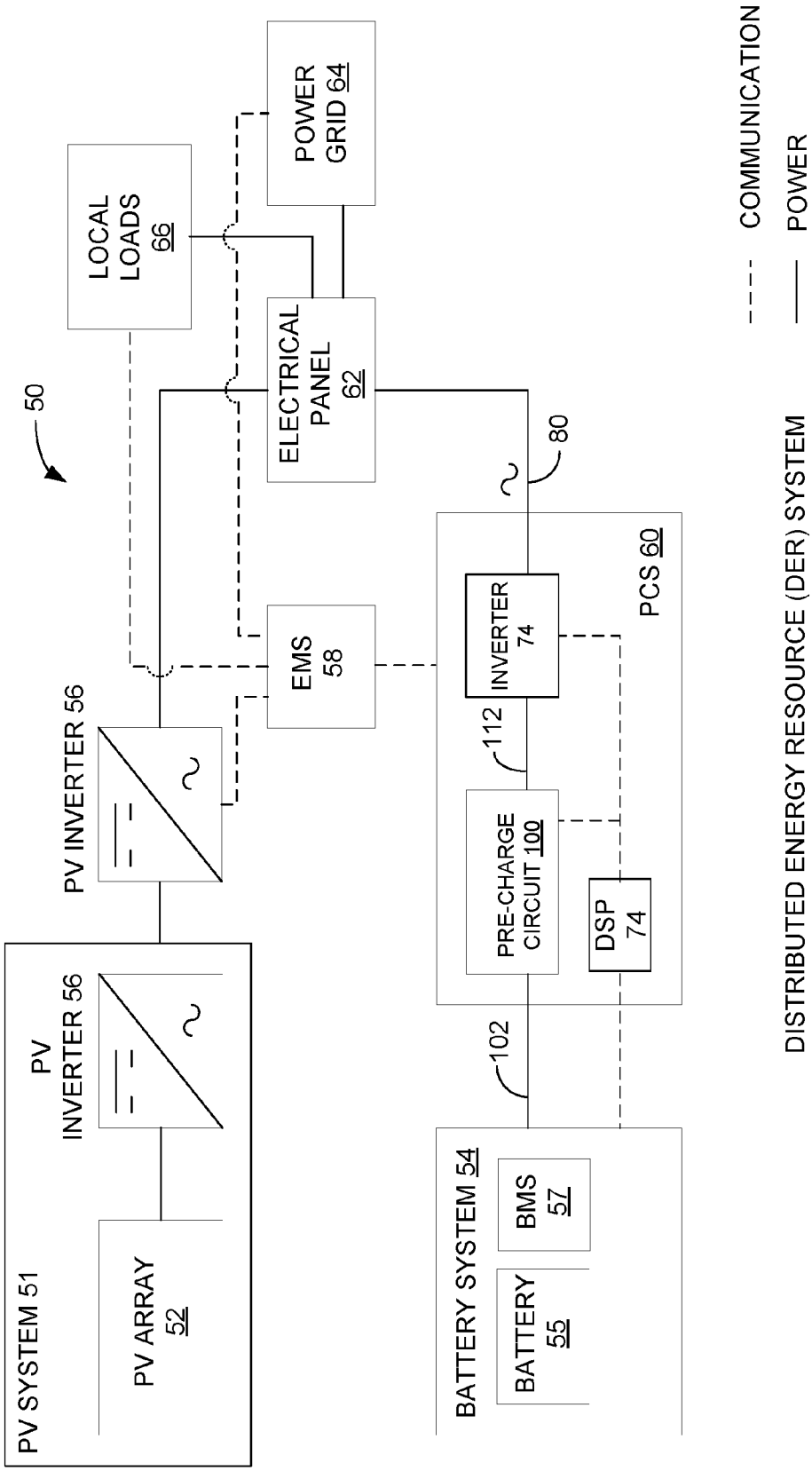
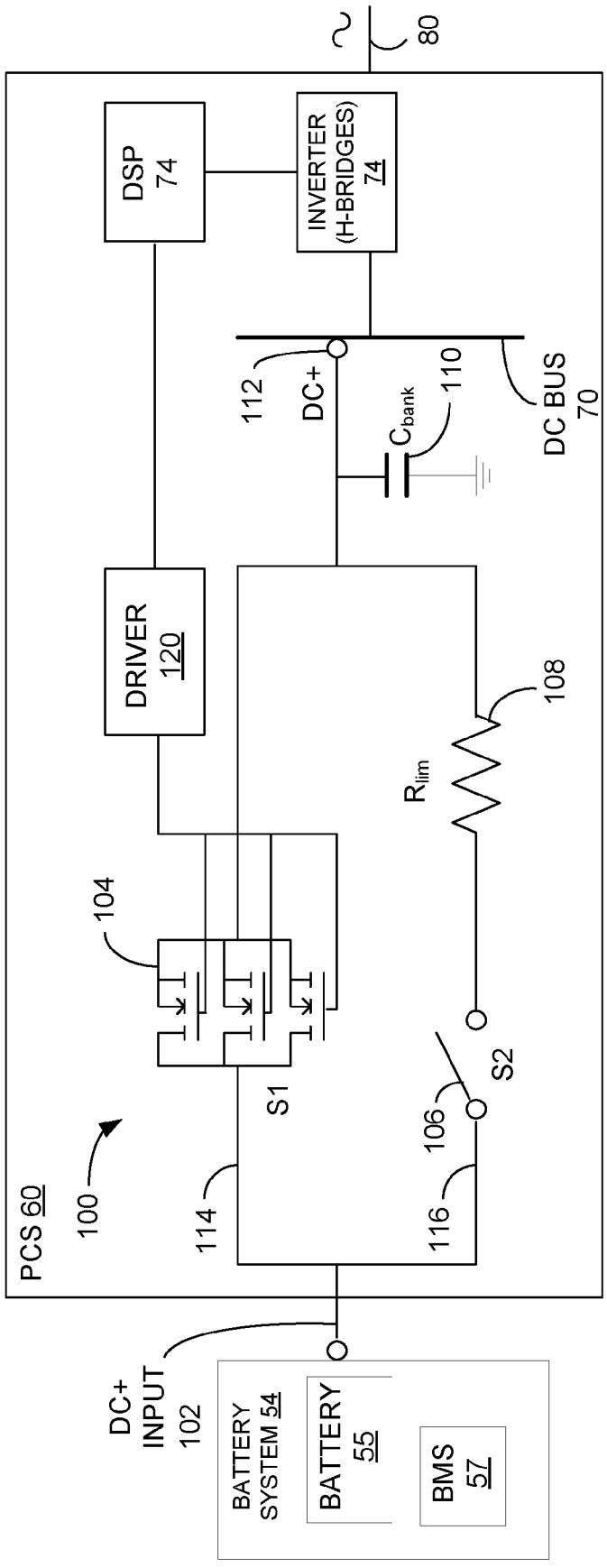


FIG. 1



DISTRIBUTED ENERGY RESOURCE (DER) SYSTEM WITH PRE-CHARGE CIRCUIT

FIG. 2



PRE-CHARGE CIRCUIT

FIG. 3

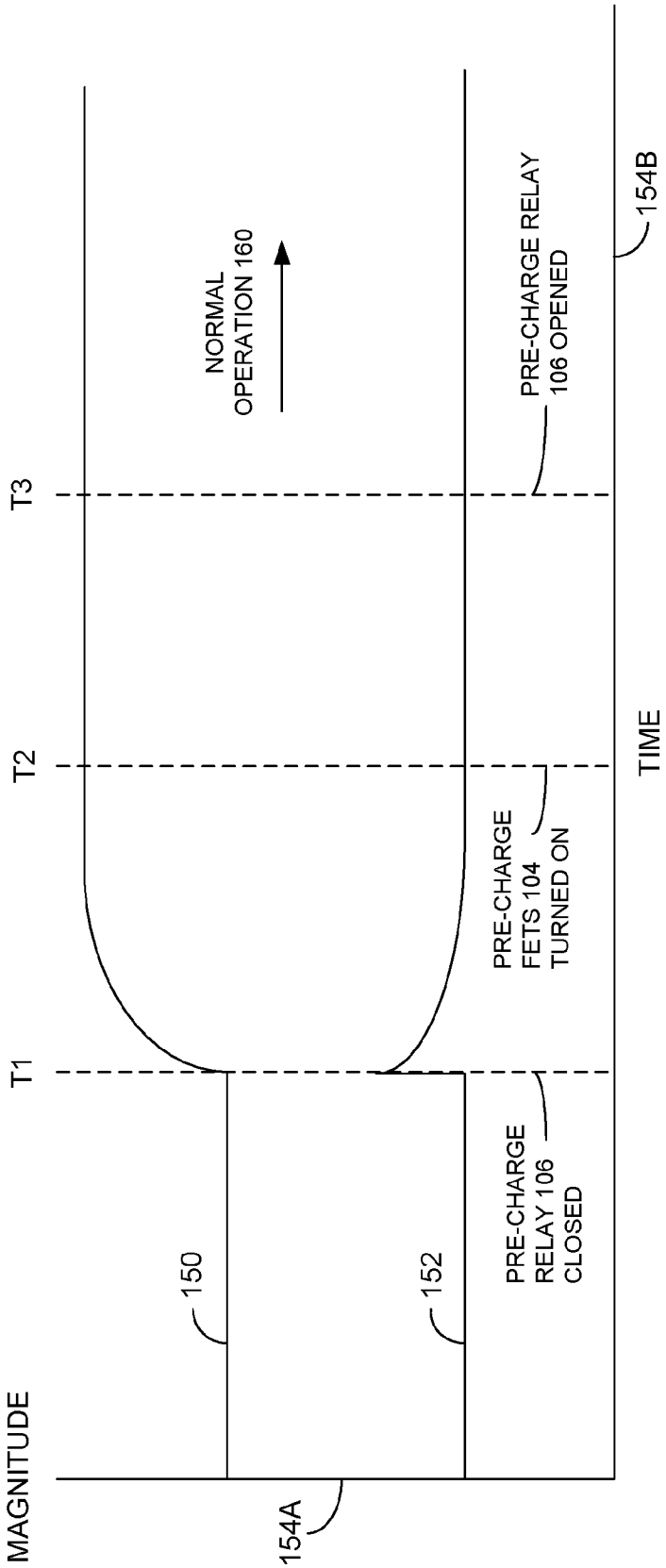

MAGNITUDE
TIME
T1
T2
T3
150
152
154A
154B
NORMAL OPERATION 160
PRE-CHARGE RELAY 106 CLOSED
PRE-CHARGE FETS 104 TURNED ON
PRE-CHARGE RELAY 106 OPENED

FIG. 4

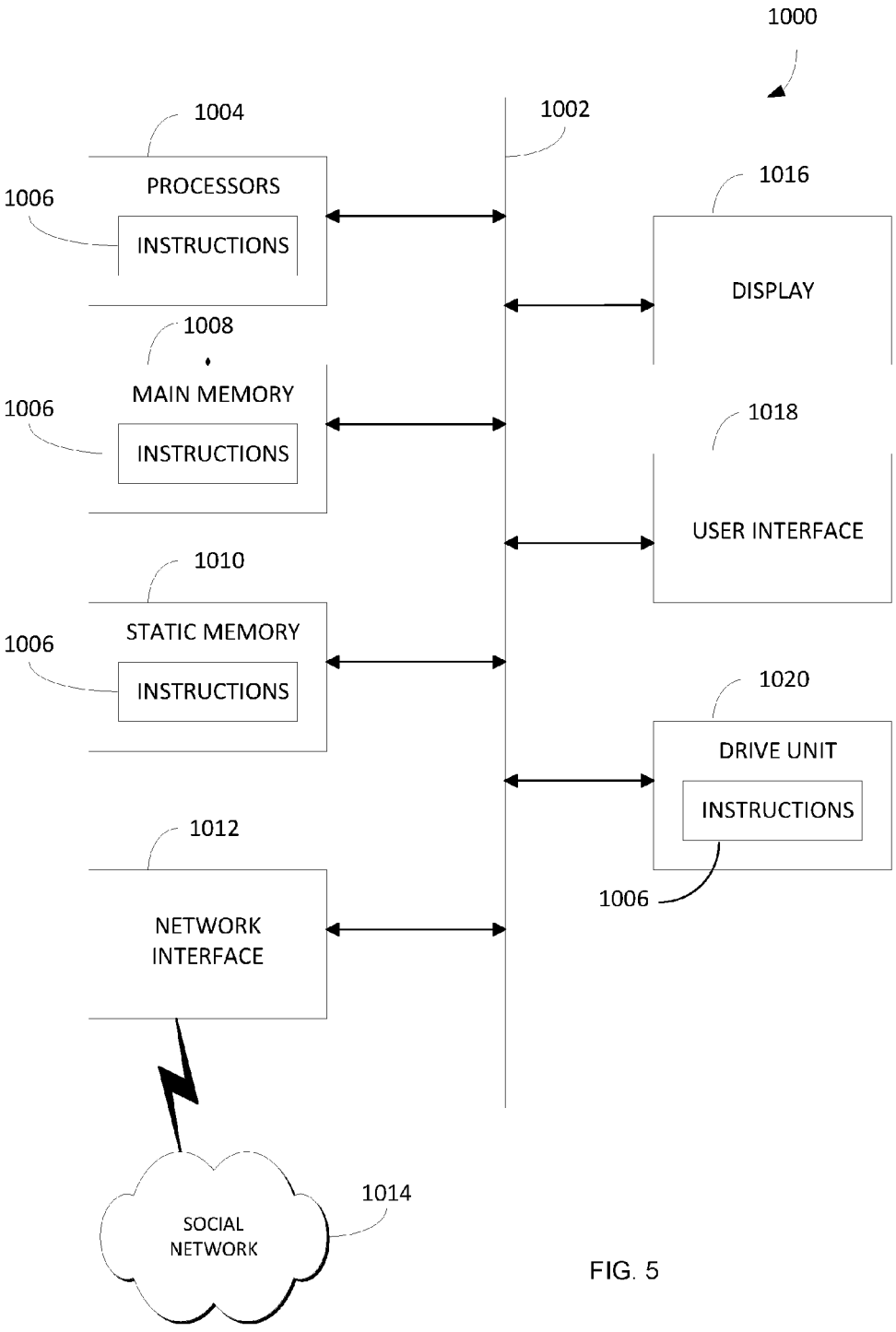

1000
1002
1004
PROCESSORS
1006
INSTRUCTIONS
1016
DISPLAY
1008
MAIN MEMORY
1006
INSTRUCTIONS
1018
USER INTERFACE
1010
STATIC MEMORY
1006
INSTRUCTIONS
1020
DRIVE UNIT
INSTRUCTIONS
1006
1012
NETWORK INTERFACE
SOCIAL NETWORK
1014

FIG. 5

INVERTER PRE-CHARGE CIRCUIT

[0001] The present application claims priority to U.S. Provisional Patent Application Ser. No. 62/293,715 filed on Feb. 10, 2016, entitled: POWER CONTROL SYSTEMS which is incorporated by reference in its entirety.

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TECHNICAL FIELD

[0003] One or more implementations relate generally to a pre-charge circuit and control based on solid-state switching.

BACKGROUND

[0004] Capacitors are often used across the DC terminals of inverters to maintain the DC voltage ripple below a specific magnitude. These capacitors provide current to the H-bridges throughout the switching operation, so they are marginally discharged during switch conduction then recharged by a DC power source.

[0005] When DC power is first connected to a power converter, the capacitors may be pre-charged to match the voltage at their input terminals. Uncharged capacitors instantaneously behave like short-circuits, so large inrush currents can be pulled from the DC power supply. This is particularly problematic for DC battery systems because they do not have limits on the magnitude of short-circuit current they can provide. When unconstrained, these large inrush currents can cause DC protection circuitry to trip and can lead to component or conductor failures in some cases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The included drawings are for illustrative purposes and serve to provide examples of possible structures and operations for the disclosed inventive systems, apparatus, methods and computer-readable storage media. These drawings in no way limit any changes in form and detail that may be made by one skilled in the art without departing from the spirit and scope of the disclosed implementations.

[0007] FIG. **1** shows a known pre-charge circuit (prior art).

[0008] FIG. **2** shows an example distributed energy resource (DER) system that includes a pre-charge circuit.

[0009] FIG. **3** shows the pre-charge circuit of FIG. **1** in more detail.

[0010] FIG. **4** shows example voltage and current waveforms generated by the pre-charge circuit of FIG. **3**.

[0011] FIG. **5** shows a computer system that may be used in combination with the pre-charge circuit.

DETAILED DESCRIPTION

[0012] FIG. **1** shows a conventional pre-charge circuit **25**, including input capacitor bank C_{bank}, current limiting resistor R_{lim}, a shunting branch contactor **S1**, and a resistive branch relay **S2**. To address the problem of large inrush currents, current limiting resistor R_{lim} is located in resistive branch **28** to reduce the current magnitude to manageable levels (i.e., within electrical specifications of cables, copper traces on circuit boards, electronic components, etc.). After input capacitor bank C_{bank} is pre-charged, current limiting resistor R_{lim} is removed from circuit **25** by opening relay **S2**. An uninhibited parallel current path on shunting branch **26** is provided through contactor **S1** that bypasses current limiting resistor R_{lim}. Large mechanical switches are often used for contactor **S1** to switch in the shunting branch **26**, and resistive branch **28** is subsequently switched out using a large mechanical relay **S2**.

[0013] Some downsides to circuit **25** relate to the limitations of switching mechanisms **S1** and **S2**. Contactors **S1** and **S2** rely on mechanical operations that are inherently slow and prone to latency. This makes it difficult to control the switching operation with a high degree of accuracy.

[0014] Given the magnitude of the current flowing through contactors **S1** and **S2**, the power dissipation due to contact resistance can be substantial. This can lead to excessive heating which can impact the operation (e.g., accuracy of current sensing devices) and reliability (e.g., due to accelerated component aging) of surrounding components. The contact resistance can also increase throughout the operational lifetime of the part, which can lead to further heating and accelerated degradation.

[0015] High current contactors are also usually bulky power components that are not well-suited to a printed circuit board (PCB) application. This necessitates an external mounting and cabling solution that can be cumbersome and costly.

[0016] FIG. **2** shows a known distributed energy resource (DER) system **50** that uses an improved pre-charge circuit **100**. In one example, a photovoltaic array **52** connects through a photovoltaic (PV) inverter **56** to an electrical panel **62**. A battery system **54** may connect to electrical panel **62** through a power conversion system (PCS) **60**. Electrical panel **62** may supply power from PV array **52** and battery system **54** to different local loads **66** and/or to a power grid **64**.

[0017] PV array **52** may be any type of device capable of converting solar energy into electrical energy. In one example, PV inverter **56** may convert direct current (DC) power from PC array **52** into alternating current (AC) power for different local AC loads **66** and/or other remote AC devices connected to power grid **64**. PCS **60** may charge battery system **54** using power supplied by PV array **52** or power grid **64** and also may convert stored DC energy in battery system **54** into AC power for powering local loads **66** and exporting power to the power grid **64**.

[0018] DER system **50** may use an energy management system (EMS) **58** to coordinate power flow between PV array **52**, battery system **54**, local loads **66**, and power grid **64**. EMS **58** may communicate with other energy sources throughout the power system, manage power flow within DER **50**, and respond to varying grid conditions or dispatch commands.

[0019] Battery system **54** typically relies on three main components that interact with each other. These include a battery management system (BMS) **57**, PCS **60**, and EMS **58**. BMS **57** monitors the state and condition of battery **55** and provides protection against unsafe operating states (e.g., high battery cell temperatures). BMS **57** also provides handshaking and information transfer with other power

components. Battery **55** can be a single battery or multiple batteries combined within battery system **54**.

[0020] PCS **60** is a linking element that enables power transfer between battery **55** and loads **66** connected to electrical panel **62**. PCS **60** is designed to convert DC power from battery **55** into AC power which may be used to power local loads **66** or to export to the power grid **64**. PCS **60** may be bidirectional to convert AC power from power grid **64** and/or PV array **52** into DC power for charging battery **55**.

[0021] EMS **58** coordinates power flow between power grid **64**, battery **55**, local loads **66**, and PV array **52**. EMS **58** may implement algorithms to manage battery charging and discharging based upon electricity price structures such as time-of-use metering or demand charging.

[0022] PCS **60** may act as a bridge between BMS **57** and EMS **58**. PCS **60** converts power demand signals from EMS **58** into real power flow between the power converter and battery **55**. As a result, PCS **60** is uniquely equipped to collect detailed information about battery system **54** in real-time. PCS **60** also has access to physical and operational parameters that would not otherwise be conveyed to EMS **58**. For example, PCS **60** may convey battery temperature, instantaneous power, and state of charge of battery system **54** to EMS **58**.

[0023] PCS **60** includes a digital signal processor (DSP) **74** that manages the switching controls within an inverter power circuit **74** such as the step wave power converter described in U.S. Pat. Nos. 6,608,404 and 7,808,125 which are herein incorporated by reference in their entireties. These controls are based on a feedback process involving a parameter set point, which can be set manually by a user or set through EMS **58**.

[0024] Other example inverter and bridge circuits used in PV inverter **56** and PCS **60** are described in U.S. patent applications such as U.S. Pat. No. 6,198,178; U.S. Pat. No. 8,031,495; U.S. U.S. Pat. No. 6,628,011; U.S. Pat. No. 6,765,315; U.S. Pat. No. 6,738,692; and U.S. Pat. No. 7,087,332 which are all also herein incorporated by reference in their entireties.

[0025] Battery **55** in battery system **54** may store energy output from PV array **52**. DSP **74** operating within PCS **60** may measure current and/or voltage data from both battery system **54** and PV system **51** and perform functions in PCS **60**, such as power measurements, control, and inverter system switching.

Pre-Charge Circuit

[0026] A solid-state based pre-charge circuit **100** includes a DC input **102** that connects to battery **55** in battery system **54** and includes a DC output **112** that connects to H-bridges within inverter **74**. In one example, pre-charge circuit **100** is located within PCS **60**, but may be located and connected externally to PCS **60**, PV inverter **56**, or any other inverter circuit. It should be understood that the use of pre-charge circuit **100** in DER system **50** in FIG. **2** is just one example. Pre-charge circuit **100** may be used in any power control system with any inverter or with any other power switching circuitry that may need to pre-charge inputs.

[0027] FIG. **3** shows pre-charge circuit **100** in more detail. A first resistive branch **116** of circuit **100** includes a relay **106** (S2) coupled in series with current limiting resistor **108** (R_{lim}) between DC input **102** and DC output **112**. A second non-resistive shunting branch **114** is coupled in parallel with first resistive branch **116** and includes multiple field effect transistors (FETs) **104** that replace contactor S1 in FIG. **1**. An input capacitor bank **110** (C_{bank}) is coupled to DC output **112**. In one example, the output of pre-charge circuit **100** is coupled to a DC bus **70** that is also coupled to inverter **74**.

[0028] Pre-charge circuit **100** uses solid-state switching devices **104** to address prior pre-charge circuit shortcomings and provide improved controllability. Pre-charge circuit **100** replaces a mechanical contactor with a controllable solid-state switch **104**, such as field effect transistors (FET) or insulated-gate bipolar transistors (IGBT). Any number of solid-state devices **104** can be used, and in one example, between 1 and 10 FETs **104** are used. In any case, the solid-state switches are actuated by a driver **120** which are coordinated by a DSP **74**. In another embodiment, relay **106** (S2) within the resistive path can also be replaced with solid-state switches such as FETs or IGBTs. For example, a same number, or a different number, of stacked solid-state switches similar to switches **104** may be connected in parallel between DC input **102** and resistor **108**. It is understood that relay **106** is also actuated by a driver which is coordinated by a DSP **74**, but this is not shown in FIG. **3**.

[0029] On the shunting path **114**, rather than relying on large and expensive solid-state devices to meet power specifications (e.g., greater than 100 A), multiple solid-state devices **104** are ganged together in parallel and switched by a single driver **120**. This provides the added benefit of distributing the dissipated power (conduction losses) through a larger surface area, thereby reducing the thermal load. Since solid-state switching devices **104** are PCB-mountable, a thermal management solution can be built into the PCB by tuning the copper trace thickness and footprint. An external PCB-mounted heatsink can also be used to further dissipate heat.

[0030] In one example, driver **120** is controlled by DSP **74**, which also may control H-bridge circuitry in inverter **74**. That is, single DSP **74** may control all of the sub-circuits in inverter **74** and PCS **60**, including pre-charge circuit **100**. In another example, a separate DSP may control pre-charge circuit **100**.

[0031] FIG. **4** shows the pre-charge coordination and timing. The y-axis **154**A shows the magnitude of the current and voltage while the x-axis **154**B shows the time. Curve **150** represents the charging voltage on output **112** and curve **152** represents the charging current into output **112**. Referring to FIGS. **3** and **4**, when battery **55** is in an initial idle state, DC terminals **102** are disconnected from pre-charge circuit **100**. For example, DSP **130** opens relay **106** and solid-state switches **104**.

[0032] After being prompted to leave the idle state, DSP **130** at time T1 closes pre-charge relay **106**, which connects current limiting resistor **108** to battery system **54**. Input capacitors **110** are then charged through resistive branch **116** for a configurable charge duration, such as a 1 second default time period. The DC voltage **150** on DC bus **70** exponentially approaches some nominal value and DC current **152** spikes while charging capacitors **110** and then exponentially decays down. The charge duration depends on the characteristics of the input capacitance and pre-charge resistor; in tandem these circuit elements form an RC circuit which is well known in the art. After the charge duration has elapsed, the input capacitor bank **110** should be substantially charged to the DC voltage of the DC input terminal **102**.

[0033] After the charge duration elapses, solid-state switches **104** are switched on with driver **120** at time T2,

which connects parallel shunting branch **114** between battery system **54** and DC bus **70**. Before this occurs, it is important that the voltage at the output DC bus **70** is approximately equal to the voltage at the input terminals **102**. If the output voltage is significantly lower, large and potentially damaging currents can flow through the output DC bus **70** until the input capacitor bank **110** is fully charged. The DSP **74** measures the DC voltages at the input **102** and output **112** of the pre-charge circuit and ensures this condition is met prior to switching in the shunting branch **114**.

[0034] Once the shunting branch **114** is connected, the resistive branch **116** and shunting branch **114** provide parallel conduction paths simultaneously. This configuration remains in place for a configurable duration, such as a 1 second default time.

[0035] DSP **74** then opens pre-charge relay **106** at time T**3**, which disconnects resistive branch **116** from pre-charge circuit **100** and leaves only shunting branch **114** connected. Thereafter, solid-state switches **104** remain in conduction mode throughout the normal operation **160** of inverter **140** when converting DC power from battery **55** into AC power on AC bus **80**. Solid-state switches **104** provide a continuous electrical link between battery system **54** and DC bus **70**.

[0036] During normal operation **160**, solid-state switches **104** are opened at any time, transitioning battery system **54** back to an idle state. This disconnect mode completely disconnects DC terminals **102** from inverter **74**, preventing all power flow, and preserving stored energy in battery system **54**. Again, it should be understood that pre-charge circuit **100** may be used with any switching circuit that may need to input pre-charging. For example, DC power supplied to inverter **74** may not necessarily come from a battery **55**, but may come from PV array **52** or from any other power source.

[0037] Switching of solid-state switches **104** is coordinated precisely by DSP **74** in PCS **60** via control drivers **120**. By using faster solid-state switches **104**, DSP **74** can reduce the duration of the pre-charge routine by minimizing the activation overlap of resistive branch **116** with shunting branch **114** (the time between T**2** and T**3**).

[0038] Solid-state switching pre-charge circuit **100** improves control and reliability compared to mechanical contact approaches. Solid-state switches **104** have lower power losses, can employ simple thermal management strategies, and have better reliability and safety. Solid-state switches **104** may have a longer useful lifetime compared with mechanical contactors (typically limited to less than 1 million switching cycles) and offer more predictable resistive characteristics as they age.

[0039] Implementing solid-state switches on the resistive branch **116** further improves the controllability of the pre-charge circuit **100** through the ability to control and coordinate all pre-charge switches using a single DSP **74**. However, the current magnitudes through the resistive branch **116** are low and the conduction durations are limited, so reliability concerns, power losses, and thermal loads are less significant. In this case, it is acceptable to use a single inexpensive mechanical contactor.

[0040] By default, solid-state switches **104** remain open until powered by driver **120**. Therefore, in one example, communication and control by DSP **74** is established before pre-charge circuit **100** can be activated. By contrast, contactor systems are closed by a simple mechanical activation and may be more susceptible to false activation. In more extreme cases, contactors can fuse shut, which may completely short the pre-charge circuit **100** and may lead to large current magnitudes during start-up.

[0041] As mentioned above, solid-state switches **104** are also well-suited to board mounted applications, which are compatible with design approaches used throughout inverter systems **74**. Pre-charge circuit **100** may reduce the volume within an enclosure, constrain power flow to PCB traces, and reduce overall power system costs. Pre-charge circuit **100** may be used in any power conversion system.

[0042] FIG. **5** shows a computing device **1000** that may be used for implementing or operating in combination with DSP **74**, PV inverter **56**, PCS **60**, EMS **58**, and any combination of devices and processes discussed above. The computing device **1000** may operate in the capacity of a server or a client machine in a server-client network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. In other examples, computing device **1000** may be a personal computer (PC), a tablet, a Personal Digital Assistant (PDA), a cellular telephone, a smart phone, a web appliance, or any other machine or device capable of executing instructions **1006** (sequential or otherwise) that specify actions to be taken by that machine.

[0043] While only a single computing device **1000** is shown, the computing device **1000** may include any collection of devices or circuitry that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the operations discussed above. Computing device **1000** may be part of an integrated control system or system manager, or may be provided as a portable electronic device configured to interface with a networked system either locally or remotely via wireless transmission.

[0044] Processors **1004** may comprise a central processing unit (CPU), a graphics processing unit (GPU), programmable logic devices, dedicated processor systems, micro controllers, or microprocessors that may perform some or all of the operations described above. Processors **1004** may also include, but may not be limited to, an analog processor, a digital processor, a microprocessor, multi-core processor, processor array, network processor, etc.

[0045] Some of the operations described above may be implemented in software and other operations may be implemented in hardware. One or more of the operations, processes, or methods described herein may be performed by an apparatus, device, or system similar to those as described herein and with reference to the illustrated figures.

[0046] Processors **1004** may execute instructions or "code" **1006** stored in any one of memories **1008**, **1010**, or **1020**. The memories may store data as well. Instructions **1006** and data can also be transmitted or received over a network **1014** via a network interface device **1012** utilizing any one of a number of well-known transfer protocols.

[0047] Memories **1008**, **1010**, and **1020** may be integrated together with processing device **1000**, for example RAM or FLASH memory disposed within an integrated circuit microprocessor or the like. In other examples, the memory may comprise an independent device, such as an external disk drive, storage array, or any other storage devices used in database systems. The memory and processing devices may be operatively coupled together, or in communication with each other, for example by an I/O port, network connection, etc. such that the processing device may read a file stored on the memory.

[0048] Some memory may be "read only" by design (ROM) by virtue of permission settings, or not. Other examples of memory may include, but may be not limited to, WORM, EPROM, EEPROM, FLASH, etc. which may be implemented in solid-state semiconductor devices. Other memories may comprise moving parts, such a conventional rotating disk drive. All such memories may be "machine-readable" in that they may be readable by a processing device.

[0049] "Computer-readable storage medium" (or alternatively, "machine-readable storage medium") may include all of the foregoing types of memory, as well as new technologies that may arise in the future, as long as they may be capable of storing digital information in the nature of a computer program or other data, at least temporarily, in such a manner that the stored information may be "read" by an appropriate processing device. The term "computer-readable" may not be limited to the historical usage of "computer" to imply a complete mainframe, mini-computer, desktop, wireless device, or even a laptop computer. Rather, "computer-readable" may comprise storage medium that may be readable by a processor, processing device, or any computing system. Such media may be any available media that may be locally and/or remotely accessible by a computer or processor, and may include volatile and non-volatile media, and removable and non-removable media.

[0050] Computing device **1000** can further include a video display **1016**, such as a liquid crystal display (LCD) or a cathode ray tube (CRT) and a user interface **1018**, such as a keyboard, mouse, touch screen, etc. All of the components of computing device **1000** may be connected together via a bus **1002** and/or network.

[0051] For the sake of convenience, operations may be described as various interconnected or coupled functional blocks or diagrams. However, there may be cases where these functional blocks or diagrams may be equivalently aggregated into a single logic device, program or operation with unclear boundaries. Having described and illustrated the principles of a preferred embodiment, it should be apparent that the embodiments may be modified in arrangement and detail without departing from such principles.

1. A pre-charge circuit, comprising:
- an input configured to connect to a DC power source;
- an output configured to connect to the input of an inverter;
- a capacitor coupled to the output;
- a resistive branch including a pre-charge switch and a limiting resistor coupled in series between the input and the output; and
- a shunting branch coupled in parallel with the resistive branch including one or more solid-state switches connected between the input and the output.

2. The pre-charge circuit of claim **1**, including multiple solid-state switches stacked in parallel within the shunting branch between the input and the output.

3. The pre-charge circuit of claim **1**, wherein the solid-state switches are field effect transistors (FETs) or insulated-gate bipolar transistors (IGBTs).

4. The pre-charge circuit of claim **1**, wherein the pre-charge switch comprises one or more solid-state switches.

5. The pre-charge circuit of claim **1**, wherein a digital signal processor (DSP) is configured to:
- close the pre-charge switch enabling the DC power source to charge the capacitor through the resistive branch;
- activate the solid-state switches after charging the capacitor shunting the output of the DC power source to the input of the inverter;
- reopen the pre-charge switch after activating the solid-state switches; and
- maintain activation of the solid-state switches while operating the inverter.

6. The pre-charge circuit of claim **5**, wherein the digital signal processor (DSP) is further configured to:
- measure an input voltage at the input of the pre-charge circuit;
- measure an output voltage at the output of the pre-charge circuit; and
- activate the solid-state switches in the shunting branch when the output voltage is substantially and same as the input voltage.

7. The pre-charge circuit of claim **5**, wherein the DSP controls the switching of the H-bridges.

8. The pre-charge circuit of claim **5**, wherein the DSP is located in a power conversion system (PCS) used for converting DC power from a battery into AC power.

9. The pre-charge circuit of claim **5**, wherein the DSP is further configured to:
- close the pre-charge switch based on a request to leave a DC power source idle state; and
- open the solid-state switches based on a request to enter the DC power source idle state.

10. The pre-charge circuit of claim **5**, including a driver coupled to the DSP for activating the solid-state switches.

11. The pre-charge circuit of claim **1**, wherein the output is coupled to a DC bus in a distributed energy resource system.

12. A power conversion system (PCS) for converting between DC power and AC power, comprising:
- an inverter including an output coupled at an AC bus;
- a pre-charge circuit coupled between an output of a DC power source and an input of the inverter, the pre-charge circuit including solid-state switches and capacitors for pre-charging the input of the inverter; and
- a digital signal processor (DSP) coupled to the inverter for controlling the conversion between DC power and AC power and coupled to the pre-charge circuit to control the pre-charging at the input of the inverter.

13. The PCS of claim **12**, wherein the pre-charge circuit includes:
- an input connected to the output of the DC power source;
- an output connected to the input of the inverter and the capacitors;
- a resistive branch including a pre-charge switch and a limiting resistor coupled in series between the input and the output; and
- a shunting branch coupled in parallel with the resistive branch including solid-state switches connected between the input and the output.

14. The PCS of claim **13**, wherein the output of the pre-charge circuit is coupled to a DC bus in a distributed energy resource system.

15. The PCS of claim **13**, wherein the DSP is configured to:
- close the pre-charge switch to charge the capacitor with the DC power source through the resistive branch;
- activate the solid-state switches after charging the capacitor;

reopen the pre-charge switch after activating the solid-state switches; and

keep the solid-state switches activated while controlling the inverter.

16. The PCS of claim **15**, wherein the DSP is further configured to:

monitor an input voltage at the input of the pre-charge circuit;

monitor an output voltage at the output of the pre-charge circuit; and

activate the solid-state switches when the output voltage is substantially the same as the input voltage.

17. The PCS of claim **13**, wherein the DSP is further configured to:

close the pre-charge switch based on a request to activate the DC power source; and

open the solid state-switches based on a request to deactivate the DC power source.

18. The PCS of claim **12**, including a driver coupled to the DSP for activating the solid-state relays.

19. The PCS of claim **13**, wherein:

the solid-state switches in the shunting branch are connected in parallel between the input and the output of the pre-charge circuit; and

the pre-charge switch in the resistive branch comprises one or more solid-state switches coupled in parallel between the input of the pre-charge circuit and the limiting resistor.

20. The PCS of claim **12**, wherein the solid-state switches are field effect transistors (FETs) or insulated-gate bipolar transistors (IGBTs).

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