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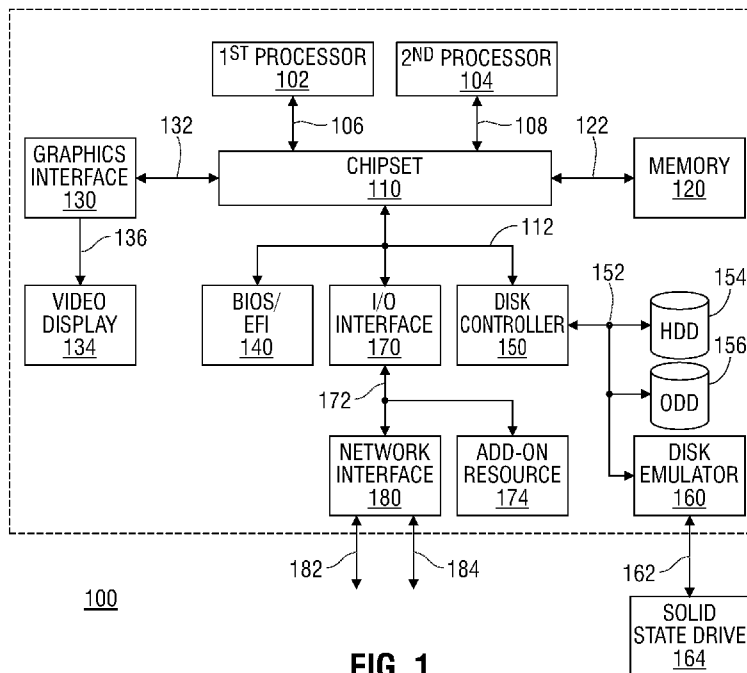
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(57) Abstract: A cooling assembly for an IOT wireless gateway device that includes a motherboard structure operatively coupled to one side of a first motherboard component, which is operatively coupled on the other side to one side of a first gap pad for conducting heat, an EMI shield operatively coupled to the other side of the first gap pad and surrounding the sides of the first motherboard component, the EMI shield also operatively coupled to the motherboard structure, the outside of the EMI shield operatively coupled to one side of a second gap pad for conducting heat, and a first heat sink operatively coupled to the other side of the second gap pad for conducting heat.

SYSTEM AND METHOD OF UNIFIED COOLING SOLUTION IN AN IOT DEVICE

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FIELD OF THE DISCLOSURE

[0001] The present disclosure generally relates to information handling systems, and more particularly a system and method of a unified cooling solution.

BACKGROUND

[0002] As the value and use of information continues to increase, individuals and businesses seek additional ways to process and store information. One option is an information handling system. An information handling system generally processes, compiles, stores, or communicates information or data for business, personal, or other purposes. Technology and information handling needs and requirements can vary between different applications. Thus information handling systems can also vary regarding what information is handled, how the information is handled, how much information is processed, stored, or communicated, and how quickly and efficiently the information can be processed, stored, or communicated. The variations in information handling systems allow information handling systems to be general or configured for a specific user or specific use such as financial transaction processing, airline reservations, enterprise data storage, or global communications. In addition, information handling systems can include a variety of hardware and software resources that can be configured to process, store, and communicate information and can include one or more computer systems, graphics interface systems, data storage systems, networking systems, and mobile communication systems. Information handling systems can also implement various virtualized architectures. Data and voice communications among information handling systems may be via networks that are wired, wireless, or some combination.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the Figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements. Embodiments incorporating teachings of the present disclosure are shown and described with respect to the drawings herein, in which:

[0004] FIG. 1 is a block diagram illustrating an information handling system according to an embodiment of the present disclosure;

[0005] FIG. 2 is a block diagram illustrating a cooling assembly for an internet of things (IOT) wireless gateway device according to an embodiment of the present disclosure;

[0006] FIG. 3 is a flow diagram illustrating a process of forming a cooling assembly for an IOT device according to an embodiment of the present disclosure;

[0007] FIG. 4 is a block diagram illustrating a further cooling assembly for an internet of things (IOT) wireless gateway device according to an embodiment of the present disclosure;

[0008] FIG. 5 is a flow diagram illustrating a process of forming a cooling assembly for an IOT device according to an embodiment of the present disclosure;

[0009] FIG. 6 is a block diagram illustrating a motherboard structure in an embodiment having a first outer surface and a second outer surface according to an embodiment of the present disclosure; and

[0010] FIG. 7 is a block diagram illustrating an EMI shield formed in an embodiment with a proximal outer surface, a distal outer surface, a proximal inner surface, and a distal inner surface relative to a motherboard structure according to an embodiment of the present disclosure.

[0011] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION OF THE DRAWINGS

[0012] The following description in combination with the Figures is provided to assist in understanding the teachings disclosed herein. The description is focused on specific implementations and embodiments of the teachings, and is provided to assist in describing the teachings. This focus should not be interpreted as a limitation on the scope or applicability of the teachings.

[0001] FIG. 1 illustrates a generalized embodiment of information handling system 100. FIG. 1 is a block diagram illustrating an information handling system according to an embodiment of the present disclosure. For purpose of this disclosure information handling system 100 can include any instrumentality or aggregate of instrumentalities operable to compute, classify, process, transmit, receive, retrieve, originate, switch, store, display, manifest, detect, record, reproduce, handle, or utilize any form of information, intelligence, or data for business, scientific, control, entertainment, or other purposes. For example, information handling system 100 can be a personal computer, a laptop computer, a smart phone, a tablet device or other consumer electronic device, a network server, a network storage device, a switch router or other network communication device, or any other suitable device and may vary in size, shape, performance, functionality, and price. Further, information handling system 100 can include processing resources for executing machine-executable code, such as a central processing unit (CPU), a programmable logic array (PLA), an embedded device such as a System-on-a-Chip (SoC), or other control logic hardware. Information handling system 100 can also include one or more computer-readable medium for storing machine-executable code,

such as software or data. Additional components of information handling system 100 can include one or more storage devices that can store machine-executable code, one or more communications ports for communicating with external devices, and various input and output (I/O) devices, such as a keyboard, a mouse, and a video display. Information handling system 100 can also include one or more buses operable to transmit information between the various hardware components.

[0002] Information handling system 100 can include devices or modules that embody one or more of the devices or modules described above, and operates to perform one or more of the methods described above. Information handling system 100 includes a processors 102 and 104, a chipset 110, a memory 120, a graphics interface 130, include a basic input and output system/extensible firmware interface (BIOS/EFI) module 140, a disk controller 150, a disk emulator 160, an input/output (I/O) interface 170, and a network interface 180. Processor 102 is connected to chipset 110 via processor interface 106, and processor 104 is connected to chipset 110 via processor interface 108. Memory 120 is connected to chipset 110 via a memory bus 122. Graphics interface 130 is connected to chipset 110 via a graphics interface 132, and provides a video display output 136 to a video display 134. In a particular embodiment, information handling system 100 includes separate memories that are dedicated to each of processors 102 and 104 via separate memory interfaces. An example of memory 120 includes random access memory (RAM) such as static RAM (SRAM), dynamic RAM (DRAM), non-volatile RAM (NV-RAM), or the like, read only memory (ROM), another type of memory, or a combination thereof.

[0003] BIOS/EFI module 140, disk controller 150, and I/O interface 170 are connected to chipset 110 via an I/O channel 112. An example of I/O channel 112 includes a Peripheral Component Interconnect (PCI) interface, a PCI-Extended (PCI-X) interface, a high-speed PCI-Express (PCIe) interface, another industry standard or proprietary communication interface, or a combination thereof. Chipset 110 can also include one or more other I/O interfaces, including an Industry Standard Architecture (ISA) interface, a Small Computer Serial Interface (SCSI) interface, an Inter-Integrated Circuit (I²C) interface, a System Packet Interface (SPI), a Universal Serial Bus (USB), another interface, or a combination thereof. BIOS/EFI module 140 includes BIOS/EFI code operable to detect resources within information handling system 100, to provide drivers for the resources, initialize the resources, and access the resources. BIOS/EFI module 140 includes code that operates to detect resources within information handling system 100, to provide drivers for the resources, to initialize the resources, and to access the resources.

[0004] Disk controller 150 includes a disk interface 152 that connects the disc controller to a hard disk drive (HDD) 154, to an optical disk drive (ODD) 156, and to disk emulator 160. An example of disk interface 152 includes an Integrated Drive Electronics (IDE) interface, an Advanced Technology Attachment (ATA) such as a parallel ATA (PATA) interface or a serial ATA (SATA) interface, a SCSI interface, a USB interface, a proprietary interface, or a combination thereof. Disk emulator 160 permits a solid-state drive 164 to be connected to information handling system 100 via an external interface 162. An example of external interface 162 includes a USB interface, an IEEE 1194 (Firewire) interface, a proprietary interface, or a combination thereof. Alternatively, solid-state drive 164 can be disposed within information handling system 100.

[0005] I/O interface 170 includes a peripheral interface 172 that connects the I/O interface to an add-on resource 174 and to network interface 180. Peripheral interface 172 can be the same type of interface as I/O channel 112, or can be a different type of interface. As such, I/O interface 170 extends the capacity of I/O channel 112 when peripheral interface 172 and the I/O channel are of the same type, and the I/O interface translates information from a format suitable to the I/O channel to a format suitable to the peripheral channel 172 when they are of a different type. Add-on resource 174 can include a data storage system, an additional graphics interface, a network interface card (NIC), a sound/video processing card, another add-on resource, or a combination thereof. Add-on resource 174 can be on a main circuit board, on separate circuit board or add-in card disposed within information handling system 100, a device that is external to the information handling system, or a combination thereof.

[0006] Network interface 180 represents a NIC disposed within information handling system 100, on a main circuit board of the information handling system, integrated onto another component such as chipset 110, in another suitable location, or a combination thereof. Network interface device 180 includes network channels 182 and 184 that provide interfaces to devices that are external to information handling system 100. In a particular embodiment, network channels 182 and 184 are of a different type than peripheral channel 172 and network interface 180 translates information from a format suitable to the peripheral channel to a format suitable to external devices. An example of network channels 182 and 184 includes InfiniBand channels, Fibre Channel channels, Gigabit Ethernet channels, proprietary channel architectures, LTE macrocellular, or a combination thereof. Network channels 182 and 184 can be connected to external network resources (not illustrated). The network resource can include another information handling system, a data storage system, another network, a grid management system, another suitable resource, or a combination thereof.

[0007] While the computer-readable medium is shown to be a single medium, the term “computer-readable medium” includes a single medium or multiple media, such as a centralized or distributed database, and/or associated caches and servers that store one or more sets of instructions. The term “computer-readable medium” shall also include any medium that is capable of storing, encoding, or carrying a set of instructions for execution by a processor or that cause a computer system to perform any one or more of the methods or operations disclosed herein.

[0008] In a particular non-limiting, exemplary embodiment, the computer-readable medium can include a solid-state memory such as a memory card or other package that houses one or more non-volatile read-only memories. Further, the computer-readable medium can be a random access memory or other volatile re-writable memory. Additionally, the computer-readable medium can include a magneto-optical or optical medium, such as a disk or tapes or other storage device to store information received via carrier wave signals such as a signal communicated over a transmission medium. Furthermore, a computer readable medium can store information received from distributed network resources such as from a cloud-based environment. A digital file attachment to an e-mail or other self-contained information archive or set of archives may be considered a distribution medium that is equivalent to a tangible storage medium. Accordingly, the disclosure is considered to include any one or more of a

computer-readable medium or a distribution medium and other equivalents and successor media, in which data or instructions may be stored.

[0009] In the embodiments described herein, an information handling system includes any instrumentality or aggregate of instrumentalities operable to compute, classify, process, transmit, receive, retrieve, originate, switch, store, display, manifest, detect, record, reproduce, handle, or use any form of information, intelligence, or data for business, scientific, control, entertainment, or other purposes. For example, an information handling system can be a personal computer, a consumer electronic device, a network server or storage device, a switch router, wireless router, or other network communication device, a network connected device (cellular telephone, tablet device, etc.), or any other suitable device, and can vary in size, shape, performance, price, and functionality.

[0010] The information handling system can include memory (volatile (e.g. random-access memory, etc.), nonvolatile (read-only memory, flash memory etc.) or any combination thereof), one or more processing resources, such as a central processing unit (CPU), a graphics processing unit (GPU), hardware or software control logic, or any combination thereof. Additional components of the information handling system can include one or more storage devices, one or more communications ports for communicating with external devices, as well as, various input and output (I/O) devices, such as a keyboard, a mouse, a video/graphic display, or any combination thereof. The information handling system can also include one or more buses operable to transmit communications between the various hardware components. Portions of an information handling system may themselves be considered information handling systems.

[0011] When referred to as a “device,” a “module,” or the like, the embodiments described herein can be configured as hardware. For example, a portion of an information handling system device may be hardware such as, for example, an integrated circuit (such as an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA), a structured ASIC, or a device embedded on a larger chip), a card (such as a Peripheral Component Interface (PCI) card, a PCI-express card, a Personal Computer Memory Card International Association (PCMCIA) card, or other such expansion card), or a system (such as a motherboard, a system-on-a-chip (SoC), or a stand-alone device).

[0012] The device or module can include software, including firmware embedded at a device, such as a Pentium class or PowerPC™ brand processor, or other such device, or software capable of operating a relevant environment of the information handling system. The device or module can also include a combination of the foregoing examples of hardware or software. Note that an information handling system can include an integrated circuit or a board-level product having portions thereof that can also be any combination of hardware and software.

[0013] Devices, modules, resources, or programs that are in communication with one another need not be in continuous communication with each other, unless expressly specified otherwise. In addition, devices, modules, resources, or programs that are in communication with one another can communicate directly or indirectly through one or more intermediaries.

[0014] FIG. 2 is a block diagram illustrating a cooling assembly for an internet of things (IOT) wireless gateway device. FIG. 2 illustrates a first motherboard component 230 in an embodiment operatively coupled to the first outer surface of the motherboard structure 210, as described further below with respect to FIG. 6.

[0015] FIG. 2 further illustrates an EMI shield 220 formed with a proximal outer surface, distal outer surface, proximal inner surface, and distal inner surface relative to the motherboard structure 210, as described further below with respect to FIG. 7.

[0016] FIG. 2 further illustrates the EMI shield 220 proximal outer surface operatively coupled to the motherboard structure 210 first outer surface to reduce signal interference at said first motherboard component 230, as described further below with respect to FIG. 7.

[0017] FIG. 2 further illustrates a first gap pad structure 240 being disposed between the first motherboard component 230 and the proximal inner surface of the EMI shield 220 to conduct heat, a second gap pad structure 250 operatively coupled to the distal outer surface of the EMI shield 220 to conduct heat, and a first heat sink 260 operatively coupled to the second gap pad structure 250 to conduct heat. It is understood that the individual components described above in FIG. 2 may further be separated by other intervening layers of various materials in some embodiments.

[0018] The first, and/or second gap pad structures 240, and/or 250, respectively may be any type of thermally conductive filler material, including, but not limited to thermal interface material, phase change material, and/or conductive grease.

[0019] The individual components 210 – 260 plus any additional intervening layers of the cooling assembly 200 for an internet of things (IOT) wireless gateway device according to embodiments of the present disclosure may be operatively coupled using any known coupling method or device, including, but not limited to one or more screws permeating each of the individual components, as shown in FIG. 2, by clips, and/ or through the use of adhesive materials disposed between one or more components. The individual components 210-260 plus any additional intervening layers in embodiments may be operatively coupled in a manner that creates increased pressure between or within certain components. For example, in an embodiment, one or more of the gap pads 240 and/or 250 may be kept at a pressure of at least 10 PSI by tightening the screw running through each of the components 210-260, as shown in FIG. 2.

[0020] FIG. 3 is a flow diagram illustrating a process of forming a cooling assembly for an IOT device according to an embodiment of the present disclosure. At block 305, in an embodiment, a motherboard structure may be formed having a first outer surface and a second outer surface. The process of FIG. 3 begins at block 310. In an embodiment, a first motherboard component 230 may be operatively coupled to the first outer surface of the motherboard surface 210, as described in further detail below with respect to FIG. 6.

[0021] At block 315, in an embodiment, an EMI shield 220 may be formed with a proximal outer surface, distal outer surface, proximal inner surface, and distal inner surface relative to the motherboard structure 210, as described in more detail below with respect to FIG. 7.

[0022] At block 320, in an embodiment, the EMI shield 220 proximal outer surface may be operatively coupled to the motherboard structure 210 first outer surface to reduce signal interference at said first motherboard component 230, as described further below with respect to FIG. 7.

[0023] At block 325, in an embodiment, a first gap pad structure 240 may be disposed between the first motherboard component 230 and the proximal inner surface of the EMI shield 220 to conduct heat. At block 330, in an embodiment, a second gap pad structure 250 may be operatively coupled to the distal outer surface of the EMI Shield 220 to conduct heat. At block 335, in an embodiment, a first heat sink 260 may be operatively coupled to the second gap pad structure 250 to conduct heat.

[0024] FIG. 4 is a block diagram illustrating a further cooling assembly for an internet of things (IOT) wireless gateway device in a further embodiment. FIG. 4 illustrates a first motherboard component 430 in an embodiment operatively coupled to the first outer surface of the motherboard structure 410, as described further below with respect to FIG. 6.

[0025] FIG. 4 further illustrates an EMI shield 420 formed with a proximal outer surface, distal outer surface, proximal inner surface, and distal inner surface relative to the motherboard 410, as described further below with respect to FIG. 7.

[0026] FIG. 4 further illustrates the EMI shield 420 proximal outer surface operatively coupled to the motherboard structure 410 first outer surface to reduce signal interference at said first motherboard component 430, as described further below with respect to FIG. 7.

[0027] FIG. 4 further illustrates a first gap pad structure 440 being disposed between the first motherboard component 430 and the proximal inner surface of the EMI shield 420 to conduct heat, a second gap pad structure 450 operatively coupled to the distal outer surface of the EMI shield 420 to conduct heat, and a first heat sink 460 operatively coupled to the second gap pad structure.

[0028] FIG. 4 further illustrates a second motherboard component 470 operatively coupled to the second outer surface of the motherboard structure 410, as described in further detail below with reference to FIG. 6.

[0029] FIG. 4 further illustrates a third gap pad structure 480 operatively coupled to the second motherboard component 470 to conduct heat, and a second heat sink 490 operatively coupled to the third gap pad structure 480 to conduct heat. It is understood that the individual components described above in FIG. 4 may further be separated by other intervening layers or various materials in some embodiments.

[0030] The first, second, and/or third gap pad structures 440, 450, and/or 480, respectively may be any type of thermally conductive filler material, including, but not limited to thermal interface material, phase change material, and/or conductive grease.

[0031] The individual components 410 - 490 plus any additional intervening layers of the cooling assembly 400 for an internet of things (IOT) wireless gateway device according to embodiments of the present disclosure may be operatively coupled using any known coupling method or device, including, but not limited to one or more screws permeating each of the individual components, as shown in FIG. 4, by clips, and/ or through the use of adhesive materials disposed between one or more components. The individual components 410-490 plus any additional intervening layers in embodiments may be operatively coupled in a manner that creates increased pressure between or within certain components. For example, in an embodiment, one or more of the gap pads 440, 450, and/or 480 may be kept at a pressure of at least 10 PSI by tightening the one or more screws running through each of the components 410-490, as shown in FIG. 4. Multiple screws or clips may provide an evened distribution of applied pressure in coupling the components.

[0032] FIG. 5 is a flow diagram illustrating a process of forming a cooling assembly for an IOT device according to an embodiment of the present disclosure. At block 505, in an embodiment, a motherboard structure may be formed having a first outer surface and a second outer surface. The process of FIG. 5 begins at block 510. In an embodiment, a first motherboard component 430 may be operatively coupled to the first outer surface of the motherboard surface 410, as described in further detail below with respect to FIG. 6.

[0033] At block 515, in an embodiment, an EMI shield 420 may be formed with a proximal outer surface, distal outer surface, proximal inner surface, and distal inner surface relative to the motherboard structure 410, as described in more detail below with respect to FIG. 7.

[0034] At block 520, in an embodiment, the EMI shield 420 proximal outer surface may be operatively coupled to the motherboard structure 410 first outer surface to reduce signal interference at said first motherboard component 430, as described further below with respect to FIG. 7.

[0035] At block 525, in an embodiment, a first gap pad structure 440 may be disposed between the first motherboard component 430 and the proximal inner surface of the EMI shield 420 to conduct heat. At block 530, in an embodiment, a second gap pad structure 450 may be operatively coupled to the distal outer surface of the EMI Shield 420 to conduct heat. At block 535, in an embodiment, a first heat sink 460 may be operatively coupled to the second gap pad structure 450 to conduct heat. At block 540, in an embodiment, a second motherboard component 470 may be operatively coupled to the second outer surface of the motherboard structure 410, as shown in further detail below with reference to FIG. 6.

[0036] At block 545, in an embodiment a third gap pad structure 480 may be operatively coupled to the second motherboard component 470 to conduct heat. At block 350, in an embodiment, a second heat sink 490 may be operatively coupled to the third gap pad structure 480 to conduct heat.

[0037] It is understood that the method steps described above in FIG. 5 may be performed in any order and that some or all steps may not be performed in every embodiment. In other embodiments, it is understood that additional steps may be performed in any combination.

[0038] FIG. 6 is a block diagram illustrating a motherboard structure in an embodiment having a first outer surface and a second outer surface. A motherboard structure in an embodiment may include one or more dual in-line memory module (DIMM) and/or one or more central processing unit (CPU). These DIMMs and CPUs may be attached to the motherboard on either side (i.e. the side of the motherboard structure closest to first motherboard component structure, or the side of the motherboard structure closest to the second motherboard component structure). A motherboard structure in an embodiment may include any or all of the components 102 – 160, and 170 – 180, shown in FIG. 1 as comprising the information handling system 100.

[0039] In an embodiment, a first motherboard structure 210 may have a first outer surface 610 and a second outer surface 620. Also in an embodiment, a first motherboard component 230 may be operatively coupled to the first outer surface 610 of the motherboard structure 210, as described further above with respect to FIG. 2 and with respect to block 310 in FIG. 3.

[0040] In a further embodiment, a first motherboard structure 410 may have a first outer surface 610 and a second outer surface 620. Also in a further embodiment, a first motherboard component 430 may be operatively coupled to the first outer surface 610 of the motherboard surface 410, as described in further detail above with respect to FIG. 4 and with respect to block 510 in FIG. 5. In a further embodiment, a second motherboard component 470 may be operatively coupled to the second outer surface 620 of the motherboard structure 410, as described in further detail above with reference to FIG. 4 and at block 540 in FIG. 5.

[0041] FIG. 7 is a block diagram illustrating an EMI shield formed in an embodiment with a proximal outer surface, a distal outer surface, a proximal inner surface, and a distal inner surface relative to a motherboard structure. In an embodiment an EMI shield 220 may be formed with a proximal outer surface 710, a distal outer surface 720, a proximal inner surface 730, and a distal inner surface 740 relative to the motherboard structure 210, as discussed in greater detail above with respect to FIG. 2, and with respect to block 320 of FIG. 3. Also in an embodiment, a first gap pad structure 240 may be disposed between the first motherboard component 230 and the proximal inner surface 730 of the EMI shield 220 to conduct heat, as discussed above in greater detail with reference to FIG. 2, and with reference to block 325 of FIG. 3. Also in an embodiment, a second gap pad structure 250 may be operatively coupled to the distal outer surface 720 of the EMI shield 220 to conduct heat, as discussed in greater detail above with respect to FIG. 2, and with respect to block 330 in FIG. 3.

[0042] In a further embodiment an EMI shield 220 corresponding to 420 in FIG. 4 may be formed with a proximal outer surface 710, a distal outer surface 720, a proximal inner surface 730, and a distal inner surface 740 relative to the motherboard structure 410, as discussed in greater detail above with respect to FIG. 4, and with respect to block 520 of FIG. 5. Also in an embodiment, a first gap pad structure 240 corresponding to 440 in FIG. 4 may be disposed between the first motherboard component 230 (corresponding to 430 in FIG. 4) and the proximal inner surface 730 of the EMI shield 220 to conduct heat, as discussed above in greater detail with reference to FIG. 4, and with reference to block 525 of FIG. 5. Also in an embodiment, a second gap pad structure 450 may be operatively coupled to the distal outer surface 720 of the EMI shield 220 corresponding to 420 I FIG. 4 to conduct heat, as discussed in greater detail above with respect to FIG. 4, and with respect to block 530 in FIG. 5.

[0043] Although only a few exemplary embodiments have been described in detail herein, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of the embodiments of the present disclosure. Accordingly, all such modifications are intended to be included within the scope of the embodiments of the present disclosure as defined in the following claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents, but also equivalent structures.

WHAT IS CLAIMED IS:

1. A cooling assembly for an IOT wireless gateway device comprising:
 - a motherboard structure having a first outer surface and a second outer surface and a first motherboard component operatively coupled to the first outer surface of the motherboard structure;
 - an EMI shield having a proximal outer surface, a distal outer surface, a proximal inner surface, and a distal inner surface relative to the motherboard structure;
 - the EMI shield proximal outer surface operatively coupled to the motherboard structure first outer surface;
 - a first gap pad structure disposed between said first motherboard component and the distal inner surface of the EMI shield to conduct heat;
 - a second gap pad structure operatively coupled to the distal outer surface of the EMI shield to conduct heat;
 - and
 - a first heat sink operatively coupled to the second gap pad to conduct heat.
2. The cooling assembly for an IOT wireless gateway device of claim 1, further comprising a second motherboard component operatively coupled to the second outer surface of the motherboard structure, a third gap pad structure operatively coupled to the second motherboard component to conduct heat, and a second heat sink operatively coupled to the third gap pad to conduct heat.
3. The cooling assembly for an IOT wireless gateway device of claim 1, wherein the EMI shield reduces signal interference at said first motherboard component.
4. The cooling assembly for an IOT wireless gateway device of claim 1, wherein the EMI shield has EMI shield sides, and wherein the EMI shield sides and distal inner surface, and the first motherboard structure surface encapsulate the first motherboard component.
5. The cooling assembly for an IOT wireless gateway device of claim 1, wherein the first, second, or third gap pads comprise thermally conductive gap filler material.

6. The cooling assembly for an IOT wireless gateway device of claim 1, wherein the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink are operatively coupled via a screw disposed through the entire cooling assembly for an IOT wireless gateway device.
7. The cooling assembly for an IOT wireless gateway device of claim 1, wherein the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink are operatively connected such that the first and second gap pads are held at a pressure of at least 10 PSI.
8. A process of forming a cooling assembly for an IOT wireless gateway device comprising:
- forming a motherboard structure having a first outer surface and a second outer surface;
 - operatively coupling a first motherboard component to the first outer surface of the motherboard structure;
 - forming an EMI shield having a proximal outer surface, a distal outer surface, a proximal inner surface, and a distal inner surface relative to the motherboard structure;
 - operatively coupling the EMI shield proximal outer surface to the motherboard structure first outer surface to enhance signal integrity;
 - disposing a first gap pad structure between a first motherboard component and a proximal inner surface of the EMI shield to conduct heat;
 - operatively coupling a second gap pad structure to the distal outer surface of the EMI shield to conduct heat; and
 - operatively coupling a first heat sink to the second gap pad to conduct heat.
9. The process of claim 8, further comprising operatively coupling a second motherboard component to the second outer surface of the motherboard structure, operatively coupling a third gap pad structure to the second motherboard component to conduct heat, and operatively coupling a second heat sink to the third gap pad to conduct heat.
10. The process of claim 8, wherein the EMI shield reduces signal interference at said first motherboard component.

11. The process of claim 8, wherein the EMI shield has EMI shield sides, and wherein the EMI shield sides and distal inner surface, and the first motherboard structure surface encapsulate the first motherboard component.
12. The process of claim 8, wherein the first, second, or third gap pads comprise thermally conductive gap filler material.
13. The process of claim 8, further comprising operatively connecting the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink by disposing a screw through the entire cooling assembly for an IOT wireless gateway device.
14. The process of claim 8, further comprising operatively coupling the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink such that the first and second gap pads are held at a pressure of at least 10 PSI.
15. A cooling assembly for an IOT wireless gateway device comprising:
 - a motherboard structure having a first outer surface and a second outer surface and a first motherboard component operatively coupled to the first outer surface of the motherboard structure;
 - an EMI shield having a proximal outer surface, a distal outer surface, a proximal inner surface, and a distal inner surface relative to the motherboard structure;
 - the EMI shield proximal outer surface operatively coupled to the motherboard structure first outer surface;
 - a first gap pad structure disposed between said first motherboard component and the distal inner surface of the EMI shield to conduct heat;
 - a second gap pad structure operatively coupled to the distal outer surface of the EMI shield to conduct heat;
 - a first heat sink operatively coupled to the second gap pad to conduct heat;
 - a second motherboard component operatively coupled to the second outer surface of the motherboard structure;
 - a third gap pad structure operatively coupled to the second motherboard component to conduct heat; and
 - a second heat sink operatively coupled to the third gap pad to conduct heat.

16. The cooling assembly for an IOT wireless gateway device of claim 15, wherein the EMI shield reduces signal interference at said first motherboard component.

17. The cooling assembly for an IOT wireless gateway device of claim 15, wherein the EMI shield has EMI shield sides, and wherein the EMI shield sides and distal inner surface, and the first motherboard structure surface encapsulate the first motherboard component.

18. The cooling assembly for an IOT wireless gateway device of claim 15, wherein the first, second, or third gap pads comprise thermally conductive gap filler material.

19. The cooling assembly for an IOT wireless gateway device of claim 15, wherein the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink are operatively coupled via a screw disposed through the entire cooling assembly for an IOT wireless gateway device.

20. The cooling assembly for an IOT wireless gateway device of claim 15, wherein the motherboard structure, motherboard component, first gap pad, EMI shield, second gap pad, and first heat sink are operatively connected such that the first and second gap pads are held at a pressure of at least 10 PSI.

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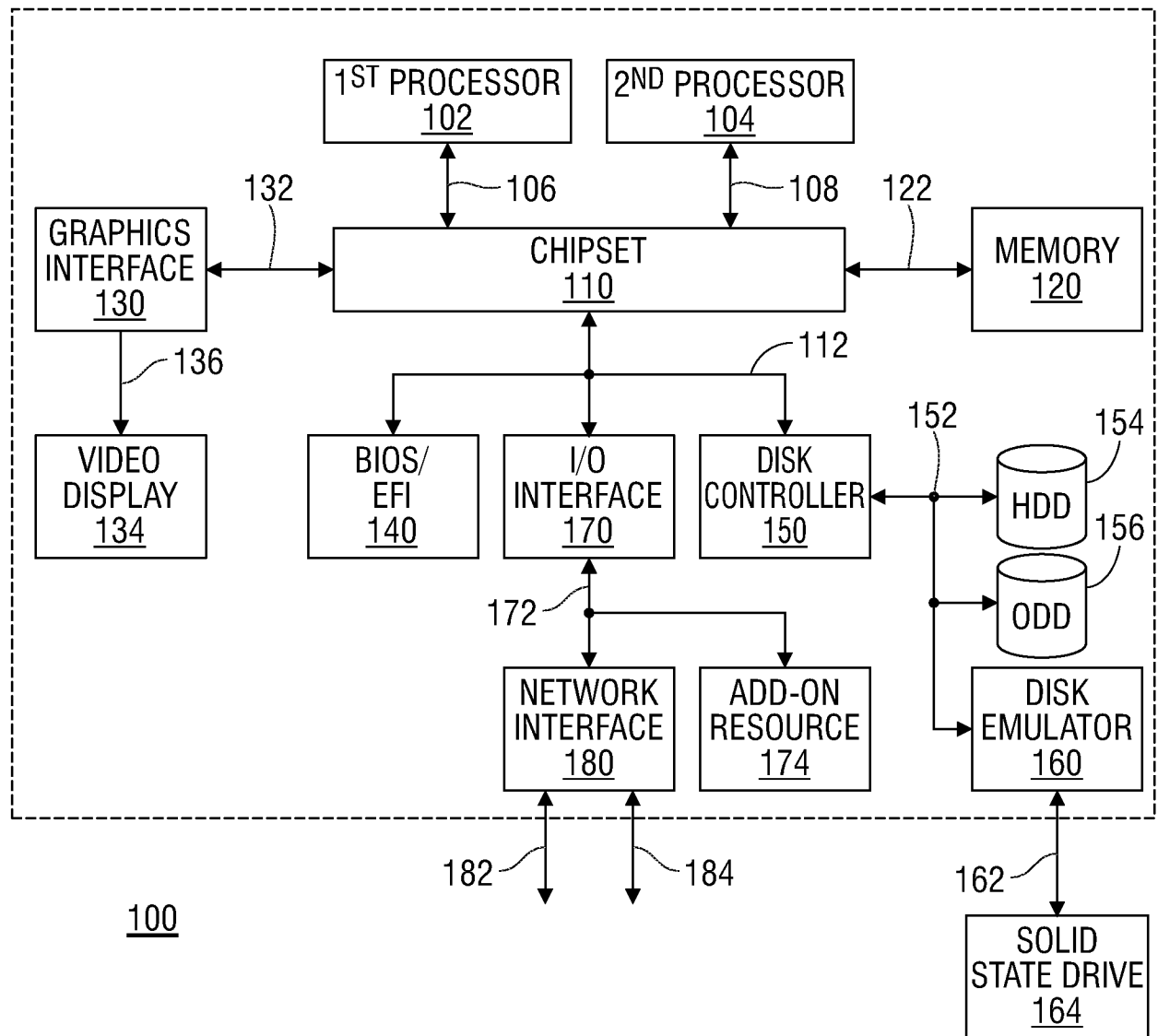


FIG. 1

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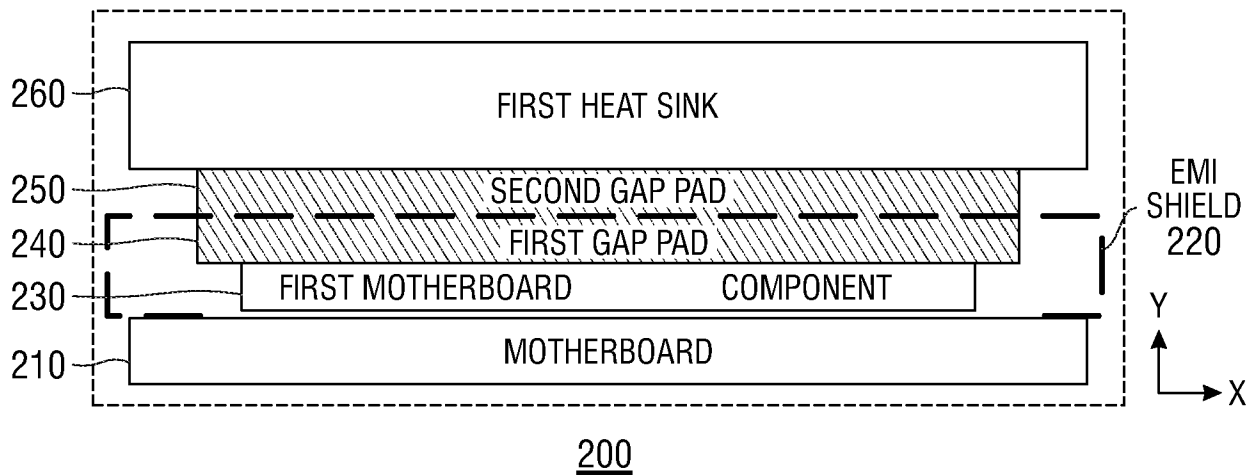


FIG. 2

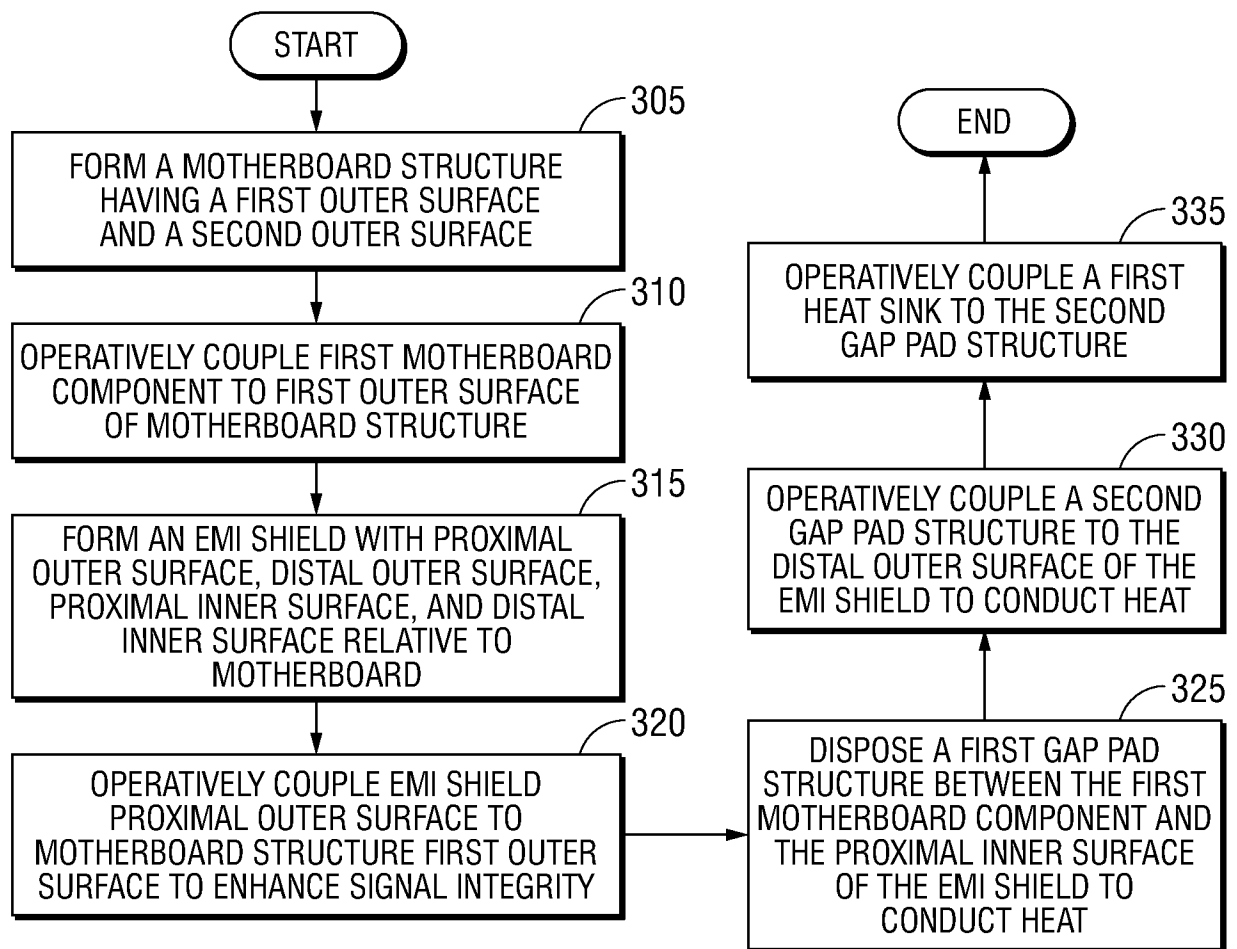


FIG. 3

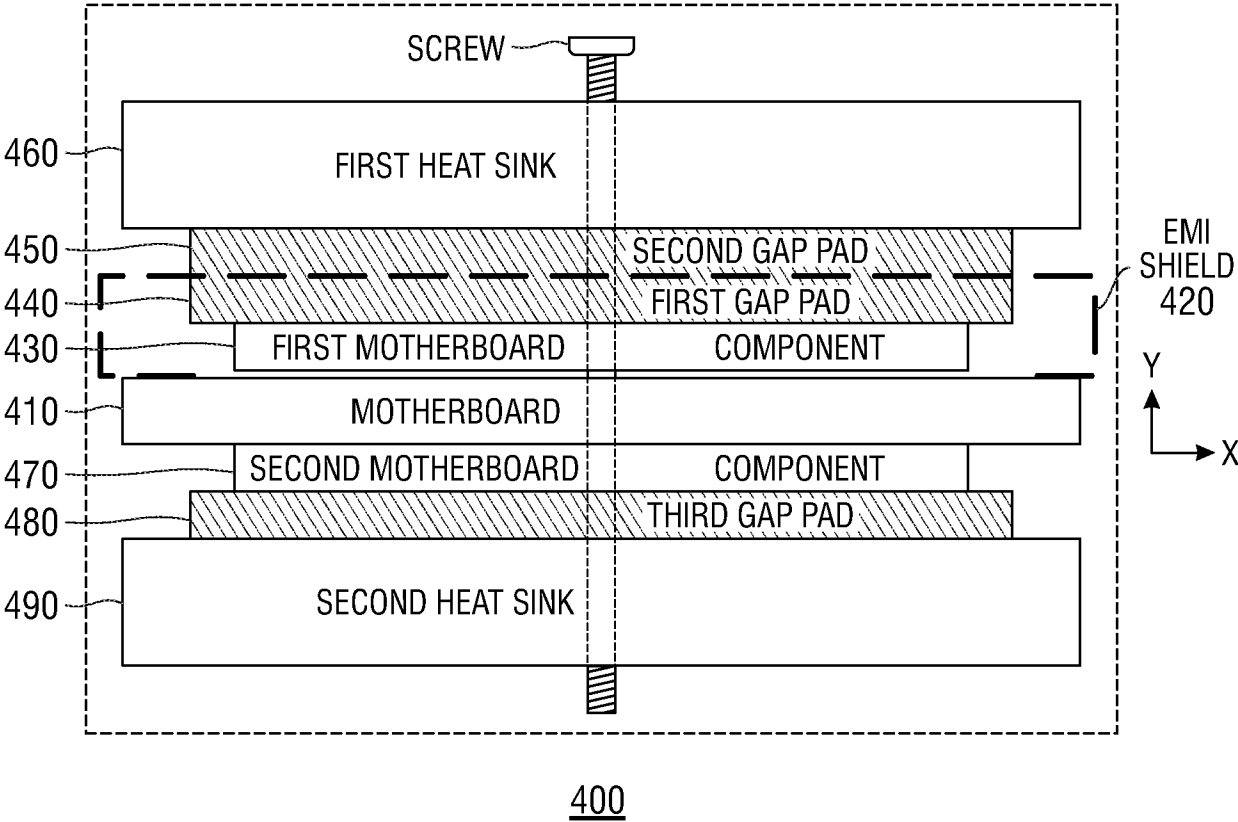


FIG. 4

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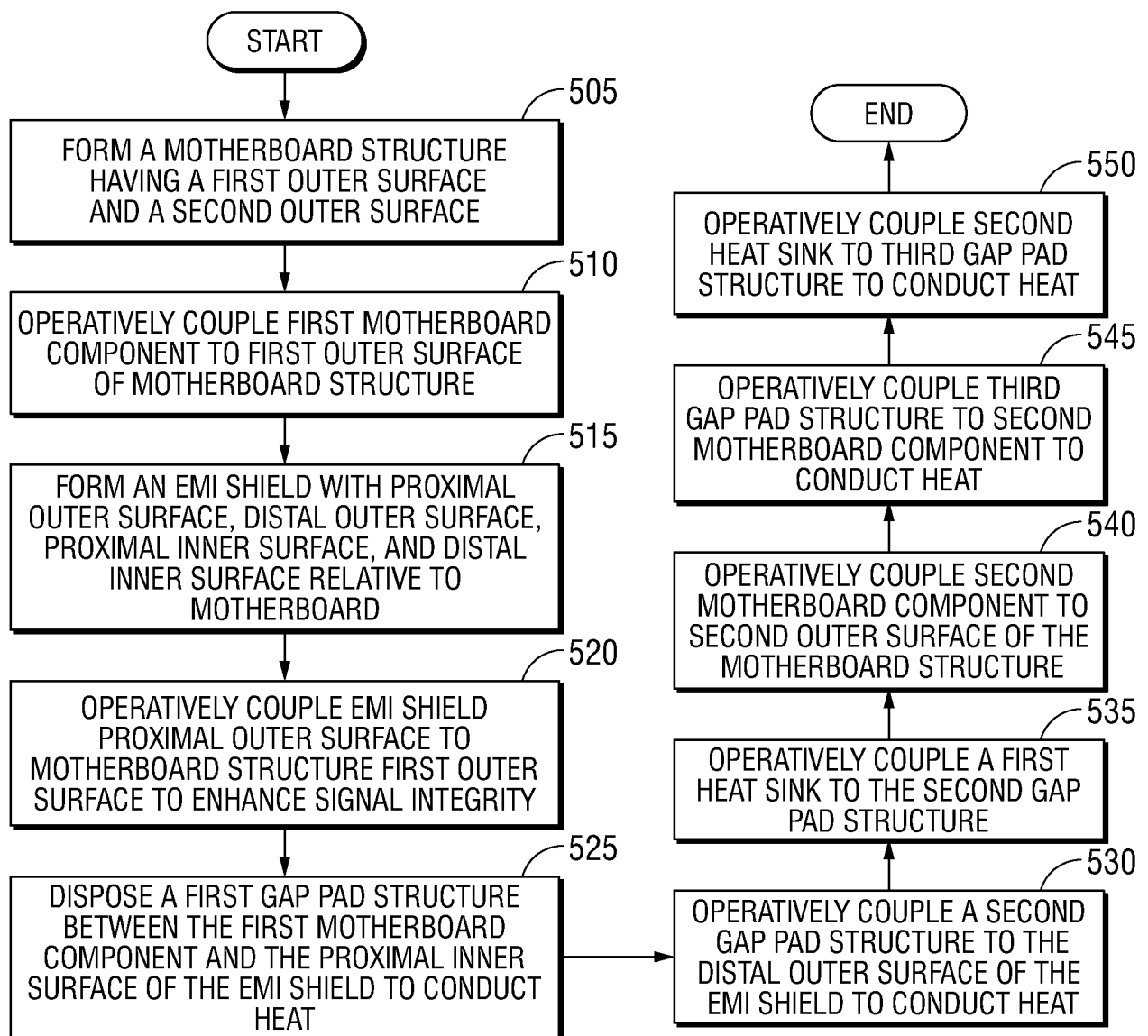


FIG. 5

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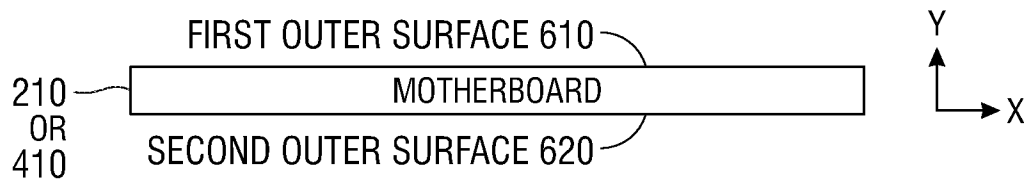


FIG. 6

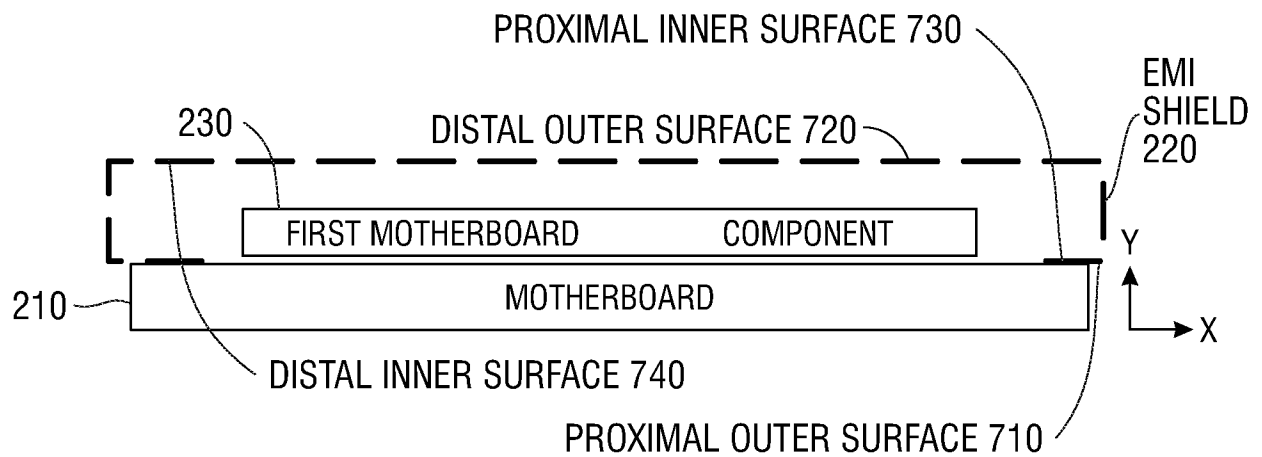


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2016/042091

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H05K 7/20 (2016.01)

CPC - H05K 7/20; H05K 1/0201; H05K 1/0203; H05K 1/0204 (2016.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC - H05K 7/20

CPC - H05K 1/0201; H05K 1/0203; H05K 1/0204; H05K 7/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 25///12; 25///18; 25///19; 361/707; 361/709; 361/716; 361/719; 361/720; 361/800; 361/816; 361/818; 361/679.540 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Orbit, Google Patents, Google Scholar.

Search terms used: board, PCB, circuit, thermal, gap, EMI, electromagnetic, interference, shield, couple, mount, connect, assembly, PSI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---	US 8,213,180 B2 (ZHAO et al) 03 July 2012 (03.07.2012) entire document	1, 3-5, 8, 10-12
Y		2, 6, 7, 9, 13-20
Y	US 7,623,349 B2 (REFAI-AHMED et al) 24 November 2009 (24.11.2009) entire document	2, 9, 15-20
Y	US 6,717,799 B2 (HAMANO et al) 06 April 2004 (06.04.2004) entire document	6, 13, 19
Y	US 8,477,499 B2 (HILL et al) 02 July 2013 (02.07.2013) entire document	7, 14, 20
A	US 7,120,027 B2 (YATSKOV et al) 10 October 2006 (10.10.2006) entire document	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

01 September 2016

Date of mailing of the international search report

23 SEP 2016

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