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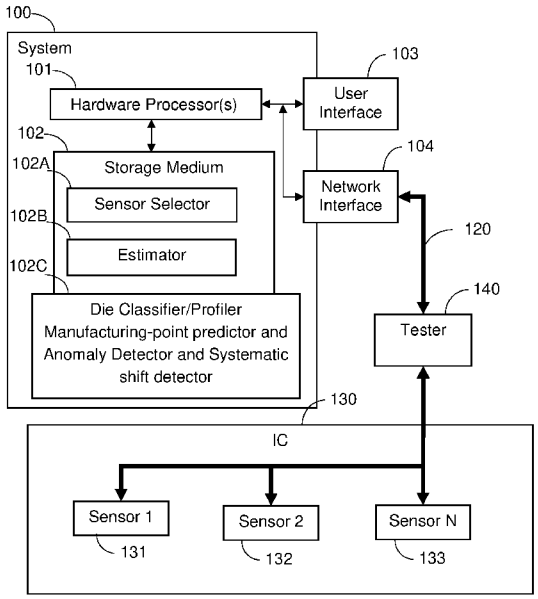


FIG. 1

(57) Abstract: A computerized method for IC classification, outlier detection and/or anomaly detection comprising using at least one hardware processor for testing each of the plurality of ICs in accordance with an IC design on a wafer, wherein the IC design comprises a plurality of sensors. The at least one hardware processor is used for testing each of the plurality of ICs by: collecting a plurality of sensor values, the plurality of sensor values including sensor values from each of the plurality of sensors; comparing the plurality of sensor values to a classification scheme, thereby obtaining a classification for each tested IC; and recording the classification of the tested IC. A computerized method for IC classification, outlier detection and/or anomaly detection comprising using at least one hardware processor for testing each of the plurality of ICs in accordance with an IC design on a wafer, wherein the IC design comprises a plurality of sensors. The at least one hardware processor is used for testing each of the plurality of ICs by: collecting a plurality of sensor values, the plurality of sensor values including sensor values from each of the plurality of sensors; comparing the plurality of sensor values to a classification scheme, thereby obtaining a classification for each tested IC; and recording the classification of the tested IC.

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INTEGRATED CIRCUIT PROFILING AND ANOMALY DETECTION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority of U.S. Provisional Patent Application No. 62/657,986, filed April 16, 2018, "INTEGRATED CIRCUIT PROFILING AND ANOMALY DETECTION", the contents of which are all incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

[0002] The invention relates to the field of integrated circuits.

BACKGROUND

[0003] Integrated circuits (ICs) may include analog and digital electronic circuits on a flat semiconductor substrate, such as a silicon (Si) wafer. Microscopic transistors are printed onto the substrate using photolithography techniques to produce complex circuits of billions of transistors in a very small area, making modern electronic circuit design using ICs both low cost and high performance. ICs are produced by assembly lines of factories, termed foundries, that have commoditized the production of ICs, such as complementary metal-oxide-semiconductor (CMOS) ICs. Digital ICs contain billions of transistors arranged in functional and/or logical units on the wafer, and are packaged in a metal, plastic, glass, ceramic casing, and/or the like.

[0004] ICs are tested during production for detection of defects, such as by using wafer tests, package tests, circuit tests, end-user device operational tests, and/or the like. For example, wafer testing may determine bad ICs on each wafer tested, and the defective ICs may be discarded. For example, package/circuit/device testing may test the product operation prior to end-user use, and defective products/batches discarded. For example, marketing, warranty, and maintenance statistics may reflect on the compliance between the requirements, specs, design, and testing during the product development. Each of these types of tests may produce lists of defective products that may be analyzed to improve the design of the next generation of products, such as by reducing the number of defective parts per million (DPPM) in the manufacturing of an IC and/or end-user product.

[0005] DPPM is a common metric used to measure quality of semiconductor product production. With electronics becoming a part of everyday life (such as wearable electronics and semi-autonomous vehicles), there's an increasing drive to improve quality and prevent failures in use. For mission-critical segments, such as automotive, medical, and/or the like, customer requirements are driving improvements to the Defective Parts Per Billion (DPPB) range.

[0006] Currently, many methods are used to improve quality in the overall manufacturing test process: data feed forward, bi- variant and multi-variant analysis, quality indexing, and/or the like. Many of these methods are used to deliver products to quality and safety-sensitive market segments, such as automotive, medical, data servers, and/or the like. These methods may lower DPPM rates and may reduce the number of expensive test steps, such as burn-in and system-level tests.

[0007] Data Feed Forward (DFF) methods leverage data collected from any step in the manufacturing flow and make the data available to any other downstream test. By analyzing manufacturing data throughout the supply chain, manufacturing and quality engineers may recall data from any test, such as wafer sort, package, final circuit test, system-level test, and/or the like, for improving the DPPM. This data may be compared in real-time for the same device being tested to check for any variations in test results (i.e., anomalies) that may indicate whether the product prematurely fail during use, changes to the manufacturing should be made, and/or the like.

[0008] Bi-variant and multi-variant analyses try to find empirical relationships between two or more tests. Tests that have strong correlations may be used to identify outliers within the populations. This may improve quality for many market segments because bi-variant and multi-variant outliers may be devices that are difficult to screen out by regular test programs. These outliers may have high correlation to devices that may fail prematurely, be returned as RMAs, and/or the like.

[0009] ICs for automotive applications are specified to satisfy long-term reliability requirements and be less sensitive to electromechanical stresses. Robustness of automotive ICs may be related to individual IC products whose test parameters are well-centered in the distributions of the main parameters reported in the datasheets of the ICs. Part-average testing (PAT) may identify the ICs with more well centered parameters, i.e., strongly on spec.

[0010] PAT may be adopted by semiconductor companies to help them meet the stringent requirements of the automotive industry (such as Automotive Electronics

Council: AEC-Q001-Rev D). Reliability studies have shown that semiconductor parts that have abnormal characteristics tend to be higher contributors to long-term quality and reliability problems. Devices that originally passed all manufacturing tests but may be considered "outliers" compared to other parts in the same population or lot may be more likely to fail in the field. This may be the basis for PAT, which proactively identifies outliers for exclusion from production shipments. PAT may operate by modifying the pass/fail test limits based on statistical sampling of multiple devices.

[0011] PAT may be a dynamic test. For example, in an Electrical Wafer Sort (EWS) process the testing procedure of a silicon wafer containing ICs may be performed by a mechanical probe that makes contact to the pads of each IC on the wafer. The probe card may be electrically connected through cables to the testing equipment. An automated system sequentially tests all the dies contained in the wafer. As the testing procedure proceeds, the data log file containing the measurement results may be analyzed by software to compute mean (μ) and standard deviation (s). Once the distributions of parameters are known, the outlier parts that passed the test but are not in the range may be identified. For example, parts are rejected and considered out of specifications at PAT 4 sigma test, such as outside of the range of from μ-4*s to μ+4*s.

[0012] The foregoing examples of the related art and limitations related therewith are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the figures.

SUMMARY

[0013] The following embodiments and aspects thereof are described and illustrated in conjunction with systems, tools and methods which are meant to be exemplary and illustrative, not limiting in scope.

[0014] There is provided, in accordance with an embodiment, a computerized method for IC classification and/or outlier detection, comprising: providing a wafer comprising a plurality of ICs in accordance with an IC design, wherein the IC design comprises a plurality of sensors; and using at least one hardware processor for testing each of the plurality of ICs by: collecting a plurality of sensor values, the plurality of sensor values including sensor values from each of the plurality of sensors; and comparing the

plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC. In embodiments, the method further comprises recording the classification of each tested IC. In embodiments, the step of providing comprises manufacturing the wafer based on the IC design using a fabrication process.

[0015] There is provided, in accordance with an embodiment, a computerized method for semiconductor integrated circuit (IC) classification, comprising using at least one hardware processor for: receiving an IC design and data descriptive of a fabrication process. The at least one hardware processor is used for simulating a plurality of IC electronic operations based on the IC design and fabrication process to produce a plurality of simulated IC operation values and a plurality of simulated device operation values. The at least one hardware processor is used for factorizing the plurality of simulated IC operation values and the plurality of simulated device operation values to determine a subset of operational values for sensor placement. The at least one hardware processor is used for selecting some of the subset of operational values producing a sensor placement set, and for each of the selected subset, analyzing the IC design to incorporate within the IC design one of a plurality of sensors configured to the specific electronic operation, wherein each element of the sensor placement set comprises a type of sensor and a location within the IC design, wherein the sensor placement set is configured to produce a plurality of sensor values that are sensitive to the IC design and the fabrication process. The at least one hardware processor is used for classifying the IC design into operational classes based on the plurality of sensor values thereby producing a classification scheme, wherein the operational classes comprise at least one outlier class. The classes (operational, outliers, etc.) may be determined either from the pre-Si simulated data or/and from the post-Si wafer test data.

[0016] There is provided, in accordance with an embodiment, a computerized method for IC anomaly detection comprising using at least one hardware processor for manufacturing a wafer based on an IC design using a fabrication process, wherein the wafer comprises a plurality of ICs, and wherein the IC design comprises a plurality of sensors. The at least one hardware processor is used for testing each of the plurality of ICs by: collecting a plurality of sensor values, at least one of the plurality of sensor values from each of the plurality of sensors; comparing the plurality of sensor values to a classification scheme; and recording the classification of the tested IC.

[0017] There is provided, in accordance with an embodiment, a testing device for reducing the test time of each of a plurality of ICs, comprising at least one hardware processor. The hardware processor is configured for testing each of a plurality of ICs by: collecting a plurality of sensor values, at least one of the plurality of sensor values from each of a plurality of sensors incorporated into each of the plurality of ICs; comparing the plurality of sensor values to a classification scheme, thereby obtaining a classification for each tested IC; and reducing the test time for each tested IC based on the classification.

[0018] In some embodiments, the classification scheme is based on simulations of a plurality of IC operations of the IC design and the fabrication process, wherein the simulations are at least one of at least one complete IC design simulation, at least one partial IC design simulation, and at least one device simulation for the fabrication process.

[0019] In some embodiments, the classification scheme is based on a plurality of training sensor values collected during a pre-production tape-out test.

[0020] In some embodiments, the classification scheme is based on the collected plurality of sensor values.

[0021] In some embodiments, the classification scheme comprises an outlier class.

[0022] In some embodiments, the comparing comprises estimating high coverage measurements from the plurality of sensor values using at least one of a function and a rule determined from a training set of sensor values and training high coverage measurements.

[0023] In some embodiments, the factorizing comprises incorporation of post-Si wafer testing data into determining the subset.

[0024] In some embodiments, the factorizing comprises incorporation of end-customer use data into determining the subset.

[0025] In some embodiments, the selecting comprises incorporation of post-Si wafer testing data into determining the sensor placement set.

[0026] In some embodiments, the factorizing comprises incorporation of end-customer use data into determining the sensor placement set.

[0027] In some embodiments, any of the computerized methods herein disclosed further comprise using the least one hardware processor for marking an IC package of the tested IC with unique identifications based on the classification.

[0028] In some embodiments, each of the plurality of sensors is selected from the group consisting of a rising time delay sensor, a falling time delay sensor, a frequency maximum detection circuit, an IC unit total leakage current detection sensor based on a frequency conversion circuit, an IC unit voltage drain to drain leakage current detection sensor based on a frequency conversion circuit, an IC unit voltage source to drain leakage current detection sensor based on a frequency conversion circuit, an IC unit SRAM minimal voltage frequency conversion circuit, and/or the like.

[0029] In some embodiments, any of the methods herein disclosed are embodied in a computer program product.

[0030] In some embodiments, any of the methods herein disclosed are embodied in a computerized system.

[0031] In some embodiments, any of the computerized methods herein disclosed further comprise using the least one hardware processor for marking an IC package of the tested IC with unique identifications based on the classification.

[0032] In some embodiments, any of the computerized methods herein disclosed further comprise using the least one hardware processor for discarding a defective IC.

[0033] In some embodiments, the each of the plurality of sensors is selected from the group consisting of a rising time delay sensor, a falling time delay sensor, a frequency maximum detection circuit, an IC unit total leakage current detection sensor based on a frequency conversion circuit, an IC unit voltage drain to drain leakage current detection sensor based on a frequency conversion circuit, and an IC unit voltage source to drain leakage current detection sensor based on a frequency conversion circuit.

[0034] In some embodiments, the computerized method further comprises: (i) from each tested IC, determining a set of parameters of the fabrication process based on the classification and the plurality of sensor values, (ii) selecting a second set of parameters of the fabrication process based on the IC design and the sets of parameters of the fabrication process for each IC, and (iii) a second manufacturing of a second wafer using the second set of parameters, wherein the selecting is performed by at least one of a manual process and an automatic computation.

[0035] In some embodiments, the computerized method further comprises determining at least one of (i) a sensor value shift and (ii) an outlier using the classification scheme during at least one of a package testing, a circuit testing, a burn-in testing, a high-temperature operating life testing, and a final product testing.

[0036] In some embodiments, the classification comprises a hierarchical data structure for determining the classification of each die.

[0037] In some embodiments, the method further comprises: identifying the classification scheme based on a plurality of classification values by: establishing a matrix representation from the plurality of classification values, each row of the matrix representation comprising classification values in respect of one of the plurality of ICs; computing a covariance matrix from the matrix representation and a singular value decomposition (SVD) for the covariance matrix; determining, using the SVD, a plurality of distance values, each distance value representing a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs; and identifying, from the plurality of distance values, at least one family, thereby defining the classification scheme.

[0038] In some embodiments, the step of identifying, from the plurality of distance values, at least one family comprises: classifying a first IC of the plurality of ICs in a first family, such that the first family is defined by the first IC; comparing a distance value, from the plurality of distance values, representing a distance between the first IC and a second IC of the plurality of ICs with a predetermined threshold; if the distance value is less than the predetermined threshold, classifying the second IC in the first family; and if the distance value is greater than the predetermined threshold, classifying the second IC in a second family, such that the second family is defined by the second IC.

[0039] In some embodiments, the step of identifying, from the plurality of distance values, a plurality of families further comprises, for each other IC of the plurality of ICs: identifying a group of distance values, from the plurality of distance values, each distance value in the group of distance values representing a distance between the other IC and a respective IC of the plurality of ICs that defines a respective family; comparing each distance value from the group of distance values with the predetermined threshold; if a distance value from the group of distance values, representing a distance between the respective other IC and a specific IC of the plurality of ICs that defines a specific family, is less than the predetermined threshold, classifying the other IC in the specific family; and if all the distance values from the group of distance values are greater than the predetermined threshold, classifying the other IC in a new family, such that the new family is defined by the other IC.

[0040] In some embodiments, the step of computing a covariance matrix from the matrix representation comprises normalizing the matrix representation prior to computing the covariance matrix.

[0041] In some embodiments, the plurality of classification values are based on one or more of: simulated sensor values determined from a simulation of the IC design; a plurality of training sensor values collected during a pre-production tape-out test; and measured sensor values.

[0042] In some embodiments, the step of identifying the classification scheme based on the plurality of classification values is at least part of the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC.

[0043] In some embodiments, the plurality of classification values are based on simulated sensor values determined from a simulation of the IC design. In some embodiments, the step of identifying the classification scheme based on a plurality of classification sensor values takes place before the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC, the step of comparing the plurality of collected sensor values to a classification scheme comprising: establishing a collected data matrix representation from the plurality of collected sensor values, each row of the matrix representation comprising collected sensor values in respect of one of the plurality of ICs; computing a collected data covariance matrix from the collected data matrix representation and a singular value decomposition (SVD) for the collected data covariance matrix; determining, using the SVD, a plurality of collected data distance values, each distance value representing a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs; and classifying, from the plurality of distance values, each of the ICs according to the classification scheme.

[0044] In some embodiments, the step of computing a covariance matrix from the matrix representation comprises normalizing the matrix representation prior to computing the covariance matrix to define normalization coefficients thereby. In some embodiments, the step of computing a collected data covariance matrix from the collected data matrix representation comprises normalizing the matrix representation using the defined normalization coefficients prior to computing the collected data covariance matrix.

[0045] In some embodiments, the matrix representation is established from simulated sensor values determined from a simulation of the IC design and/or design signature values and/or catalog values.

[0046] In some embodiments, the step of determining, using the SVD, a plurality of distance values comprises: defining a set of Pre-Si SVD signatures by identifying vectors of the SVD for which the corresponding principal values of the SVD are greater than a pre-defined value and/or a pre-defined number of principal vectors of the SVD for which the principal values of the SVD are the greatest; and determining the plurality of distance values using the set of Pre-Si SVD signatures. In some embodiments, the step of determining the plurality of distance values using the Pre-Si SVD signatures comprises calculating at least some of the plurality of distance values, each of the at least some of the plurality of distance values being based on a distance between one of the Pre-Si SVD signatures and another of the Pre-Si SVD signatures. In some embodiments, the step of determining the plurality distance values using the set of Pre-Si SVD signatures comprises: configuring a plurality of estimators from the simulated sensor values and the set of Pre-Si SVD signatures, each estimator generating an estimated SVD signature from input sensor values; estimating from the plurality of estimators, for each of the plurality of ICs, a respective Post-Si SVD signature from the plurality of sensor values; and calculating at least some of the plurality of distance values, each of the at least some of the plurality of distance values being based on a distance between one of the Post-Si SVD signatures and another of the Post-Si SVD signatures.

[0047] In some embodiments, the step of determining the plurality distance values using the set of Pre-Si SVD signatures further comprises calculating further distance values of the plurality of distance values, each of the further distance values being based on a distance between the Pre-Si SVD signature for one IC and the Post-Si SVD signature for another IC.

[0048] In some embodiments, the method further comprises computing at least one conversion rule comprising an input data and an output data.

[0049] In addition to the exemplary aspects and embodiments described above, further aspects and embodiments will become apparent by reference to the figures and by study of the following detailed description. Moreover, the various features and embodiments of the invention described above are specifically contemplated to be used alone as well as in various combinations.

BRIEF DESCRIPTION OF THE FIGURES

[0050] Exemplary embodiments are illustrated in referenced figures. Dimensions of components and features shown in the figures are generally chosen for convenience and clarity of presentation and are not necessarily shown to scale. The figures are listed below.

[0051] FIG. 1 shows schematically a computerized system for integrated circuit profiling and outliers detection;

[0052] FIG. 2 shows flowcharts of methods for integrated circuit profiling and anomaly detection;

[0053] FIG. 3A shows schematically a first circuit for IC unit high-coverage timing-margin detection;

[0054] FIG. 3B shows schematically a second circuit for IC unit high-coverage timing-margin detection;

[0055] FIG. 4 shows a radar (spider) plot of IC profiles;

[0056] FIG. 5 shows a graph of distributions of values for different IC profiles;

[0057] FIG. 6 shows a graph of distribution separation between two different IC profiles;

[0058] FIGs. 7A thru 7D show a graph of distributions of values for two IC profiles under varying voltage and temperature;

[0059] FIG. 8 shows a graphical distribution of simulated values for an IC profile and an outlier;

[0060] FIG. 9 shows a graphical distribution of the error between the values of a simulated High-coverage measurement and its estimator, while an outlier is planted;

[0061] FIG. 10A shows a first systematic-shift detection;

[0062] FIG. 10B shows a second systematic-shift detection;

[0063] FIG. 11 shows example IDDQ measurement distributions for devices formed on a wafer, classified into families;

[0064] FIG. 12 shows example cycle-time measurement distributions for devices formed on a wafer of FIG. 11, classified into families;

[0065] FIG. 13 shows, for the ICs formed on a wafer of FIG. 11, a histogram of differences between IDDQ measurements and the average value for the Family associated with the respective IC;

[0066] FIG. 14 shows the data shown in FIG. 11, illustrating identification of an outlier die.

DETAILED DESCRIPTION

Glossary

[0067] **Si-Manufacturing (process) space**

[0068] Si manufacturing (process) space is the joint distribution of Si-related parameters (process parameters) over a large number of manufactured dies. The process space is the joint distribution of device-related parameters over a large number of manufactured dies, for example, the distribution of a device threshold voltage over a large number of manufactured dies. The process space affects the performance distribution of a large number of manufactured dies, for example, the joint distribution of Maximum-frequency (Fmax) and leakage current (Ioff) across many dies. As used herein, the terms process space or manufacturing space mean the set of possible manufacturing parameters (i.e., tolerances, manufacturing variability, etc.) as represented by the manufacturing of a specific die.

[0069] **Device type**

[0070] A certain process-technology is characterized by the device types that are manufactured using the technology (i.e., process, fab, etc.), for example:

[0071] SVT-type: N or P devices manufactured with standard threshold voltage,

[0072] LVT-type: N or P devices manufactured with low threshold voltage, and

[0073] ULVT-type: N or P devices manufactured with ultra-low threshold voltage.

[0074] **Pre-Si data (or Pre-Silicon Data)**

[0075] Data that is generated by simulating a certain IC design manufactured by a certain process, such as by Monte-Carlo simulations.

[0076] **Post-Si data (or Post-Silicon Data)**

[0077] Data that is measured from manufactured dies, such as data recorded during wafer testing.

[0078] **Signature**

[0079] Sets of values or expected distributions used in determining manufactured IC performance (class, outlier, etc.), such as IC-design simulated parameter superset,

tested die sensor values, and/or the like. Most uses of the word signature herein may be replaced with the word data.

[0080] **Agent (sensor)**

[0081] A Sensor/Agent is an electrical circuit, implemented on the die, that is used to sense or measure a certain device parameter, a sub-circuit parameter, a die-level parameter, and/or the like. For example, a sensor measures the delay of a certain logic cell.

[0082] **IC Design Simulation Values**

[0083] IC design operational parameters are simulated electronic parameters (i.e., voltage, current, delay, etc.) of a specific IC design with a specific simulated manufacturing process, such as the electrical parameters of an IC design over the process space. This may be a finite set, such as a large number, of possible parameters that may be measured, such as the set of all possible parameters at circuit locations that may be candidates for placing a sensor (agent).

[0084] The IC design is determined by the device-types, device-sizes, device occurrence, device locations, devices connectivity, and/or the like, that are used in the specific logic units (cells) of the IC design. The parameters may be simulated over the manufacturing space by performing Monte-Carlo (MC) simulations. For example, distributions of parameter values are simulated for the average leakage current of a specific unit within the IC design. The IC design parameters are used as an input for the singular value decomposition (SVD) computation.

[0085] **Device-process Simulated Values**

[0086] Device-process parameters are sets of simulated device operational parameters, such as a catalog of device operational parameters, for individual (single) devices in a specific process, such as transistors, FETs, diodes, and/or the like. The device parameters are simulated over the manufacturing space by performing Monte-Carlo (MC) simulations. For example, the catalog includes MC data of the saturation current of a certain device (IDSAT). The device-process parameter catalog is used as an input for the SVD computation.

[0087] **Inter-Connect simulated values**

[0088] Inter-Connect simulated values are a set of simulated delay-parameters values of Inter-Connect networks. For example, the delay of Resistor-Capacitor (RC) networks connecting devices. The delay value of the RC networks is extracted over the

manufacturing space by performing Inter-Connect extraction methods followed by a circuit simulation.

[0089] **Classification/Profiling**

[0090] Classification or profiling is the process of binning dies into Si-profiles, where each bin (profile) comprises a cluster of IC-design parameters and resulting device-level-parameters, such as high coverage parameters. During Pre-Si, the IC-design parameters and device-process parameters may be used as an input for the profiling process. During Post-Si, the sensor values and/or certain high coverage measurements may be used as input for the profiling process.

[0091] **IC Profile**

[0092] A specific cluster of signatures (data) values and distributions that may apply to field performance (specs, defects, etc.) For example, a specific cluster of the manufacture-space (data) values and distributions that may apply to field performance (specs, defects, etc.).

[0093] **Family (of dies)**

[0094] A group of physical dies with the same Si-profile/classification. In addition, a family is a group of MC samples, for which the simulated IC Design Simulation Values and the Device-Process Simulated Values have the same Si-profile/classification as those of the physical family members.

[0095] **Singular Value Decomposition (SVD)**

[0096] The SVD of a matrix σ is a set of three matrixes U, D and V such that $\Sigma = UDV^T$ where U and V denote orthogonal matrix of the left and right principal vectors of Σ, and D denotes a diagonal matrix with diagonal elements known as the singular values of Σ. For the profiling implementation, Σ denotes a covariance matrix and therefor $\mathrm{U} = V$. The singular value corresponds to a principal vector may be the variance at the vector direction.

[0097] The inputs to the SVD computation are the IC-design simulation values and device-process simulation values, and the output is a subset (i.e., such as a Device-Reduced-Representation, DRR) of the IC-design parameters that attempt to provide the most information efficiently, such as with the least number of parameters, least number of sensors, least value of sensor Silicon area, least value of total sensor power, and/or the like. The subset (i.e., DRR) may be used for finding the most informative potential locations of the sensor agent placements in the IC design, and thus the resulting sensor values may be used to gain maximum information on a specific die being tested. The

final sensor placements may be determined from this subset and implemented in tape out tests during the manufacturing ramp up to best classify the dies and detect manufacturing outliers. The output subset may be chosen to be significantly smaller than the complete set of inputs and estimated using a predefined set of sensors to reduce the computation cost needed during testing of physical dies.

[0098] In addition, unsupervised learning/clustering methods, such as Self-Organized Map (SOM), can be used directly with the sensors data as their input to classifies dies into families and profiles.

[0099] **High-coverage measurements (HCMs)**

[00100] A high-coverage measurement is a Post-Si die-level measurement that characterizes a certain die, for example, the total leakage current of a certain die measured during IDDQ testing, or a large-scale timing-margin measurement of the IC logic paths during functional testing using the circuit.

[00101] The HCM and sensor values may be analyzed to correlate between them directly. For example, a set of measured sensor values predicts (estimates) the HCM, such as without profiling the dies as described above using MC simulations. The predicted HCM may be estimated with a function, such as a function determined using Machine-Learning (ML) algorithms, modeling techniques, and/or the like.

[00102] **Estimator – parameter relationship functions and/or conversion rules (also Protean estimators)**

[00103] An estimator is a function and/or rule that converts between values (i.e., defines the relationships between the die operational values analytically, empirically, heuristically, etc.), such as using sensor values as input arguments to determine a profile (profile classifier), predicted HCM values (HCM conversion function), predict subset (DRR) values, predict manufacturing point, and/or the like. As used herein, the term manufacturing point means the set of parameters that determine the manufacturing of the IC design. Similar relationships may be found between HCM values and sensor values. The results of the die testing and Protean analysis may better determine the specific dies that may operationally meet or exceed the engineering specifications.

[00104] **Outlier (Manufacturing Anomaly)**

[00105] An outlier is a die whose measured HCM and/or like does not match the value range expected from the die's profile, such as expected from the distribution of

the values from measurements of a group of ICs of the same profile (i.e., mean plus or minus a multiple number of standard deviations).

[00106] Alternatively, an outlier may be a die whose measured HCM and/or like does not match a predicted HCM and/or like value that was calculated by the estimator function. These outliers represent dies manufactured with defects, manufacturing anomalies, and/or the like, that do not belong to the simulated profiles.

Description of Embodiments

[00107] Described herein are devices, systems, and methods, for die classification (profiling) and/or outlier detection and/or manufacturing point binning/estimation. These processes may benefit integrated circuit manufacturing (IC) and testing, such as to improve wafer testing, and thereby producing fewer defects in the end-user product due to IC failure (i.e., performance or operational outlier detection).

[00108] A hardware processor and/or like executes instructions to analyze an IC design and incorporates multiple sensor agents based on the IC design. The IC design with sensors may be simulated Pre-Si or measured Post-Si to determine the sensor output values for specific designs, fabrication processes, random defects, manufacturing point estimation and/or the like.

[00109] The distributions of the sensors values may be reflected in the high-coverage measurements values, such as providing a correlation between them. The distribution of the measured values may not match the estimated distribution value from the simulations and may change in time or between IC testing systems, or between IC operational systems and thus indicate a potential manufacturing/performance/environmental and/or the like type of long term value shift, differences between IC testing systems and/or sets of hardware and/or like.

[00110] The sensor agents may be iteratively repositioned within the IC design to increase the sensitivity to outliers and/or increase the numerical separation of sensor values between families of (i.e., performance and/or operationally) similar ICs and/or to increase the sensitivity of the sensor values to the manufacturing point. These numerical value distributions may be clustered to form combinations of different ranges of sensor values used to identify the classes/families. Rule-based and/or analytical functions may describe the relationship between the sensor values,

Manufacturing point (Process-Binnig), HCM values, and IC families, so given one of the data sets, the others may be determined, at least in part, such as by probabilities.

[00111] The sensor agents may be distinct circuits incorporated to the IC design that measure IC operational parameters of unites, sub-units, cells, sub-cells, devices, of the IC design, such as digital delay timing, rising edge delay, falling edge delay, device-leakage current, and/or the like.

[00112] Once the IC products with the incorporated sensor agents are manufactured, such as during tape-out cycles, preproduction, production, of the like, the sensor values are collected for each IC during wafer testing (i.e., to compute classes and/or outliers). ICs (i.e., dies) that are determined to have sensor and/or HCM values that are not within the constraints of the relationship rules/functions (i.e., estimators), may be discarded as defective, packaged for less critical applications (re-classified), separated into classes of products (such as meeting certain industry specifications), and/or the like. Dies incorporating manufacturing outliers/anomalies may be determined using multivariate analysis, outlier algorithms, and/or the like.

[00113] The data used for the relationship computations may be the results of at least two of the simulated IC design superset data, the device-process simulation data, the simulated sensor value data, the SVD results subset (DRR's, e.g., determined by the principal components, etc.), the SVD results with heuristic rules subset, the simulated HCM data, measured HCM data, the measured sensor values (i.e., during testing), operational data (i.e., defect analysis, on-specification determination, etc.), operational conditions i.e., voltage/temperature and/or the like. These relationships, and the techniques for their computation/adjustment, solve the problem in IC manufacturing of lowering defect count, increasing production yield, estimating manufacturing point, and/or the like. For example, the simulation data is used to classify the IC design-process combinations into profiles, such as predicted operational profiles based on simulated data. The profiles may be used to mark the ICs and detect outliers, thereby reducing defects and improving reliability.

[00114] Optionally, an improved yield is determined from the detection of systematic shifts in sensor values over time (i.e., manufacturing volume, etc.) For example, manufacturing equipment drift issues, correction of process point for shift detected downstream, and/or the like, may be detected by comparing the sensor values at wafer testing, package testing, circuit testing, device testing, end-of-life testing, and/or the like. For example, the shift data detected over time may be used to adjust

the manufacturing process parameters (i.e., process point) so that yield is matched toward sales demand of different profiles of the same IC.

[00115] Optionally, a hierarchal data structure is used for classification to produce hierarchal classes. For example, a hierarchy of profiles is determined during wafer testing, such as when some classes in a sub-hierarchy may inherent parameters, specification, performance metrics, physical metrics, operational metrics, and/or the like.

[00116] Optionally, the testing data is used to determine profiles. For example, relationships between tested sensor values may determine that the IC is defective and not all tests need to be performed, thereby saving testing costs. Optionally, testing data and simulation data are used to determine profiles. Optionally, operational defect data is used to determine relationships, such as data acquired from analysis of post-sale customer use, defect logging, defect analysis, and/or the like. Optionally, estimated manufacturing point may be used for a further tuning/adjusting of the manufacturing process for increasing yield, improving ICs performance and/or the like.

[00117] Reference is now made to FIGs. 1 and 2, which show (respectively) a schematic of a computerized system 100 and flowcharts 200 and 210 of methods (Pre-Si 200 and Post-Si 210, respectively) for integrated circuit profiling, manufacturing-point prediction, and outliers detection. System 100 comprises one or more hardware processors 101, a non-transitory computer-readable storage medium 102, a user interface 103, and a network interface 104. Storage medium 102 has encoded thereon program code, comprising processor instructions to execute on hardware processor(s) 101, thereby causing hardware processor(s) 101 to perform actions. As such, the program code is said to be configured to perform actions, though it is understood that the program code processor instructions are configured to perform the actions when executed on hardware processor(s) 101, and the actions are performed by hardware processor(s) 101. It may also be understood that the configuration of the program code is a specific arrangement of processor instructions that cause hardware processor(s) 101 to operate in a non-conventional manner, such as by execution of the unique program code.

[00118] The program code comprises a Sensor Selector 102A that is configured to receive 201 an IC design and a target process for manufacturing the ICs, and based on the IC design and target process, is configured to perform 202 simulations on the IC design to determine the distribution of operational values (IC Design Simulation

Values and Inter-Connect simulation values i.e., simulation superset), and also simulate the individual electronic component operational values over the manufacturing process space (Device-process Simulation Values – i.e., Catalog). For example, Sensor Selector 102A is configured to perform 202 Monte-Carlo (MC) simulations to simulate individual ICs characteristic, IC signature generation, produce resulting sensor values (i.e., agents value), and/or the like. Sensor Selector 102A is configured to compute 203 a covariance matrix of the data for use in the factorization 205.

[00119] Sensor Selector 102A is configured to compute 204 sensitivity/weight vectors and is configured to factorize 205 (i.e., perform SVD on) the simulated values (IC design and device-process) the simulations to produce singular-value decompositions (SVDs), and a resulting subset of potential sensor locations. The SVD factorization results allow enhancing the sensitivity of the signatures to the individual IC's characteristics and design signatures and may be used to iteratively select the sensors and further increase the sensitivity of the signatures. Sensor location and type selection 206 within the IC design may be done based on SVD subset, such as the top-k principal components (i.e., top k components that explain 95% of the variance), etc.

[00120] The program code comprises a Profiler/Estimator 102B that receives 208 separation ratios and the signature SVDs, selects 206 sensor locations from the SVD subset based on the separation ratios to produce relationships between the IC classes, the HCM parameters and the sensor values. The program code is also configured to compute the Estimators block (FIG. 2). This block produce estimators, such as relationship rules, functions, and/or the like, that are used to compute the SVD-subset values by the sensors readout during the post/Si stage. The program code is configured to compute 207 relationships between measured (i.e., from testing) and simulated (i.e., pre-Si) parameters (i.e., estimators/rules/ profilers/classifiers etc.) that receive an individual IC's SVD-subsets and determine the class (i.e., category/family/profile) of performance for that IC based on the signatures and classifiers. Profiler/Estimator 102B may also be configured to receive 209 operational statistics, such as defect statistics, defect engineering analyses, and/or the like, and these used to align the simulated and measured classes with the performance of the IC product in the field. As discussed below, the Pre-Si stage may be optional in embodiments, although features of this stage may be implemented with reference to a Post-Si stage.

[00121] In the Post-Si stage, ICs 130 with incorporated sensors (as at 131, 132, 133, and/or the like) are manufactured 211 (i.e., post-Si flowchart 210). A Die Classifier/Profiler Manufacturing-point predictor and Anomaly Detector and Systematic shift detector 102C (i.e., part of the program code) is configured to test 212 each die (i.e., IC) of a wafer (or receive the tests results for each IC from a tester 140 through network interface 104 and a network 120). Die Classifier/Profiler Manufacturing-point predictor and Anomaly Detector and Systematic shift detector 102C is configured to use the relationships with the data received from the IC test to determine 213 IC profiles (from the simulations and classification), manufacturing outliers (i.e., anomalies) and manufacturing point. For example, Die Classifier/Profiler Manufacturing-point predictor and Anomaly Detector and Systematic shift detector 102C is configured classify 213 each IC according to the tested sensor values, determine that an IC is a manufacturing outlier, and/or the like. One approach for classifying dies may use the steps 203 – 207 from the Pre-Si flowchart 200, but with reference to Post-Si data (as will be discussed below). In embodiments, die Classifier/Profiler Manufacturing-point predictor and Anomaly Detector and Systematic shift detector 102C receives the high coverage measures and the Pre-Si estimators to detect 213 when the IC may be an outlier of the classification scheme. Outliers may be discarded 214, and the classification may be used to mark 215 the IC classes on the IC (such as track the IC class according to the location on the wafer), IC packaging (such as a different grade of IC according to the class, and/or the like. The Systematic shift may marked 216 on ICs, used for planning new ICs, improving yield to ICs, used for recalibrating manufacturing parameters, and/or the like. The estimated manufactured point may be used for tuning/adjusting of the dies manufacturing process for increasing yield, improving IC's performance, and/or the like.

[00122] The use of IC profiling and IC signatures may allow increasing the quantity and quality of parameters used for the multivariate analysis in determining IC classes and outliers. Since classes (i.e., family's) are not environment dependent (i.e., invariant across voltage and temperature), dies from the same classification should behave the same way at different die environments like SORT, Final-test, and system. When the behavior of a certain die is different between environments it may indicates a problem in the environment. Reference is now made to FIG. 10A and FIG. 10B, which demonstrate a detection of a systematic shift within and between environments. FIG. 10A demonstrates a detection of a pre-profiling systematic shift, i.e., a detection

of a parameter shifts at the wafer-SORT testing conditions. FIG. 10B demonstrates a detection of a post-profiling systematic shift i.e., change in the environmental conditions that split a family into two groups before and after the change in conditions. As the sensors are placed within an IC design for lowering DPPM, the sensor values later used during the IC testing, device testing, failure analysis, and/or the like may better differentiate between categories/families/profiles of ICs and thus allow classification based on performance, outlier detection during testing, process binning, manufacturing point estimation, and/or the like.

[00123] Following are the details of the sensors and how the sensors are incorporated in the IC design for IC profiling, outlier detection and manufacturing point estimating.

[00124] Post-Si IC profiling may be considered the classification of individual ICs to one of multiple Si characteristic range i.e., process parameter range mapped into device electrical parameters range. The profiling may be performed by collecting from an IC a number of sensor values converted to SVD-signatures and comparing the SVD-signatures to the range of SVD-signatures assigned to a specific profile, such as by a classification method. Alternatively, the profiling may be performed directly by comparing the sensors values to ranges assigned to specific profiles, without classification based on Pre-Si simulations.

[00125] The SVD-signatures are generated Pre-Si based on device characteristics and unique Design-related signatures that are based on individual cells within the IC and the connectivity between cells within the IC. A set of device parameters characteristics is defined as the device parameters CATALOG. The Design-related signature generation may be an automatic process that may be simulated with electronic design analysis (EDA) and dynamic-timing analysis simulation tools, MC tools and circuit simulation tools.

[00126] Design related signatures may be clustered to reflect significant performance differences of a given IC design manufactured by a specific fab, etc. The clustering, classification, selection of sensors, selection of sensor locations, and/or the like, may be based on empirical or a-priori knowledge of the process (i.e., fab) and circuit design expected behavior. For example, design related signatures include values that estimate (for a variety of voltages and temperatures):

- Leakage VSS,
- Leakage VDD,

- Total leakage
- Average delay fall,
- Average delay rise,
- Total cells delay
- Total Inter-Connect delay (RC-delay)
- Fmax
- Timing margin
- SRAM minimal voltage per SRAM type
- Chip VDD-min per all SRAM types & Register-Files and State-Elements types
- and/or the like.

[00127] Reference is now made to FIG. 3A and FIG. 3B, which show circuits for IC unit timing margin detection. These circuits are an enhancement of the circuits described in US provisional application no. 62/586,423, filed December 5, 2017, and titled "INTEGRATED CIRCUIT FAILURE PREDICTION DEVICE", incorporated herein by reference in its entirety.

[00128] Following are examples of Pre-Si signature generation algorithm, and sensor value computation/derivations. As used herein, the terms sensor value, sensor agent, sets of sensor values, signatures, and/or the like are used interchangeably to mean the sets of sensor values (i.e., data) from an IC used for the techniques disclosed herein.

[00129] A generic Pre-Si design related signature generation process may be defined as follows:

Step1: Define a represented vector of measurements M

Step2: Run MC-simulation to extract the measurement M joint-statistics behavior

[00130] A generic Pre-Si Device-related parameter signature generation process may be defined as follows:

Step1: Define a vector of process parameters P

Step2: Run MC-simulation to extract the parameters P joint-statistics behavior, joint-statistic with the measurements M behavior, and\or the like.

[00131] For example, to use an Fmax signature of a specific IC design, the process may be:

Step1: Define Fmax measurement as the maximum operation frequency of the IC design. Fmax may be determined by Critical-Paths (CPs) of the IC, i.e., paths that comprise a limiting delay thus limiting the maximum frequency

Step2: Find the CP in the specific IC design for each of multiple manufacturing process values (i.e., fab parameter ranges). For example, determine a set of CPs that limit the frequency throughout the entire manufacturing ranges.

[00132] The Fmax signature manifests itself as the Minimal Margin per Unit (MMU) signature. The MMU signature measures the minimal margin per unit of the IC per MC point. Namely, the MMU apply the Fmax signature per unit. At post-Si the MMU signature may be measured by the circuits shown in FIG. 3A & FIG. 3B, given a certain configuration of the IC inputs.

[00133] For example, the total leakage signature of a specific IC design may be generated as follows:

Step1: Define total leakage measurement as the sum of all cell's leakage:

$$Total\ leakage \mid PVT = \sum_{all\ cells} I_{off}(i) \mid PVT$$

Step2: Extract each cell's leakage current at each process point in the manufacturing range using Monte-Carlo (MC) simulations.

[00134] For example, the total cells delay signature of a specific IC design may be generated as follows:

Step1: Define Total cell-delay measurement as the sum of all cells delay:

$$Total\ cells\ delay \mid PVT = \sum_{all\ cells} D(i) \mid PVT$$

Step2: The cell delay at each process point is computed using Monte-Carlo (MC) simulations

For example, the total inter-connect (RC) delay signature of a specific IC design may be generated as follows:

Step1: Define total RC-delay measurement as the sum of all RC delays:

$$Total\ RC\ delay \mid PVT = \sum_{all\ RCs} RC(i) \mid PVT$$

Step2: Extract an RC delay at each process point using Monte-Carlo (MC) simulations and different RC models.

[00135] The delay signature may be generated to represent individual rise and fall transitions with all VT's, per VT type, and/or the like. For example, delay signatures may be computed using the following equations.

$$DS_{unit} = \sum_i arc(i) \times Df(i) \times \frac{\#\ of\ arc(i)}{\#\ total\ arcs(all\ VT's\ /\ per\ VT)}$$

$$DS_{rise} = \sum_i arc_{rise}(i) \times Df(i) \times \frac{\#\ of\ arc_{rise}(i)}{\#\ total\ arcs_{rise}(all\ VT's\ /\ per\ VT)}$$

$$DS_{fall} = \sum_i arc_{fall}(i) \times Df(i) \times \frac{\#\ of\ arc_{fall}(i)}{\#\ total\ arcs_{fall}(all\ VT's\ /\ per\ VT)}$$

[00136] For example, the minimal voltage is based on the SRAM operation of a specific IC design to be generated as follows:

Step1: Define the minimal required voltage as the minimal voltage required by all SRAM cells:

$$minimal\ required\ voltage\ |\ PVT = \min_{all\ SRAM\ cells}(V(i)|\ PVT)$$

Step2: The minimal voltage required at each process point is computed using Monte-Carlo (MC) simulations.

[00137] Following are examples of sensor circuits.

1. A Delay sensor may sense the delay of a certain logic cell. It may be implemented by a Ring-oscillator circuit that its frequency reflects the average delay of the logic cells.
2. Another delay-sensor may sense the delay of the rising-edge of a certain logic cell and the falling-edge of a logic cell in a separate way.
3. Another delay sensor may sense the RC-delay per-metal or per a subset of metals and or like.

4. A leakage-sensor may be used to sense the leakage of a certain P-device and a certain N-device in separate ways, as described in US provisional application no. 62/614,706 Entitled "INTEGRATED CIRCUIT SUB-THRESHOLD LEAKAGE SENSOR", incorporated herein by reference in its entirety.

[00138] The contribution factor of each Vth-type may be computed for each signature. The contribution factor reflects the contribution of each Vth-type to the leakage or to the average delay signatures and or/like. The contribution factors may be generated as part of the signature generation process or computed by linear regression. The vector of contributing factors for each process parameter may be considered, where the maximum over the data may be referred as the sensitivity vector and denoted by $\overline{w}$.

[00139] Let $P^{complete}$ denote the set of process parameters obtained from the device parameter catalog. Let P denote a subset of $P^{complete}$ which is obtained after selecting parameters from $P^{complete}$ for which the values in the sensitivity vector are above a given threshold. Let S denote the set of signatures at each of the operation points (M signature-operation point samples). Namely, s_1 is the MC samples of a given signature at a given operation point (V,T).

[00140] For each $s_j \in S$ let $\hat{s}_j = s_j - s_j|\{P \cup \{\hat{s}_i\}_{i<j}\}$, namely,

- $\hat{s}_1$ denotes the part missing in the catalog for a fully estimation of the first signature at the first operation point - $s_1|P$ is the estimator of s_1 given P, and
- $\hat{s}_j$ denotes the part missing in the catalog and all the $\hat{s}$'s added to it, for a fully estimation of the j-th signature-operation point - $s_j|P \cup \{\hat{s}_i\}_{i<j}$ is the estimator of s_j given $P \cup \{\hat{s}_i\}_{i<j}$.

Then, the returned set of vectors is $P \cup \{\hat{s}_j\}_{1\leq j\leq M}$.

[00141] The SVD of a matrix σ is a set of three matrixes U, D and V such that $\Sigma = UDV^T$ where U and V denote orthogonal matrix of the left and right *principal vectors* of Σ, and D denotes a diagonal matrix with diagonal elements known as the *singular values* of Σ. For the profiling implementation, Σ denotes a covariance matrix and therefor $U = V$. The singular value corresponds to a principal vector may be the variance at the vector direction.

Implementing SVD for profiling in steps:

- Normalize any column that is not normal distributed, for example, apply log() on values obtained from log-normal distribution
- Scale the columns of table 1: $\mu = 0, \sigma = 1$
- In case that a subset P has not been taken from $P^{complete}$ with respect to the sensitivity vector. Rescale the columns with the weights vector $\overline{w}$
- Produce the covariance matrix Σ from Table 1
- Produce the SVD signatures by performing SVD operation on Σ , note that the set $\{\hat{s}_j\}_{1\leq j\leq M}$ can be used instead or in additional to $\{s_j\}_{1\leq j\leq M}$

p_1^n : value of parameter n, at MC run 1

s_1^m : value of signature at operation point m, at MC run 1

TABLE 1:

MC run	**Process parameters**		**Signatures (at operation point)**	
1	p_1^1	p_1^n	s_1^1	s_1^m
	..	..	..	..
	..	..	..	..
500	p_{500}^1	p_{500}^n	s_{500}^1	s_{500}^m

[00142] To have a robust classification with defined error an appropriate number of families may be essential. To reduce the number of families that may form, a reduced dimensional data domain should be considered, for example, an IC design that may be sensitive to 2 Vth-types may be spread by 8 process parameters (dimensions) before reduction ->(applying SVD); {VT,IDS}x{p,n}x{SVT,LVT}. To find the reduced dimensional data domains, the orthogonal basis of the matrix Σ may be extracted. Each direction of the orthogonal basis may be a linear combination of the process parameters. The SVD also provides metrics of each of the principal directions.

[00143] For example, the following steps may determine the profiling of an IC design and a process using the sensor agents:

[00144] Profiling step (1):

[00145] Define the distance between 2 samples (i,j) as the weighted q-norm distance $\Delta(i,j)$ computed with the given # of SVD signature (input)

$$\Delta(i,j) = \left(\sum_k w_k \left|SVD_i^k - SVD_j^k\right|^q\right)^{1/q}$$

where SVD_i^k denotes the value of the k-th SVD signature of the sample i. For q=2 and 1's as weights the above is the Euclidean norm.

[00146] Note that the weighted q-norm can be generalized by considering multiple sets of weights (for example, the values of the principal vector) and a procedure for choosing which member of the set should be chosen (for example, the one for which the distance is maximal) - $\Delta_U(i,j) = \max\left(abs\left(\left(\overline{SVD_i} - \overline{SVD_j}\right)U^{-1}\right)\right)$

[00147] Note that Mahalanobis distance $\Delta(i,j) = \sqrt{\left(\overline{SVD_i} - \overline{SVD_j}\right)\Sigma\left(\overline{SVD_i} - \overline{SVD_j}\right)^T}$ may be used instead or in additional of performing the SVD procedure, where $\overline{SVD_i}$ is a vector consisting of the SVD signatures of sample i and U is the principal vectors matrix.

[00148] Profiling step (2):

- Define the families: the distance between a sample to a certain family is the distance to the sample that defines the family
    1. Define the first sample as a family
    2. Go over all the samples and when the distance Δ of the current sample to all the defined families is larger than the given radius then defines a new family
- Associate samples to the closest family (correction process)
    1. Go over all the samples and associate the sample to the family to which the distance is minimal

[00149] The above procedure may be performed on a batch of samples, for example on a set of MC samples or a group of dies with known test results (for example, in case that the tester is offline), or performed online, for example when the tester is online.

[00150] FIG. 4 show the profiling results, families are defined by the median of device parameters per device types {VT,IDS}x{p,n}x{SVT,LVT}. Each vertex of the polygon represents a normalized device parameter value (in sigma terms) with respect to its typical/center value.

[00151] FIG. 5 show the spread of the Pre-Si average leakage-current signature over the profiling process resulted families. FIG. 6 is a zoom version of FIG. 5 showing 2 families at a bounded sigma range, Family A range: -1.37 to 0.23 sigma's, Family B range: -0.03 to 1.63 sigma's. FIGs. 7A,7B,7C and 7D show the stability/invariance of the profiling process & resulted families per voltage and temperature.

[00152] When the number of the SVD signatures is smaller than the number of the principal components, then the distance computed by the chosen SVD signatures may be smaller than the real distance. For the case of q-norm with 1's as weights and q=2, the real distance between samples i and j defined by $\Delta^F(i,j)$:

$$\Delta^F(i,j) = \sqrt{\sum_n \left(SVD_i^n - SVD_j^n\right)^2} = \sqrt{\sum_n \overline{w}_n \left(p_i^n - p_j^n\right)^2}$$

where the left term is a sum over all of the SVD principal vectors and the right term is a sum over all the parameters for which $\overline{w}$ has 1's, namely, those processes parameters were included in the set P. The error definition is as follows:

Let i and j stand for two samples, then the distribution of the error $\left(\left(\Delta^F(i,j)\right)^2 - \left(\Delta(i,j)\right)^2\right)$ is generalized chi-square in which the variances are the singular values not included in $\Delta(i,j)$.

For other norms the above computations would be with respect to the chosen norm.

[00153] When the number of the SVD signatures is smaller than the number of the principal components, then for a given process parameter, 2 samples i and j for which $\Delta(i,j) = 0$ may have different process value. Denote the distance between the values of a given process parameter of samples i and j by $\Delta^P(i,j)$. Then, $\Delta^P(i,j)$ is normal distributed with zero mean and variance bounded by $2d$, where d is the maximal singular value which is not included in $\Delta(i,j)$.

[00154] Estimators (such as profilers, classifiers, and/or the like) are functions that generate an output value based on the sensor values. Generating estimators for the

SVD signatures based on the sensor's values may be done using a Gaussian estimator, a Lasso estimator, a Ridge regression estimator, Generalized adaptive model estimators, splines, Neural network, and/or the like. The estimation error may be empirically computed by validation data. Based on the error, the distance between each sample to it the associated family is smaller than $r + \epsilon$ with a probability smaller than $1 - \delta$.

[00155] The Protean classifier block classifies dies into families at the Post-Si stage. The input for the block is pre-Si data composed of SVD-signatures estimators and the separation radios, and post-Si sensor values from the testing equipment. Based on the pre-Si estimators, SVD signatures values are computed for each sample. The estimators may be tuned, adjusted, improved and/or the like based on data collected at Post-Si stage. Families are generated as follows:

- Define the first sample as a family
- Given a new sample
    - When the distance Δ of the new sample to all of the defined families is larger than the given radius (input) – Define a new family
    - When not, associate it to the closest family
- When a new family has been defined, go over all the samples and associate them to the closest family.

Optionally, families of ICs may be classified Post-Si by the median of device parameters per device types {VT,IDS}x{p,n}x{SVT,LVT}. Each vertex of the polygon represents a normalized device parameter value (in sigma terms) with respect to its typical/center value.

[00156] Optionally, histograms may be built per profile and per sensor measurements and or high coverage measurements. For example, post-SI sensor values are collected per family for high coverage measurement and for sensors values. The data may be normalized when it is not normal distributed. A mean and variance may be computed for each data set and based on a desired false-positive rate the bounds on the high coverage measurements may be computed per family. The signatures are re-

used for separating to different classes/families. Therefore, they can't be out of a given limit.

[00157] Optionally, anomaly testing is done after profiling. For example, testing may measure the bounds of high coverage measurement per family. For example, the family classification of the current die may be used as input for testing. When one of the high coverage measurements of the given die is outside the bounds correspond to the die's family/profile, then the die is classified as outlier`. The high coverage measurements bounds may be computed by considering the joint-distribution of the high coverage measurements for each of the families.

[00158] Optionally, classification and/or estimators are used for package testing. For example, anomaly testing is done after and/or during High-Temperature-Operating-Life test (HTOL) or Burn-In test (BI). Dies that were classified to the same family by the profiling process belongs to the same Si-profile and are expected to have a close behavior over the same stress conditions. Means that the performance degradation of dies from the same family is expected to be bounded during and after the tests. Dies that show performance degradation outside the family-bounds are identified as outliers and may be rejected.

[00159] A high coverage measurement may be an IC-level measurement that reflects the total die behavior, for example, total die leakage at a certain temperature. Another example is the timing-margin of a large-scale paths. The histogram is build according the following steps:

1. post-SI data is collected per family per high coverage measurement
2. Normalize any data that is not normal distributed
3. Compute mean and the variance for each data set
4. Based on a given false-positive rate, bounds on the high coverage measurements are computed per family
5. Alternatively, the bounds on high coverage measurements can be taken as the empirical lower and upper alpha-quantile values, where alpha is determined by the false positive rate. This approach may be applied when a specific high coverage measurement for a given family cannot be normalized and/or the like.
6. Optionally, an estimator may be built for each high coverage measurements based on the the Post-Si data. Then, an histogram on the estimator error,

namely, the difference between the estimated value and the real high coverage measurement may be built. Then the above procedure (1-5) may be applied on this histogram.

[00160] FIG. 8 and FIG. 9 show a demonstration by experiment of the Outlier detection process.

- Experiment target:
    - Plant an outlier in the Average-Ioff signature
    - Detect the outlier using the Outlier-detection algorithm
- Outlier description:
    - Change MC point 428 by 1s
        - Equivalent to +35% increase in Ioff

[00161] FIG. 9 show the experiment results, the outlier that was shift by 1-sigma is emphasized by the Outlier-detection process as 7-sigma WRT estimator average.

[00162] The figures mentioned above (FIGs. 8 and 9) demonstrate outlier's detection based on building histogram (FIG. 8) and estimators (FIG. 9). Namely, an estimator for the high coverage measurement is computed. Then, the measured high coverage value is compared to the estimated one and the die is detected as outlier based on a given false positive rate.

[00163] For example, different sensors may yield different cluster separations, and thus have different sensitivities to the sensor selection and locations within the IC design. For example, good separation between the clusters based on Vt NLVT on and Vt PLVT on, but an overlap may exist between the two clusters.

[00164] For example, the separation of the average-leakage signature and total leakage signature may determine profiles.

[00165] For example, different high coverage parameters may yield different cluster separations, and thus have different sensitivities to detecting an IC's profile classification.

[00166] Reference is now made to FIG. 4, which shows a radar (spider) plot of IC profiles. The graph shows the profile, i.e., process origin of profiles 1, 8, and 13. The radar (spider) plots are another way to visualize the process profiles.

[00167] Reference is now made to FIG. 5, which shows a graph of distributions of values for different IC profiles.

[00168] Reference is now made to FIG. 6, which shows a graph of distribution separation between two different IC profiles.

[00169] Reference is now made to FIG. 7A thru 7D, which show a graph of distributions of values for two IC profiles under varying voltage and temperature.

[00170] Optionally the profiling process can be performed using only Post-Si data. In such a case, the inputs to the profiling algorithm are: a) radius R; b) a file of ICs agents' readouts; c) a smooth parameter λ; and d) a constant k.

[00171] The profiling algorithm is performed by the following steps: 1) For each IC, create a representative vector (an example of the representative vector for a given IC is $v_{ic1} = (Ag_1, Ag_2, \ldots Ag_n)$, in which Ag_n stands for the readout of agent n of the given IC; 2) create a matrix such that each row is the representative vector of one of the dies (namely, the number of rows is the number of ICs, and the number of columns is the length of the vectors representing the IC); 3) scale the matrix such that the average of each column is 0 and the sigma is 1 (as a product of this, each agent has its own normalization coefficients, the normalized representative vector of IC1 is denoted by $\bar{v}_{ic1}$, namely, the vector's values are the normalized agents' readouts); 4) compute the covariance matrix of the scaled matrix (as computed at 3); 5) perform SVD process on the covariance matrix and denote the results by UDV; 6) compute the distance matrix as follows: dist_mat=U*D', where D' is the diagonal matrix D in which the first k values (d_k) are replaced with $\sqrt{\frac{d_k}{d_k+\lambda}}$, the rest of the values are replaced with zeroes (namely, given D: $\begin{pmatrix} d_1 & 0 & 0 \\ 0 & d_2 & 0 \\ 0 & 0 & d_3 \end{pmatrix}$, for k=1 and λ, D' is: $\begin{pmatrix} \sqrt{\frac{d_1}{d_1+\lambda}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}$); 7) create the families based on the procedure described in "Profiling step (2)" above with the following distance computation, in which the distance between ic1 and ic2 is: $\Delta = \sqrt{(\bar{v}_{ic1} - \bar{v}_{ic2}) * UD' * (UD')^T * (\bar{v}_{ic1} - \bar{v}_{ic2})^T}$, $\bar{v}_{ic1}$ and $\bar{v}_{ic2}$ are the normalized vectors representing ic1 and ic2 respectively and D' is the matrix computed in step 6.

[00172] Optionally, the distance between ic1 and ic2 can be calculated as follows: $\Delta = \max |(\bar{v}_{ic1} - \bar{v}_{ic2}) * UD'|$ (using the same notation as above).

[00173] Optionally the profiling process described in the immediately preceding paragraphs can be performed in an incremental mode. In other words, the Post-Si data may arrive in batches or by using Pre-Si & and Post-Si data, in which the Pre-Si data is considered the first batch.

[00174] In such a case, the profiling algorithm is described as follows (with an example of using Pre-Si as first batch and then Post-Si data as a second batch): 1) run the post-Si data algorithm with the pre-Si data instead of the post-Si data (the normalization coefficients of each agent and the distance matrix should be stored and at this stage, the Families are generated based on the Pre-Si data); 2) when the post-Si data has arrived, normalize it with the normalization coefficients computed based on the pre-Si data, with the distances being computed using the distance matrix computed based on the pre-Si data; and 3) the algorithm uses the new data to generate new families: if possible, it will add the new data to the pre-defined families and if not, it will create new families, making sure that each of the new data is associated to the closest family (new/pre-defined).

[00175] The algorithm will check if additional agents are needed to improve its performance. It will be done by performing the following steps using the Pre-Si data: 1) compute the distance between all the MC points; and 2) for each signature and/or process parameter, compute the distance (in sigmas) between all the MC points.

[00176] Then, for each of the signature and/or process parameter, check if there exists a constant ($const$), such that: $dist_{sig/proc}(MC_i \leftrightarrow MC_j) \leq const \times dist_{profiling}(MC_i \leftrightarrow MC_j)$. The $const$ value should not be large such that the equations always holds, namely, $const$ value should be such that $const \times dist_{profiling}(MC_i \leftrightarrow MC_j) \leq r$ for some fraction of the number of MC points which is stable when we enlarge the number of MC.

[00177] In a generalized sense, there may be considered a (computerized) method for IC classification and/or outlier detection. The method uses a wafer comprising a plurality of ICs in accordance with an IC design. The IC design comprises a plurality of sensors (which may provide diagnostic and/or performance information regarding the functionality of the IC). The method comprises using at least one hardware processor for testing each of the plurality of ICs. This is advantageously

effected by: collecting a plurality of sensor values, the plurality of sensor values including sensor values from each of the plurality of sensors (preferably at least one sensor value from each of the sensors); comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC. Beneficially, the classification of each tested IC is then recorded. In embodiments, the method may include manufacturing the wafer based on the IC design using a fabrication process.

[00178] The step of comparing the plurality of collected sensor values to a classification scheme may include determining or identifying the classification scheme in embodiments. The classification scheme is optionally based on one or more sets of data. For example, the one or more sets of data may include: simulations of a plurality of IC operations of the IC design and the fabrication process (in which case, the simulations may be at least one of at least one complete IC design simulation, at least one partial IC design simulation, and at least one device simulation for the fabrication process); a plurality of training sensor values collected during a pre-production tape-out test; and the collected plurality of sensor values. In other words, the sets of data may include pre-Si and/or post-Si data. In embodiments, the classification scheme may comprise an outlier class. The classification may comprise a hierarchical data structure for determining the classification of each die.

[00179] The step of comparing preferably comprises estimating high coverage measurements from the plurality of sensor values using at least one of a function and a rule. The function and/or rule may be determined from a training set of sensor values and training high coverage measurements, for example.

[00180] Various uses of the classifications of the tested ICs may be made. For example, the at least one hardware processor may be used for: marking an IC package of the tested IC with unique identifications based on the classification; and/or discarding a defective IC. In an approach, from each tested IC, a set of parameters of the fabrication process may be determined based on the classification and the plurality of sensor values. Then, a second set of parameters of the fabrication process may be selected based on the IC design and the sets of parameters of the fabrication process for each IC. A second manufacturing of a second wafer may then be performed using the second set of parameters. The selecting is advantageously performed by at least one of a manual process and an automatic computation. In that way, a wafer

comprising a plurality of ICs is provided in accordance with an IC design, in particular with the IC design comprising a plurality of sensors.

[00181] In some embodiments, the classification scheme may be identified based on a plurality of classification values. The classification values may be based on one or more of: Pre-Si or simulated sensor values; Pre-Si design signatures; operational parameters determined from a simulation of the IC design (Pre-Si Catalog simulated values) and Post-Si measured sensor values. The classification values are preferably normalized. The classification scheme may be implemented by the following process. Initially, a matrix representation is established from the plurality of classification values, each row of the matrix representation comprising classification values in respect of one of the plurality of ICs (in other words, a matrix in which each column relates to a specific, different parameter, such as a sensor value or other data and each row relates to a certain IC, although the transverse of such a matrix could be used in other implementations). The process may continue as follows: computing a covariance matrix from the matrix representation and a singular value decomposition (SVD) for the covariance matrix; determining, using the SVD (in a variety of ways, as will be discussed below), a plurality of distance values. Each distance value represents a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs (for instance, based on known mathematical techniques for determining such distance values); and identifying, from the plurality of distance values, at least one family, thereby defining the classification scheme (in particular, comparing the distance values against a threshold, specified as a radius).

[00182] Two particular classification approaches are considered: direct and indirect. In a direct method, each of the ICs is represented by a vector based on sensor values (these may be the collected sensor values for Post-Si data and/or the simulated sensor values for Pre-Si data). A matrix is defined based on the sensor values (each row of the matrix being a vector for a single IC), which are advantageously normalized. The covariance matrix of this matrix is calculated. A SVD is performed on the covariance matrix and the SVD (specifically, the principal values from the SVD) is used to create a distance matrix. Beneficially, the distance matrix is also determined using a smoothing parameter λ and a constant (integer) k (such that only the first k principal values from the SVD are used). The distances between ICs are calculated from the distance matrix and the (normalized) vectors for the ICs. The ICs are grouped based on their distances from one another (within a "radius") to define the Families.

Each Family may be identified by a representative vector. When both Pre-Si and Post-Si data are used, the distance between the measured IC using the Post-Si data and a representative vector for each Family defined using Pre-Si data is also calculated.

[00183] In the indirect classification method, a matrix is defined based on Pre-Si data, such as one or more of: (normalized) simulated sensor values; operational parameters determined from a simulation of the IC design (Catalog values); and (normalized) design Signature values (each row of the matrix being a vector for a single IC). The covariance matrix of the matrix is calculated. An SVD is performed on the covariance matrix. A set of Pre-Si SVD signatures are defined/denoted by identifying vectors of the SVD for which the corresponding principal values of the SVD are greater than a pre-defined value (d) and/or identifying vectors of the SVD for which the corresponding principal values of the SVD are the greatest (maximal). The plurality of distance values may be determined using the set of Pre-Si SVD signatures (specifically, if only Pre-Si data is used). For example, at least some of the plurality of distance values may be calculated, each of the at least some of the plurality of distance values being based on a distance between one of the Pre-Si SVD signatures and another of the Pre-Si SVD signatures. If Post-Si data is used, a plurality of estimators are configured (built) from the simulated sensor values and the set of Pre-Si SVD signatures. Each estimator is configured to generate an estimated SVD signature from input sensor values. Each of the ICs (At Post-Si) and MCs (At Pre-Si) represented by its own SVD signatures values. Then the plurality of estimators are used to estimate, for each of the plurality of ICs, a respective Post-Si SVD signature from the plurality of collected sensor values. At least some of the plurality of distance values are calculated, wherein each of the at least some of the plurality of distance values is based on a distance between one of the Post-Si SVD signatures and another of the Post-Si SVD signatures. The ICs are grouped based on their distances from one another (within the “radius”) to define the Families. Each Family may be identified by a representative vector (from the signatures). When both Pre-Si and Post-Si data are used, the distance between the measured IC using the Post-Si data and a representative vector for each Family defined using Pre-Si data is also calculated. In other words, further distance values of the plurality of distance values are calculated, each of the further distance values being based on a distance between one of the Pre-Si SVD signatures and one of the Post-Si SVD signatures.

[00184] The identification of one or more families, from the plurality of distance values, may typically comprise: classifying a first IC of the plurality of ICs in a first family, such that the first family is defined by the first IC (in other words, the first IC analyzed may always define a new family, since no families have previously been defined and thus, the first IC represents the first family); comparing a distance value, from the plurality of distance values, representing a distance between the first IC and a second IC of the plurality of ICs with a predetermined threshold (for example, such that the distance value between the two ICs is either greater than or less than the threshold); if the distance value is less than the predetermined threshold, classify the second IC in the first family (because the distance between the two ICs is small, so that they are considered to be in the same family); and if the distance value is greater than the predetermined threshold, classify the second IC in a second family, such that the second family is defined by the second IC (in other words, such that a new family is defined and this family is represented by the second IC). The case where the distance value is same as the predetermined threshold is left to implementation as such cases would be extremely rare and therefore the classification for the second IC could be defined as the first family (with the first IC) or a new, second family without causing difficulties.

[00185] This approach may be repeated for each of the ICs in the plurality of ICs. For instance, the identifying of the plurality of families, from the plurality of distance values, may further comprise a procedure for each other IC of the plurality of ICs. This procedure may proceed in the following way. Initially, a group of distance values, from the plurality of distance values, are identified. Each distance value in the group of distance values represents a distance between the other IC and a respective IC of the plurality of ICs that defines a respective family (in other words, the group of distance values may only be concerned with distance values between the other IC, which is the IC being classified, and each of the ICs that represents a family). Each distance value from the group of distance values is then compared with the predetermined threshold (this is advantageously the same predetermined threshold as used for the first and second ICs and is beneficially the same for all ICs on the same wafer). A number of results are possible from this comparison. If a distance value from the group of distance values, which represents a distance between the other IC (that is the IC currently being classified) and a specific IC of the plurality of ICs that defines a specific family (that is, an IC that represents a family), is less than the predetermined

threshold, the other IC is classified in the specific family (such that the two ICs are considered in the same family). This condition, if it is met at all, should only be met for one family. If all the distance values from the group of distance values are greater than (or, depending on the implementation, greater than or equal to) the predetermined threshold, the other IC is classified in a new family, such that the new family is defined by the other IC. This procedure is advantageously repeated for each unclassified IC (other IC) until all of the plurality of ICs have been classified.

[00186] As previously indicated, the plurality of classification values may be based on one or more of: simulated sensor values determined from a simulation of the IC design (Pre-Si data); one or more design signatures; a plurality of training sensor values collected during a pre-production tape-out test; and measured sensor values for a batch of devices, which may include any number of ICs, a lot, many lots and/or the wafer (Post-Si data). When only Post-Si data is used, for instance, the plurality of classification values may be based on the collected sensor values for the wafer. Then, the identification of the classification scheme based on the plurality of classification values may be at least part of the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC. Alternatively, the identification procedure may be followed first for the Pre-Si data (for instance, such that the plurality of classification values are based on simulated sensor values determined from a simulation of the IC design), resulting in Families being identified. Then, the step of identifying the classification scheme based on a plurality of classification values may take place before the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC (in particular using Post-Si data, especially based on a distance matrix and/or distance function, as described herein). The comparing of the plurality of collected sensor values to a classification scheme may be implemented by following a further procedure (in the direct approach discussed above), as follows. A collected data matrix representation may be established from the plurality of collected sensor values. Each row of the matrix representation comprises collected sensor values in respect of one of the plurality of ICs (such that the collected data matrix representation has the same format as the matrix representation discussed above). From the collected data matrix representation, a plurality of collected data distance values may be determined. Each distance value represents a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs, with the

plurality of ICs preferably including both simulated ICs (from the step of identifying) and actual ICs (from the collected data), considered as separate ICs (although the simulated ICs will normally be simulations of the actual ICs). The distances between the plurality of the Post-Si ICs and/or the plurality of the Pre-Si ICs are thereby computed by the distances functions/matrix computed based on the Pre-Si data. From the plurality of distance values, each of the ICs may then be classified according to the classification scheme. This classifying advantageously follows the procedure discussed above (in the preceding two paragraphs).

[00187] In any of these approaches, the matrix representation may be normalized, for example prior to computing the covariance matrix from the matrix representation (in other words, the covariance matrix is computed from the normalized matrix representation). Normalization coefficients may be defined thereby. Where Pre-Si and Post-Si data are both used, collected data matrix representation may be normalized using the defined normalization coefficients (that is, from the Pre-Si data).

[00188] Experimental data is now provided to show that the classification of Families, as disclosed herein, is invariant to other physical Si parameters and temperature. Referring now to FIG. 11, there are shown example IDDQ measurement distributions for devices formed on a wafer, classified into families. The ICs were profiled/classified into Families based on data from a post-Si agent. Family 2 is highlighted in the drawing. The measured IDDQ (Ioff current or leakage current) of each of the ICs is also presented in the plot, showing the distribution of IDDQ within the wafer. The results of the profiling process are that different Families were created per the different Si type, that the IDDQ range of each Family is narrower than the IDDQ distribution range of the whole wafer (the full Si range). This evidences that ICs were profiled based on physical Si parameters.

[00189] Referring now to FIG. 12, there are shown example cycle-time measurement distributions for the devices formed on a wafer of FIG. 11, classified into families. The ICs were profiled/classified into Families based on data from a post-Si agent. Family 2 is highlighted. The measured cycle-time of each of the ICs is also presented in the plot, showing the distribution of cycle-time within the wafer. The results of the profiling process are that different Families were created per the different Si type, that the cycle-time range of each Family is narrower than the cycle-time distribution range of the whole wafer (the full Si range). This further evidences that ICs were profiled based on physical Si parameters.

[00190] Referring now to FIG. 13, there is shown, for the ICs formed on a wafer of FIG. 11, a histogram of differences between IDDQ measurements and the average value for the Family associated with the respective IC. This illustrates the reduced IDDQ range within a Family. The histogram shows the distribution relative to an average: for each of the ICs, the value is the difference between the IC measured IDDQ to family IDDQ-center in terms of σ(IDDQ). This histogram shows the typical distance of ICs to their family's centers with respect to the IDDQ measurement. It was observed that the typical distance is not affected by temperature changes. Hence, the Families that were generated are invariant to the temperature which evidences that ICs were profiled based on physical Si parameters.

[00191] Referring now to FIG 14, there is shown the data shown in FIG. 11, illustrating identification of an outlier IC. The outlier IC was identified by implementing the concept of Family correlation to a High-Coverage Measurement (HCM). In this case, the HCM is IDDQ. The outlier is IC_x which is one of the ICs that belongs to Family number-9. IC_x passed the IDDQ test with respect to the full Si sample, i.e. IC_x measured IDDQ value is within the range of the full Si sample IDDQ distribution. IC_x also passed the IDDQ test with respect to the IDDQ distribution of Wafer-A, i.e. its IDDQ measurement is within the IDDQ distribution of its own wafer. IC_x was identified as an outlier with respect to the measured IDDQ distribution of Family number-9. From FIG. 13, it can be observed that the average sigma value of a Family-IDDQ that was generated by the profiling algorithm is around 0.15. The distance for IC_x from the center of Familiy-9 (its own Family) is 1.55 sigma. Its distance, in terms of number of sigmas, is in the order of 10 (1.55/0.15). On that basis (having a distance that is at least a predetermined multiple of the average distance within the family), it was detected as an outlier.

[00192] The measurements for classification of the ICs into Families were performed at three different temperatures: low-temperature (-5C); medium temperature (25C); and high temperature (85C). The Families that were generated were found invariant to the temperature. This evidences that ICs were profiled based on physical Si parameters.

[00193] Throughout this application, various embodiments of this invention may be presented in a range format. It should be understood that the description in range format is merely for convenience and brevity and should not be construed as an inflexible limitation on the scope of the invention. Accordingly, the description of a

range should be considered to have specifically disclosed all the possible subranges as well as individual numerical values within that range. For example, description of a range such as from 1 to 6 should be considered to have specifically disclosed subranges such as from 1 to 3, from 1 to 4, from 1 to 5, from 2 to 4, from 2 to 6, from 3 to 6 etc., as well as individual numbers within that range, for example, 1, 2, 3, 4, 5, and 6. This applies regardless of the breadth of the range.

[00194] Whenever a numerical range is indicated herein, it is meant to include any cited numeral (fractional or integral) within the indicated range. The phrases "ranging/ranges between" a first indicate number and a second indicate number and "ranging/ranges from" a first indicate number "to" a second indicate number are used herein interchangeably and are meant to include the first and second indicated numbers and all the fractional and integral numerals therebetween.

[00195] In the description and claims of the application, each of the words "comprise" "include" and "have", and forms thereof, are not necessarily limited to members in a list with which the words may be associated. In addition, where there are inconsistencies between this application and any document incorporated by reference, it is hereby intended that the present application controls.

[00196] To clarify the references in this disclosure, it is noted that the use of nouns as common nouns, proper nouns, named nouns, and the/or like is not intended to imply that embodiments of the invention are limited to a single embodiment, and many configurations of the disclosed components can be used to describe some embodiments of the invention, while other configurations may be derived from these embodiments in different configurations.

[00197] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It should, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[00198] Based upon the teachings of this disclosure, it is expected that one of ordinary skill in the art will be readily able to practice the present invention. The descriptions of the various embodiments provided herein are believed to provide ample insight and details of the present invention to enable one of ordinary skill to practice the invention. Moreover, the various features and embodiments of the invention described above are specifically contemplated to be used alone as well as in various combinations.

[00199] Conventional and/or contemporary circuit design and layout tools may be used to implement the invention. The specific embodiments described herein, and in particular the various thicknesses and compositions of various layers, are illustrative of exemplary embodiments, and should not be viewed as limiting the invention to such specific implementation choices. Accordingly, plural instances may be provided for components described herein as a single instance.

[00200] While circuits and physical structures are generally presumed, it is well recognized that in modern semiconductor design and fabrication, physical structures and circuits may be embodied in computer readable descriptive form suitable for use in subsequent design, test or fabrication stages as well as in resultant fabricated semiconductor integrated circuits. Accordingly, claims directed to traditional circuits or structures may, consistent with particular language thereof, read upon computer readable encodings and representations of same, whether embodied in media or combined with suitable reader facilities to allow fabrication, test, or design refinement of the corresponding circuits and/or structures. Structures and functionality presented as discrete components in the exemplary configurations may be implemented as a combined structure or component. The invention is contemplated to include circuits, systems of circuits, related methods, and computer-readable medium encodings of such circuits, systems, and methods, all as described herein, and as defined in the appended claims. As used herein, a computer readable medium includes at least disk, tape, or other magnetic, optical, semiconductor (e.g., flash memory cards, ROM), or electronic medium and a network, wireline, wireless or other communications medium.

[00201] The foregoing detailed description has described only a few of the many possible implementations of the present invention. For this reason, this detailed description is intended by way of illustration, and not by way of limitations. Variations and modifications of the embodiments disclosed herein may be made based on the

description set forth herein, without departing from the scope and spirit of the invention. It is only the following claims, including all equivalents, which are intended to define the scope of this invention. Even though the preferred embodiments are described in the context of a PLL operating at exemplary frequencies, the teachings of the present invention are believed advantageous for use with other types of circuitry in which a circuit element, such as an inductor, may benefit from electromagnetic shielding. Moreover, the techniques described herein may also be applied to other types of circuit applications. Accordingly, other variations, modifications, additions, and improvements may fall within the scope of the invention as defined in the claims that follow.

[00202] Embodiments of the present invention may be used to fabricate, produce, and/or assemble integrated circuits and/or products based on integrated circuits.

[00203] The present invention may be a system, a method, and/or a computer program product. The computer program product may include a computer readable storage medium (or media) having computer readable program instructions thereon for causing a processor to carry out aspects of the present invention.

[00204] The computer readable storage medium can be a tangible device that can retain and store instructions for use by an instruction execution device. The computer readable storage medium may be, for example, but is not limited to, an electronic storage device, a magnetic storage device, an optical storage device, an electromagnetic storage device, a semiconductor storage device, or any suitable combination of the foregoing. A non-exhaustive list of more specific examples of the computer readable storage medium includes the following: a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), a static random access memory (SRAM), a portable compact disc read-only memory (CD-ROM), a digital versatile disk (DVD), a memory stick, a floppy disk, a mechanically encoded device having instructions recorded thereon, and any suitable combination of the foregoing. A computer readable storage medium, as used herein, is not to be construed as being transitory signals per se, such as radio waves or other freely propagating electromagnetic waves, electromagnetic waves propagating through a waveguide or other transmission media (e.g., light pulses passing through a fiber-optic

cable), or electrical signals transmitted through a wire. Rather, the computer readable storage medium is a non-transient (i.e., not-volatile) medium.

[00205] Computer readable program instructions described herein can be downloaded to respective computing/processing devices from a computer readable storage medium or to an external computer or external storage device via a network, for example, the Internet, a local area network, a wide area network and/or a wireless network. The network may comprise copper transmission cables, optical transmission fibers, wireless transmission, routers, firewalls, switches, gateway computers and/or edge servers. A network adapter card or network interface in each computing/processing device receives computer readable program instructions from the network and forwards the computer readable program instructions for storage in a computer readable storage medium within the respective computing/processing device.

[00206] Computer readable program instructions for carrying out operations of the present invention may be assembler instructions, instruction-set-architecture (ISA) instructions, machine instructions, machine dependent instructions, microcode, firmware instructions, state-setting data, or either source code or object code written in any combination of one or more programming languages, including an object oriented programming language such as Java, Smalltalk, C++ or the like, and conventional procedural programming languages, such as the "C" programming language or similar programming languages. The computer readable program instructions may execute entirely on the user's computer, partly on the user's computer, as a stand-alone software package, partly on the user's computer and partly on a remote computer or entirely on the remote computer or server. In the latter scenario, the remote computer may be connected to the user's computer through any type of network, including a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider). In some embodiments, electronic circuitry including, for example, programmable logic circuitry, field-programmable gate arrays (FPGA), or programmable logic arrays (PLA) may execute the computer readable program instructions by utilizing state information of the computer readable program instructions to personalize the electronic circuitry, in order to perform aspects of the present invention.

[00207] Aspects of the present invention are described herein with reference to flowchart illustrations and/or block diagrams of methods, apparatus (systems), and

computer program products according to embodiments of the invention. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, can be implemented by computer readable program instructions.

[00208] These computer readable program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks. These computer readable program instructions may also be stored in a computer readable storage medium that can direct a computer, a programmable data processing apparatus, and/or other devices to function in a particular manner, such that the computer readable storage medium having instructions stored therein comprises an article of manufacture including instructions which implement aspects of the function/act specified in the flowchart and/or block diagram block or blocks.

[00209] The computer readable program instructions may also be loaded onto a computer, other programmable data processing apparatus, or other device to cause a series of operational steps to be performed on the computer, other programmable apparatus or other device to produce a computer implemented process, such that the instructions which execute on the computer, other programmable apparatus, or other device implement the functions/acts specified in the flowchart and/or block diagram block or blocks.

[00210] The flowchart and block diagrams in the Figures illustrate the architecture, functionality, and operation of possible implementations of systems, methods, and computer program products according to various embodiments of the present invention. In this regard, each block in the flowchart or block diagrams may represent a module, segment, or portion of instructions, which comprises one or more executable instructions for implementing the specified logical function(s). In some alternative implementations, the functions noted in the block may occur out of the order noted in the figures. For example, two blocks shown in succession may, in fact, be executed substantially concurrently, or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved. It will also be noted that each block of the block diagrams and/or flowchart illustration, and combinations of

blocks in the block diagrams and/or flowchart illustration, can be implemented by special purpose hardware-based systems that perform the specified functions or acts or carry out combinations of special purpose hardware and computer instructions.

[00211] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application, or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

What is claimed is:

1. A computerized method for IC classification and/or outlier detection, comprising:

providing a wafer comprising a plurality of ICs in accordance with an IC design, wherein the IC design comprises a plurality of sensors; and

using at least one hardware processor for testing each of the plurality of ICs by:

collecting a plurality of sensor values, the plurality of sensor values including sensor values from each of the plurality of sensors;

comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC; and

recording the classification of each tested IC.

2. The method of claim 1, wherein the step of providing comprises manufacturing the wafer based on the IC design using a fabrication process.

3. The method of claim 1 or claim 2, wherein the classification scheme is based on one or more of:

simulations of a plurality of IC operations of the IC design and the fabrication process, wherein the simulations are at least one of at least one complete IC design simulation, at least one partial IC design simulation, and at least one device simulation for the fabrication process;

a plurality of training sensor values collected during a pre-production tape-out test; and

the collected plurality of sensor values.

4. The method of any preceding claim, wherein the classification scheme comprises an outlier class.

5. The method of any preceding claim, wherein the comparing comprises estimating high coverage measurements from the plurality of sensor values using at least one of a function and a rule determined from a training set of sensor values and training high coverage measurements.

6. The method of any preceding claim, further comprising using the least one hardware processor for marking an IC package of the tested IC with unique identifications based on the classification and/or using the least one hardware processor for discarding a defective IC.

7. The method of any preceding claim, further comprising:

(i) from each tested IC, determining a set of parameters of the fabrication process based on the classification and the plurality of sensor values;

(ii) selecting a second set of parameters of the fabrication process based on the IC design and the sets of parameters of the fabrication process for each IC; and

(iii) a second manufacturing of a second wafer using the second set of parameters, wherein the selecting is performed by at least one of a manual process and an automatic computation, providing a wafer comprising a plurality of ICs in accordance with an IC design, wherein the IC design comprises a plurality of sensors.

8. The method of any preceding claim, wherein the classification comprises a hierarchical data structure for determining the classification of each die.

9. The method of any preceding claim, further comprising:

identifying the classification scheme based on a plurality of classification values by:

establishing a matrix representation from the plurality of classification values, each row of the matrix representation comprising classification values in respect of one of the plurality of ICs;

computing a covariance matrix from the matrix representation and a singular value decomposition (SVD) for the covariance matrix;

determining, using the SVD, a plurality of distance values, each distance value representing a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs; and

identifying, from the plurality of distance values, at least one family, thereby defining the classification scheme.

10. The method of claim 9, wherein the step of identifying, from the plurality of distance values, at least one family comprises:

classifying a first IC of the plurality of ICs in a first family, such that the first family is defined by the first IC;

comparing a distance value, from the plurality of distance values, representing a distance between the first IC and a second IC of the plurality of ICs with a predetermined threshold;

if the distance value is less than the predetermined threshold, classifying the second IC in the first family; and

if the distance value is greater than the predetermined threshold, classifying the second IC in a second family, such that the second family is defined by the second IC.

11. The method of claim 10, wherein the step of identifying, from the plurality of distance values, a plurality of families further comprises, for each other IC of the plurality of ICs:

identifying a group of distance values, from the plurality of distance values, each distance value in the group of distance values representing a distance between the other IC and a respective IC of the plurality of ICs that defines a respective family;

comparing each distance value from the group of distance values with the predetermined threshold;

if a distance value from the group of distance values, representing a distance between the respective other IC and a specific IC of the plurality of ICs that defines a specific family, is less than the predetermined threshold, classifying the other IC in the specific family; and

if all the distance values from the group of distance values are greater than the predetermined threshold, classifying the other IC in a new family, such that the new family is defined by the other IC.

12. The method of any one of claims 9 to 11, wherein the step of computing a covariance matrix from the matrix representation comprises normalizing the matrix representation prior to computing the covariance matrix.

13. The method of any one of claims 9 to 12, wherein the plurality of classification values are based on one or more of: simulated values determined from a simulation of

the IC design; a plurality of training sensor values collected during a pre-production tape-out test; and measured sensor values.

14. The method of any one of claims 9 to 13, wherein the step of identifying the classification scheme based on the plurality of classification values is at least part of the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC.

15. The method of any one of claims 9 to 14, wherein the plurality of classification values are based on simulated sensor values determined from a simulation of the IC design and wherein the step of identifying the classification scheme based on a plurality of classification sensor values takes place before the step of comparing the plurality of collected sensor values to a classification scheme, thereby obtaining a classification for each tested IC, the step of comparing the plurality of collected sensor values to a classification scheme comprising:

establishing a collected data matrix representation from the plurality of collected sensor values, each row of the matrix representation comprising collected sensor values in respect of one of the plurality of ICs;

determining, using the collected data matrix representation, a plurality of collected data distance values, each distance value representing a respective distance between one IC of the plurality of ICs and another IC of the plurality of ICs; and

classifying, from the plurality of distance values, each of the ICs according to the classification scheme.

16. The method of claim 15, wherein the step of computing a covariance matrix from the matrix representation comprises normalizing the matrix representation prior to computing the covariance matrix to define normalization coefficients thereby and wherein the step of establishing a collected data covariance matrix comprises normalizing the matrix representation using the defined normalization coefficients.

17. The method of any one of claims 9 to 16, wherein the matrix representation is established from one or more of: simulated sensor values determined from a simulation of the IC design; operational parameters determined from a simulation of the IC design; and design signature values.

18. The method of any one of claims 9 to 17, wherein the matrix representation is established from Pre-Si data and wherein the step of determining, using the SVD, a plurality of distance values comprises:

defining a set of Pre-Si SVD signatures by identifying vectors of the SVD for which the corresponding principal values of the SVD are greater than a pre-defined value and/or a pre-defined number of vectors of the SVD for which the corresponding principal values of the SVD are the greatest; and

determining the plurality of distance values using the set of Pre-Si SVD signatures.

19. The method of claim 18, wherein the step of determining the plurality of distance values using the Pre-Si SVD signatures comprises calculating at least some of the plurality of distance values, each of the at least some of the plurality of distance values being based on a distance between one of the Pre-Si SVD signatures and another of the Pre-Si SVD signatures.

20. The method of claim 18 or claim 19, wherein the step of determining the plurality distance values using the set of Pre-Si SVD signatures comprises:

configuring a plurality of estimators from the simulated sensor values and the set of Pre-Si SVD signatures, each estimator generating an estimated SVD signature from input sensor values;

estimating from the plurality of estimators, for each of the plurality of ICs, a respective Post-Si SVD signature from the plurality of sensor values; and

calculating at least some of the plurality of distance values, each of the at least some of the plurality of distance values being based on a distance between one of the Post-Si SVD signatures and another of the Post-Si SVD signatures.

21. The method of claim 16, wherein the step of determining the plurality distance values using the set of Pre-Si SVD signatures further comprises calculating further distance values of the plurality of distance values, each of the further distance values being based on a distance between one of the Pre-Si SVD signatures and one of the Post-Si SVD signatures.

22. A computerized method for semiconductor integrated circuit (IC) classification, comprising:

using at least one hardware processor for:

receiving an IC design and data descriptive of a fabrication process;

simulating a plurality of IC electronic operations based on the IC design and fabrication process to produce a plurality of simulated IC operation values and a plurality of simulated device operation values;

factorizing the plurality of simulated IC operation values and the plurality of simulated device operation values to determine a subset of operational values for sensor placement;

selecting at least some of the subset of operational values producing a sensor placement set, and for each of the selected subset, analyzing the IC design to incorporate within the IC design one of a plurality of sensors configured to the specific electronic operation, wherein each element of the sensor placement set comprises a type of sensor and a location within the IC design, wherein the sensor placement set is configured to produce a plurality of sensor values that are sensitive to the IC design and the fabrication process; and

classifying the IC design into operational classes based on the plurality of sensor values thereby producing a classification scheme, wherein the operational classes comprise at least one outlier class.

23. The computerized method of claim 18, further comprising computing at least one conversion rule comprising an input data and an output data.

24. The computerized method of claim 18 or claim 19, wherein the factorizing comprises incorporation of post-Si wafer testing data into determining the subset.

25. The computerized methods of any one of claims 18 to 20, wherein the factorizing comprises incorporation of end-customer use data into determining the subset.

26. The computerized methods of any one of claims 18 to 21, wherein the selecting comprises incorporation of post-Si wafer testing data into determining the sensor placement set.

27. The computerized methods of any one of claims 18 to 22, wherein the selecting comprises incorporation of end-customer use data into determining the sensor placement set.

28. The computerized methods of any one of claims 18 to 23, wherein the classification comprises a hierarchical data structure for determining the classification of each die.

29. The method of any preceding claim, wherein the each of the plurality of sensors is selected from the group consisting of a rising time delay sensor, a falling time delay sensor, a frequency maximum detection circuit, an IC unit total leakage current detection sensor based on a frequency conversion circuit, an IC unit voltage drain to drain leakage current detection sensor based on a frequency conversion circuit, and an IC unit voltage source to drain leakage current detection sensor based on a frequency conversion circuit.

30. The method of any preceding claim, further comprising determining at least one of (i) a sensor value shift and (ii) an outlier using the classification scheme during at least one of a package testing, a circuit testing, a burn-in testing, a high-temperature operating life testing, and a final product testing.

31. A testing device for reducing the test time of each of a plurality of ICs, comprising:

at least one hardware processor configured for:

testing each of a plurality of ICs by:

collecting a plurality of sensor values, at least one of the plurality of sensor values from each of a plurality of sensors incorporated into each of the plurality of ICs;

comparing the plurality of sensor values to a classification scheme, thereby obtaining a classification for each tested IC; and

reducing the test time for each tested IC based on the classification.

32. A computer program product, comprising computer readable instructions configured when operated on a hardware processor to perform the computerized method of any one of claims 1 to 26.

33. A computerized system configured to perform the computerized method of any one of claims 1 to 26.

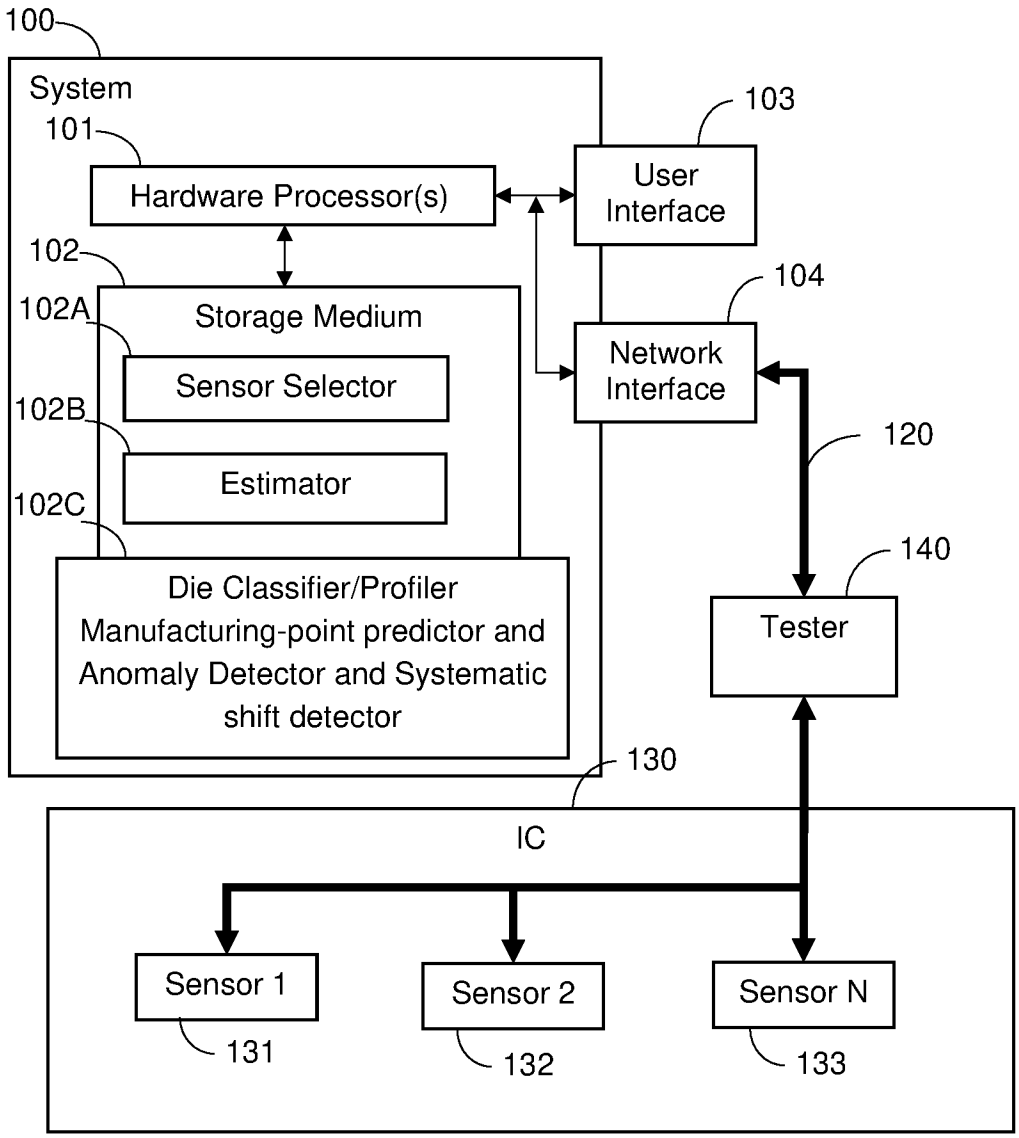

100
System
101
Hardware Processor(s)
102
Storage Medium
102A
Sensor Selector
102B
Estimator
102C
Die Classifier/Profiler
Manufacturing-point predictor and
Anomaly Detector and Systematic
shift detector
103
User
Interface
104
Network
Interface
120
140
Tester
130
IC
Sensor 1
131
Sensor 2
132
Sensor N
133

FIG. 1

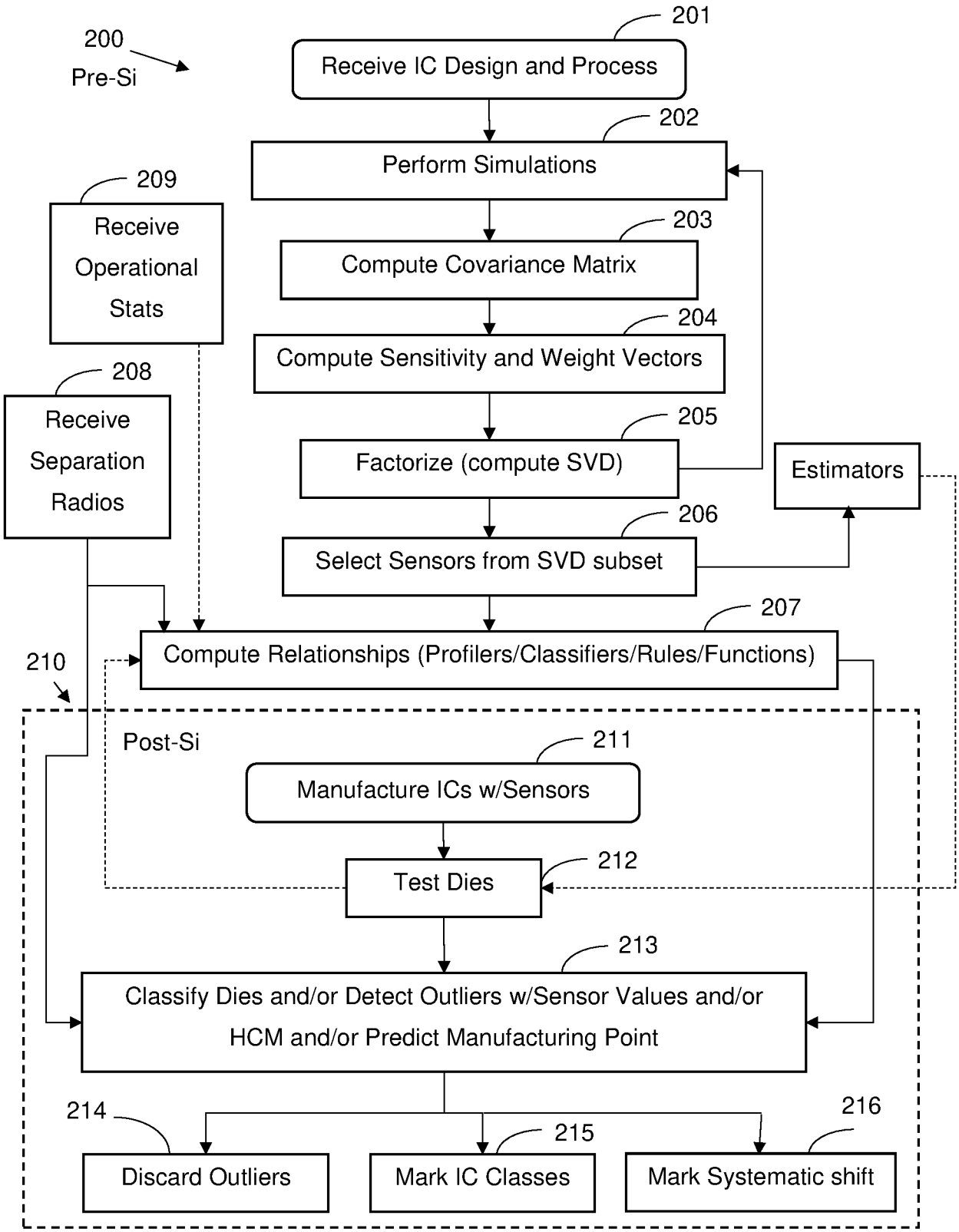

200
Pre-Si
201
Receive IC Design and Process
202
Perform Simulations
209
Receive Operational Stats
203
Compute Covariance Matrix
204
Compute Sensitivity and Weight Vectors
208
Receive Separation Radios
205
Factorize (compute SVD)
Estimators
206
Select Sensors from SVD subset
207
Compute Relationships (Profilers/Classifiers/Rules/Functions)
210
Post-Si
211
Manufacture ICs w/Sensors
212
Test Dies
213
Classify Dies and/or Detect Outliers w/Sensor Values and/or HCM and/or Predict Manufacturing Point
214
Discard Outliers
215
Mark IC Classes
216
Mark Systematic shift

FIG. 2

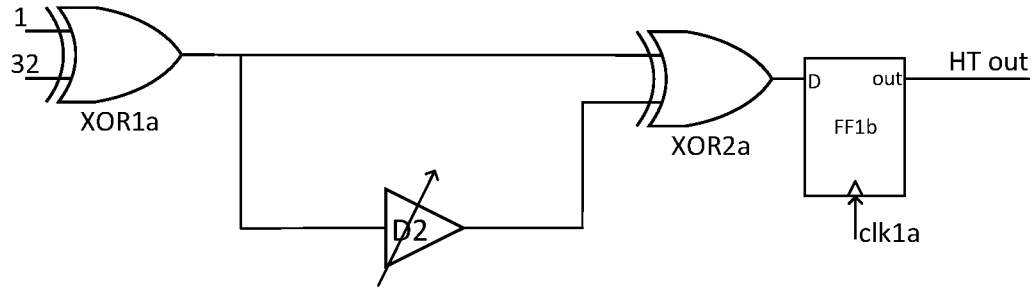

1
32
XOR1a
D2
XOR2a
D
out
FF1b
HT out
clk1a

FIG. 3A

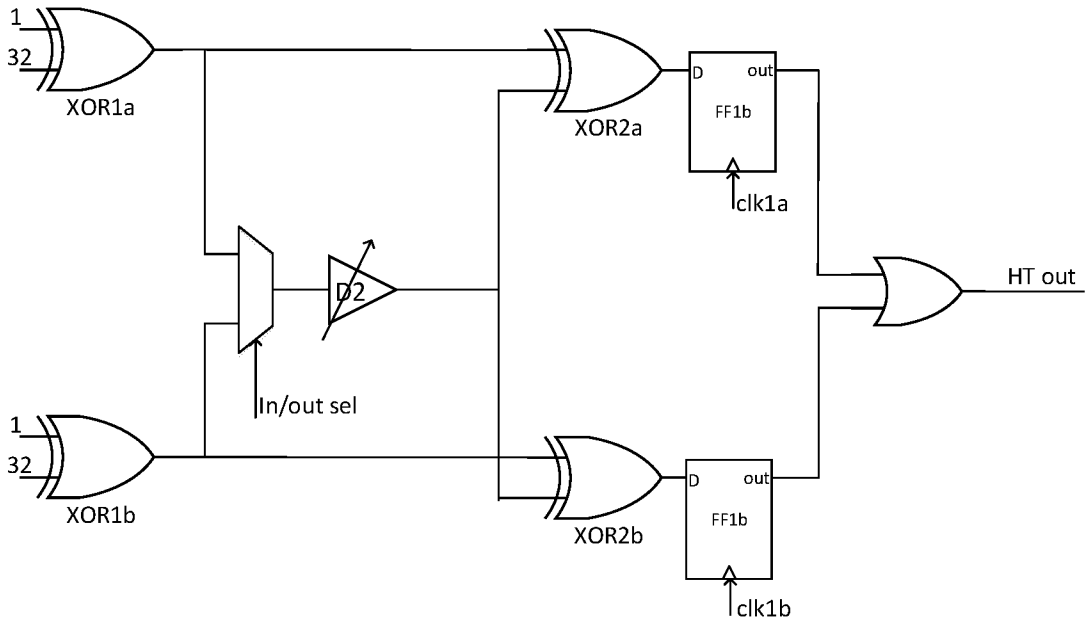

1
32
XOR1a
XOR2a
D
out
FF1b
clk1a
D2
HT out
In/out sel
1
32
XOR1b
XOR2b
D
out
FF1b
clk1b

FIG. 3B

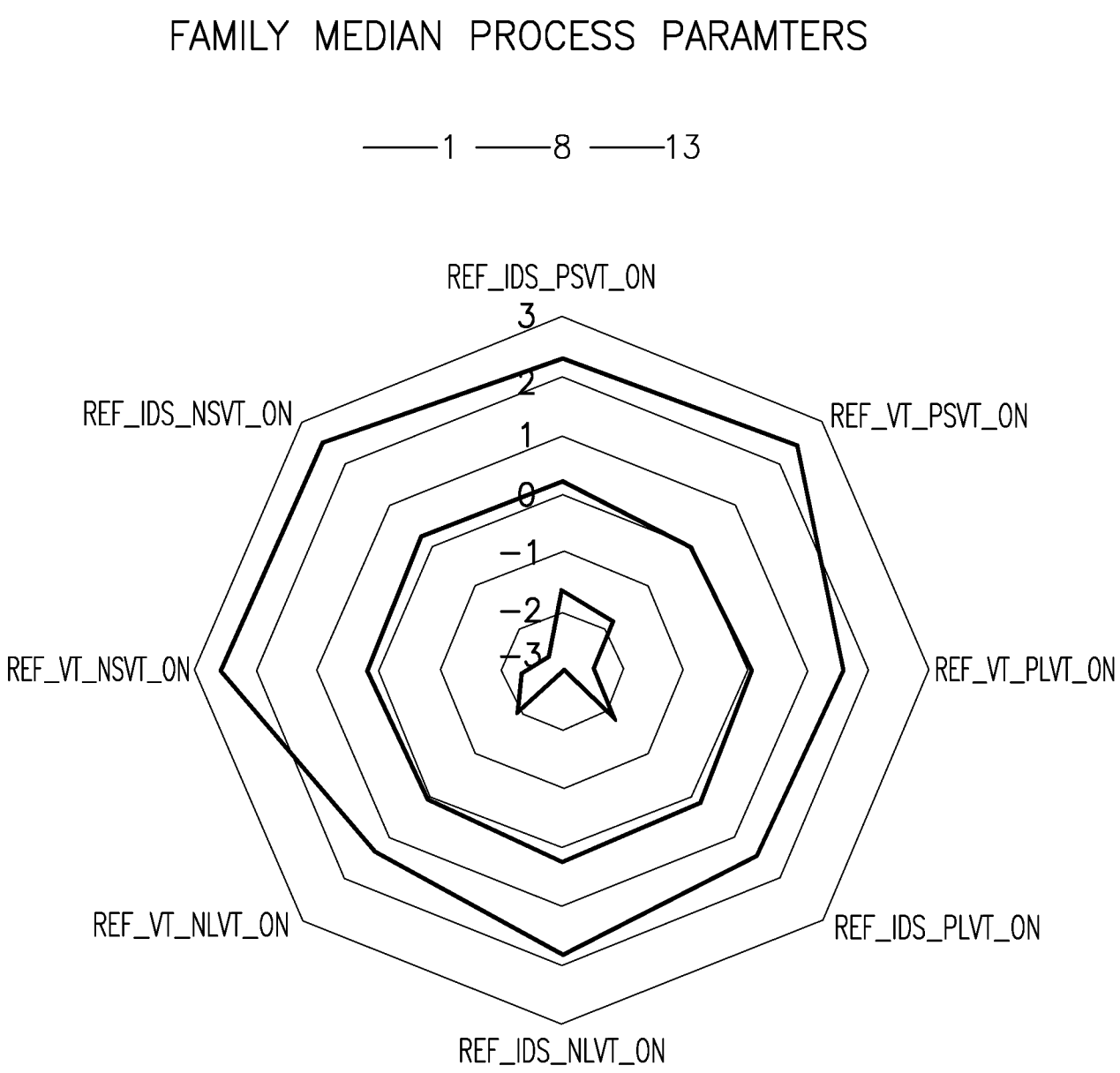

FAMILY MEDIAN PROCESS PARAMTERS
1
8
13
REF_IDS_PSVT_ON
REF_VT_PSVT_ON
REF_VT_PLVT_ON
REF_IDS_PLVT_ON
REF_IDS_NLVT_ON
REF_VT_NLVT_ON
REF_VT_NSVT_ON
REF_IDS_NSVT_ON
3
2
1
0
−1
−2
−3

FIG.4

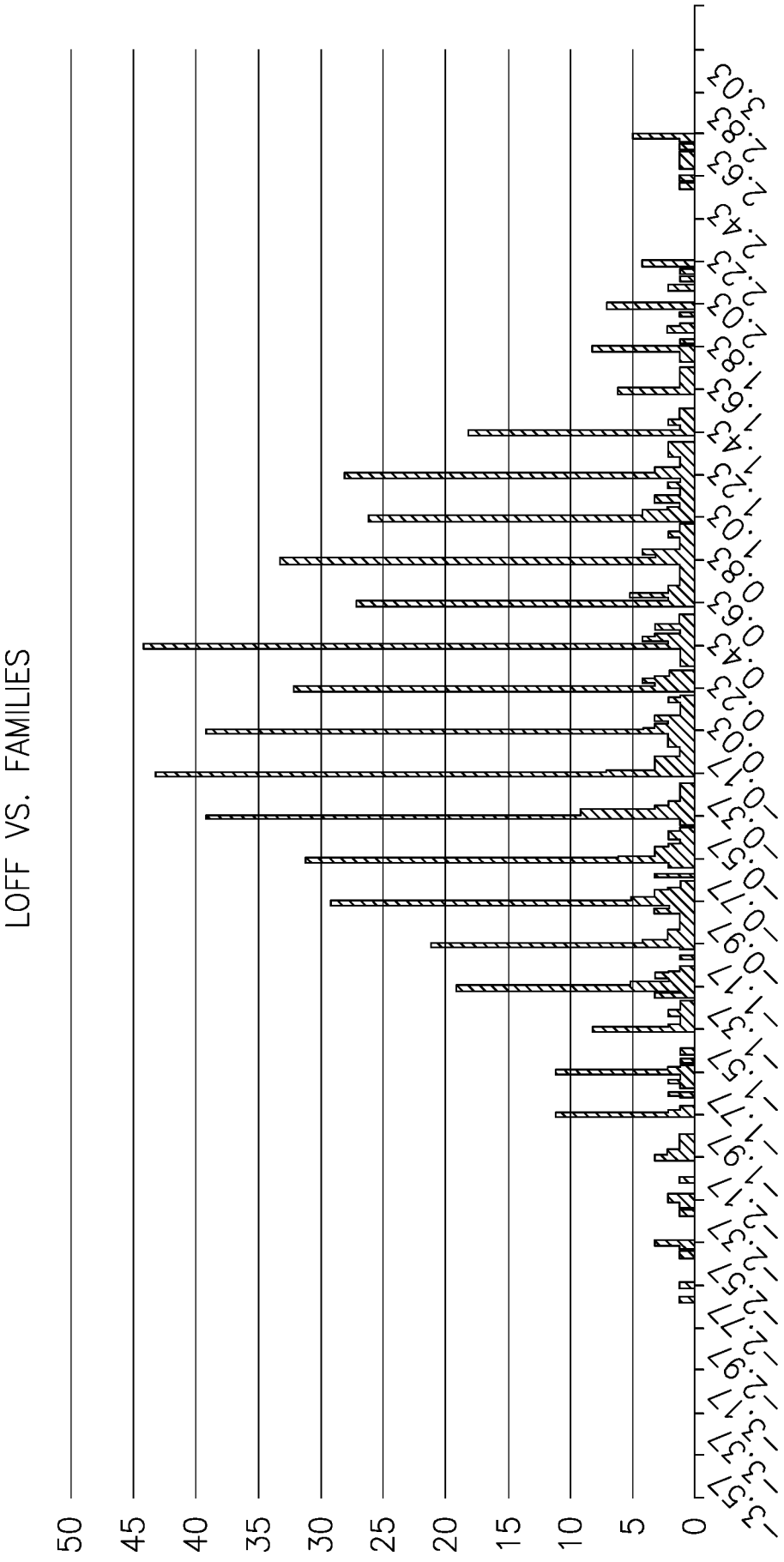


FIG.5

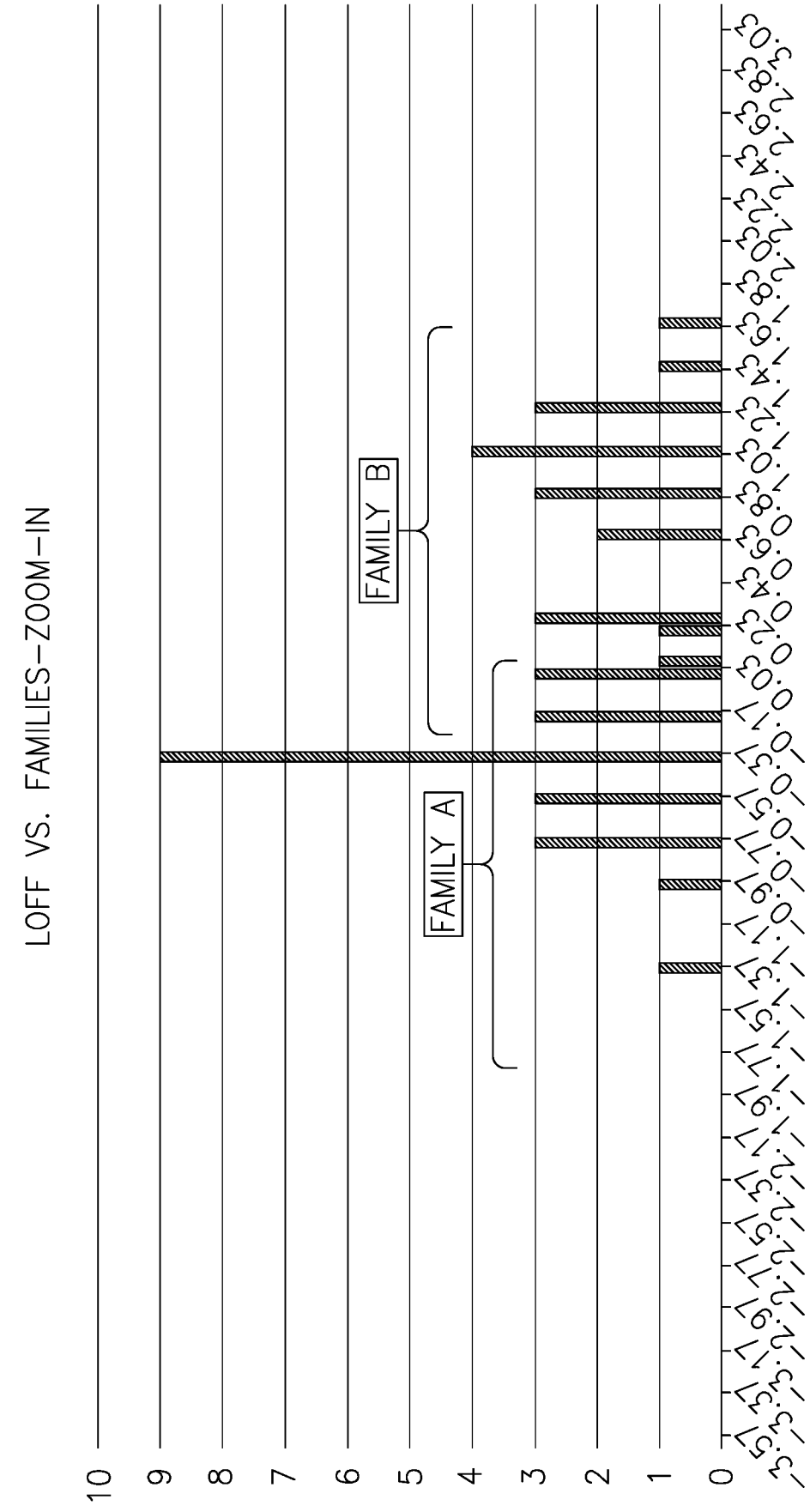


FIG.6

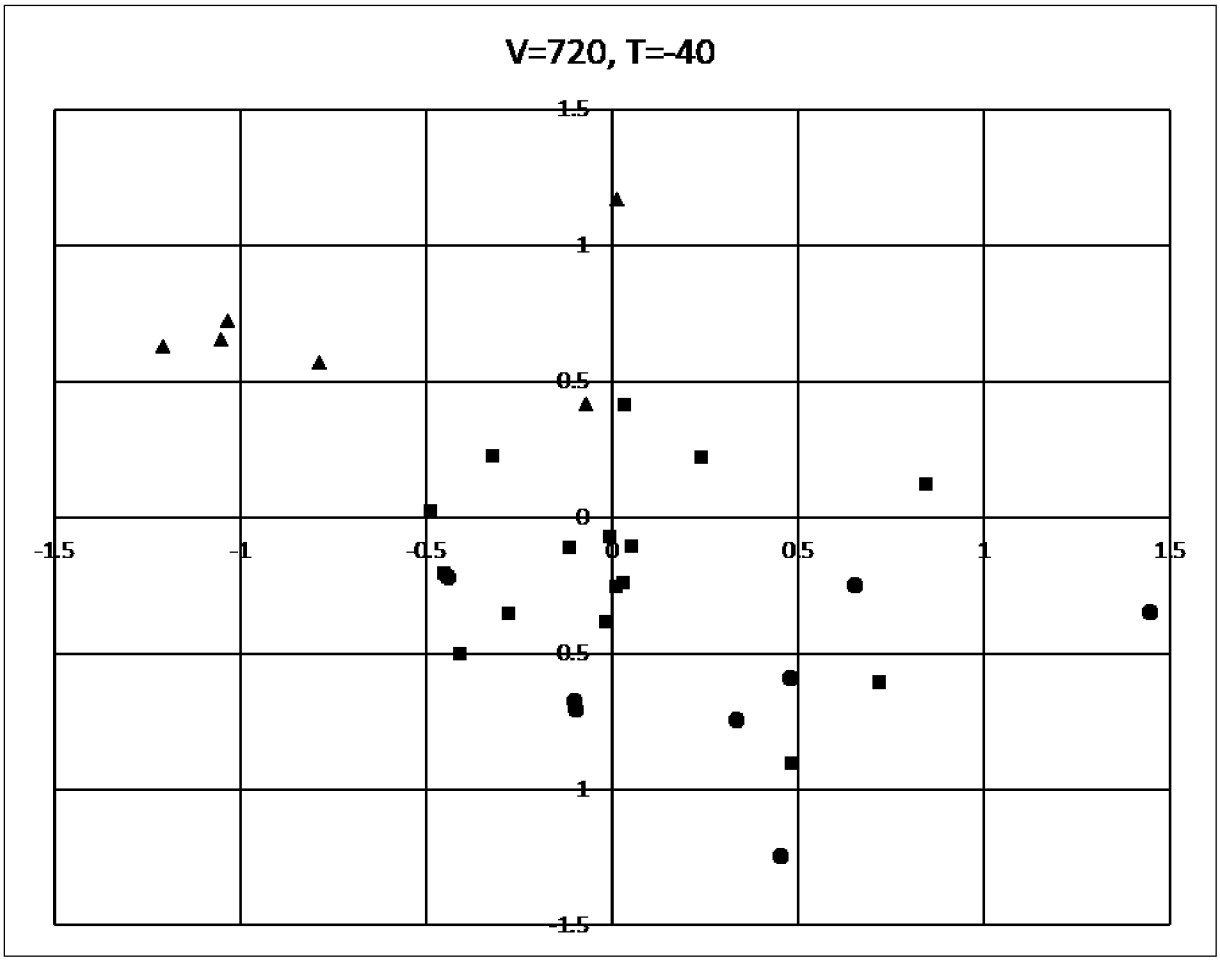


FIG. 7A

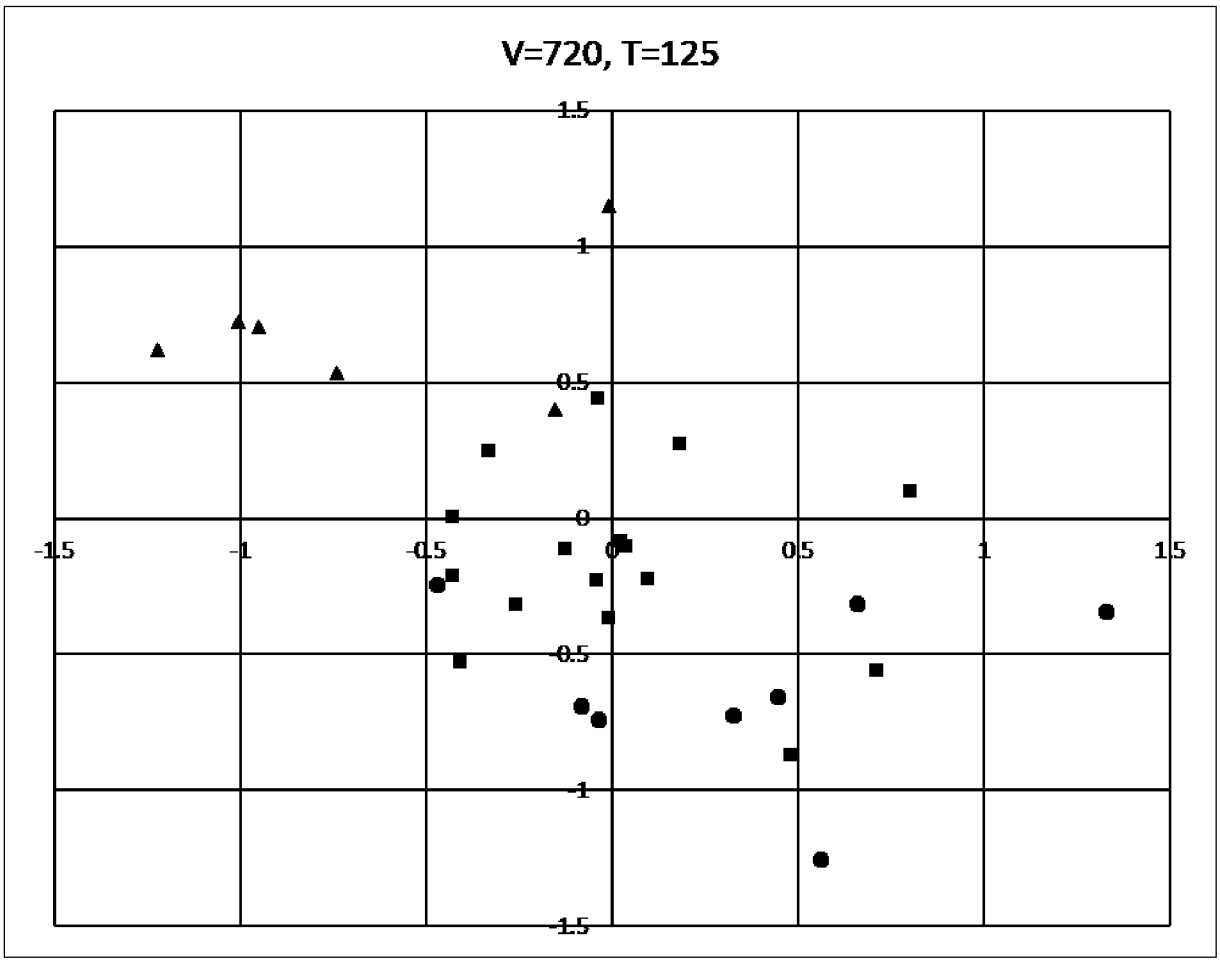


FIG. 7B

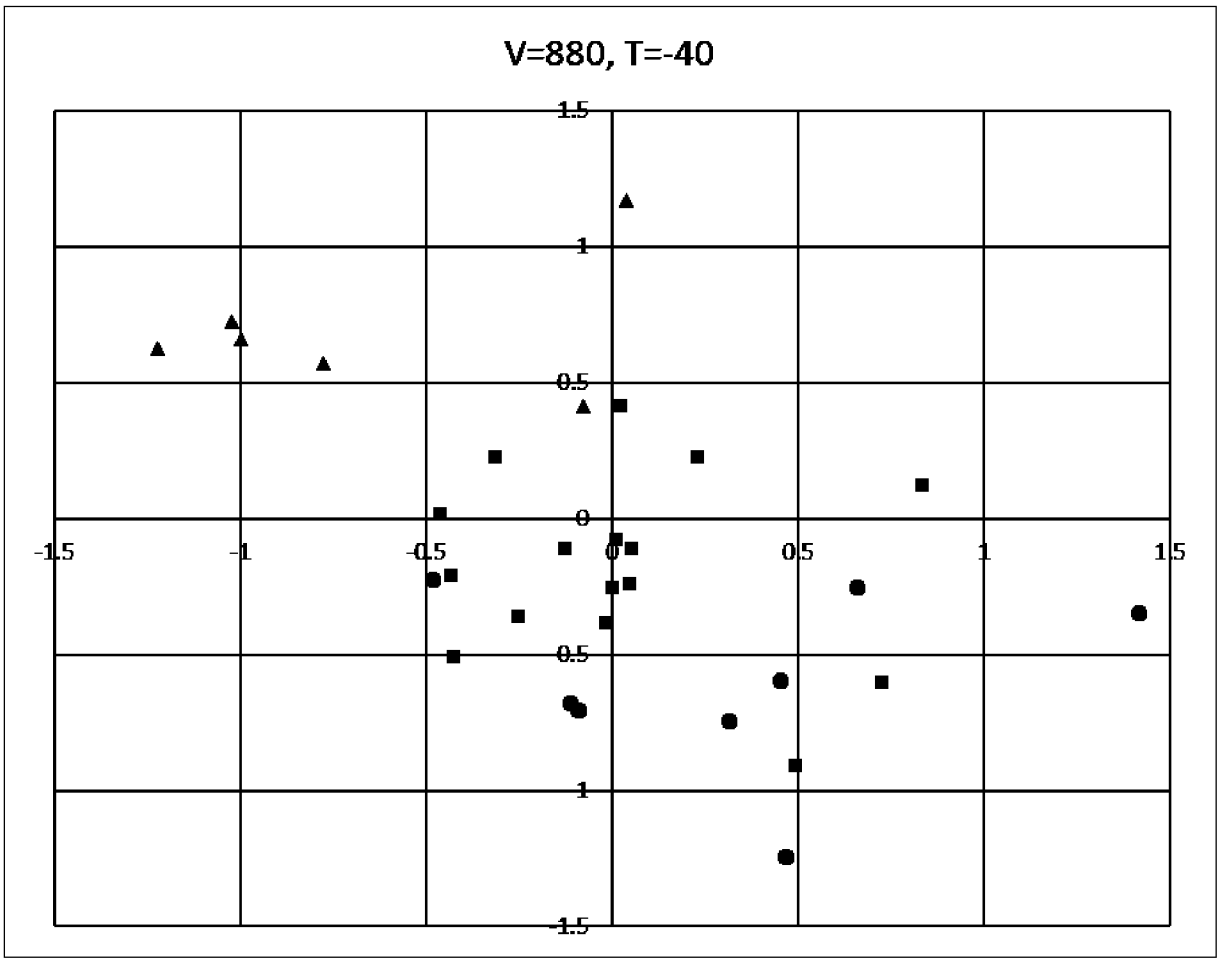


FIG. 7C

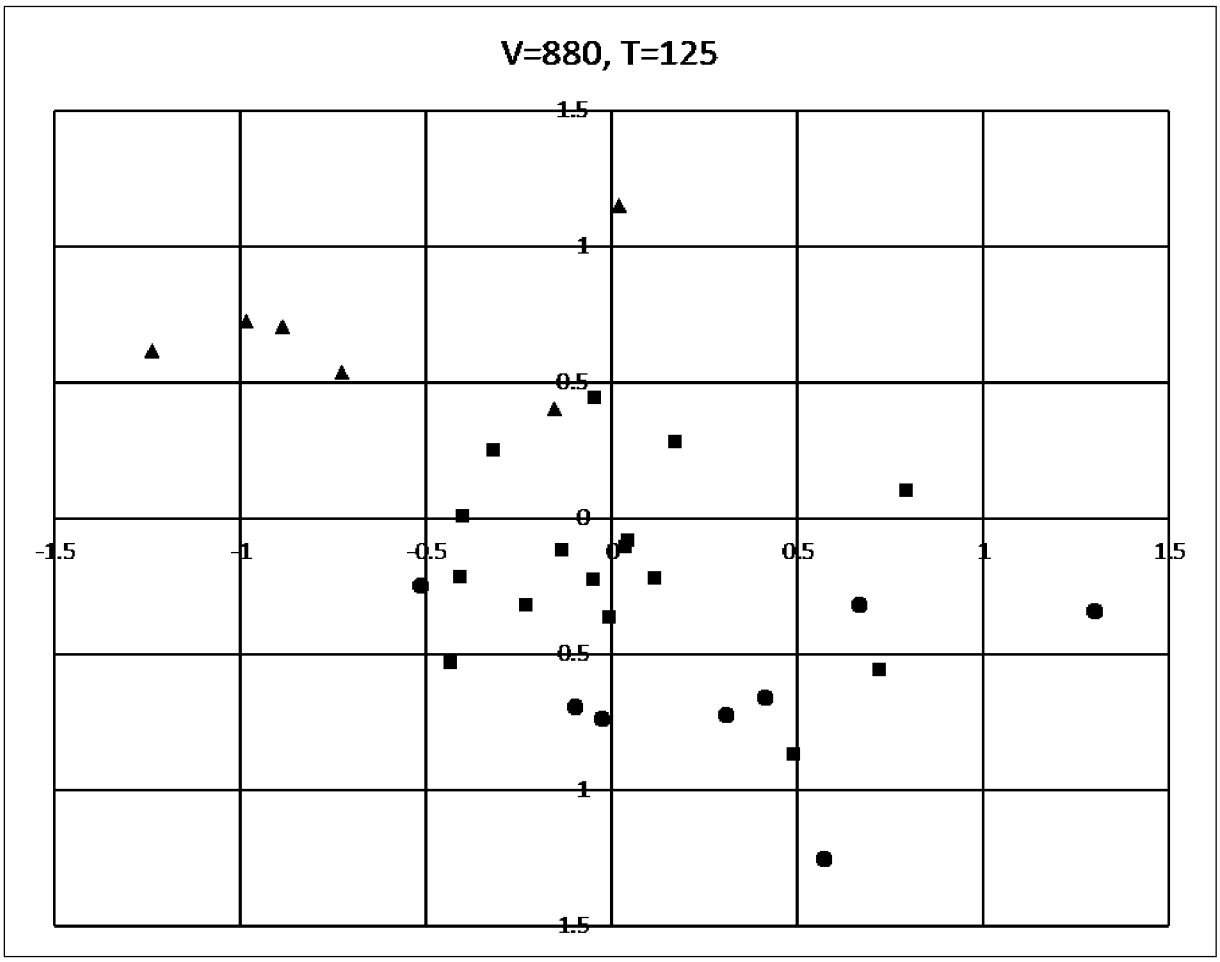


FIG. 7D

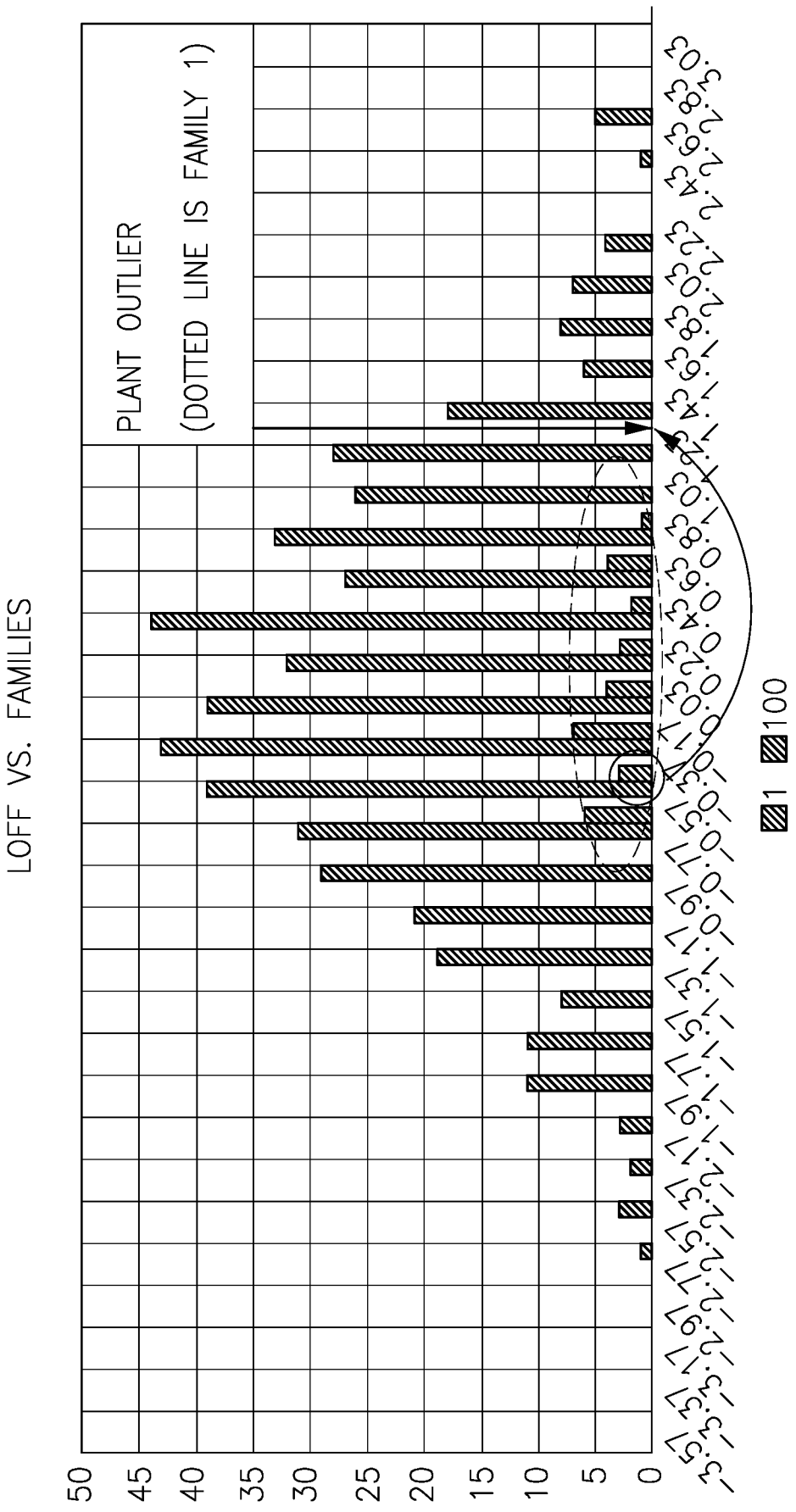

LOFF VS. FAMILIES
PLANT OUTLIER
(DOTTED LINE IS FAMILY 1)
50
45
40
35
30
25
20
15
10
5
0
1
100

FIG.8

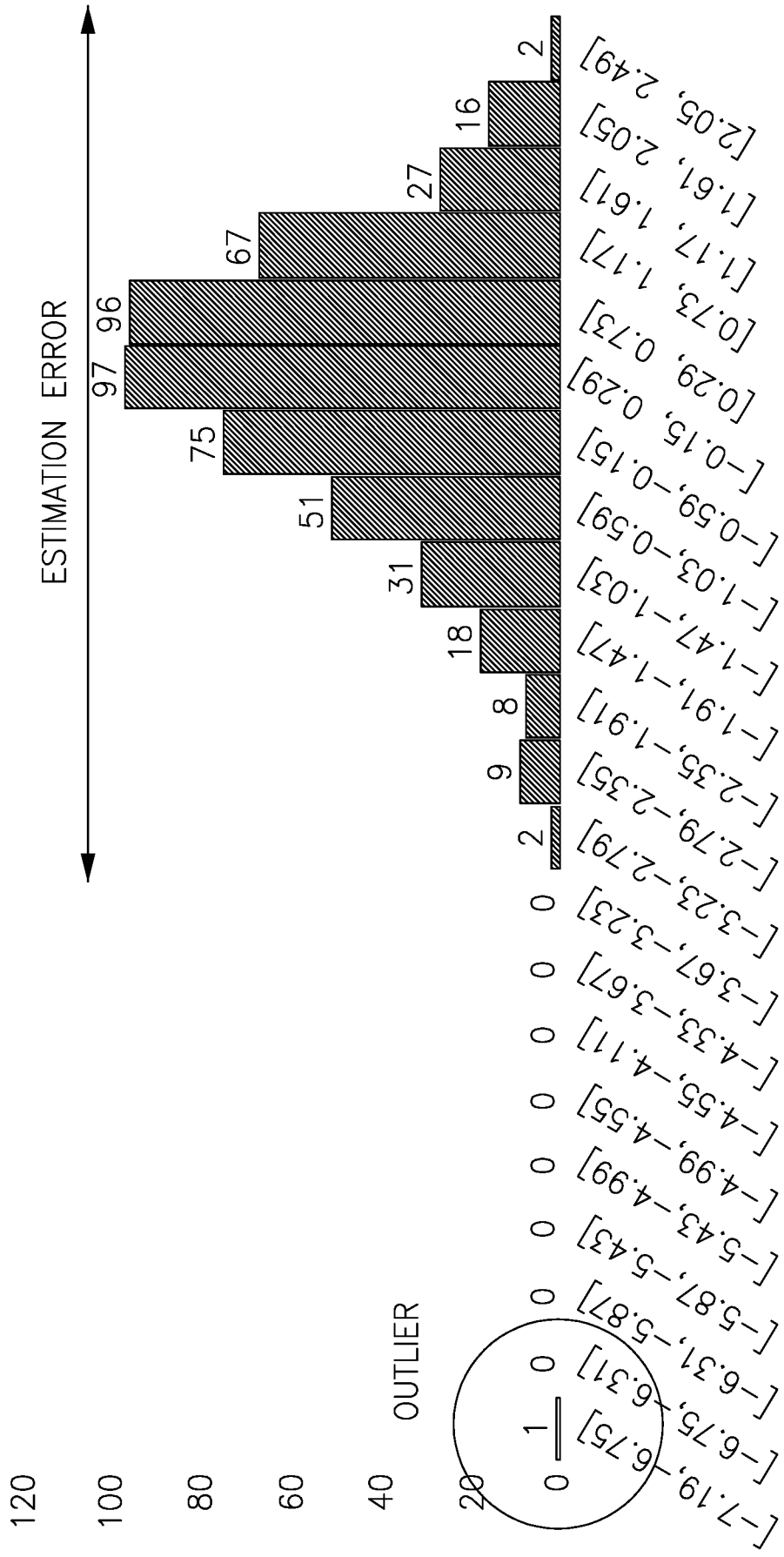

ESTIMATION ERROR
OUTLIER
120
100
80
60
40
20
0
1
0
0
0
0
0
0
0
0
0
0
0
2
9
8
18
31
51
75
97
96
67
27
16
2
[−7.19, −6.75]
[−6.75, −6.31]
[−6.31, −5.87]
[−5.87, −5.43]
[−5.43, −4.99]
[−4.99, −4.55]
[−4.55, −4.11]
[−4.33, −3.67]
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[−2.35, −1.91]
[−1.91, −1.47]
[−1.47, −1.03]
[−1.03, −0.59]
[−0.59, −0.15]
[−0.15, 0.29]
[0.29, 0.73]
[0.73, 1.17]
[1.17, 1.61]
[1.61, 2.05]
[2.05, 2.49]

FIG.9

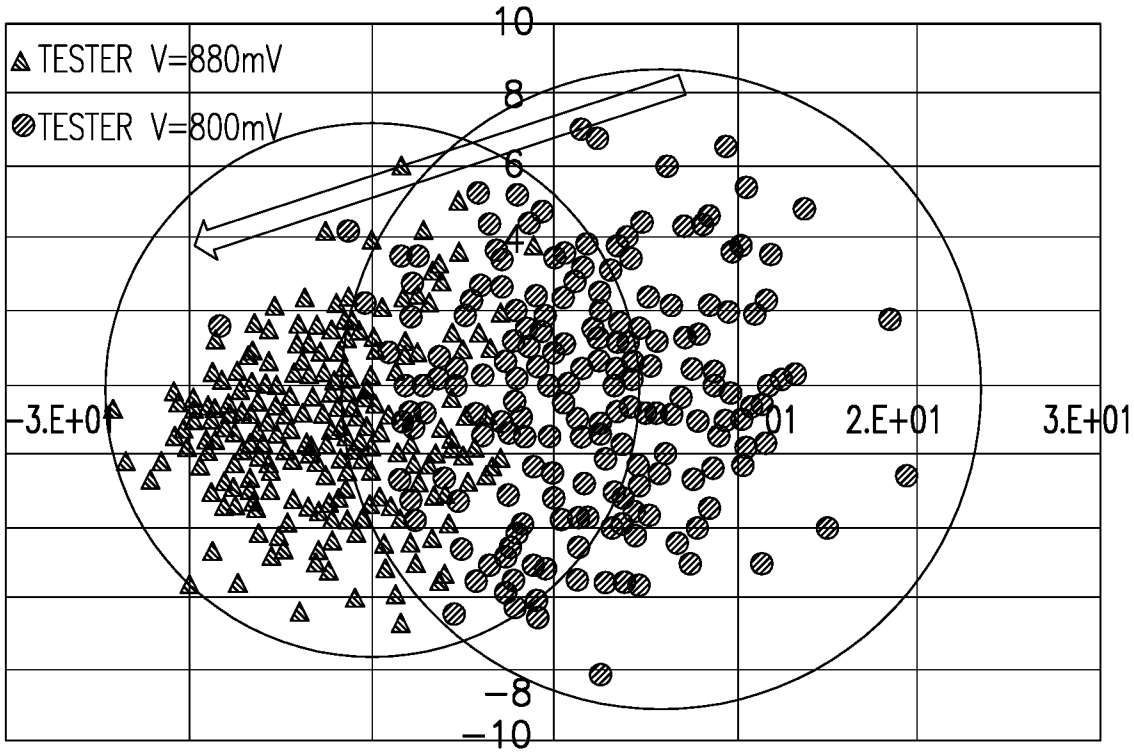


FIG.10A

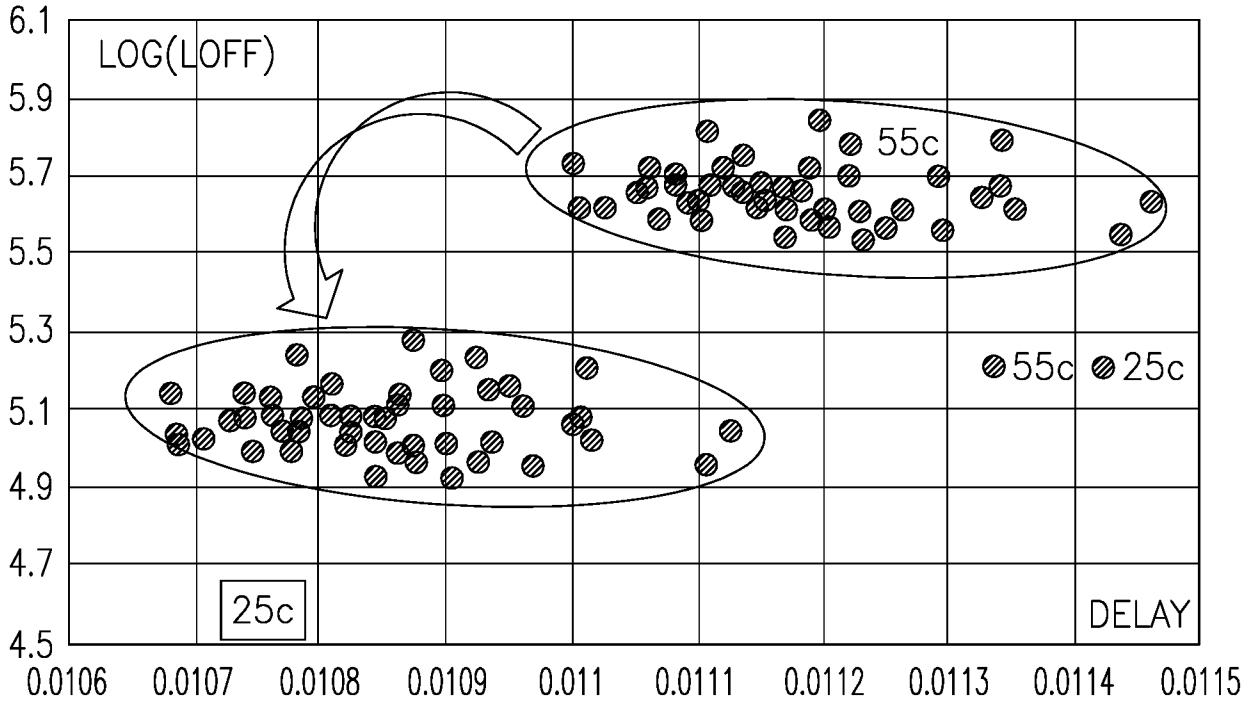


FIG.10B

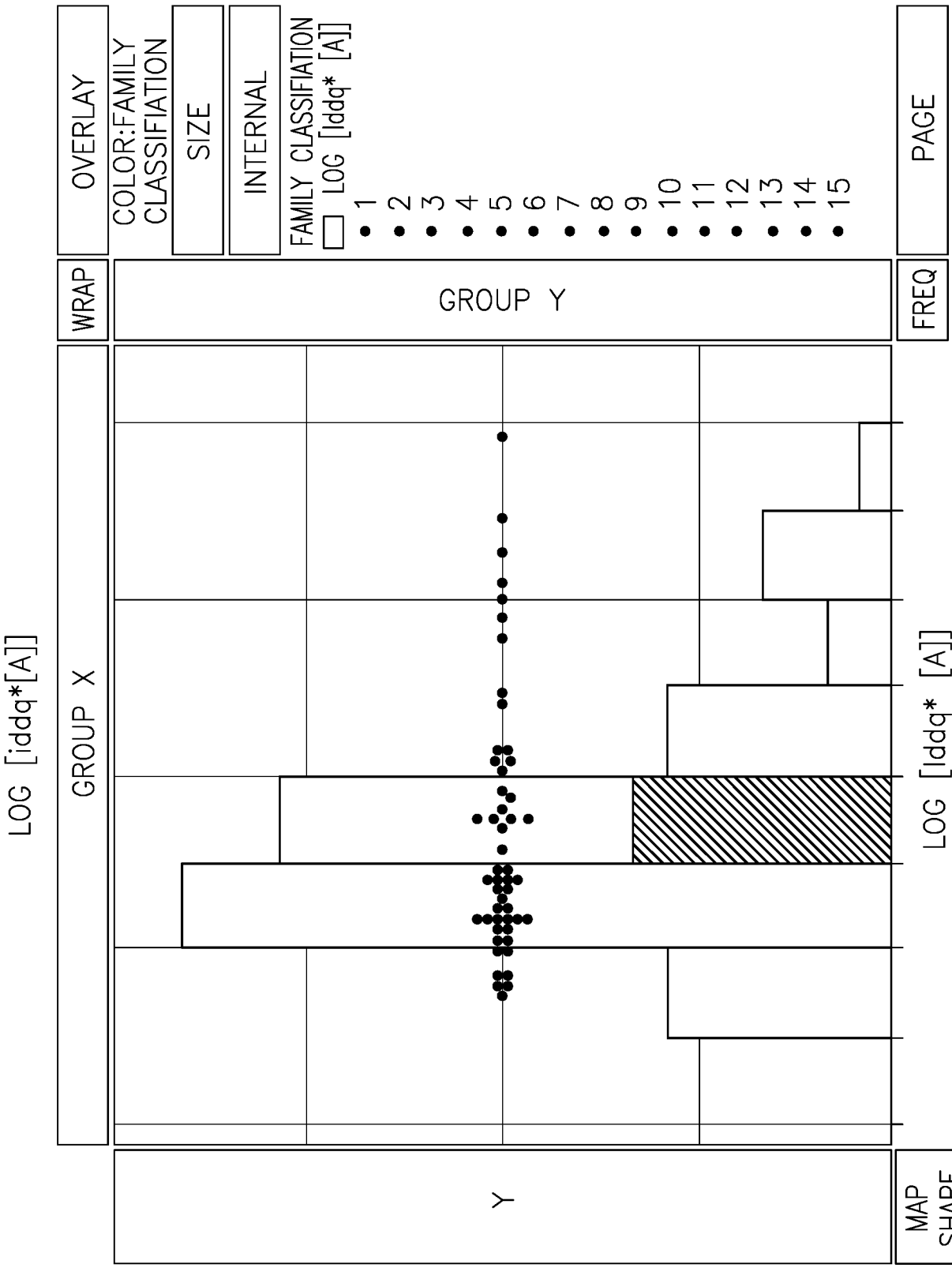

LOG [iddq*[A]]
GROUP X
WRAP
OVERLAY
COLOR:FAMILY CLASSIFIATION
SIZE
INTERNAL
FAMILY CLASSIFIATION
LOG [Iddq* [A]]
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
GROUP Y
PAGE
FREQ
LOG [Iddq* [A]]
Y
MAP SHAPE

FIG.11

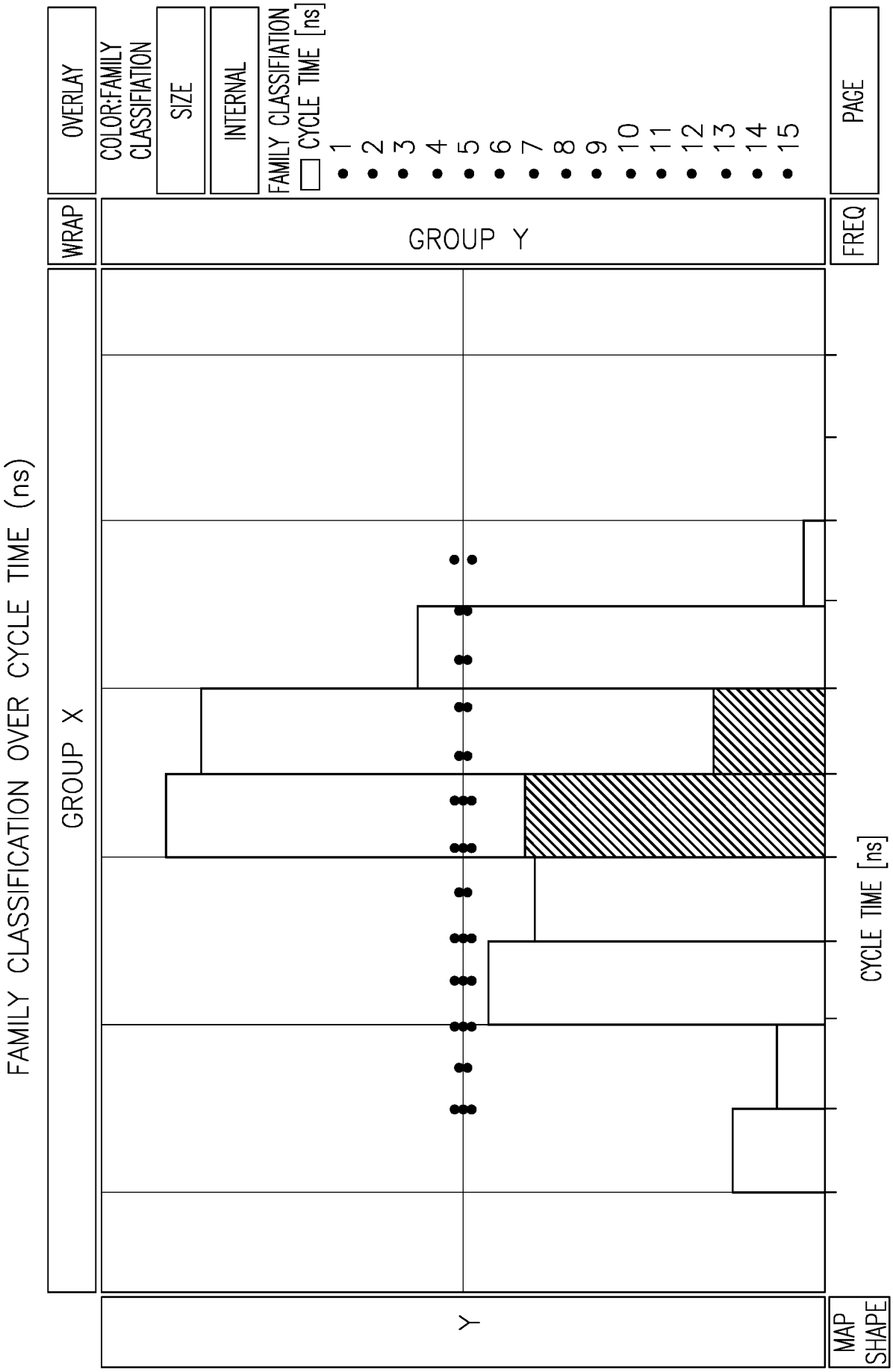

FAMILY CLASSIFICATION OVER CYCLE TIME (ns)
GROUP X
GROUP Y
CYCLE TIME [ns]
Y
WHERE (WAFER=A)
OVERLAY
WRAP
MAP SHAPE
COLOR:FAMILY CLASSIFIATION
SIZE
INTERNAL
FAMILY CLASSIFIATION
CYCLE TIME [ns]
1
2
3
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11
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13
14
15
PAGE
FREQ

FIG.12

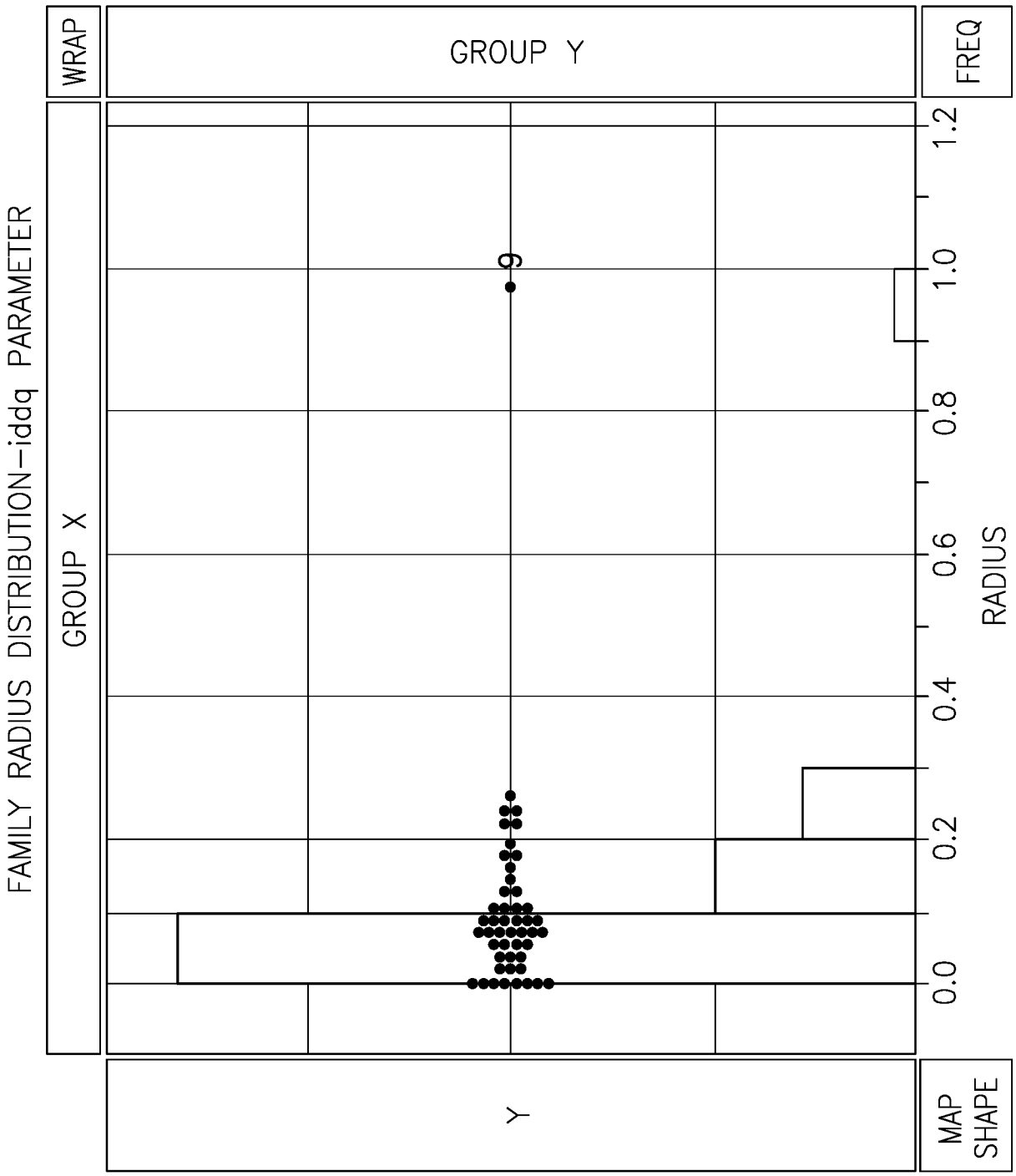

FAMILY RADIUS DISTRIBUTION—iddq PARAMETER
WRAP
GROUP X
GROUP Y
FREQ
MAP SHAPE
Y
9
0.0
0.2
0.4
0.6
0.8
1.0
1.2
RADIUS

FIG.13

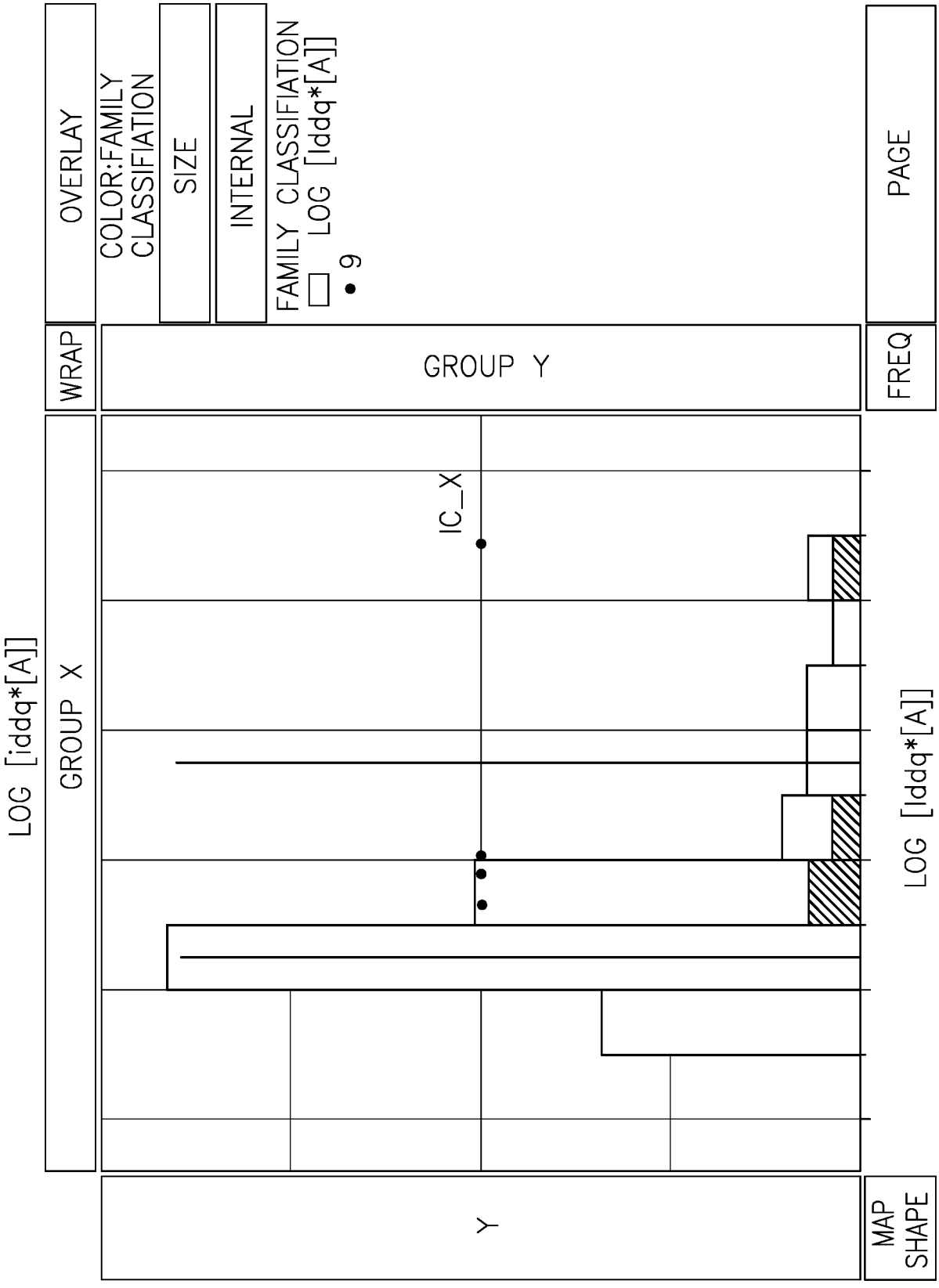

OVERLAY
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FAMILY CLASSIFIATION
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WRAP
GROUP Y
FREQ
LOG [iddq*[A]]
GROUP X
IC_X
LOG [Iddq*[A]]
Y
MAP SHAPE

FIG.14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL2019/050433

A. CLASSIFICATION OF SUBJECT MATTER
IPC (20190101) G01R 31/317, G01R 31/28, G06N 7/00, G06F 17/50
CPC (20130101) G01R 31/31718, G01R 31/2856, G06N 7/005, G06F 17/5068
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (20190101) G01R 31/317, G01R 31/28, G06N 7/00, G06F 17/50
CPC (20130101) G01R 31/31718, G01R 31/2856, G06N 7/005, G06F 17/5068

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See extra sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017038265 A1 Intel Corp. 09 Feb 2017 (2017/02/09) entire document	1-4,6-8,31-33
Y	entire document	5
Y	US 2017364818 A1 Business Objects Software Ltd. 21 Dec 2017 (2017/12/21) entire document	5
A	US 8001512 B1 Cadence Design Systems Inc. 16 Aug 2011 (2011/08/16) entire document	22-30
A	US 6807503 B2 ASML Netherlands BV. 19 Oct 2004 (2004/10/19) entire document	1-33

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 Aug 2019	28 Aug 2019

Name and mailing address of the ISA:	Authorized officer
Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Facsimile No. pctoffice@justice.gov.il	ZAHDEH Jihad Telephone No. 972-73-3927237

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL2019/050433

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016203036 A1 Ecorithm Inc. 14 Jul 2016 (2016/07/14) entire document	1-33
A	US 2008147355 A1 Polaris Innovations Ltd. 19 Jun 2008 (2008/06/19) entire document	1-33
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Search terms used: Simulation , IC Outlier Identification, Statistical outlier identification, Built in self test , SVD , defect, faulty , sensors , classification , threshold