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(54) Title: AN IR DETECTOR ARRAY DEVICE

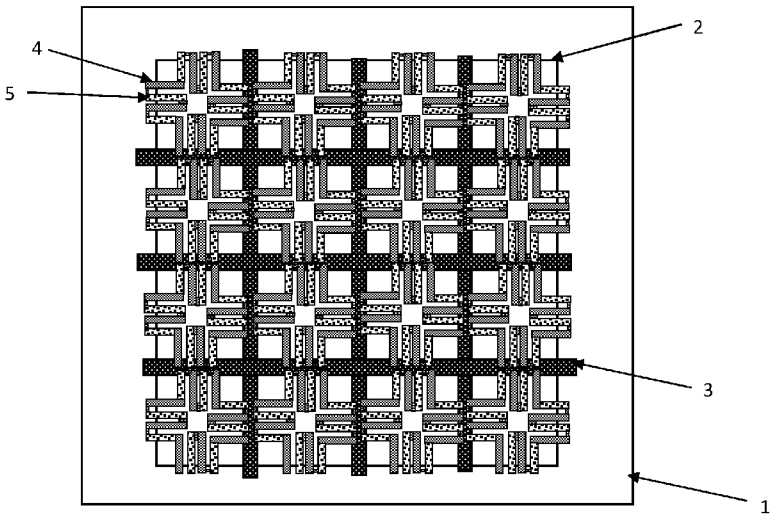


Figure 3

(57) Abstract: We disclose herein a thermal IR detector array device comprising a dielectric membrane (2), supported by a substrate, the membrane having an array of IR detectors (4, 5), where the array size is at least 3 by 3 or larger, and there are tracks (3) embedded within the membrane layers to separate each element of the array, the tracks also acting as heatsinks and/or cold junction regions.

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An IR Detector Array Device

Field of the Invention

This invention relates to an Infra-Red (IR) detector array device, particularly but not exclusively, to micro-machined thermal Infrared detector arrays.

Background of the Invention

Micro-machined thermal infrared (IR) detectors are a well-established technology, and are typically based on thermopiles, bolometers, pyrodetectors or even diodes. These typically include of a structure thermally insulated from the substrate (such as a membrane or micro-bridge) which heats up due to incident IR radiation, and this change in temperature is detected using various methods. For example Graf et al. "Review of micromachined thermopiles for infrared detection" Meas. Sci. Technol. 18 (2007) R59-R75 reviews several thermopile based IR detectors which are typically on a membrane. Kim et al., "A new uncooled thermal infrared detector using silicon diode," Sensors and Actuators A 89 (2001), pp. 22-27, discusses a diode on a micro-bridge membrane used for IR radiation measurement.

It is also well known to fabricate arrays of IR detectors. For example, Hirota et al., "120x90 Element thermopile array fabricated with CMOS technology," Proceedings of SPIE Vol. 4820 (2003) pp. 239 – 249 describe an array of thermopile IR detectors, where each IR detector pixel is a separate front-side etched membrane.

Sarro et al., "An integrated thermal infrared sensing array," Sensors and Actuators 14 (1998) pp. 191-201, describe a linear 8-element thermopile array where each IR detector is on a cantilever structure. Jones et al., "MEMS thermal imager with optical readout", Sensors and actuators A 155 (2009), pp. 47-57, describe a two dimensional array where each detector is on a cantilever.

Foote et al., "High performance micromachined thermopile linear arrays," SPIE Vol. 3379, 1998, pp. 192-197, describe a linear array with each thermopile IR detector on a micro-bridge.

Calaza et al., "An uncooled infrared focal plane array for low-cost applications fabricated with standard CMOS technology," Sensors and Actuators A 132 (2006) pp. 129-138, describe a two dimensional IR detector array, where each detector is on a suspended membrane/microbridge structure.

Kanno et al., "Uncooled infrared focal plane array having 128x128 thermopile detector elements," SPIE Vol. 2269, pp. 450 – 459 describe a 128x128 IR detector array, where each element is on a suspended membrane/diaphragm.

US7842922 describes an IR detector array based on thermopiles, where each element is on membrane.

US7005644 describes an IR detector array based on diodes, where each element is on a separate micro-bridge type structure.

In each of these examples, the individual element of the array is on its own separate membrane/cantilever/diaphragm structure. These structures usually cannot be made very small, and as a result the pixel size tends to be large. This results in the overall array occupying a large chip area and is costly.

However, a number of linear arrays with 1 or 2 rows are known in literature. For example:
Baer et al., "A 32-element micromachined thermal imager with on-chip multiplexing" Sensors and Actuators A 48 (1995) pp. 47-54 described a 2x16 IR detector array on a single membrane.

Kessler et al., "A 256 pixel linear thermopile array using materials with high thermoelectric efficiency," Proceedings of Thermoelectrics 1997, pp. 734-737, and Dillner et al., "A 64-pixel linear thermopile array chip designed for vacuum environment," Proceedings of IRS^2 2006, pp. 295-300, both describe linear arrays.
EP1413861B1 describes a linear array with only one row, having all the detectors on a single membrane.

US8441093 describes linear arrays of detectors based on thermopiles all on the same membrane, where the cold junction is on the substrate. It also shows a circular

membrane with thermopiles placed radially, with the cold junctions on the substrate. In this case as well, the array cannot have a large number of pixels as cold junction connection to the substrate is needed.

These structures are possible as with a 1 or 2 row array of IR detectors on the same membrane, there is a substrate region next to each pixel which is cooler than the pixel area. For example, if using a thermopile based detector, the substrate region can be used as the cold junction region. However, for an array including 3 or more rows, the rows in the centre do not have access to the substrate region. For example, EP1413861 describes an array of detectors including of several rows, but they are made with each two row on a single membrane to allow a cold junction on the substrate for the thermopile.

In the above documents, it still requires several membranes for a large number of rows.

US6040579 and Schaufelbuehl et al., "256-Pixel CMOS-Integrated Thermoelectric Infrared Sensor Array" Proceedings of MEMS 2001, pp. 200-203, describe an array of thermopile IR detectors all on the same membrane, and use gold on top of the membrane to separate each pixel and act as the heat sink.

Similarly, Oliver et al., "A 1024-element bulk-micromachined thermopile infrared imaging array," Sensors and Actuators 73 (1999) pp. 222-231, describe a two-dimensional array on a single membrane, where the device thermal isolation is performed by the use of thick silicon underneath the membrane.

Rubio et al., "Thermopile sensor array for an electronic nose integrated non-selective NDIR gas detection System," Proceedings of Spanish Conference on Electron Devices 2005, pp. 503-505, describe a two dimensional IR detector array on a single membrane, using silicon below the membrane to provide the cold junction for the thermopiles.

In these cases a single membrane is used for the entire array. However, in case of using silicon underneath the membrane as a heatsink, the etching process is much more complicated. Additionally, the silicon heat sinks cannot be made very small, hence the spacing between pixels is large.

In the case of using gold tracks on top of the membrane, gold is not CMOS compatible, and this results in a non-standard process and increased fabrication cost.

Summary

Aspects and preferred features are set out in the accompanying claims.

According to one aspect of the present invention there is provided an infra-red (IR) detector array device comprising:

a two dimensional array of a plurality of IR detectors;

a dielectric membrane formed on a semiconductor substrate which comprises an etched portion;

a plurality of separator regions formed within the dielectric membrane;

wherein at least some of the plurality of IR detectors are formed on or within the dielectric membrane, and wherein said at least some of the plurality of IR detectors are separated from one another by at least some of said plurality of separator regions.

The separator regions may be more thermally conductive than the dielectric membrane. In one embodiment, the separator region comprises at least one layer that is thermally more conductive (or has higher thermal conductivity) that the dielectric membrane (or than the the dielectric layers in the dielectric membrane).

The two dimensional array may comprise at least a 3 by 3 array. The size of the array may be larger than the 3 by 3 array. In general the design of a 3x3 or large array requires more than one membrane as the pixels in the centre do not have access to the substrate to form a temperature difference required for thermal IR detection. This increases the overall chip area. However, in this invention, the a 3x3 or larger array can be made on a single membrane, using the separate regions within the membrane dielectric layers which act as the heat sink, or cold junction region. This results in smaller chip size and lower cost.

The separator regions are thermally more conductive than the dielectric membrane and may be two dimensionally formed within the dielectric membrane. The separator regions may comprise at least two first separator regions extending in a first direction and at least two second separator regions extending in a second direction transverse to the first direction, the second separator regions intersecting the first separator regions.

The at least some of the plurality of IR detectors may be spaced from one another by said at least two first separator regions and by said at least two second separator regions.

Two adjacent IR detectors may be separated from one another by the first and second separator regions.

Some of the at least of some of the IR detectors are not separated from one another by the first and second separator regions. In this example, at least two adjacent IR detectors may be coupled directly with one another without having any separator regions between them. In one embodiment, at least two detectors are located within one pixel of the array device.

The separator regions each may comprise at least one separator layer. The at least one separator layer comprises at least one layer of metal, polysilicon and/or single crystal silicon. The at least one separator layer may compris at least one layer of interconnect material to connect the IR detectors within the array of the IR detectors.

Each IR detector may form a pixel of the device. Each pixel can have at least one IR detector. The separator regions may each provide thermal isolation between each pixel of the device.

The IR detectors or pixels comprise any one or more of a thermopile, a resistor, transistor and a diode. It is possible that each pixel has a combination of two or more of a thermopile, a resistor, a transistor and a diode.

According to the embodiments of the invention, there is provided a two-dimensional infrared detector array of a size 3x3 or larger, where all the detectors are on the same membrane and separated by at least one layer of metal, polysilicon and/or single crystal silicon within the separator regions and embedded within the dielectric

membrane. The membrane includes one or more dielectric materials supported on a substrate, and the membrane is thermally isolated from the substrate by bulk etching.

The IR detectors can be a thermopile, a diode, a transistor, or a resistor. The metal, polysilicon and/or single crystal silicon layers/tracks may form a thermal isolation between each pixel and can also be considered as a heat sink region, while the rest of the pixel area can be considered the hot region. The heat sink region may also contain interconnects to connect to the IR detectors within the array.

In the case of a thermopile, it includes one or more thermocouples connected in series. Each thermocouple includes two dissimilar materials which form a junction at the hot region of the pixel (to form the hot junction), while the other ends of the materials are in the heat sink region where they are connected electrically to the adjacent thermocouple to form the cold junction.

For the pixels at the edge of the membrane, some of the cold junctions will be formed outside the membrane on the substrate area.

The thermocouple materials may include metal such as Al, Copper, Tungsten, Titanium or combination of those, doped polysilicon (n or p type) or doped single crystal silicon (n or p type). In the example that both the material are polysilicon and/or single crystal silicon, a metal link may be used to form the junctions between them.

In the example of using diode detectors or transistor based, each pixel will have one diode in the centre, or more than one diode connected in series in the centre. The diode can be made of polysilicon or of single crystal silicon. The transistor can be made of single crystal silicon. Each pixel may also have a reference diode or transistor in the heat sink region.

In the example of using a resistor as a detector, each pixel will have a resistor in the centre. The resistor can be made of metal such as Al, Copper, Tungsten, titanium, Platinum, polysilicon (n or p type) or single crystal silicon (n or p type). The resistance of such resistors will change with a change in temperature. There can also be a reference resistor in the heat sink area of each pixel.

Alternately, the IR detection can be done by a combination of different sensor types. For example, a thermopile, where both the Seebeck effect, and the resistance change effect is used to determine the IR radiation. Alternatively for example the thermopile uses a reference diode for the cold junction temperature estimation in order to determine the absolute temperature in the hot junction.

The dielectric membrane may comprise:

a membrane cavity comprising vertical side walls or sloping side walls;

one or more dielectric layers comprising silicon dioxide and/or silicon nitride;

one or more layers of spin on glass, and

a passivation layer over the one or more dielectric layers.

The membrane may be formed by back-etching using Deep Reactive Ion Etching (DRIE) of the substrate, which results in vertical sidewalls. The back-etching can also be performed using anisotropic etching such as KOH (Potassium Hydroxide) or TMAH (TetraMethyl Ammonium Hydroxide) which result in slopping sidewalls.

The membrane can also be formed by a front-side etch to result in a suspended membrane structure, supported by at least two or more beams.

The starting substrate can be silicon, or silicon on insulator (SOI) or any semiconductor, besides silicon, such as Silicon Carbide, Gallium Arsenide or Gallium nitride or a combination of those together with silicon.

The device is preferably fabricated using CMOS-based or CMOS-usable materials. Here the terms “CMOS-based” material or “CMOS-usable” material refer to the materials which are compatible in the state-of-art CMOS processing steps or CMOS process. In this example the metals used maybe CMOS materials such as tungsten, aluminium, copper, titanium, molybdenum. Silicon, polysilicon and silicides can also be used to form various IR detectors or for the tracks/layers within the separator regions to isolate the pixels.

Alternatively the device may also be fabricated with some or all non-CMOS materials. The metals used may comprise platinum or gold. The IR detector material may

comprise other materials such as vanadium oxide, or various silicides, including magnesium silicide.

The dielectric membrane itself may be circular, rectangular, or rectangular shaped with rounded corners to reduce the stresses in the corners, but other shapes are possible as well. There may also be holes on each pixel of the membrane to improve the response of each pixel.

There can also be several membranes on one chip, with each membrane having an array of IR detectors.

The array can also have circuitry integrated on the same chip. The circuitry can comprise switches, multiplexer, decoder, filter, amplifier, analogue to digital converter, and/or other circuitry. This will typically be outside the membrane area.

Additionally, there can also be pixel addressing circuitry within the membrane. If using SOI technology, then the thin silicon layer will be on the membrane and can be used for circuitry within the heat sink region. The simplest circuit can comprise a FET switch. More complicated circuits using amplifiers or buffers are also possible.

In non-SOI technology, polysilicon diodes can be used to address the appropriate pixel.

The arrays may also have plasmonic structures on them to improve the absorbance at preferred wavelengths or filter out specific unwanted wavelengths or bands of wavelengths. These structures could be made of metal such as tungsten, aluminium, copper, titanium, molybdenum, gold or platinum, silicides or polysilicon or single crystal silicon, and are periodically repeated in a lateral direction. The structures can be circle, ellipse, rectangular, trapezoid, or any other shape or combination of different shapes. The structures can be dots of these shapes or holes of these shapes within the layer. The repeat pattern can be hexagonal or square. The structures can be in more than one layer. All the pixels in the array may have an identical plasmonic structure, or the plasmonic structure can be different for different pixels. There may also be some pixels with plasmonic structures and some without.

The device maybe packaged in a metal TO type package. The device can also be packaged in a ceramic, metal or plastic SMD (surface mount device) package. The package may have one or more IR filters or windows, or a filter whose characteristics vary laterally. The package maybe hermetically or semi-hermetically sealed with air, dry air, argon, nitrogen, xenon or any other noble gas. The device may also be packaged in a vacuum. The device may also be packaged with a lens. The device may also be packaged with a reflector. The package can also be a chip or wafer level package, formed for example, by wafer-bonding an etched wafer/chip on top, with the etched wafer/chip having a portion that is transparent to at least some wavelengths of IR. The device can also be packaged directly on a PCB, or be packaged in a flip-chip method.

The device can also have an IR emitter fabricated on the same chip. The IR emitter can be on a separate membrane, and may comprise a heater made of tungsten, aluminium, copper, polysilicon, single crystal silicon, titanium, platinum, or gold. The IR emitter may also have one or more plasmonic patterned layer within or on one side of the membrane.

The array of IR detectors can be used in portable electronic devices, buildings or in automobiles. Some or all of the signal processing can by performed by the circuitry on-chip, or on a chip co-packaged with the detector, or a chip on the same PCB, or within the device, or maybe processed at a remote device or system.

According to a further aspect of the present invention there is provided a method of manufacturing an infra-red (IR) detector array device, the method comprising:

forming a semiconductor substrate;

depositing or growing one or more layers of polysilicon and/or metals and dielectric layers to form a two dimensional array of IR detectors and a plurality of separator regions;

bulk etching the semiconductor substrate to form adielectric membrane,

wherein at least some of the plurality of IR detectors are formed on or within the dielectric membrane, and wherein said at least some of the plurality of IR detectors are separated from one another by at least some of said plurality of separator regions.

The semiconductor substrate may be a plain substrate such as silicon substrate or a layered substrate such as a silicon on insulator (SOI) substrate.

Brief Description of the Preferred Embodiments

Some preferred embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Fig. 1 shows a schematic top view of a dielectric membrane with separations;

Fig. 2 shows a schematic top-view a thermopile structure;

Fig. 3 shows the schematic top-view of an array of thermopile based IR detectors all on the same membrane with separations;

Fig. 4 shows the schematic top-view of an array of thermopile based IR detectors all on the same membrane with separations, and also having the separating material at the border of the membrane;

Fig. 5 shows the schematic top-view of an array of diode based IR detectors all on the same membrane with separations;

Fig. 6 shows the schematic cross-section of an array of thermopile based IR detectors, with metal embedded within the membrane acting as a separation;

Fig. 7 shows the schematic cross-section of an array of thermopile based IR detectors, with a metal embedded within the membrane acting as a separation, where the membrane trench has sloping side-walls;

Fig. 8 shows an example pattern arrangement of a plasmonic type structure that can be used to improve the absorption at certain wavelengths;

Fig. 9 shows the schematic top-view of an array of thermopile based IR detectors all on the same membrane with separations, and having a patterned layer on each detector to improve the absorbance;

Fig 10 shows the schematic cross-section of an array of thermopile based IR detectors, with metal embedded within the membrane acting as a separation, and having a patterned layer above the detector to improve absorbance;

Fig 11 shows the schematic cross-section of an array of thermopile based IR detectors, with metal embedded within the membrane acting as a separation, with circuitry on the same chip;

Fig 12-15 show different circuit diagrams for addressing the pixels within the array, and

Fig 16 illustrates an exemplary flow diagram outlining the manufacturing method of the IR detector array device.

Detailed Description of the Preferred Embodiments

Figure 1 shows a schematic top-view of a chip **1**, with a membrane **2** having separations **3** within it. The separations or separator regions **3** are made from material embedded within the membrane layers and may comprise metal, silicon or polysilicon. The membrane is a dielectric membrane and may comprise one or more layers of silicon dioxide and/or silicon nitride. The separations can also act to define each pixel in the array.

Figure 2 shows a schematic top-view of a thermopile comprising two different materials **4** and **5**. The materials can be metal, or doped polysilicon or doped single crystal silicon.

Figure 3 shows a schematic top-view of an IR detector array based on thermopiles, with the whole array on a single membrane **2**. This combines structures from figures 1 and 2. Each IR detector element is separated by a material **3** embedded within the membrane, which acts as a heat sink and cold junction area. The separation **3** allows isolation between each pixel. For the pixels on the edge of the membrane, some of the thermopile cold junctions are on the substrate. The two different materials **4** and **5** form two types of junctions: the hot junctions are formed within the pixel area, while the cold junctions are formed on the separator region, or on the substrate (for pixels on the

edge of the membrane). The temperature difference between the hot and cold junctions allows the IR detection.

As can be seen, the middle four pixels use the separator region to form the cold junction, and the cold junction is formed on the membrane, not the substrate. This reduces the need for more membranes, and hence results in smaller chip area and lower cost. This is applicable for any two dimensional array of 3x3 or larger size where there is at least one pixel without direct contact to the substrate.

Figure 4 shows a schematic top-view of an IR detector array based on thermopiles, with the whole array on a single membrane **2**, each pixel separated by a material **3** embedded within the membrane. Additionally, this separation material is also at the edge of the substrate – to make the whole structure a bit more symmetrical.

Figure 5 shows a schematic top-view of an IR detector array based on diodes, with the whole array on a single membrane **2**. Each pixel comprises a diode **6**, and tracks **7** which are used to electrically connect the diode. Each pixel is separated by use of a separator **3** embedded within the membrane. The diode can be made of polysilicon or single crystal silicon.

Figure 6 shows the schematic cross-section of an IR detector array based on thermopile with the whole array on a single membrane. The membrane is supported on an etched substrate **8**, and comprises dielectric layers **9** and may comprise one or more layers of silicon dioxide and/or silicon nitride. The thermopiles comprise p-doped silicon **4**, and n-doped silicon **5**, and a metal **10** is used to form a junction between them. Metal layers **3** are used to form a first separator region between the thermopiles and further metal layers 3' are used to form a second separator region between further thermopiles. This separation area also acts as a heat sink and/or cold junction area.

The thermopiles materials can comprise many other configurations, for example, n-doped silicon and metal, or p-doped silicon and metal. The silicon for the thermopiles can be polysilicon or single crystal silicon. The separation **3**, while made of metal in this figure, can also be made from single crystal silicon or polysilicon, or may comprise metal, polysilicon and/or single crystal silicon. The substrate in this example is etched by Deep Reactive Ion Etching (DRIE) which results in vertical sidewalls.

Figure 7 shows a thermopile based IR detector array on a single membrane, where the substrate has been etched by anisotropic method such as KOH or TMAH resulting in sloping sidewalls.

Figure 8 shows a plasmonic patterning on metal. The pattern comprises a shape repeated periodically in a hexagonal repeat pattern. Using this patterning within an IR detector can improve the absorbance of the detector. The pattern can alternately be a square repeat pattern. Alternately, the shape being repeated can be a rectangle, ellipse, trapezoid, star or any other shape.

Figure 9 shows the schematic top-view of a thermopile based IR detector array with plasmonic structures **11** on each detector. The figure shows identical plasmonic structures on each array. However, the plasmonic structures can be different on each pixel as well. Additionally not all the pixels may have the plasmonic structures.

Figure 10 shows the schematic cross-section on a thermopile based IR detector array, with all the detectors on the same membrane, where there are plasmonic structures **11** above the thermopiles.

Figure 11 shows a thermopile based IR detector array where there is circuitry on the same chip, outside the membrane area. As an example, a MOSFET **13** is shown, which comprises implant regions **12**, a polysilicon gate and interconnect metal.

Figure 12 shows an example circuit diagram. Each pixel comprise a MOSFET switch **15** and a detector **14** which can be a thermopile or a resistor. A decoder circuit selects the columns by turning the MOSFET on, while the multiplexer selects between rows. Preferably, the design is made in an SOI process to fabricate the MOSFETs on the membrane.

Figure 13 shows a circuit diagram, where diodes **16** are used to address each pixel. The column to be selected has to be set to a low voltage, and a multiplexing circuit can be used to select the row. The diodes can be made from either single crystal silicon or polysilicon.

Figure 14 shows a circuit diagram where diodes are used to address each pixel, where each pixel also has a reference diode **18** and a reference thermopile/resistor **17**. These can be placed within the cold junction area of the membrane. The reference elements help to improve the signal for each detector.

Figure 15 shows a circuit diagram where the IR detector is based on diodes **19**. In this embodiment, each pixel also has a reference diode **20** within the cold junction area, and these can also be addressed by a column decoder and a row multiplexer circuit.

Fig 16 illustrates an exemplary flow diagram outlining the manufacturing method of the IR detector array device.

The skilled person will understand that in the preceding description and appended claims, positional terms such as 'above', 'overlap', 'under', 'lateral', etc. are made with reference to conceptual illustrations of an apparatus, such as those showing standard cross-sectional perspectives and those shown in the appended drawings. These terms are used for ease of reference but are not intended to be of limiting nature. These terms are therefore to be understood as referring to a device when in an orientation as shown in the accompanying drawings.

It will be appreciated that all doping polarities mentioned above could be reversed, the resulting devices still being in accordance with embodiments of the present invention.

Although the invention has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure which are contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

CLAIMS:

1. An infra-red (IR) detector array device comprising:

a two dimensional array of a plurality of IR detectors;

a dielectric membrane formed on a semiconductor substrate which comprises an etched portion;

a plurality of separator regions formed within the dielectric membrane;

wherein at least some of the plurality of IR detectors are formed on or within the dielectric membrane, and wherein said at least some of the plurality of IR detectors are separated from one another by at least some of said plurality of separator regions.

2. A device according to claim 1, wherein the separator regions comprise at least one layer which is thermally more conductive than said dielectric membrane.

3. A device according to claim 1, wherein the two dimensional array comprises at least a 3 by 3 array.

4. A device according to claim 1, wherein the separator regions are two dimensionally formed within the dielectric membrane.

5. A device according to claim 1, wherein the separator regions comprise at least two first separator regions extending in a first direction and at least two second separator regions extending in a second direction transverse to the first direction, the second separator regions intersecting the first separator regions.

6. A device according to claim 5, wherein said at least some of the plurality of IR detectors are thermally separated from one another by said at least two first separator regions and by said at least two second separator regions.

7. A device according to claim 5, wherein two adjacent IR detectors are separated from one another by the first and/or second separator regions.

8. A device according to claim 5, wherein some of said at least of some of the IR detectors are not separated from one another by the first and second separator regions.

9. A device according to claim 1, wherein the separator regions each comprise at least one separator layer.

10. A device according to claim 9, wherein said at least one separator layer comprises at least one layer of metal, polysilicon and/or single crystal silicon.

11. A device according to claim 9, wherein said at least one separator layer comprises at least one layer of interconnect material to connect the IR detectors within the array of the IR detectors.

12. A device according to claim 1, wherein each IR detector forms a pixel of the device.

13. A device according to claim 12, wherein the separator regions each provide thermal isolation between each pixel of the device.

14. A device according to claim 1, wherein each separator region is a heat sink region.

15. A device according to claim 1, wherein the IR detectors comprise any one or more of a thermopile, a resistor, transistor and a diode.

16. A device according to claim 1, wherein each IR detector comprises a thermopile.

17. A device according to claim 16, wherein each thermocouple within the thermopile comprises at least first and second dissimilar materials.

18. A device according to claim 16, wherein each thermocouple further comprises a first thermal junction, and a connection to an adjacent thermocouple forms a

second thermal junction, the first thermal junction being a hot junction and the second thermal junction being a cold junction.

19. A device according to claim 18, wherein the hot junction is located inside the pixel and the cold junction is located on the separator region, or outside the dielectric membrane.

20. A device according to claim 17, wherein at least one of the first and second materials comprises metal comprising aluminium, copper, tungsten, titanium or combination of these materials.

21. A device according to claim 17, wherein at least one of the first and second materials comprises N+ or P+ doped polysilicon, or vanadium oxide or tungsten silicide, or N+ or P+ doped single crystal silicon.

22. A device according to claim 1, wherein each IR detector comprises at least one diode, wherein said at least one diode is located in the centre of the pixel, wherein said at least one diode comprises a material comprising polysilicon or single crystal silicon.

23. A device according to claim 22, wherein each detector further comprises a reference diode coupled within the separator regions.

24. A device according to claim 1, wherein each IR detector comprises at least one transistor, wherein said at least one transistor is located in the centre of the pixel, wherein said at least one transistor comprises a material comprising single crystal silicon.

25. A device according to claim 1, wherein each IR detector comprises at least one resistor, wherein said at least one resistor is located in the centre of the pixel.

26. A device according to claim 25, wherein said at least one resistor comprises a material comprising:

metal comprising aluminium, copper, tungsten, titanium, and/or platinum;
n or p type polysilicon; and/or
n or p type single crystal silicon.

27. A device according to claim 25, wherein each detector further comprises a reference resistor located within the separator regions.

28. A device according to claim 1, wherein each IR detector comprises a thermopile in which Seeback effect and resistance change effect are used to determine IR radiation.

29. A device according to claim 1, wherein each IR detector comprises a thermopile coupled with a reference diode located at the separator regions to determine a cold junction temperature estimation which is used to determine an absolute hot junction temperature.

30. A device according to claim 1, wherein the dielectric membrane comprises:

a membrane cavity comprising vertical side walls or sloping side walls;
one or more dielectric layers comprising silicon dioxide and/or silicon nitride;
one or more layers of spin on glass, and
a passivation layer over the one or more dielectric layers.

31. A device according to claim 1, wherein the dielectric membrane is formed by any one of:

back-etching using Deep Reactive Ion Etching (DRIE) of the substrate, and

using anisotropic etching such as Potassium Hydroxide (KOH) or TetraMethyl Ammonium Hydroxide (TMAH).

32. A device according to claim 1, wherein the dielectric membrane is formed by a front-side etch to result in a suspended membrane structure, supported by at least two beams.

33. A device according to claim 1, wherein the substrate comprises any one of:

silicon;
silicon on insulator;
silicon carbide;
gallium arsenide;
gallium nitride; and/or
a combination of silicon carbide, gallium arsenide, gallium nitride with silicon.

34. A device according to claim 1, wherein the device is fabricated using a CMOS-usable metal selected from a group comprising tungsten, copper, aluminium, titanium, and molybdenum.

35. A device according to claim 1, wherein the IR detectors and the separator regions are formed using a CMOS-usable material selected from a group comprising Silicon, polysilicon and silicides.

36. A device according to claim 1, wherein the device is fabricated using a non-CMOS material.

37. A device according to claim 12, further comprising holes on each or some of the pixels.

38. A device according to claim 1, further comprising circuitry integrated on the same chip, wherein the circuitry comprise any one of switches, multiplexer, decoder, filter, amplifier, analogue to digital converter, and/or other circuitry.

39. A device according to claim 38, wherein the circuitry is placed outside the dielectric membrane area.

40. A device according to claim 1, further comprising pixel addressing circuitry on or within the dielectric membrane.

41. A device according to claim 40, where the pixel addressing circuitry comprises diodes made in polysilicon or single crystal silicon, and comprises a reference diode and/or a detector within the separator region.

42. A device according to claim 1, further comprising pixel circuitry integrated on the membrane using a silicon on insulator (SOI) technology, wherein the circuitry comprises any one of a MOSFET, a buffer and an amplifier for each IR detector of the device.

43. A device according to claim 1, wherein the separator regions within the dielectric membrane extend at least partly over the etched substrate.

44. A device according to claim 1, further comprising at least one plasmonic structure on at least some of the IR detectors.

45. A device according to claim 44, wherein said at least one plasmonic structure comprises metal comprising any one of tungsten, aluminium, copper, titanium, molybdenum, gold, platinum, or comprising silicides such as magnesium silicide or tungsten silicide, or polysilicon, single crystal silicon.

46. A device according to claim 44, wherein said at least one plasmonic structure comprises a structure repeated periodically in a lateral direction forming a repeat pattern, wherein the repeat pattern comprises a hexagonal or square shape.

47. A device according to claim 44, wherein said at least one plasmonic structure comprises a circle, ellipse, rectangular, trapezoid or a combination of different shapes, or as a pattern of holes of one or more shapes within a layer.

48. A device according to claim 44, wherein said at least one plasmonic structure on each IR detector comprises an identical shape or a different shape.

49. A device according to claim 1, wherein the device is packaged using one or more of:

a metal transistor output (TO) type package;
a ceramic, metal or plastic surface mount package;
IR filters;
a reflector;
a flip-chip method;
a chip or wafer level package;
a lens;
a printed circuity board (PCB).

50. A device according to claim 49, wherein the package is hermetically or semi-hermetically sealed with air, dry air, argon, nitrogen, xenon or any other noble gas; and/or the device is packaged in vacuum.

51. A device according to claim 1, further comprising an IR emitter formed on the same chip.

52. A device according to claim 1, further comprising a coating layer formed on top or back of the dielectric membrane, wherein the coating layer comprises carbon-black, polymer or metal black.

53. A device according to claim 11, wherein the size of each pixel is in a range from about 2 μm by 2 μm to about 600 μm by 600 μm.

54. A device according to claim 53, wherein the size of each pixel within the array is different from one another.

55. A device according to claim 2, further comprising further separator regions formed on top and/or below the dielectric membrane.

56. An infra-red (IR) detector array assembly comprising:

a plurality of IR detector array devices according to claim 1, wherein said plurality of array devices are formed on the same chip.

57. A method of manufacturing an infra-red (IR) detector array device, the method comprising:

forming a semiconductor substrate;

depositing one or more layers of polysilicon and/or metals and dielectric layers to form a two dimensional array of IR detectors and to form a plurality of separator regions;

bulk etching the semiconductor substrate to form a dielectric membrane,

wherein at least some of the plurality of IR detectors are formed on or within the dielectric membrane, and wherein said at least some of the plurality of IR detectors are separated from one another by at least some of said plurality of separator regions.

58. A method according to claim 57, wherein the separator regions comprise at least one layer which is thermally more conductive than said dielectric membrane.

59. A method according to claim 57, wherein the semiconductor substrate comprises a plain substrate comprising silicon, or a layered substrate comprising silicon on insulator (SOI) layers.

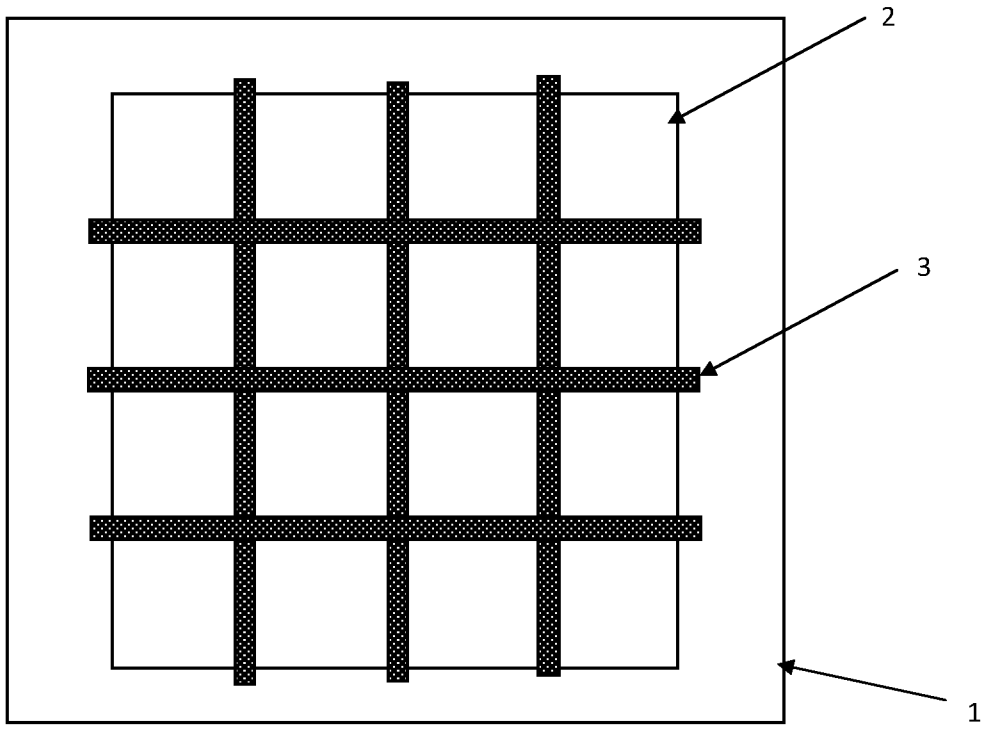


Figure 1

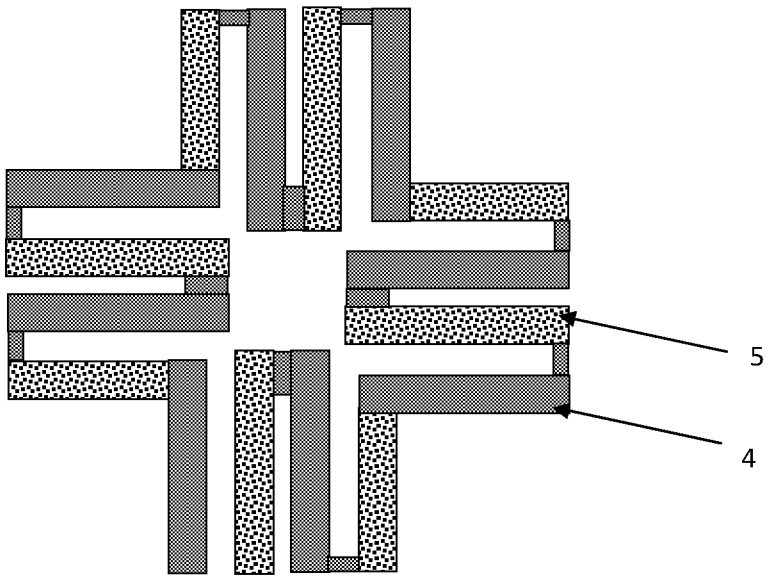


Figure 2

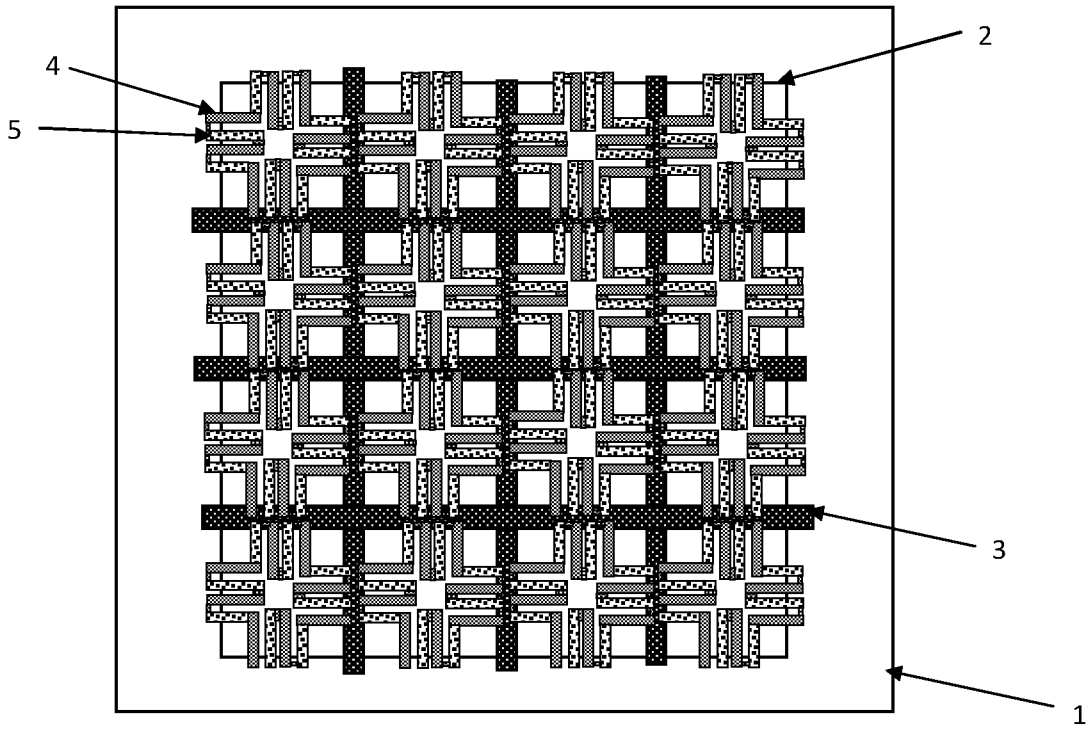


Figure 3

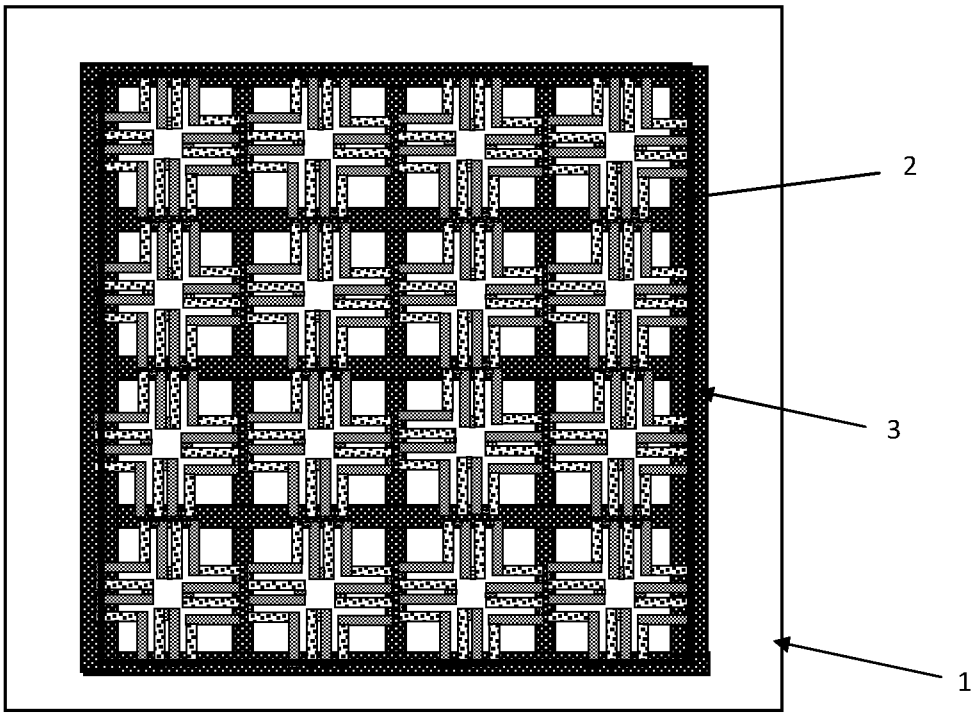


Figure 4

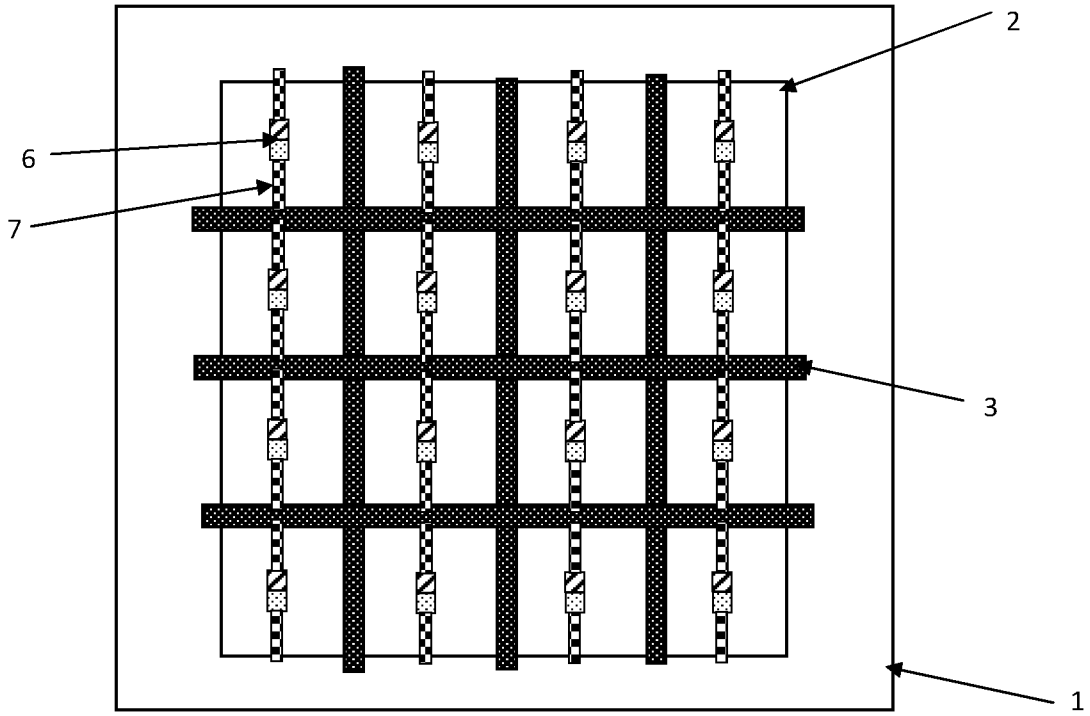


Figure 5

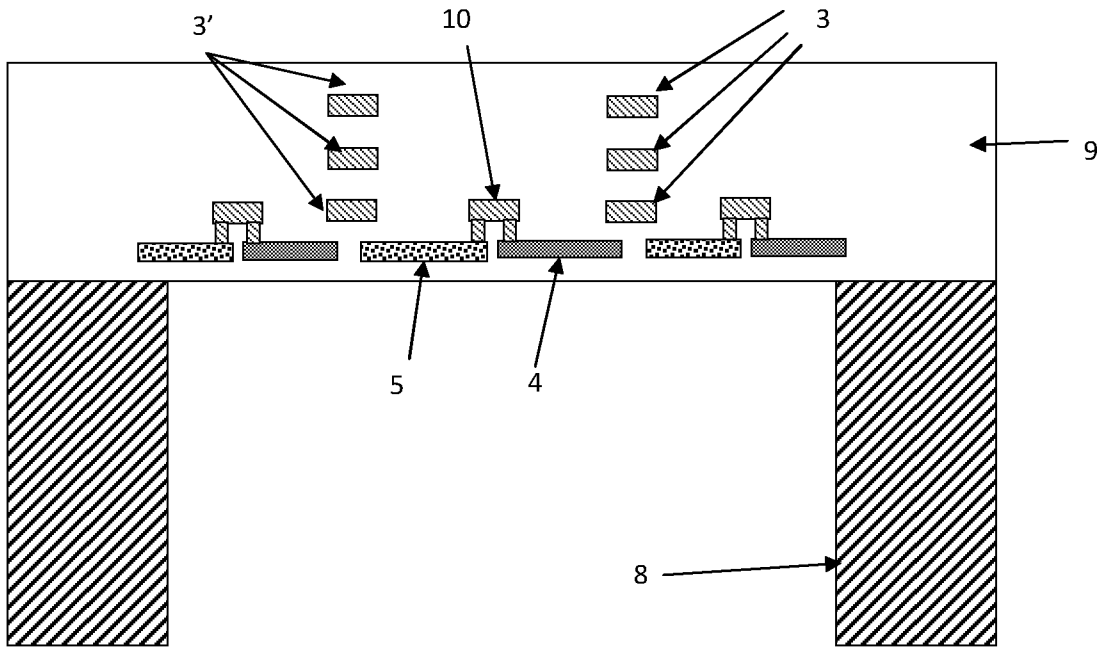


Figure 6

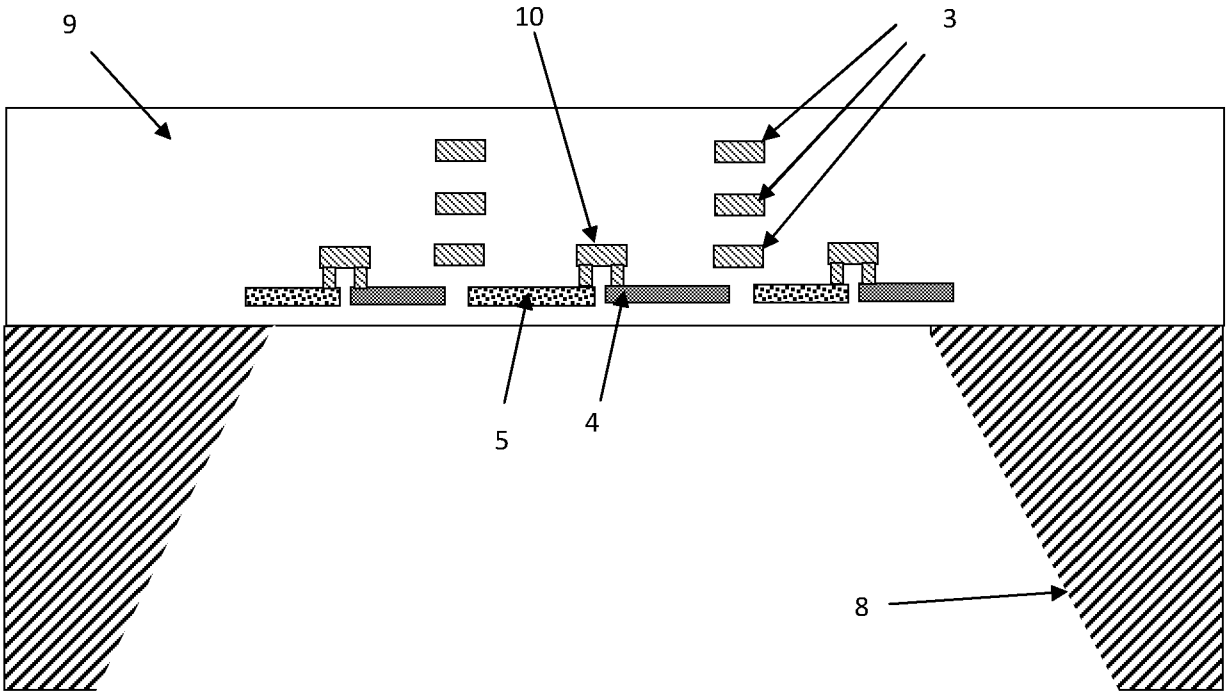


Figure 7

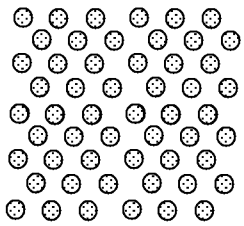


Figure 8

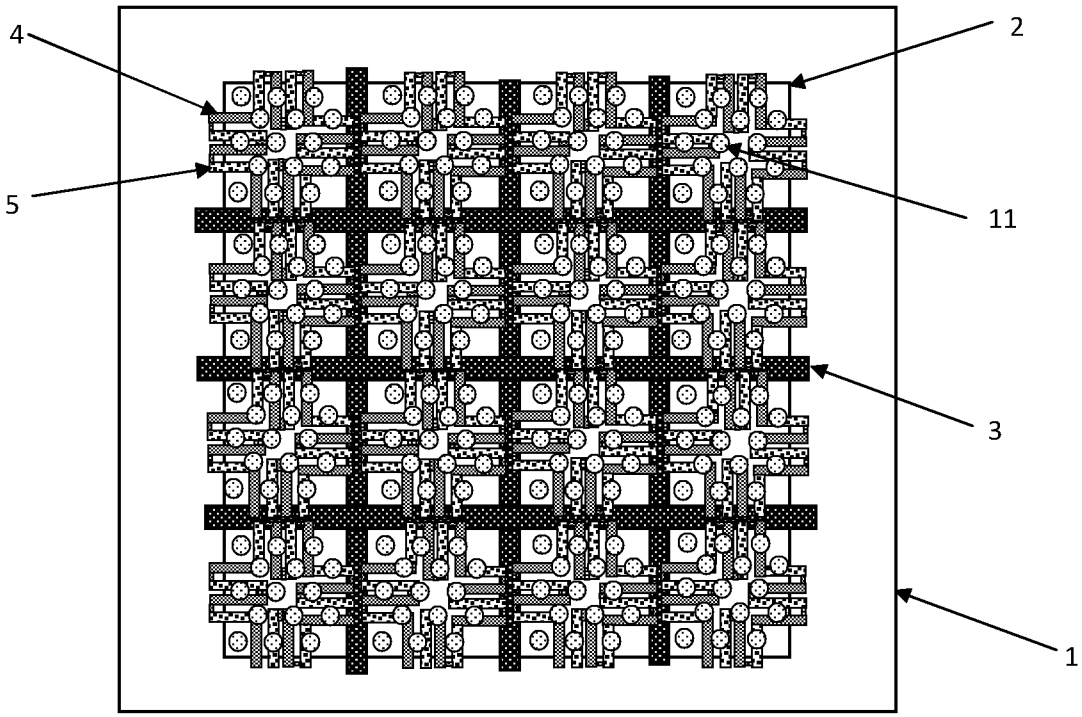


Figure 9

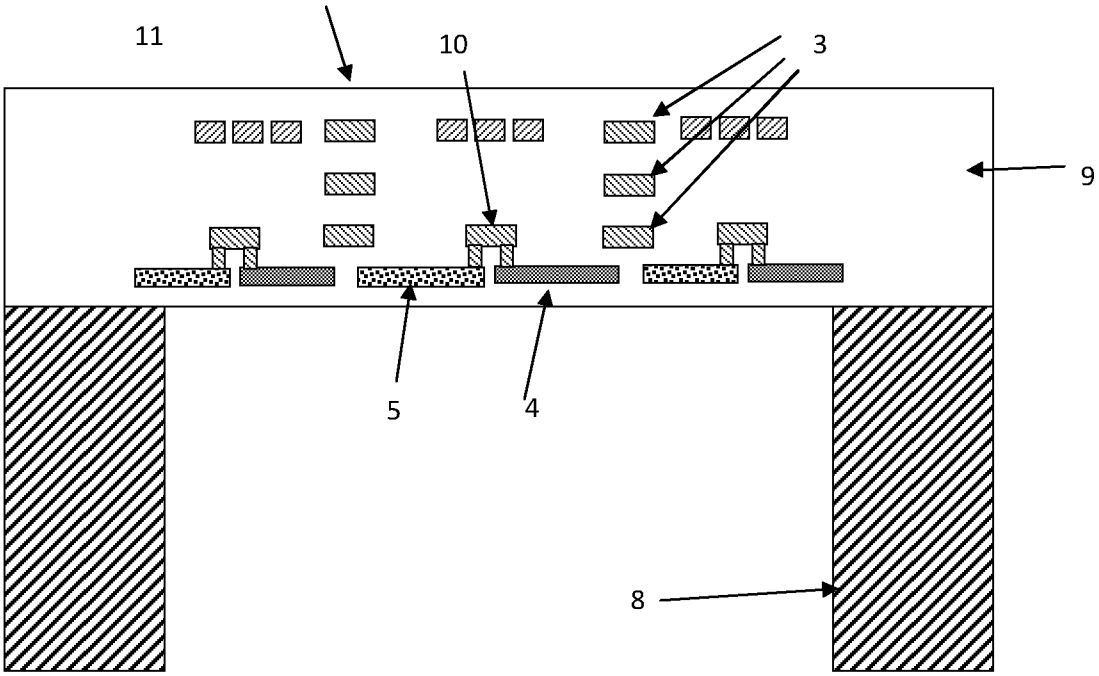


Figure 10

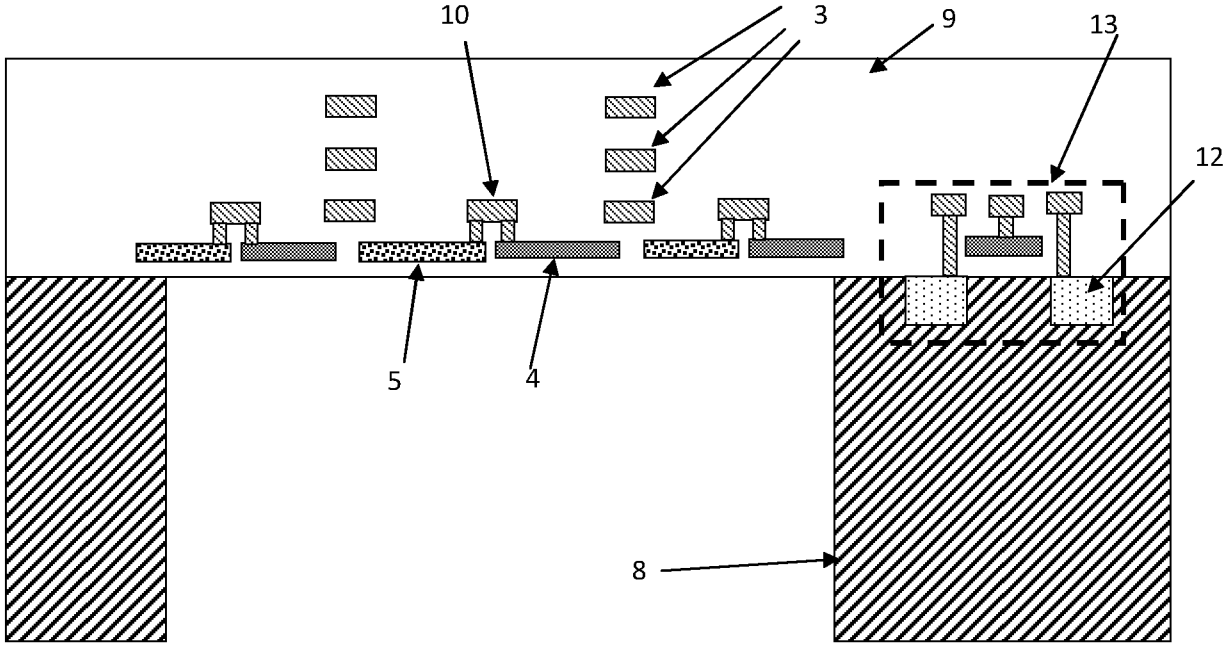


Figure 11

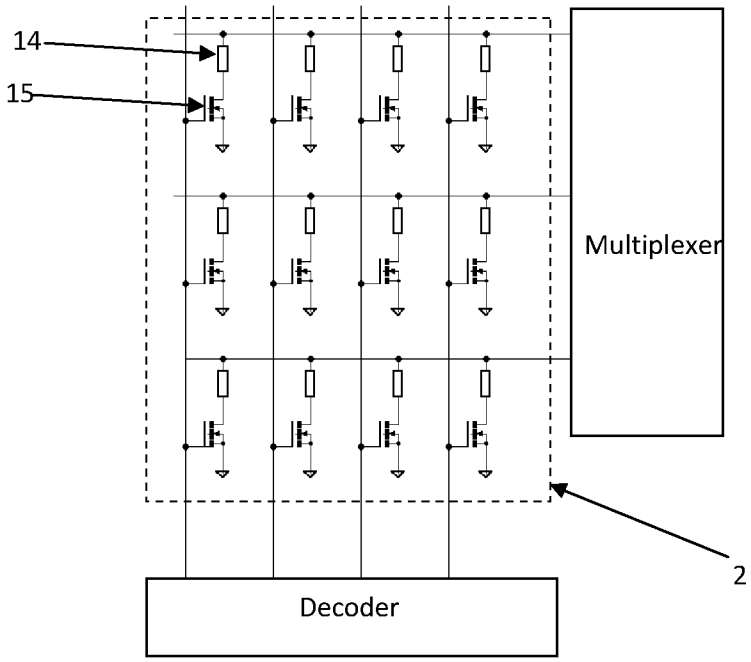


Figure 12

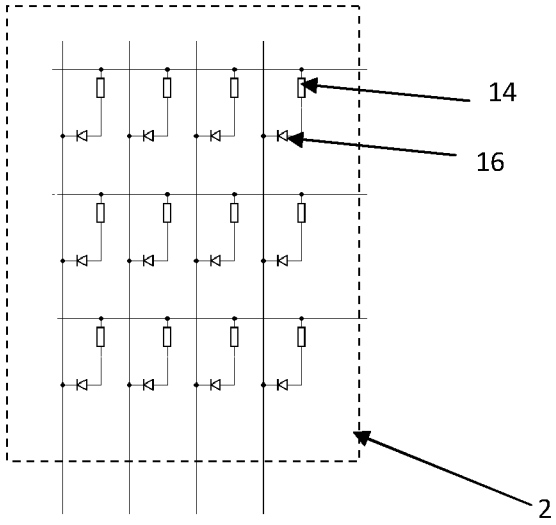


Figure 13

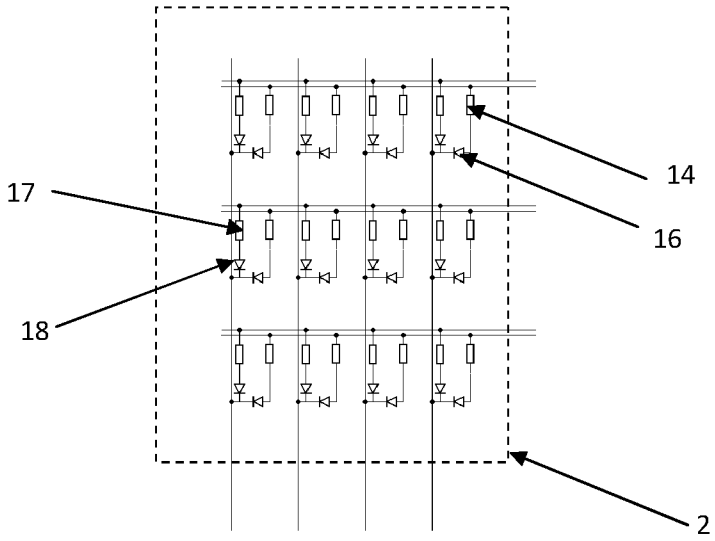


Figure 14

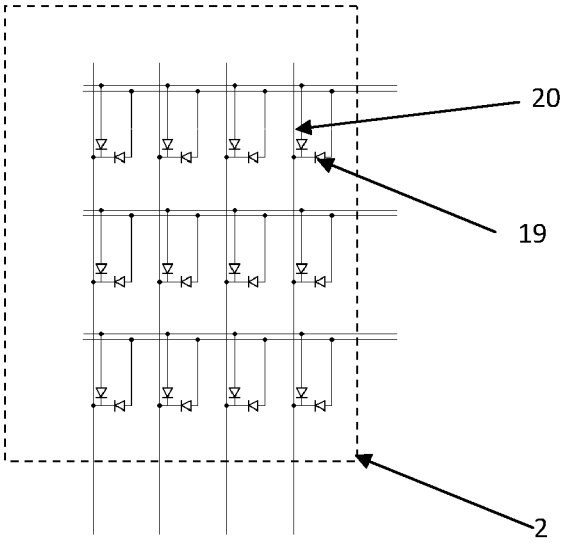


Figure 15

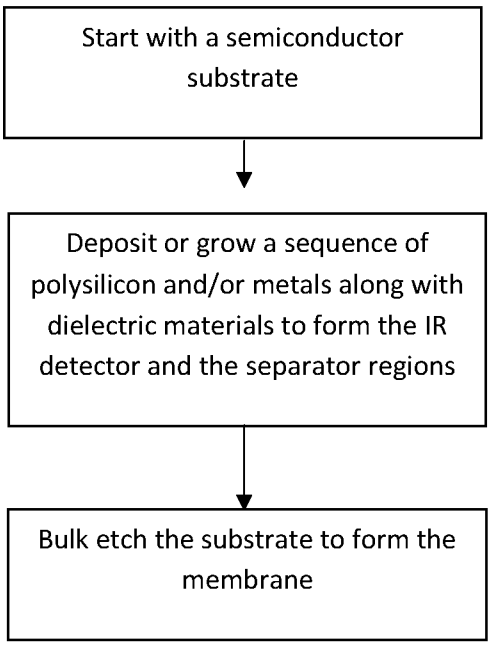


Figure 16

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/050176

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01J5/12 G01J5/02 G01J5/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 842 922 B2 (LENEKE WILHELM [DE] ET AL) 30 November 2010 (2010-11-30) cited in the application	1-21,28, 33-36, 38-40, 42,43, 53,55-59
Y	column 7, line 40 - column 8, line 48; claims 1, 2; figures 2,3	22,23, 29,41, 52,54

X	US 8 441 093 B2 (BARLOW ARTHUR J [GB] ET AL) 14 May 2013 (2013-05-14) cited in the application	1,3-7, 10, 12-19, 33-36, 43,52, 53,56, 57,59
	column 4, line 17 - column 5, line 35; claims 1, 7; figure 6	

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 May 2017	11/07/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Besser, Veronika

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/261445 A1 (SUGINO TAKAKI [JP]) 22 October 2009 (2009-10-22) paragraphs [0028], [0037] - paragraph [0055]; figures 1, 4A-4E	1,3-7,9, 12-15, 22,33, 35,36, 38-40, 42,53, 56,57,59
Y	US 8 552 380 B1 (FLORIN UDREA [GB] ET AL) 8 October 2013 (2013-10-08) column 8, line 26 - column 10, line 38; claim 27; figures 8, 18	22,23, 29,41, 52,54
A	US 2004/040592 A1 (SCHNEIDER PHILIP K [US]) 4 March 2004 (2004-03-04) paragraph [0024] - paragraph [0046]; figures 3-5	1-23,28, 29, 33-36, 38-43, 52-57
A	MENOLFI C ET AL: "256-pixel CMOS-integrated thermoelectric infrared sensor array", PROCEEDINGS OF THE IEEE 14TH. ANNUAL INTERNATIONAL CONFERENCE ON MICRO ELECTRO MECHANICAL SYSTEMS. MEMS 2001. INTERLAKEN, SWITZERLAND, JAN. 21 - 25, 2001; [IEEE INTERNATIONAL MICRO ELECTRO MECHANICAL SYSTEMS CONFERENCE], NEW YORK, NY : IEEE, US, 25 January 2001 (2001-01-25), pages 200-203, XP032403330, DOI: 10.1109/MEMSYS.2001.906513 ISBN: 978-0-7803-5998-7 cited in the application the whole document	1-23,28, 29, 33-36, 38-43, 52-57
A	OLIVER A D ET AL: "A 1024-element bulk-micromachined thermopile infrared imaging array", SENSORS AND ACTUATORS A: PHYSICAL, ELSEVIER BV, NL, vol. 73, no. 3, 30 March 1999 (1999-03-30) , pages 222-231, XP004167985, ISSN: 0924-4247, DOI: 10.1016/S0924-4247(98)00276-3 cited in the application the whole document	1-23,28, 29, 33-36, 38-43, 52-57

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 92 09 183 U1 (INSTITUT FÜR PHYSIKALLISCHE HOCHTECHNOLOGIE E.V.) 17 September 1992 (1992-09-17) the whole document -----	1-23,28, 29, 33-36, 38-43, 52-57

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2017/050176

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-14, 16-23, 28, 29, 33-36, 38-43, 52-59(completely); 15(partially)

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-14, 16-23, 28, 29, 33-36, 38-43, 52-59(completely); 15(partially)

Claim 1 concerns an infrared (IR) detector array with a two-dimensional arrangement of IR detectors on or within a dielectric membrane and, at least partly, separated by separator regions formed within the membrane. Independent method claim 57 corresponds to this device claim.
The scope of dependent claims 15 and 22 includes the IR detector comprising either a thermopile or a diode. The remaining dependent claims refer to further details.

1.1. claims: 38-42

These dependent claims concern circuitry on the periphery of the dielectric membrane and/or on or within the dielectric membrane.

1.2. claim: 52

Claim 52 concerns a coating layer on top or back of the membrane.

1.3. claim: 54

This claim concerns the size of the thermopiles, each forming a pixel, to be different from each other.

---

2. claims: 24(completely); 15(partially)

These claims concern the formation of the IR detector as transistor.

---

3. claims: 25-27(completely); 15(partially)

These claims concern the formation of the IR detector as resistor.

---

4. claims: 30-32

These claims concern different aspects of the formation of the dielectric membrane.

---

5. claims: 37, 44-48

These claims concern a plasmonic structure on at least some of the IR detectors.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

6. claims: 49, 50

These claims concern the packaging of the device using one or more of a wide diversity of specific alternatives, such as e.g. a TO type package, an IR filter, a lens etc.

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7. claim: 51

This claim concerns an IR emitter in the device.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2017/050176

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7842922 B2	30-11-2010	DE 112006000959 A5	24-01-2008
		JP 5308814 B2	09-10-2013
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