



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
09.05.2018 Bulletin 2018/19

(51) Int Cl.:
G09G 3/3225^(2016.01) G09G 3/20^(2006.01)

(21) Application number: **16197152.8**

(22) Date of filing: **03.11.2016**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
MA MD

(72) Inventors:
• **GENOE, Jan**
3001 Leuven (BE)
• **DEHAENE, Wim**
3001 Leuven (BE)
• **DE ROOSE, Florian**
3001 Leuven (BE)

(71) Applicants:
• **IMEC VZW**
3001 Leuven (BE)
• **Katholieke Universiteit Leuven**
3000 Leuven (BE)

(74) Representative: **DenK iP**
Hundelgemsesteenweg 1116
9820 Merelbeke (BE)

(54) **POWER SUPPLY LINE VOLTAGE DROP COMPENSATION FOR ACTIVE MATRIX DISPLAYS**

(57) Driving system circuitry for an active matrix display comprises: a data driver module for receiving a digital data bit stream representing an image to be displayed by pixels of the active matrix display, one or more power supply lines for powering a plurality of pixels each comprising at least one light emitting element, a voltage source connected to the one or more power supply lines, and calibration means for compensating for power drop over the one or more supply lines. The calibration means comprise means for flowing a current through an individ-

ual pixel, means for determining a voltage drop across the pixel and for comparing this to a pre-determined reference voltage for that pixel, means for determining, from the comparison, calibration values for that pixel which take into account resistance of wiring connected to the voltage source and to ground, and means for applying the calibration values to a received digital data bit stream to generate therefrom data driver voltages to be applied to the data driver module for representation of a corrected image.

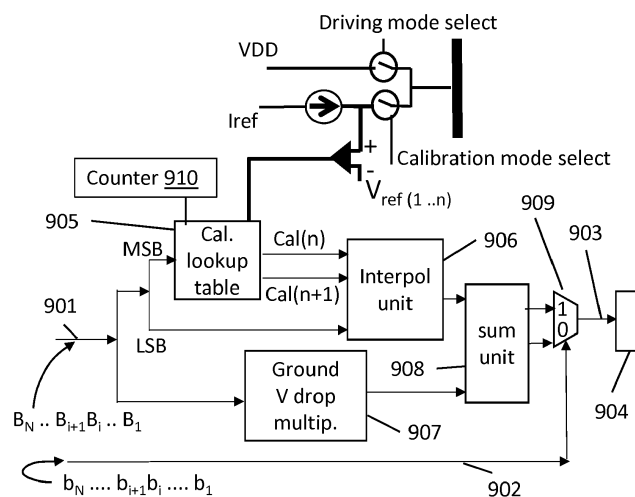


FIG. 9

Description**Field of the invention**

5 **[0001]** The invention relates to the field of active-matrix LED panels. More specifically it relates to methods for driving and compensating non-uniformities of digitally driven AMLED or AMOLED displays.

Background of the invention

10 **[0002]** Active Matrix Light-Emitting Diode (AMLED) display panels, and the version comprising organic Light-Emitting Diode (AMOLED), usually comprise three major parts: the frontplane containing the LEDs or OLEDs, the backplane with the active matrix pixel array (comprising TFTs) and the electronic drivers, usually at the edge of the display.

15 **[0003]** There is significant degradation of both frontplane and backplane during the display operation, and the production procedure for flat panel displays is not homogeneous. Lack of uniform or homogeneous manufacturing conditions seem at present unavoidable, because these non-uniformities in the displays come from various uncontrollable sources: non-uniformities in the production process (for example, variations in the dielectric thickness across the panel and interface quality of the semiconductor, deposition changes and variations of the material forming the (O)LED, etc.), non-uniformities in the materials of the matrix (e.g. grain boundaries in LTPS) and other sources. Degradation of the display can manifest in many ways: e.g. shift of the OLED characteristics (degradation due to use, degradation due to time

20 having elapsed), shift of the TFT characteristics, in general mostly dominated by bias stress (either voltage or illumination), etc. Another effect contributing in degradation and non-uniformities may rise from variations of supply and ground line resistance on the current distribution over all the pixels.

25 **[0004]** In order to compensate for the shifts and variations produced by degradation, the current in every pixel needs to be matched to the desired digital value of the pixel to be displayed. Several strategies have been developed to set the pixel current accurately. Traditional and most used techniques use fine tuning of the current in every pixel by driving the drive transistor as a current source in saturation, i.e. by applying a source-drain voltage (VDS) that is substantially larger than VGS-VT. This high source-drain voltage leads to higher power consumption, because a significant portion of the power is lost in the backplane across the drive transistor acting as a current source. Additionally, parasitic effects are usually introduced by the contact leads between sets of pixels (e.g. columns in the display) and the power source.

30 These parasitic effects (such as voltage drops) can be compensated by addition of a Digital to Analog converter (DAC) in each column. However, this increases the complexity of the circuit and introduces further parasitic effects and voltage drops. Since the current in all pixels should be equal under all circumstances for a digital (PWM) driven active matrix display, this might lead to a deterioration of the image quality.

35 **[0005]** Other techniques have been developed, which use a PWM scheme in order to set a particular brightness level in every pixel. However, this requires that the pixel current can be set very accurately to either 0 or a fixed value (based on pixel size and required display luminosity). WO2014/080014 describes how a uniform current can be achieved using a current source for every line. This, however, requires twice the number of contact pads to drive the display (thus introducing additional parasitic effects) compared to an analog driving scheme, since in that solution both the data line and the power supply have to be provided by the silicon drivers on a per-row basis. Furthermore, it requires a host of

40 current sources in the drivers, which will take up significant area of the wafer. This is suboptimal, as less pixels per unit area can be fabricated, resulting in suboptimal display resolution. Therefore, it is not a very cost-effective method for driving a display.

Summary of the invention

45 **[0006]** It is an object of embodiments of the present invention to provide a good method and device to drive an AMOLED (active matrix OLED) display or an AMLED (active matrix LED) display. It is an advantage of embodiments of the present invention that the display is driven in a uniform way so as to get good image quality.

50 **[0007]** In a first aspect, the present invention provides driving system circuitry for an active matrix display. The driving system circuitry comprises:

- a data driver module for receiving a digital data bit stream representing an image to be displayed by pixels of the active matrix display,
- one or more power supply lines for powering a plurality of pixels each comprising at least one light emitting element,
- 55 - a voltage source connected to the one or more power supply lines, and
- calibration means for compensating for power drop over the one or more supply lines.

The calibration means comprise

- means for flowing a current through an individual pixel
- means for determining a voltage drop across the pixel and for comparing this to a predetermined reference voltage for that pixel
- means for determining, from the comparison, calibration values for that pixel which take into account resistance of wiring connected to the voltage source and to ground, and
- means for applying the calibration values to a received digital data bit stream to generate therefrom data driver voltages to be applied to the data driver module for representation of a corrected image.

[0008] It is an advantage of embodiments of the present invention that correction can be performed dynamically, correcting differences in the output due to differences in transistor characteristics, differences in light emitting element characteristics, temperature changes, degradation in time, taking into account the voltage at the power supply line and ground line of several rows together.

[0009] In embodiments of the present invention, the driving system may further comprise a variable impedance, such as for example a tunable resistor, connected in series with the LED or OLED in each pixel, adapted to provide a same current flowing through every pixel upon pixel activation.

[0010] In a driving system according to embodiments of the present invention, the calibration means may comprise a memory for storing determined calibration values.

[0011] In a driving system according to embodiments of the present invention, the calibration means may comprise a reference current source connected to a feedback loop and further connected, via a "calibration mode" switching means, to the at least one power supply line.

[0012] It is an advantage of such embodiments of the present invention that the current source can be made highly accurate and can be implemented in an integrated circuit, which can be easily distributed over several data driver chips in an active matrix panel. It is an additional advantage that the internally generated voltage may be used as a reference, so the impedance matching is independent of the silicon chip.

[0013] In a driving system according to embodiments of the present invention, the calibration means may comprise an interpolation unit and ground voltage drop multiplication unit, both adapted, via a sum unit, to provide voltage regulation to the data driver module of the active matrix panel. Voltage regulation and compensation can thus be provided through data drivers already present in active matrix displays, with no need of extra current sources, DAC, etc., which saves wafer area and allows obtaining displays with high resolution. It is an additional advantage that variations of impedance due to grounding can be taken into account.

[0014] In a driving system according to embodiments of the present invention, the voltage source and calibration means may be connectable to a first side of the at least one power supply line. The at least one power supply line may further comprise a second side connectable to the voltage source via a second "driving-mode" switching means.

[0015] In a driving system according to embodiments of the present invention, the voltage source may comprise a DC/DC converter. This way, a highly efficient voltage source can be obtained, without need of ADCs or DACs and their additional voltage drops

[0016] In a second aspect, the present invention provides an active matrix display comprising an array of pixels logically organized in rows and columns, each pixel comprising at least one light emitting element, and a driving system circuitry according to any of embodiments of the first aspect of the present invention.

[0017] In an active matrix display according to embodiments of the present invention, the pixels may comprise a 2T1C structure. Such implementation has a simple layout and is easily controlled, with few components, which reduces losses.

[0018] In an active matrix display according to embodiments of the present invention, the array may be divided in two sets of pixels, each set comprising driving system circuitry according to any of the embodiments of the first aspect. It is an advantage of embodiments of the present invention that calibration of multiple pixels on different rows can be done in parallel, by duplicating the number of reference current I_{ref} sources, mode select switches and comparators.

[0019] In a third aspect, the present invention provides a method of calibrating an active matrix display comprising an array of pixels logically organized in rows and columns. The method comprises flowing a current through an individual pixel of a row of pixels of the array, determining a voltage drop across the pixel and comparing this to a pre-determined reference voltage for that pixel, determining, from the comparison, calibration values for that pixel which take into account resistance of wiring connected to the voltage source and to ground, and storing the calibration values.

[0020] In a fourth aspect, the present invention provides a method of driving an active matrix display. The method comprises receiving a digital data bit stream representing an image to be displayed on the active matrix display, applying previously determined calibration values to the received data bit stream to generate therefrom data driver voltages to be applied to a data driver module of the active matrix display for representation of an image which is corrected at least for power drop over supply lines.

[0021] In such method, the driving transistor is used as a variable impedance, more in particular as a variable (tunable)

resistor.

[0022] In such method, the calibration values may be determined according to the method of the third aspect.

[0023] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

[0024] These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

Brief description of the drawings

[0025]

FIG. 1 illustrates two exemplary embodiments of the power distribution and calibration circuit for two types of AM(O)LED displays with a single panel and a panel divided in two subsets of pixels, respectively.

FIG. 2 shows the voltage drop profiles for three implementations of connections of power supply line: connection to both sides of the panel, to a single side, and to both sides with a panel divided in two subsets of pixels.

FIG. 3 shows, in a schematic way, an exemplary embodiment comprising a variable voltage source and current sensors.

FIG. 4 shows an exemplary outline for a digitally driven display according to embodiments of the present invention.

FIG. 5 shows exemplary options for configurations of data driver wiring.

FIG. 6 shows two implementations of pixel configurations applicable to embodiments of the present invention.

FIG. 7 shows two resistive models of displays according to embodiments of the present invention.

FIG. 8 shows exemplary reference levels of voltage drops which can be calculated and used during calibration, in accordance with embodiments of the present invention.

FIG. 9 illustrates a schematic block diagram showing the calibration of the power supply line voltage drops for addressing the data driver.

FIG. 10 shows a calibration method according to embodiments of the present invention, for a single pixel.

FIG. 11 illustrates a practical embodiment of a digitally driven OLED display.

FIG. 12 to FIG. 15 illustrate simulation results.

[0026] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0027] Any reference signs in the claims shall not be construed as limiting the scope.

[0028] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of illustrative embodiments

[0029] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

[0030] The terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

[0031] Moreover, the terms top, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

[0032] It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0033] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular

feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0034] Similarly it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

[0035] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0036] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0037] OLED displays are displays comprising an array of light-emitting diodes in which the emissive electroluminescent layer is a film of organic compound which emits light in response to an electric current. OLED displays can either use passive-matrix (PMOLED) or active-matrix (AMOLED) addressing schemes. In case of OLED displays, the present invention relates to AMOLED displays. The corresponding addressing scheme makes use of a thin-film transistor backplane to switch each individual OLED pixel on or off. AMOLED displays allow for higher resolution and larger display sizes than PMOLED displays.

[0038] The present invention, however, is not limited to AMOLED displays, but in a broader concept relates to active matrix displays. Any type of active matrix displays may use the concepts of embodiments of the present invention, although AMOLED displays are particularly advantageous in view of the current switching speeds of their pixel elements. It is advantageous if the pixel elements of the active matrix displays can switch faster, as this allows to obtain higher frame rates, hence less flickering images.

[0039] An active matrix display, e.g. an AMLED or AMOLED display, according to embodiments of the present invention comprises a plurality of pixels, each comprising a light emitting element, e.g. a light-emitting diode (LED), or an organic LED (OLED) element. The light emitting elements are arranged in an array, and are logically organized in rows and columns. Throughout the description of the present invention, the terms "horizontal" and "vertical" (related to the terms "row" and "column", respectively) are used to provide a co-ordinate system and for ease of explanation only. They do not need to, but may, refer to an actual physical direction of the device. Furthermore, the terms "column" and "row" are used to describe sets of array elements which are linked together. The linking can be in the form of a Cartesian array of rows and columns; however, the present invention is not limited thereto. As will be understood by those skilled in the art, columns and rows can be easily interchanged and it is intended in this disclosure that these terms be interchangeable. Also, non-Cartesian arrays may be constructed and are included within the scope of the present invention. Accordingly the terms "row" and "column" should be interpreted widely. To facilitate in this wide interpretation, the description and claims refer to logically organized in rows and columns. By this is meant that sets of pixel elements are linked together in a topological linear intersecting manner; however, that the physical or topographical arrangement need not be so. For example, the rows may be circles and the columns radii of these circles and the circles and radii are described in this invention as "logically organized" rows and columns. Also, specific names of the various lines, e.g. select line and data line, are intended to be generic names used to facilitate the explanation and understanding, and to refer to a particular function. This specific choice of words is not intended to in any way limit the invention.

[0040] In embodiments thereof, the present invention relates to a driving circuit for an active matrix LED (AMLED) or OLED (AMOLED) display panel, allowing uniform pixel powering and thus reducing display degradation and non-uniformities. It also relates to an AMLED and AMOLED display panels, comprising driving circuitry according to embodiments of the present invention. It also relates to a method for digital driving of an AM(O)LED displays including power supply line voltage drop compensation.

[0041] In embodiments of the present invention, voltage mode digital driving is used for driving the display panels. Compensation schemes to substantially reduce or eliminate non-uniformities and degradation of both frontplane and backplane are provided, based on impedance matching at block level.

[0042] The array of pixels can be calibrated in various ways when using the voltage mode digital driving. Essentially, there is a feedback which somehow either checks or programs the current flowing in the individual pixels. The present

invention encompasses several mechanisms which are all based on this concept. As a core principle, the current in the pixel is determined by changing the pixel impedance, as also described in WO 2014/080014, which is incorporated herein by reference. The techniques described in this document can be used for the present concept as well. The impedance matching is done to eliminate variations in the TFTs and OLEDs and to compensate for the voltage drop over the lines.

[0043] In order to obtain the calibration values, a first scheme comprises monitoring the current during a calibration cycle, with a current sensor monitoring the current consumed by a single pixel. This would require activating one pixel per channel (row or column, determined by the direction of the power lines, which define the voltage drop) each calibration cycle and tuning the driving transistor, until the pixel current reaches a predetermined reference value. This would result in tuning a single pixel per current sensor during the calibration cycle. This is not the preferred scheme, because measurement data would be obtained for a lot of currents and in the digital driving methods, only a single current is needed.

[0044] A second, preferred, scheme comprises sending a current during a calibration cycle, and adapting a tunable resistor until the effective supply voltage V_{DD} for which the system is designed is reached, thus taking into account the number of pixels per row and its resistive model. An advantage of this embodiment is that the current source can be made very accurately, for instance in silicon, and that it can easily be distributed over several chips. The internally generated voltage is used as a reference, so the impedance matching is independent of the (silicon) chip.

[0045] These two options have the advantage to take into account the resistances of the wiring connected to the power source and the wiring connected to ground of several rows together, thereby reducing the number of semiconductor, e.g. silicon, contacts, as well as the number of calibration circuits in the (silicon) chip. This, however, reduces the update speed of the calibration, since less hardware is available to execute the calibration. The calibration refresh time depends on the number of pixels per calibration channel (i.e. a row or a plurality of rows taken together) and the time between pixel calibration. The time between the calibration of different pixels depends on whether the calibration is done only at startup or during the display runtime. In case of runtime calibration of digitally driven displays (and in the case the power supply lines are perpendicular to the data lines), any unused time slots within the digital driving scheme can be used for the calibration. This gives the advantage of having a perfectly hidden calibration. For example, a duty cycle as described in page 15, line 10 to page 16, line 15 of WO 2014 068017 shows that a first time slot of the first sub-frame is 0, and the rest of time slots will be either 1 (if the most significant bit is 1) or 0 (if the most significant bit is 0). Even if, for an 8-bit number, the digital signal is 11111111, the first time slot will be 0 in this type of duty cycle, as it is seen in page 16, lines 23 to 28 of the same document. Such unused time slot can be used for calibration according to embodiments of the present invention.

[0046] In one aspect, a method for digital driving and calibrating of an AM(O)LED display is provided. Embodiments of the present method can provide compensation of shift of the (O)LED characteristics (time-dependent degradation, degradation due to use) and of the TFT characteristics, which are in general mostly dominated by bias stress (either voltage or illumination bias), thus obtaining a good picture quality for an AM(O)LED display. In general for (O)LED, the current in every pixel needs to be matched to the digital value of the pixel to be displayed.

[0047] A strategy to accurately set the pixel current and to compensate for voltage drops along the power supply lines will be described in the present method. In some embodiments, a calibration value is obtained for each pixel, for example by using a reference current I_{ref} and measuring and regulating the voltage drop across the pixel, or by directly measuring the current through the pixel by means of a current sensor. Each of the calibration values required for obtaining a calibrated pixel, are stored in a calibration memory. When the AM(O)LED display is actually used, a data stream representing an image to be displayed is obtained, and introduced in a data driver for driving the active matrix in a compensated way. The AM(O)LED display is then driven, taking into account the previously determined calibration values for each pixel. Obtaining the calibration data and performing calibration and voltage corrections can be made with the same hardware block.

[0048] FIG. 4 shows an exemplary system outline for a digitally driven active matrix display according to embodiments of the present invention. It comprises image interface hardware 107, first data driver hardware 401 and optionally second data driver hardware 402 (for example data drivers which may be all or a part thereof implemented in chips), a first set of dedicated line drivers 403 and a optionally a second set of dedicated line drivers 404 (e.g. embedded line drivers) which comprise the "select" lines for selecting pixels in the array, a first "voltage distribution and voltage drop calibration" block, or "power distribution" block 109 and an optional second voltage distribution unit or block 108 according to embodiments of the second aspect of the present invention, and a pixel backplane 405. The voltage distribution unit (e.g. comprising voltage source 101 for power distribution and switch 103, 104) may form a single unit 108 (FIG. 1). The voltage distribution unit together with voltage compensation unit (e.g. the current source 106 and image interface hardware 107) may also form a compact unit 109, for example an integrated unit. In an alternative embodiment, only the unit 109 is present. The actual frontplane containing the pixels including the LEDs or OLEDs is not illustrated in FIG. 4.

[0049] During normal use of the active matrix display, i.e. during displaying of images, image input, under the form of digital data representing an image to be displayed, reaches the image interface hardware 107 through an input 406, e.g. wires or a bus. From the image interface hardware 107 control and data signals are sent to the data driver hardware

401 and optionally 402, and control signals are sent to the first and optionally second set of dedicated line-drivers 403, 404. Also, signals may come back from the voltage drop calibration block 109 towards the image interface hardware 107 as a feedback.

[0050] FIG. 5 shows two possible embodiments of data driver wiring. In the left hand embodiment 500, first data drivers 401 and second data drivers 402 are present on both sides of the display, respectively, for each controlling a subset of the pixels. For example, each data driver may control a set of data lines 501, 502 that may run until the middle of the display. In the right hand embodiment 510, only data drivers 401 are present on one side of the display and its corresponding data lines 511 run over the whole display, until the other side thereof. In both embodiments, if the drivers are fast enough, multiplexing of the data drivers can also be used. In this case, a part of the data driver block (e.g. a multiplexer) can be implemented in the display backplane technology.

[0051] Select wiring may present options similar to the ones of the data wires (data lines). They may for example run perpendicular to the data wires of FIG. 5 (this example not limiting the present invention). For example the select wires (select lines) may run from the dedicated line-drivers 403, 404 on both sides of the display up to the middle of the display, or may run from line drivers 403 on one side of the display up to the other side thereof, in which case only one set of dedicated line drivers 403 would be needed.

[0052] The active matrix display further comprises driving circuitry comprising on the one hand a set 102 powering voltage lines, which may run parallel to the select lines in some embodiments of the present invention, depending on design, or in any other suitable way, and on the other hand the voltage distribution and voltage drop calibration unit 109 and optionally the second voltage distribution unit 108. In embodiments of the present invention, power supply lines comprise both the VDD and GND connections for each pixel of the array.

[0053] FIG. 1 shows two examples for driving circuitry. The upper circuit 100 presents a voltage source 101 connected to both sides of a set of power supply lines 102 for powering the LEDs of a display. However, in some embodiments, the power source is only connected to one side of the panel. In any case, this connection may be provided by a switch, e.g. "driving mode" switch or switches 103, 104, e.g. transistors, for select (enabling or disabling) driving of the panel. Thus, the display panel can be driven with a voltage source, and this makes the introduction of a DAC in each row unnecessary, reducing the amount of components and saving space in the display, thus improving design scaling. Moreover, the display is not limited by the DAC bit resolution (which usually needs to be bigger than the number of pixels being steered). The drivers can be made simple, lowering the cost. Using a voltage source and avoiding the use of DAC brings the additional advantage that additional voltage drops from connections are reduced or eliminated. When using DAC, a certain amount of voltage drop is required in order for the DAC to operate, and this is lost power. On the other hand, the voltage source 101 can be made with high efficiency (with for example a DC/DC converter). Therefore, a driving circuit comprising a voltage source is advantageously energy saving.

[0054] During the driving mode of the display, the "driving mode" switch or switches 103, 104 are turned on and the power source VDD is connected on both sides of the power supply lines 102, and turned off when not active. During calibration, the "driving mode" is off and the "calibration mode" switch 105 is active, a unity current I_{ref} is driven through the power supply line, e.g. with a current source 106.

[0055] The lower drawing 110 of FIG. 1 shows a double driving circuit configuration, in which there are two sets of "driving mode" switches 103, 113 and "calibration mode" switches 105, 115, and two reference current sources 106, 116. They may form two integrated units 109, 119 connected to each side of the panel. This configuration may divide the rows, and each set can drive a subset of the pixels in the panel 112, e.g. each half of the pixels. The calibration and powering can be parallelized, in this configuration.

[0056] In one aspect, the present invention relates to a driving circuit for an active matrix display, such as an AM LED or AMOLED display panel. The driving circuit comprises a set 102 of power supply lines (e.g. wires, buses, other electronic pathways) for powering a group of pixels, which may be arranged as rows, each group of pixels being connected to a separate power supply line of the set 102. In particular embodiments of the present invention, where the pixels are arranged in rows and columns, all pixels on a row are connected to a same power supply line, and pixels of different rows are connected to different power supply lines. In embodiments of the present invention, as for instance illustrated in FIG. 1, a set 102 of supply lines is provided such that there is one power supply line for each row of pixels in the array. In embodiments of the present invention, the power supply lines comprise both the lines connected to the source VDD and lines connected to ground GND. In embodiments of the present invention, a voltage source VDD is used to supply the panel. The voltage source VDD can be connected to or disconnected from both sides of the set 102 of power supply lines, via switches 103, 104, 113.

[0057] During the "normal driving" mode of the display, a signal labeled "driving mode select" is active, closing the switches 103, 104, and the power source VDD is connected on both sides of the set 102 of power supply lines. When "driving mode select" is not active, the power source VDD is disconnected from both sides of the set 102 of power supply lines. Due to the fact that the display can be powered with a voltage source, despite the fact a current source is needed, there is no need to include current mode Digital-to-Analog converters (DACs) for all the rows. This also improves scaling of the design, because for bigger displays, a larger number of pixels needs to be supplied from these DACs, and the

accuracy of the DACs needs to be bigger than the number of pixels being steered. Moreover, a further advantage of using a voltage supply is the elimination of the voltage drop within the current DAC. The voltage source can be made with high efficiency (with for example a DCDC convertor). In the current DAC, a predetermined amount of voltage drop will be required in order for the DAC to operate, and this is lost power. Therefore, the use of a voltage source as in

accordance with embodiments of the present invention is a better solution from a power perspective.

[0058] When "calibration mode select" is active, another switch 105 is closed, and a unity current I_{ref} is driven through a power supply line. Hereto, a reference current source is provided at one side of the set 102 of power supply lines. This is used for calibration, as explained in more detail below. A voltage is measured at the same side of the power supply line where the current is injected, and this measured voltage is sent to a comparator unit where it is compared with a set of reference voltages $V_{ref(i)}$, with i going from 1 to p , p being the number of reference voltages having been predefined for the calibration. The result of this comparison is provided to the digital logic in the image interface hardware 107.

[0059] Due to the reduced degradation of illumination in active matrix displays, e.g. LED or OLED panels of the present invention, pixels may comprise a relatively simple configuration such as 2T1C (a circuit with 2 transistors and 1 capacitor), as shown in FIG. 6.

[0060] However, the present invention is not limited to 2T1C configurations, and other configurations (e.g. 4T2C, 5T2C, 6T2C) may also be applied for keeping the TFT voltage threshold shift very low, thus reducing variations in pixel luminance.

[0061] The present invention can be applied to p-type as well as n-type transistors and to driving circuitry comprising any type of back-plane, e.g. comprising for instance hydrogenated amorphous Si (a-Si:H), polycrystalline silicon, organic-semiconductors, (amorphous) indiumgallium zinc oxide(a-IGZO, IGZO) TFT, or others.

[0062] FIG. 6 shows two basic configurations for pixel structures of an AM(O)LED display according to embodiments of the present invention. The illustrated embodiments are 2T1C (2 transistor, 1 capacitor) configurations, but any other suitable configuration can be applied. The pixel structures comprise a LED or an OLED 601 connected in series with a drive transistor M1. The (O)LED 601 can either be coupled between ground line 603 coupled to ground GND and transistor M1, as shown in the left hand part of FIG. 6, or between the power supply line 604 coupled to the power supply V_{DD} and the transistor M1, as in the right hand part of FIG. 6. The sum of the voltages over the (O)LED and transistor M1 results in the voltage over the pixel. The transistor M1 acts as a switch for powering the (O)LED 601 with power from the power supply line 604. The select transistor M2 connects a data line 606 with the gate of the drive transistor M1. The gate of the select transistor M2 is connected to a select line 607, which is shown as running parallel to the power supply line 604 and the ground line 603. The select lines 607 run perpendicular to the data lines 606. The capacitor C1 is connected between gate and source of drive transistor M1.

[0063] In an AM(O)LED display, a plurality of such pixels as represented in FIG. 6 may be logically arranged in rows and columns. Pixels arranged in a same column may be connected to a same data line 606, and pixels arranged in a same row may be connected to a same select line 607.

[0064] The voltages, currents, impedances and related parameters used for calibration in each pixel will have different values depending on the position of each pixel in the row, because the resistance between the power source and each pixel depends on its position in the row due to contact leads, contacts between pixels, etc.

[0065] Embodiments of the present invention provide impedance matching per pixel, during normal use of the display, i.e. during displaying of an image. Hereto, firstly the voltage over each pixel is measured while a reference current is introduced in that pixel according to predetermined calibration schemes, as will be set out below, and then the current is controlled in each pixel via impedance matching to eliminate variations in the active matrix and (O)LEDs and to compensate for voltage drop over the rows. Impedance matching is realized for each pixel by tuning a variable impedance connected in series with the LED or OLED of the pixel. In embodiments of the present invention the driving transistor of each pixel is used as a variable resistor. FIG. 7 shows that each pixel in a row is subject to a voltage drop which depends on the position (n) of the pixel in the row of N pixels, because the resistance in series between the pixel and the connection to the power source increases with increasing distance to the power source.

[0066] Two possible configurations of a pixel row connected to the power supply line 604 are shown in FIG. 7, together with the resistances between pixels, in a resistive model. The upper implementation of FIG. 7 illustrates a resistive model for a row of pixels driven from both sides, while the lower implementation illustrates a resistive model of a row of pixels driven from a single side. Between two neighboring pixels, each comprising a (O)LED 601, 611 (only the LED and the drive transistor M1 of each pixel is shown), in a row with N pixels, power supply line resistance $R1$ (between neighboring pixels) and a ground line resistance $R2$ (between neighboring pixels) are present. These resistances $R1$, $R2$ originate from the metal wiring, and they can be well known (e.g. modelled, measured, etc.). They can be calculated from the layout.

[0067] The sum of the resistance between two pixels in the power supply line and in the ground line is the reference resistance, $R1+R2=R_{ref}$. Typically the wiring to the external power source V_{DD} and to ground GND will have a larger resistance R_{S1} , R_{S2} , resp., than the inter-pixel wire resistances $R1$ and $R2$. The ratio M is defined as the resistance ratio with respect to the internal pixel resistance. R_{S1} and R_{S2} are typically defined by:

$$R_{S1} + R_{S2} = M R_{ref} = M(R_1 + R_2)$$

[0068] The upper implementation 700 in FIG. 7 comprises power supply lines contacted from both sides, thus the pixels at the extremities of the row are connected to the power source VDD. The resistive voltage drop for this case (power supply lines contacted to the power source VDD at both extremities) is illustrated in FIG. 8. FIG. 8 illustrates 3 cases: graph 201 - no (O)LED is on, graph 202 - a typical distribution of (O)LEDs along the row are on, and graph 203 - all (O)LEDs along the row are on. It can be seen from these graphs that the power drop on the power supply lines increases with increasing number of pixels being switched on between the connection point of the power supply line to the power source, and the pixel at location n under consideration.

[0069] The resistive voltage drop for the case the power lines are contacted from both sides may be calculated as herein below.

[0070] During calibration, a current source, e.g. the current source 106 of FIG. 1, introduces a current through a power supply line, by opening of the switches 103, 104, closing of the switch 105 and routing of the current by means of the power distribution blocks 109, 108. Thus, during calibration, only one pixel per current source is on at a time (the pixel being calibrated), the rest of pixels in the row being turned off. If two or more reference current sources (106, 116) were used, it would be possible to calibrate two or more pixels at the same time. The resistive voltage drop over the pixel at location n in the row of N pixels (the pixel number n being a number between 1 and the total number of pixels on the row, being N) is obtained from the injected reference current I_{ref} .

[0071] The current flowing in the row is firstly calculated at the pixel in position n, as a function of the current at the contact I_0 and the binary code b_i (b sub i) that defines when a pixel is ON (and hence draws the current I_{ref}). The algorithm hence uses a stream of N bits from a row of the image data. This stream of N bits is $b_N \dots b_{i+1} b_i \dots b_1$.

$$I_n = I_0 - \sum_{i=1}^n b_i I_{ref}$$

The resistance of the wiring between two pixels R_{ref} defines the voltage drop ∂V_n between two pixels.

$$\partial V_n = R_{ref} I_n = R_{ref} (I_0 - \sum_{i=1}^n b_i I_{ref})$$

When all these voltage drops are summed until pixel n and the voltage drop at the contact lead with resistance $R_s = R_{s1} + R_{s2}$ is added, the equation for the voltage drop until pixel n is obtained:

$$\Delta V_n = R_s I_0 + \sum_{j=1}^n \partial V_j = (M + n) R_{ref} I_0 - R_{ref} I_{ref} \sum_{j=1}^n \sum_{i=1}^j b_i$$

In this expression the factor M is introduced as the ratio between R_s and R_{ref} : $R_s = M R_{ref}$. However, I_0 has to be determined from the fact that the voltage at the last position N corresponds to the resistive drop over the other power contact wire:

$$\Delta V_N = -R_s I_N = -M R_{ref} I_N$$

This translates to:

$$(M + N) R_{ref} I_0 - R_{ref} I_{ref} \sum_{j=1}^N \sum_{i=1}^j b_i = -M R_{ref} (I_0 - \sum_{i=1}^N b_i I_{ref})$$

$$(2M + N) I_0 - I_{ref} \sum_{j=1}^N \sum_{i=1}^j b_i = M \sum_{i=1}^N b_i I_{ref}$$

$$(2M + N) I_0 = I_{ref} \sum_{j=1}^N (M b_j + \sum_{i=1}^j b_i)$$

Substituting I_0 in the equation of ΔV_n results in:

$$\Delta V_n = R_{ref} I_{ref} \left(\frac{M+n}{2M+N} \sum_{j=1}^N (M b_j + \sum_{i=1}^j b_i) - \sum_{j=1}^n (\sum_{i=1}^j b_i) \right)$$

The voltage drop is thus expressed in units of $R_{ref} I_{ref}$. The only constant needed in the calculation is the number M as defined above ($M = \frac{R_{S1}+R_{S2}}{R_1+R_2}$). This number M is dependent on the geometry of the layout of the external wiring to the display. When there are more than 1000 pixels in a row, the precision with which the voltage drop is calculated is less than a microvolt. Due to this high precision, some of the least significant bits can be disregarded at the final outcome. **[0072]** The calculation of the voltage drop can for instance be done in two steps. In a first step, a number A_N is calculated:

$$A_N = \frac{1}{2M+N} \sum_{j=1}^N \left(M b_j + \sum_{i=1}^j b_i \right)$$

This number A_N may be calculated one row ahead of the actual driving during operation. Hence the number A_N for row $x+1$ is calculated during driving of row x . With A_N , a binary number representing the voltage drop in the power line at each pixel, B_n , can be obtained. This number can be calculated in real time, for every pixel of row $x+1$, taking into account the previously calculated value for A_N , while loading the data to the first and/or second data driver hardware 401, 402:

$$B_n = (M+n)A_N - \sum_{j=1}^n \left(\sum_{i=1}^j b_i \right)$$

[0073] The expression for the voltage drop can be separated in two terms A_N and B_n , each of which can be calculated iteratively.

[0074] The value $A_N = \frac{1}{2M+N} \sum_{j=1}^N (M b_j + \sum_{i=1}^j b_i)$ can be calculated in a hardware block. This hardware block may be present in the image interface hardware 107. It may comprise one counter and two adders. The algorithm implemented this way may look as follows
Iteration:

```

s0=0
p0= 0
Loop (i,1,N)

    Si= Si-1+ bi
    pi= pi-1+ si
    if (bi=1): pi= pi+ M

End loop

```

$$A_N = C * p_i \text{ with } C = 1/(2M+N)$$

The result of the iteration can be multiplied by the constant $C=1/(2M+N)$ at the end, but this constant C can be calculated upfront, which enables a compact multiplication. In total, this is a very compact hardware block. The result is only provided at the end of the row.

[0075] Once the value A_N is acquired, the set of terms $B_n = (M+n)A_N - \sum_{j=1}^n (\sum_{i=1}^j b_i)$ representing the power line voltage drop at each pixel in a row can be calculated in realtime also in a hardware block (which also may be present in the image interface hardware 107). It may comprise one counter and two adders and a multiplier. In total this is a very compact hardware block. The algorithm implemented this way may look as follows:

Iteration:

$$s_0=0$$

$$p_0= M \cdot AN$$

Loop (i,1,N)

$$s_i= s_{i-1}+ b_i$$

$$p_i= p_{i-1}- s_i$$

$$p_i= p_i+ A_N$$

$$B_i=p_i$$

End loop

This loop defines the different values of B_n .

[0076] FIG. 8 illustrates how, in accordance with embodiments of the present invention, the power line voltage drop reference levels $V_{ref(1..N)}$ are defined. The maximum (graph 203) and minimum (graph 201) power line voltage drops are known (they are calculated exactly from the values of the resistances and the imposed reference current I_{ref}), and in between a set of equally spaced voltage drop reference levels 801 that can occur during operation are defined (the number of levels is defined by the required accuracy or maximum cost of the system). For convenience, the levels corresponding to the most significant bits (MSBs) of the B_n numbers calculated are defined. For each voltage drop level defined in 801 and for each pixel, a calibration will be done during the calibration phase of the display. During calibration binary values are obtained which (if they are provided to the data driver) generate a voltage on the gate of the drive transistor such that over the pixel the previously determined reference voltage is obtained. For each MSB of B_n a reference voltage is provided. The LSBs are obtained by interpolation.

[0077] As a particular example, it is considered B_n is a binary number representative of the voltage drop for a bit string in a pixel n , and for example three MSBs are chosen. This choice determines the number of voltage drop reference levels, which, for the three MSBs, corresponds to eight voltage drop reference levels 801. During calibration, only one pixel (per current source 106, 116) is ON in the row, and only eight possible voltage drops are measured. The value "000" corresponds to no resistive drop (case of minimum drop 201), and the value "111" corresponds to the maximal resistive drop, only obtained in the middle of the maximum drop diagram 203. In the memory of the interface hardware 107, a calibration voltage value for each pixel and for each of the eight levels is stored. The actual B_n numbers comprise a string longer than their three MSBs. Thus, the real value used for calibration is a linear interpolation between the relevant pixel n and the next pixel $n+1$. The rest of the string (the least significant bits) can be used to improve interpolation.

[0078] It is noted that, for each pixel, all calibration levels are obtained in order not to affect the hardware speed, even if theoretically the pixels closer to the power source, e.g. at the sides of the display in FIG. 8, will not reach all possible reference levels.

[0079] FIG. 10 shows the calibration method for one pixel, similar to method the method disclosed on page 13, line 23 to page 14, line 10 of WO2014/080014. During calibration, the display is thus driven row by row (activation of select transistor M2 by line drivers 403, 402, and flowing the reference current I_{ref} through the power supply line). The reference current I_{ref} is only applied in a pixel row through one single active pixel, keeping the rest of pixels of the row inactive. Because I_{ref} is injected through both the (O)LED and the transistor M1, the total voltage is the sum of the voltage over the (O)LED, V^* , and the voltage over the transistor, between V^* and the voltage over the pixel V_L at that I_{ref} . The voltage at the gate of the drive transistor M1 of the active pixel is set at its lowest relevant value for the switch formed by the drive transistor M1 to be ON, and, as a consequence, the voltage V_L over the pixel is higher than the supply voltage V_{DD} . Increasing the voltage at the gate of the transistor results in a lower V_L . The gate voltage is increased until the voltage over the pixel is the same as the supply voltage. Thus subsequently, the voltage at the gate of drive transistor

M1 is step by step increased until the power voltage V_L^* (= supply voltage V_{DD}) is obtained as the voltage over the pixel. This value corresponds to the minimal voltage drop in the power supply line, e.g. V_{DD} , usually taking place in the pixel at the beginning of the power supply line, i.e. directly connected to the power source. This value is stored in the calibration memory of the pixel as the minimum power line voltage drop. The process can be described as a gate voltage sweep during calibration, shown by the arrow 1001 in FIG. 10. This is performed for each pixel until all power supply line voltage drop reference levels are obtained and stored in the calibration memory. Hence, for each pixel the delta for n voltage drop calibration levels are stored in the calibration memory of the pixel. One of the differences with the method of WO2014/080014 is that the pixel is now driven by a voltage source, and the calibration values can be used for voltage regulation directly on the data line.

[0080] Calibration of multiple pixels on different rows in parallel can be done by duplicating the number of reference current I_{ref} sources, mode select switches and comparators as illustrated in FIG. 1.

[0081] FIG. 9 shows how the actual data driver can be addressed. This hardware block may be present inside the image interface hardware 107. It has two input data streams: the power supply line voltage drop 901 ($B_N \dots B_{i+1} B_i \dots B_1$) and the digital data bit stream 902 ($b_N \dots b_{i+1} b_i \dots b_1$) representing the image to be displayed. As output, a stream of data driver voltage values 903 $D_N \dots D_{i+1} D_i \dots D_1$ is obtained and can be introduced in the data driver module 904 of the active matrix panel display. For each pixel, the most significant bit (MSB) of the power supply line voltage drop values are sent to the calibration memory 905. The calibration value for the voltage drop of pixel n and the calibration value for the voltage drop of the next pixel n+1 are provided to an interpolation unit 906. The least significant bits (LSB) of the same voltage drop of pixel n are also provided to the interpolation unit 906 and enables to do an accurate interpolation between both calibrations.

[0082] In both cases, the influence of the ground line voltage drop can advantageously be taken into account in the calculation of the voltage drop, for example, to drive the gate of the transistor M1 (see FIG. 6) which controls the powering of the LED. Typically, the ratio between ground line voltage drop and the total power supply line voltage drop is known (usually it is half), so the ground line voltage drop is obtained in the multiplication unit 907 by the multiplication with this known ratio. This voltage needs to be added in the sum unit 908 to the voltage driven to the gate of M1. Finally, based on the digital data bit stream ($b_N \dots b_{i+1} b_i \dots b_1$), the output multiplexer 909 selects the output, which is the calculated gate voltage when the bit is '1', and 0 when the bit is '0'.

[0083] The same module can be used during the calibration procedure. A counter 910 may be included for regulating the calibration process and/or storing the values in the calibration memory. The counter 910 is at the beginning of the calibration procedure set at a value corresponding to the lowest possible gate voltage, and when the obtained pixel voltage is higher than the first reference voltage, the corresponding counter value is stored in the first calibration value address. As the calibration value is also applied to the MSB input of the calibration lookup table 905, its value is also obtained at the output. During calibration, the LSB bits are set to zero (thus disabling interpolation), and the digital data stream 902 is set to '1', thus turning each pixel on, giving the requested data driver voltage at the output. This increases until the requested reference voltage is obtained. This is subsequently done for all reference voltages.

[0084] The calibration per pixel shown in FIG. 10 can be done for each pixel in a recursive manner, including storing the values in the memory 905 (e.g. lookup table) of the calculation unit of FIG. 9.

[0085] The relationship between the power supply line voltage drop and the required gate voltage (the voltage introduced through the data line for controlling the gate of M1) has a $1/(a-x)$ behavior, with "a" being larger than the maximal power supply line resistive drop as illustrated in FIG. 8. This would require multiple calibration reference levels to accurately perform calibration. However, the data driver can be advantageously implemented with $1/(a-x)$ behavior, thus reducing the required number of calibration levels and increasing the accuracy. This correction can be implemented occasionally (e.g. periodically) by tweaking the gamma response curve that can be implemented in some existing display data drivers. The regulation of the gamma curve is known in the art, for example it can be implemented as interpolation of values that can be uploaded by software, and it can be readily integrated within embodiments of the present invention.

[0086] The power line voltage drop along the row of N pixels, for an exemplary sequence of driven pixels on and off, is shown in graph 202 in FIG. 8, and the upper leftmost drawing 200 of FIG. 2, for a row of pixels being driven from both sides. The pixel number n is a number between 1 and the total number of pixels on the row, being N. The algorithm may use a stream of N bits from a row of the image data as defined in the prior art, for example in document WO2014068017A1. This stream of N bits is $b_N \dots b_{i+1} b_i \dots b_1$. These bits may represent pixel intensity data representing the image.

[0087] The connections between the pixels, between pixels and power source, and between pixels and ground GND are conductive connections, typically metallic connections and leads, which present electric resistance and generate a voltage drop along the rows, which voltage drop depends on the position of the pixel. Pixels close to the center of the display (e.g. farther away from the connection with the power source) will show, on average, higher voltage drop than pixels close to the source. FIG. 2 shows the voltage drop profiles for the minimum drop 201 (all (O)LEDs are off), a typical drop 202 (few (O) LEDs are on, others off), and maximum drop 203 (all (O) LEDs are on) for three cases:

- in the upper left drawing 200 for the embodiment in which the power supply line is connected from both sides to the

voltage source 101 (e.g. for the embodiment 100 of FIG. 1 with connection to the power source in both sides), both sides of the profiles end in the voltage level VDD.

- in the upper right drawing 210, the power supply lines are not connected from both sides but only from one side. The single side alternative is advantageous in practical implementations when power cannot be connected at both sides of the display. However, the voltage drop is usually high.
- in the lower drawing 220, a double driving circuit is used. In this alternative, power VDD and ground GND lines are not connected on both sides of the panel, rather the panel is divided, each division comprising only one connection to the voltage source and GND. This embodiment divides the power supply lines in two parts. The voltage drop profile corresponds to the lower drawing 110 of FIG. 1. It needs twice the amount of calibration units and presents high voltage drops, but it requires less calculations. Under certain circumstances, the power and ground voltages may not be equal in the middle of the power supply lines (not even the maximum voltage drop; especially the maximum voltage drop may be very different if each subset do not comprise the same number of pixels and, thus, resistors, as explained with reference to FIG. 7). This embodiment has the advantage that it requires slightly lower amount of calculation, but can have (under some conditions) higher voltage drops. It also doubles the amount of calibration units.

[0088] In case the power supply lines are only contacted from one side (corresponding to the graph in the upper right drawing 210 of FIG. 2, the corresponding resistive model is illustrated in the lower implementation 710 at the bottom of FIG. 7. The resistive voltage drop may be calculated in a similar process as before. The current flowing in the row is firstly calculated as before, at position of pixel n as a function of the current at the contact I_0 and the binary codes b_i that define when a pixel is on and hence draws the current I_{ref} :

$$I_n = I_0 - \sum_{i=1}^n b_i I_{ref}$$

The voltage drop ∂V_n between two pixels is defined with the resistance R_{ref} of the wiring between two pixels.

$$\partial V_n = R_{ref} I_n = R_{ref} (I_0 - \sum_{i=1}^n b_i I_{ref})$$

When all these voltage drops until pixel n are summed and the voltage drop at the contact lead is added, the equation for the voltage drop until pixel n is obtained, being:

$$\Delta V_n = R_S I_0 + \sum_{j=1}^n \partial V_j = (M + n) R_{ref} I_0 - R_{ref} I_{ref} \sum_{j=1}^n \sum_{i=1}^j b_i$$

[0089] In this, the factor M obtained as before is introduced as the ratio between R_S and R_{ref} ($R_S = M R_{ref}$). The current I_0 still needs to be determined, but taking into account that the current at the end of the power supply line: $I_N = 0$, this translates into

$$I_0 = \sum_{i=1}^N b_i I_{ref}$$

and thus:

$$\Delta V_n = (M + n) R_{ref} \sum_{i=1}^N b_i I_{ref} - R_{ref} I_{ref} \sum_{j=1}^n \sum_{i=1}^j b_i$$

$$\Delta V_n = R_{ref} I_{ref} \left((M + n) \sum_{i=1}^N b_i - \sum_{j=1}^n \sum_{i=1}^j b_i \right)$$

[0090] As before, two units can be used for sequential calculation of AN and B_i for each pixel on a row of the display. The unit that calculates AN for such embodiment may comprise only a counter (or two counters for the parallelization of the calculation, if the panel is driven by two voltage sources and two calibration units, as illustrated in the lower drawing 110 of FIG. 1).

$$A_N = \sum_{j=1}^N (b_j)$$

[0091] Iteration:

$s_0=0$
Loop (i, 1, N)

$s_i = s_{i-1} + b_i$

End loop
 $A_N = s_i$

[0092] The unit that calculates B_n for such embodiment comprises only a counter and two adders (which may be duplicated for parallelization in a double configuration, as illustrated in the lower drawing 110 of FIG. 1). As such these are very compact hardware implementations.

$$B_n = (M + n)A_N - \sum_{j=1}^n \left(\sum_{i=1}^j b_i \right)$$

The iteration is equivalent to the previous example of iteration for B_n .

[0093] Thus in summary, the bit stream of data, comprising a bit b per pixel in a row of N pixels, is used to calculate the parameter A_N . Then both the bit stream and the parameter A_N are used to calculate a voltage drop per pixel (thus, N voltage drops) for that bit of data.

[0094] In alternative embodiments of the present invention, during calibration the voltage can be swept and the current can be directly measured by means of a current sensor, using the configuration of a current source and an ADC (as it is shown in of FIG. 3). The current sensor would monitor the current through a single pixel during a calibration cycle, and the drive transistor acting as a tunable resistor can be used to tune the current until the pixel current is the same as the reference pixel current. FIG. 3 shows an embodiment comprising a variable voltage source 301, so the voltage can be swept during calibration, and current sensors 302, 303 for measuring the current. This implementation is compatible with driving circuits with double connection to the voltage source (upper drawing 100 of FIG. 1) or double driving circuits (lower drawing 110 of FIG. 1). The implementation of FIG. 3 requires complex and accurate Analog to Digital converters (ADC) 304, 305, as well as double sweeping during calibration because both the gate voltage of M1 and the VDD need to vary, to get the accurate current through the pixel. In yet an alternative embodiment, the power is connected to only one side of the display, and the driving circuit comprises a single current sensor 302 and single ADC 304.

SIMULATION RESULTS

[0095] To evaluate the operation and timing, as well as the effectiveness of the calibration method of embodiments of the present invention for digitally driven displays, calibration has been simulated for one line using the analog electronic circuit simulator program SPICE ("Simulation Program with Integrated Circuit Emphasis"). FIG. 11 shows a practical implementation of a digitally driven OLED display. Power and ground are connected from one side, which is the worst-case scenario for calibration methods. When power and ground are connected from both sides, calibration is expected to be much better. Additionally, the simulation has been performed using a blue OLED in order to have the worst case for the simulation. Calibration is expected to be better for other OLEDs (red, green) which require lower current.

[0096] The resistivity of the power supply line is an important factor in calibration quality. Power supply line is simulated at $4\Omega/\text{pixel}$ (4 ohms/pixel) (15.4 k Ω for the complete power supply line of 3840 pixels). With a lower power supply line resistivity, better calibration is expected. The chosen values for V_T and V_{OLED} are significantly spread. Thus, it would be valid for a transistor with a V_T of +0.4 and also a transistor of a V_T of -0.4V. The same holds for the OLED spread. If these spreads were lower, variation would be lower, so again, the calibration is expected to be better in actual applications.

[0097] The display of FIG. 11 and the pixel of FIG. 6 have been used for the simulation. The calibration of marked display line 1101 was simulated, as it is representative for all lines., considering the display fully on, with the following characteristics:

Display: 4K resolution: 3840x2160; pixel size: 60 μm for three colors = 423ppi; pixel: standard IGZO (n-type) with common cathode OLED.
Output brightness: 500nit

Current for the blue OLED subpixel: $0.15\mu\text{A}$ (dominant for calculation)

Resistivity per pixel on the supply line: $4\Omega/\text{pixel}$

TFT: the mobility of the IGZO is assumed not subject to variation in the current simulation. Only V_T variation: average

$V_T = 1\text{V}$, $\sigma_{V_T} = 0.1\text{V}$

OLED: $I_{\text{OLED}} = 0.15\mu\text{A}$ (microamperes), average $V_{\text{OLED}} = 3.5\text{V}$, $\sigma_{V_{\text{OLED}}} = 0.1\text{V}$

[0098] The results for pixel current vs. pixel position are compared in an uncalibrated display (FIG. 12), a calibration (level 1) without the resistivity of the power supply line correction in the calibration method (FIG. 13) and full calibration (level 2), including the resistivity of the power supply line correction in the calibration method (FIG. 14). The graphs show the pixel current as a function of the pixel position along the row of the display according to FIG. 11, the first pixel 1102 of the row 1101 at the 0 position (closest to the power connector) and the last pixel 1103 of the row (in the middle of the display) at the position 1920, which is the largest distance from the power connector. Absolute pixel current is shown in full line, and the relative error with respect to the reference current (predetermined as $0.15\mu\text{A}$) is shown in dashed line in FIG. 12 to FIG. 14.

[0099] FIG. 12 shows that for the uncalibrated case, the standard global deviation over one line and the relative difference in neighboring pixels are, respectively: Global: $\frac{\sigma_{I_{\text{OLED}}}}{I_{\text{OLED}}} = 10.7\%$; Neighboring pixels: $\frac{\Delta I_{\text{OLED}}}{I_{\text{OLED}}} = 46.6\%$

[0100] Thus, without calibration, the largest difference in light output between two neighboring pixels can be as big as 50%. This is far too high, indicating that calibration is strictly needed. Additionally, it is noticed that the effect of voltage drop along the power supply line is visible, but the current is dominated by local spread.

[0101] FIG. 13 shows that for the calibrated case (level 1), the standard global deviation and the relative difference in neighboring pixels are, respectively:

$$\text{Global: } \frac{\sigma_{I_{\text{OLED}}}}{I_{\text{OLED}}} = 5.74\%; \text{ Neighboring pixels: } \frac{\Delta I_{\text{OLED}}}{I_{\text{OLED}}} = 9.38\%$$

[0102] These results do not include the step that compensates for the resistive drop of the power supply line. As a consequence the following features can be observed:

a) Due to the resistive drop, the current in the middle of the display is lower than at the edge, when all pixels on the row are on (the highest display output case, 500 nits).

b) Moreover, the calibration gets also worse: pixels in the middle of the display have a worse calibration, when compared to pixels at the edge of the display.

[0103] Under the conditions of high light output and/or high resistivity of the power supply lines, the effect of resistive drop in the calibration procedure can be advantageously introduced.

[0104] FIG. 14 shows that for the calibrated case (level 2), the standard global deviation and the relative difference in neighboring pixels are, respectively

$$\text{Global: } \frac{\sigma_{I_{\text{OLED}}}}{I_{\text{OLED}}} = 0.354\%; \text{ Neighboring pixels: } \frac{\Delta I_{\text{OLED}}}{I_{\text{OLED}}} = 0.623\%$$

[0105] The SPICE simulation shows high uniformity of display after taking into account the resistive drops of the power supply lines. The spread on the transistors and OLEDs is equal to the spread in the former simulations. The obtained pixel output is very uniform and does not depend on the position on the display. The pixels in the middle of the display (position close to 1920) have an intensity almost equal to the pixels at the edge of the display. Also, the global spread on the pixel current is less than the least significant bit (LSB) when using an 8-bit per color coding. The largest difference between two pixels corresponds to 1.5 times LSB

[0106] This calibration has been done in the worst-case scenario, so in other cases calibration will be even better (e.g. lower power supply line resistivity further reduces the final obtained spread after calibration).

[0107] FIG. 15 shows a comparison of the three methods (thin line 1501 for the uncalibrated result, thick line 1502 for the level 1 calibration, dashed line 1503 for the level 2 calibration), for the same row of the display. The upper graph shows the absolute pixel current, and in the lower graph the relative error, with respect to the reference current ($0.15\mu\text{A}$). The encircled area 1510 closest to the power connection shows the initial variations. When resistive drop is not taken into account (level 1 calibration), the initial variations present in the non-calibrated current mostly disappear, and

a uniform current is obtained. However the current drops linearly towards the center of the display (the end of the row). However, when resistive drop is taken into account (level 2), variations disappear from the simulations and the current remains equal between the edge and the center of the display. The encircled area 1511 shows the variations at the end of the row. When resistive drop is not taken into account (level 1), the initial variations of the non-calibrated current all are still all present in the current after calibration. They are only smaller. Moreover, the average current is about 20% lower in the center of the display (the end of the row). When resistive drop is taken into account in the calibration (level 2), variations disappear from the simulations and the current remains virtually equal between the edge and the center of the display.

[0108] In summary, embodiments of the method of the present invention manages to reduce pixel variations and intensity gradients from edge to end of row or edge to middle of display. This is advantageous, for example, in cases where there are more than 640 pixels on a 4Ω/pixel powerline of the display, as the method can take the resistive drops into account.

[0109] With added compensation for the resistive drop, it is possible to obtain a better uniformity than 1 LSB (of 8 bit) on a 3840x2160 (ultra-high density) display.

Claims

1. Driving system circuitry for an active matrix display, the driving system circuitry comprising:

- a data driver module for receiving a digital data bit stream representing an image to be displayed by pixels of the active matrix display,
- one or more power supply lines for powering a plurality of pixels each comprising at least one light emitting element,
- a voltage source connected to the one or more power supply lines,
- calibration means for compensating for power drop over the one or more supply lines, the calibration means comprising

Means for flowing a current through an individual pixel

Means for determining a voltage drop across the pixel and comparing this to a pre-determined reference voltage for that pixel

Means for determining, from the comparison, calibration values for that pixel which take into account resistance of wiring connected to the voltage source and to ground, and

Means for applying the calibration values to a received digital data bit stream to generate therefrom data driver voltages to be applied to the data driver module for representation of a corrected image.

2. The driving system according to claim 1, further comprising a variable impedance connected in series with the LED or OLED in each pixel, adapted to provide a same current flowing through every pixel upon pixel activation.

3. Driving system according to any of the previous claims, wherein the calibration means comprises a memory for storing determined calibration values.

4. The driving system of any of the previous claims wherein the calibration means comprises a reference current source connected to a feedback loop and further connected, via a "calibration mode" switching means, to the at least one power supply line.

5. The driving system of any of the previous claims, wherein the calibration means comprise an interpolation unit and ground voltage drop multiplication unit, both adapted, via a sum unit, to provide voltage regulation to the data driver module of the active matrix panel.

6. The driving system of any of the previous claims, wherein the voltage source and calibration means are connectable to a first side of the at least one power supply line, the at least one power supply line further comprising a second side connectable to the voltage source via a second "driving-mode" switching means.

7. An active matrix display comprising an array of pixels logically organized in rows and columns, each pixel comprising at least one light emitting element, the active matrix display further comprising driving system circuitry according to any of the previous claims.

8. The active matrix display according to claim 7, wherein the pixels comprise a 2T1C structure
9. The active matrix display of any of claims 7 or 8, wherein the array is divided in two sets of pixels, each set comprising driving system circuitry according to any of claims 1 to 6.
- 5 10. A method of calibrating an active matrix display comprising an array of pixels logically organized in rows and columns, the method comprising
flowing a current through an individual pixel of a row of pixels of the array, determining a voltage drop across the pixel and comparing this to a pre-determined reference voltage for that pixel,
10 determining, from the comparison, calibration values for that pixel which take into account resistance of wiring connected to the voltage source and to ground, and storing the calibration values.
11. A method of driving an active matrix display, the method comprising
receiving a digital data bit stream representing an image to be displayed on the active matrix display,
15 applying previously determined calibration values to the received data bit stream to generate therefrom data driver voltages to be applied to a data driver module of the active matrix display for representation of an image which is corrected at least for power drop over supply lines.
12. The method according to claim 11, wherein the calibration values are determined according to the method of claim 10.
- 20

25

30

35

40

45

50

55

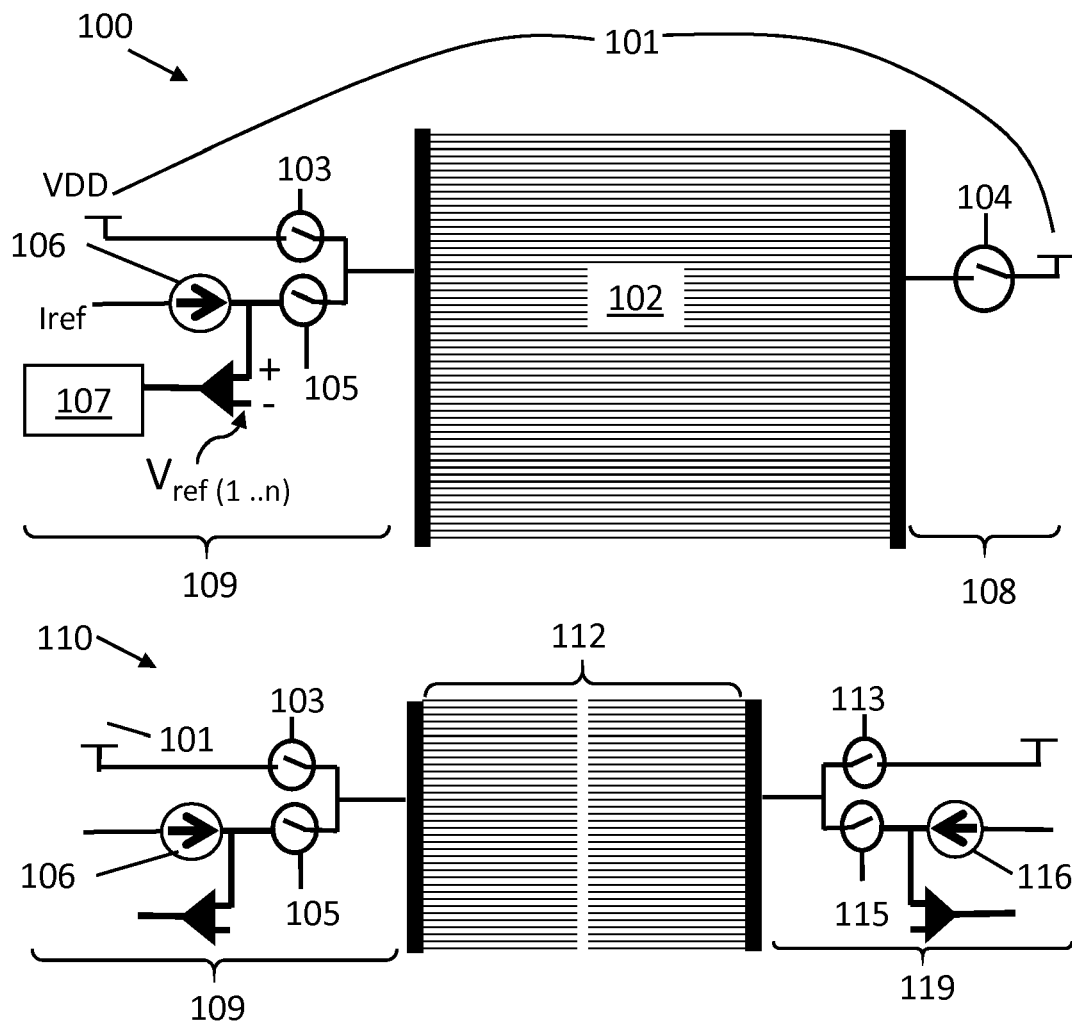


FIG. 1

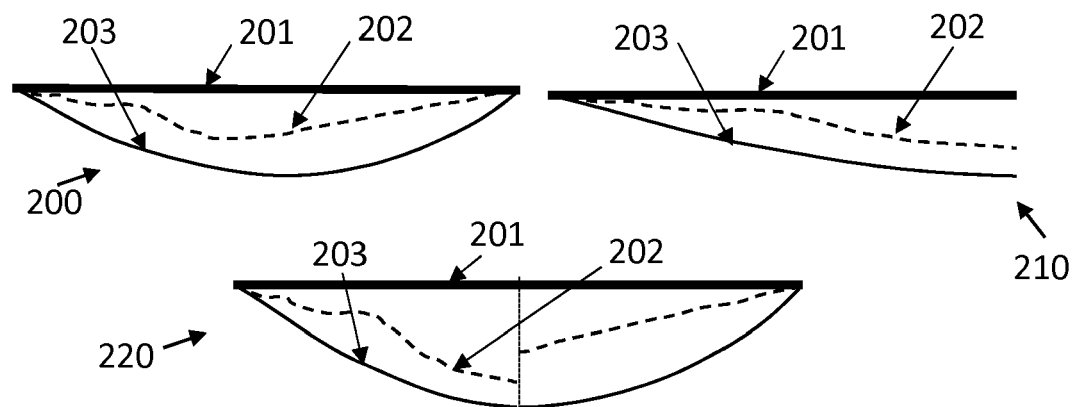


FIG. 2

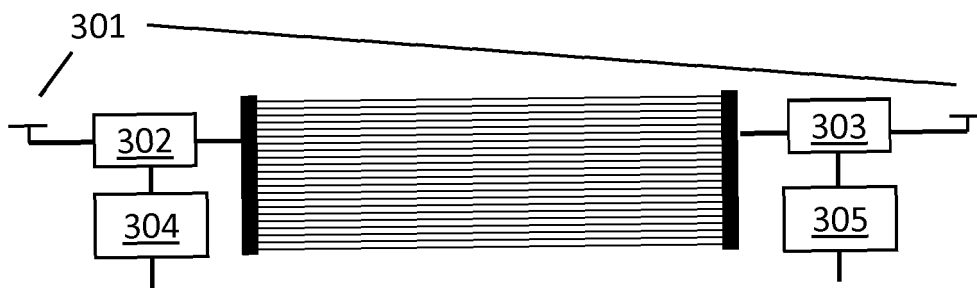


FIG. 3

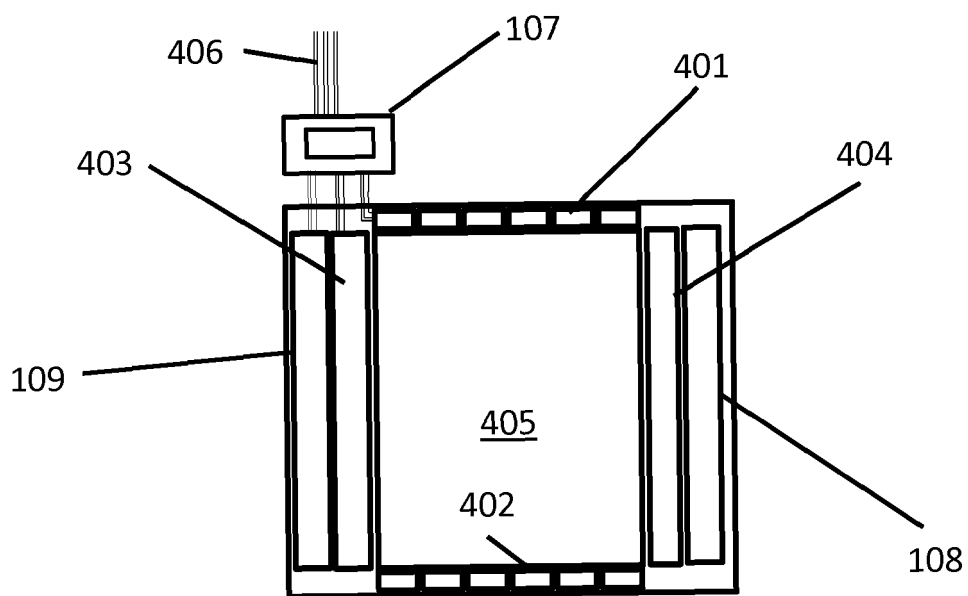


FIG. 4

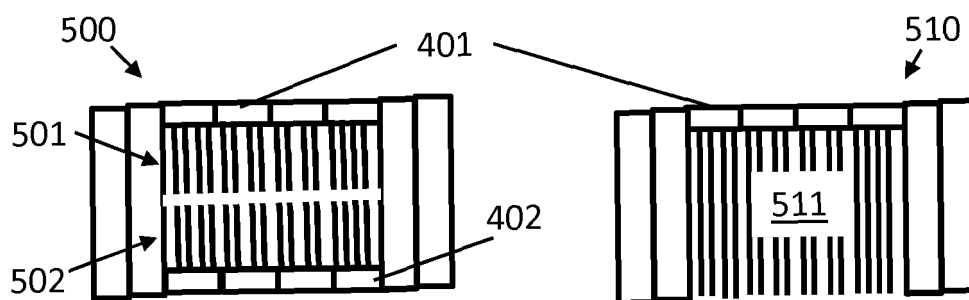


FIG. 5

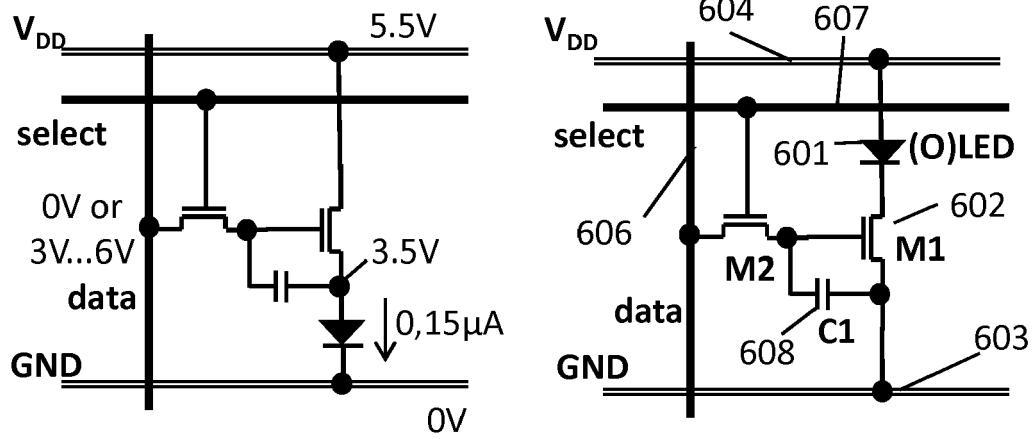


FIG. 6

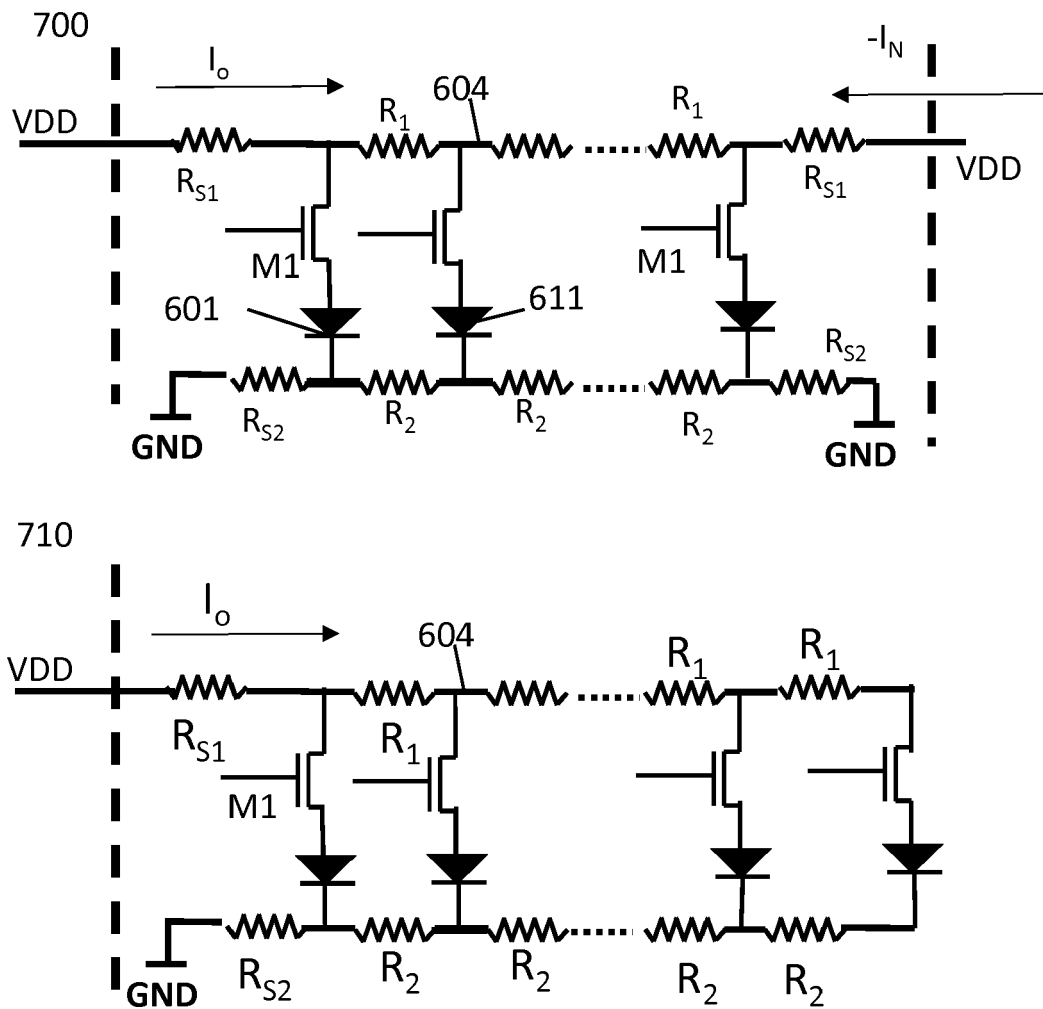


FIG. 7

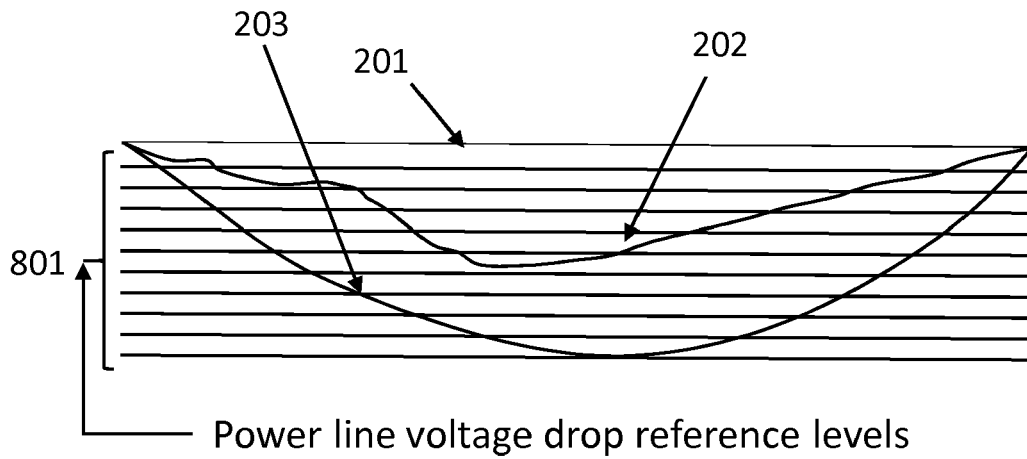


FIG. 8

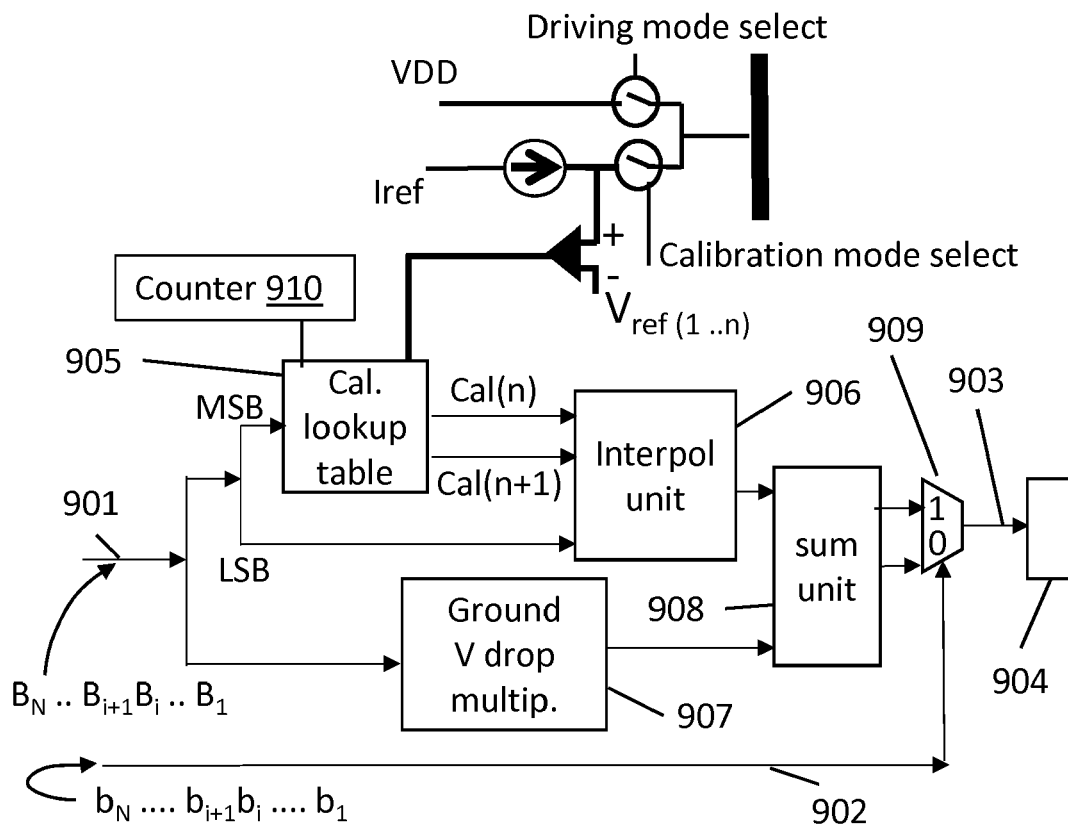


FIG. 9

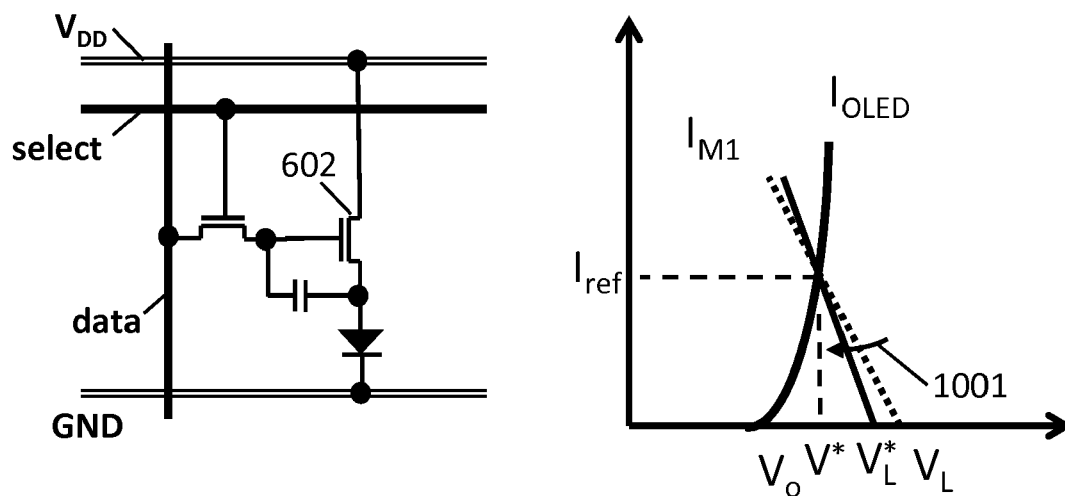


FIG. 10

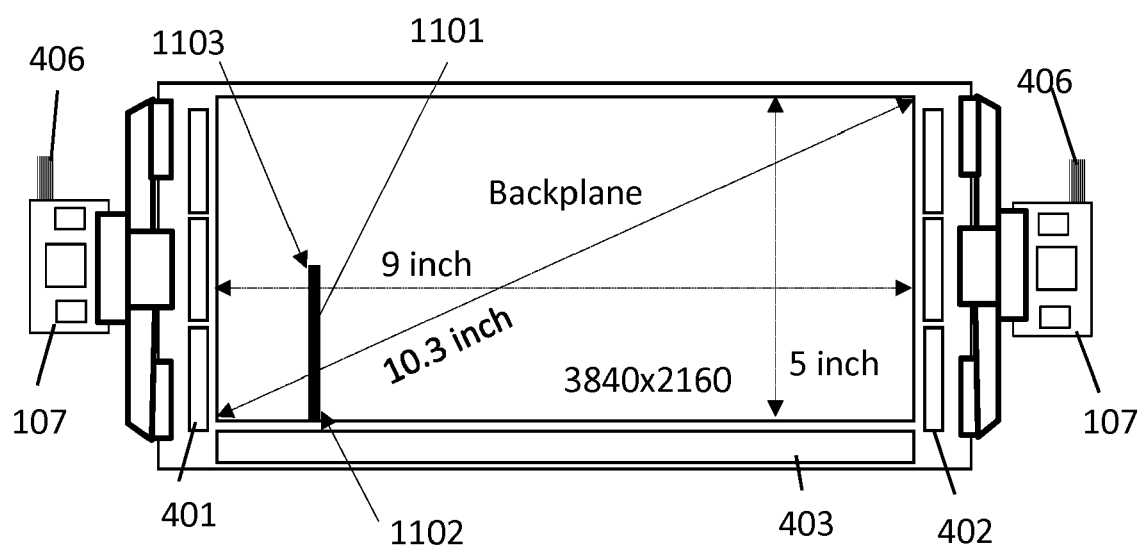


FIG. 11

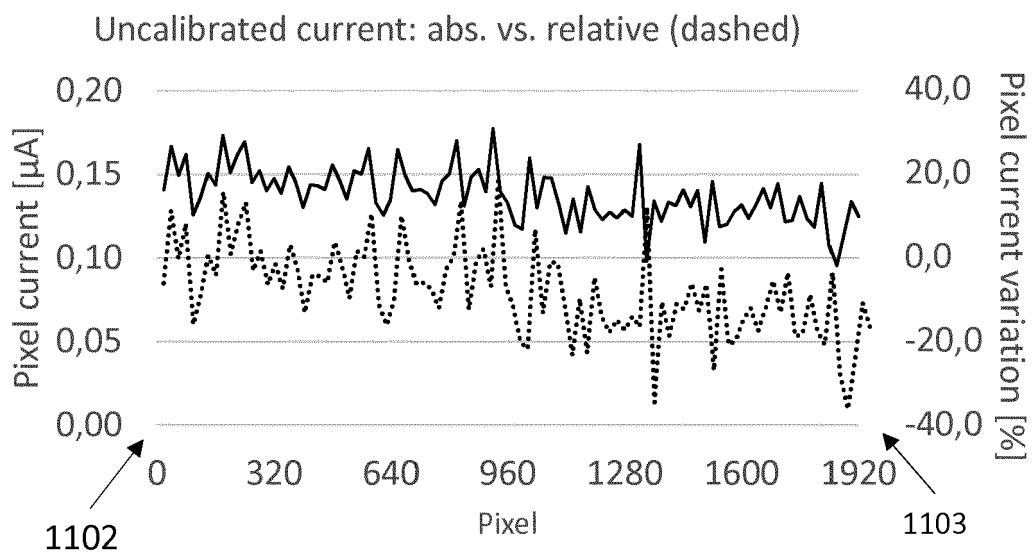


FIG. 12

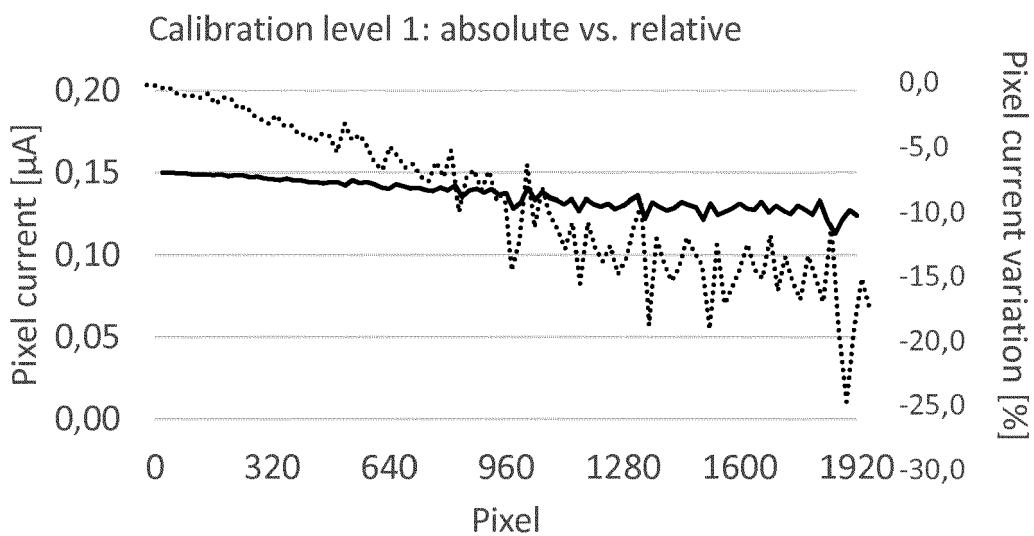


FIG. 13

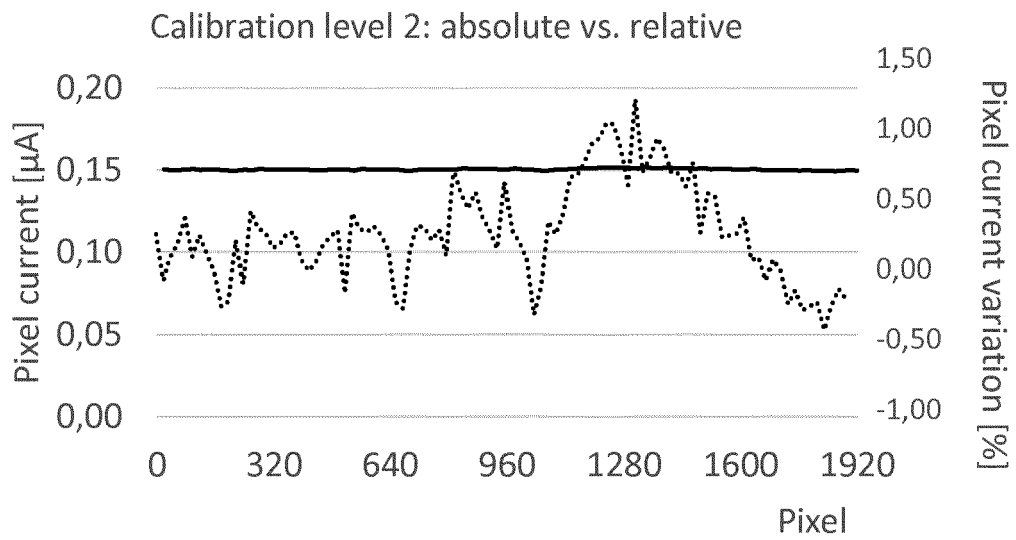


FIG. 14

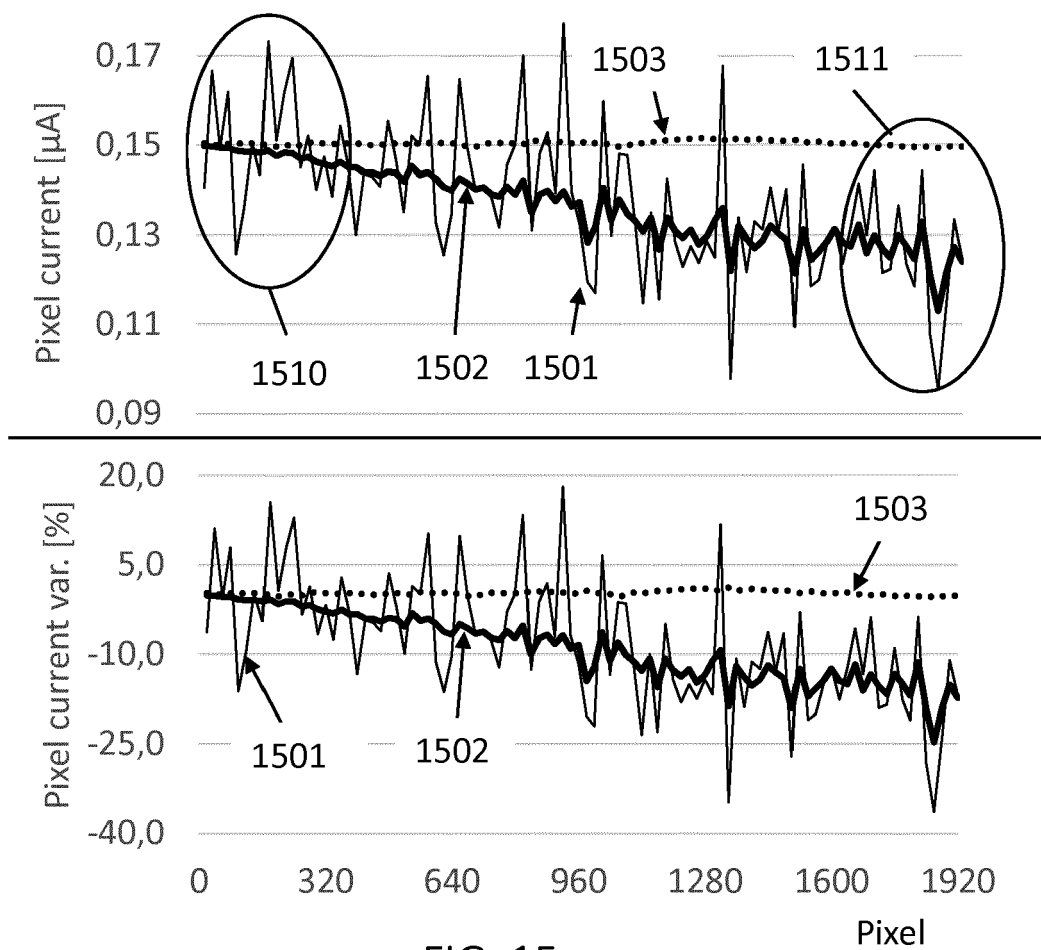


FIG. 15



EUROPEAN SEARCH REPORT

Application Number
EP 16 19 7152

5

10

15

20

25

30

35

40

45

50

55

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2007/164937 A1 (JUNG KWANG-CHUI [KR] ET AL) 19 July 2007 (2007-07-19) * paragraph [0019] - paragraph [0045]; figures 1-5 *	1-3,7-12	INV. G09G3/3225 G09G3/20
			TECHNICAL FIELDS SEARCHED (IPC)
			G09G
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
Munich		27 January 2017	Gartlan, Michael
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

 1
EPO FORM 1503 03.02 (P04C01)



Application Number

EP 16 19 7152

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-3, 7-12

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).



LACK OF UNITY OF INVENTION
SHEET B

Application Number

EP 16 19 7152

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-3, 7-12

a variable impedance connected in series with the LED or OLED in each pixel, adapted to provide a same current flowing through every pixel upon pixel activation, solving the problem of implementing a range of gradations.

2. claims: 4, 6

a reference current source connected to a feedback loop and further connected, via a "calibration mode" switching means, to the at least one power supply line, solving the problem of enabling pixel monitoring independent of the pixel power source.

3. claim: 5

an interpolation unit and ground voltage drop multiplication unit, both adapted, via a sum unit, to provide voltage regulation to the data driver module of the active matrix panel, solving the problem of reducing circuit area.

27-01-2017

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007164937 A1	19-07-2007	CN 1897093 A	17-01-2007
		KR 20070006331 A	11-01-2007
		US 2007164937 A1	19-07-2007

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- WO 2014080014 A [0005] [0042] [0079]
- WO 2014068017 A [0045]
- WO 2014068017 A1 [0086]