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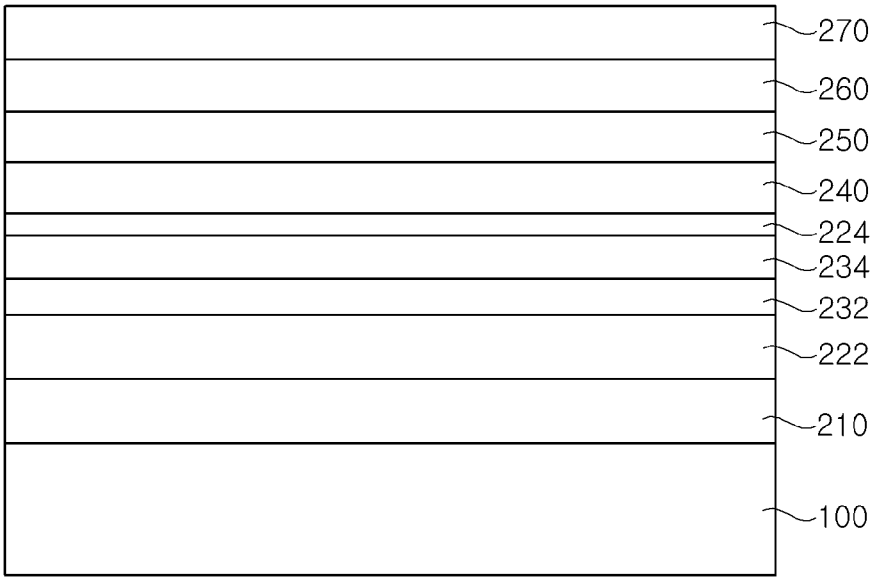
(54) **Title**: LIGHT EMITTING DIODE AND METHOD FOR FABRICATING THE SAME



(57) **Abstract**: The present invention relates to a light emitting diode and a method for fabricating the same. According to the present invention, there is provided a method for fabricating a light emitting diode, which comprises preparing a sapphire substrate; growing a first n-type semiconductor layer on one surface of the sapphire substrate; growing a bowing prevention layer including $Al_xIn_{1-x}N$ ($x > 0.82$) on the first n-type semiconductor layer; growing a second n-type semiconductor layer on the bowing prevention layer; and growing an active layer and a p-type semiconductor layer on the second n-type semiconductor layer.

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Description

Title of Invention: LIGHT EMITTING DIODE AND METHOD FOR FABRICATING THE SAME

Technical Field

[1] The present invention relates to a light emitting diode and a method for fabricating the same.

Background Art

[2] A light emitting diode is basically a PN junction diode having a junction of a p-type semiconductor and an n-type semiconductor.

[3] In the light emitting diode, if the p-type and n-type semiconductors are joined together and then supplied with voltage so that current flows through the p-type and n-type semiconductors, holes of the p-type semiconductor move toward the n-type semiconductor while electrons of the n-type semiconductor move toward the p-type semiconductor, whereby the electrons and the holes move toward the PN junction.

[4] The electrons moving toward the PN junction are coupled with the holes while falling from a conduction band to a valence band. In this case, energy corresponding to a potential difference between the conduction band and the valence band, i.e., an energy difference, is emitted in the form of light.

[5] The light emitting diode which is a semiconductor device emitting light has characteristics of environmental-friendliness, low voltage, long lifespan, low price, and the like. Conventionally, the light emitting diode was frequently used in a lamp for display or a display for simple information such as numbers. However, with the development of industrial technologies, particularly with the development of information display and semiconductor technologies, the light emitting diode has recently used in various fields including displays, car headlamps, projectors, and the like.

[6] The light emitting diode may be fabricated by growing epitaxial layers including a p-type semiconductor layer, an active layer and an n-type semiconductor layer on a sapphire substrate.

[7] Here, in the method for growing the epitaxial layer on the sapphire substrate, the epitaxial layer is grown by loading the sapphire substrate into a growth apparatus such as a MOCVD (Metal Organic Chemical Vapor Deposition) apparatus, heating the sapphire substrate at a high temperature, and then introducing gases necessary for growth of the epitaxial layer.

[8] If the growth of the epitaxial layer is completed, the sapphire substrate is cooled and then extracted to the outside.

[9] In this case, if the epitaxial layer is grown and then cooled, there is a problem in that

a bowing phenomenon that the sapphire substrate is bowed due to a difference in lattice constant between the sapphire substrate and the epitaxial layer, a high growth temperature, and the like.

[10] In order to solve the bowing phenomenon, conventionally, the thickness of the growth substrate was made thick, or an AlN or AlGaN layer was formed during the growth of the epitaxial layer.

[11] However, using a thick growth substrate causes a problem of increasing fabrication cost. In addition, there is a problem in that internal defects occur in the epitaxial layer since the AlN or AlGaN layer has a lattice constant different from that of GaN that is a material constituting the epitaxial layer.

Disclosure of Invention

Technical Problem

[12] An object of the present invention is to provide a light emitting diode, in which a bowing phenomenon is minimized and internal defects are also minimized in an epitaxial layer when the epitaxial layer is grown on a sapphire substrate, and a method for fabricating the light emitting diode.

Solution to Problem

[13] According to an aspect of the present invention for achieving the object, there is provided a method for fabricating a light emitting diode, which comprises preparing a sapphire substrate; growing a first n-type semiconductor layer on one surface of the sapphire substrate; growing a bowing prevention layer including $Al_xIn_{1-x}N$ ($x > 0.82$) on the first n-type semiconductor layer; growing a second n-type semiconductor layer on the bowing prevention layer; and growing an active layer and a p-type semiconductor layer on the second n-type semiconductor layer.

[14] The method may further comprise growing a defect propagation prevention layer comprising $Al_xIn_{1-x}N$ ($x = 0.82$) on the bowing prevention layer, before growing the second n-type semiconductor layer.

[15] The growth of the bowing prevention layer may be performed during cooling from a growth temperature of the first n-type semiconductor layer to a growth temperature of the defect propagation prevention layer.

[16] The growth temperature of the defect propagation prevention layer may be 740 to 840℃.

[17] The bowing prevention layer and the defect propagation prevention layer may be grown by supplying a source gas containing N, a source gas containing trimethyl indium (TMIn) and a source gas containing trimethyl aluminum (TMAl), and the source gas containing TMIn and the source gas containing TMAl may be supplied by 130 to 230 μmol and 15 to 25 μmol, respectively.

[18] According to another aspect of the present invention, there is provided a light emitting diode, comprising: a sapphire substrate; a first n-type semiconductor layer formed on one surface of the sapphire substrate; a bowing prevention layer formed on the first n-type semiconductor layer, the bowing prevention layer including $Al_xIn_{1-x}N$ ($x > 0.82$); a second n-type semiconductor layer formed on the bowing prevention layer; and an active layer and a p-type semiconductor layer, formed on the second n-type semiconductor layer.

[19] The light emitting diode may further comprise a defect propagation prevention layer comprising $Al_xIn_{1-x}N$ ($x = 0.82$), and formed between the second n-type semiconductor layer and the bowing prevention layer.

[20] The bowing prevention layer may be formed to have a thickness of 10 to 30Å

Advantageous Effects of Invention

[21] According to the present invention there is provided a light emitting diode, in which a bowing phenomenon is minimized and internal defects are also minimized in an epitaxial layer when the epitaxial layer is grown on a sapphire substrate, and a method for fabricating the light emitting diode.

Brief Description of Drawings

[22] Fig. 1 is a sectional view of a light emitting diode according to an embodiment of the present invention.

[23] Fig. 2 is a sectional view of a light emitting diode device according to an embodiment of the present invention.

[24] Fig. 3 is a sectional view of a light emitting diode device according to another embodiment of the present invention.

Mode for the Invention

[25] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. The invention, however, is not limited to these embodiments and applications or to the manner in which the embodiments and applications operate or are described herein. Moreover, the drawings may show simplified or partial views, and the dimensions of elements in the Figures may be exaggerated or otherwise not in proportion for clarity. In addition, as the terms "on" is used herein, one object (e.g., a material, a layer, a substrate, etc.) can be "on" another object regardless of whether the one object is directly on the other object or there are one or more intervening objects between the one object and the other object.

[26] Fig. 1 is a sectional view of a light emitting diode according to an embodiment of the present invention.

[27] Hereinafter, a method for fabricating the light emitting diode according to the embodiment of the present invention will be described with reference to Fig. 1.

[28] First, a growth substrate 100 is prepared.

[29] The growth substrate 100 may be any substrate, on which epitaxial layers described later can be grown, i.e., a sapphire substrate, a silicon carbide substrate, a silicon substrate, or the like. However, the growth substrate 100 may be preferably a sapphire substrate.

[30] In this case, the epitaxial layers may comprise a buffer layer 210, a first n-type semiconductor layer 222, a second n-type semiconductor layer 224, a bowing prevention layer 232, a defect propagation prevention layer 234, a superlattice layer 240, an active layer 250, an electron blocking layer 260 and a p-type semiconductor layer 270.

[31] The buffer layer 210 may be grown on the growth substrate 100.

[32] The buffer layer 210 may be provided in order to reduce lattice mismatch between the growth substrate 100 and the first n-type semiconductor layer 222 described later. The buffer layer 210 may also be single- or multi-layered. In a case where the buffer layer is multi-layered, the buffer layer may comprise a low-temperature buffer layer and a high-temperature buffer layer. Such a buffer layer (not shown) may be made of AlN. In this case, the buffer layer 210 may be omitted.

[33] Then, the first n-type semiconductor layer 222 may be grown on the buffer layer 210.

[34] The first n-type semiconductor layer 222 may be a Group III-N based compound semiconductor layer doped with an n-type impurity, e.g., an (Al, Ga, In)N-based Group III nitride semiconductor layer.

[35] The first n-type semiconductor layer 222 may be a GaN layer doped with an n-type impurity, i.e., an N-GaN layer, and/or may be an N-AlGaN layer that is an N-GaN layer doped with aluminum. The n-type impurity may be Si. The n-type semiconductor layer 222 may also be single- or multi-layered. For example, in the case where the n-type semiconductor layer 222 is multi-layered, the n-type semiconductor layer may be formed to have a superlattice structure.

[36] Subsequently, the bowing prevention layer 232 may be grown on the first n-type semiconductor layer 222.

[37] The bowing prevention layer 232 may comprise $Al_xIn_{1-x}N$ ($x > 0.82$). The bowing prevention layer 232 may be grown to a thickness of 10 to 30Å

[38] Subsequently, the defect propagation prevention layer 234 may be grown on the bowing prevention layer 232. In this case, the defect propagation prevention layer 234 may be omitted if necessary.

[39] The defect propagation prevention layer 234 may comprise $Al_xIn_{1-x}N$ ($x = 0.82$).

[40] Then, the second n-type semiconductor layer 224 may be grown on the defect propagation prevention layer 234.

[41] The second n-type semiconductor layer 224 may be grown in the same manner as the first n-type semiconductor layer 222, and therefore, its detailed description will be

omitted.

[42] As described above, the bowing prevention layer 232 is preferably grown between the n-type semiconductors 222 and 224.

[43] If the epitaxial layer is grown at a high temperature on the growth substrate such as the sapphire substrate, particularly, a growth substrate having a large diameter of 4 inches or more as described above (particularly, the n-type semiconductor layers 222 and 224 are grown at a high temperature for the purpose of smooth impurity doping), a bowing phenomenon occurs so that the growth substrate such as the sapphire substrate is bowed due to a difference in lattice constants between the growth substrate such as the sapphire substrate and the epitaxial layers, and/or a high growth temperature, and the like. The bowing prevention layer 323 can reduce and minimize the bowing phenomenon of the growth substrate such as the sapphire substrate, particularly, the growth substrate having a large diameter of 4 inches or more.

[44] This is not only because the lattice constant of the bowing prevention layer 232 is large but also because the bowing prevention layer 232 is grown at a growth temperature lower than a temperature at which the n-type semiconductor layers 222 and 224 are grown. Thus, it is possible to reduce and minimize the bowing phenomenon.

[45] In this case, the bowing prevention layer 232 is grown to be formed of a material with a large lattice constant, i.e., a material comprising $Al_xIn_{1-x}N$ ($x > 0.82$) so as to minimize the bowing phenomenon, and accordingly, there is a difference in lattice constant between the bowing prevention layer 232 and the n-type semiconductor layers 222 and 224. Therefore, if the second n-type semiconductor layer 224 is directly grown on the bowing prevention layer 232, many defects may occur in the second n-type semiconductor layer 224.

[46] Here, the defects in the second n-type semiconductor layer 224 can be reduced by growing the defect propagation prevention layer 234, which is formed of the same composition material as the bowing prevention layer 232 but has a different compositional ratio therefrom, on the bowing prevention layer 232, i.e., between the bowing prevention layer 232 and the second n-type semiconductor layer 224. That is, the defects in the second n-type semiconductor layer 224 can be reduced by growing the defect propagation prevention layer 234 being formed of the same composition material as the bowing prevention layer 232, and having the same lattice constant as the n-type semiconductor layers 222 and 224. For example, the defect propagation prevention layer 234 may comprise $Al_xIn_{1-x}N$ ($x = 0.82$).

[47] The process of growing the first n-type semiconductor layer 222, the bowing prevention layer 232, the defect propagation prevention layer 234 and the second n-type semiconductor layer 224 will be described in detail. After the first n-type semiconductor layer 222 is grown, the bowing prevention layer 232 is grown while the

growth temperature is lowered to a predetermined temperature. Then, the defect propagation prevention layer 234 is grown at the predetermined temperature. Subsequently, the growth temperature is again raised by heating, and the second n-type semiconductor layer 224 is then grown.

[48] Here, the predetermined temperature, at which the defect propagation prevention layer 234, i.e., the layer formed of the material comprising $Al_xIn_{1-x}N$ (x = 0.82) is grown, is within a temperature range of 740 to 840℃.The first and second n-type semiconductor layers 222 and 224 are grown in a temperature range of 1000℃ or so.

[49] After the first n-type semiconductor layer 222 is grown, a source gas containing N, a source gas containing trimethyl indium (TMIn) and a source gas containing trimethyl aluminum (TMAl) are supplied, and the bowing prevention layer 232 and the defect propagation prevention layer 234 are grown while lowering the growth temperature. In this case, the bowing prevention layer 232 is grown while lowering the growth temperature, and the defect propagation prevention layer 234 is grown while maintaining a predetermined temperature.

[50] Here, for the growth, the source gas containing TMIn is introduced by 130 to 230 μmol, and the source gas containing TMAl is introduced by 15 to 20 μmol.

[51] The reason why the bowing prevention layer 232 is grown while lowering the growth temperature is that $Al_xIn_{1-x}N$ containing In with a relatively low content is grown when the $Al_xIn_{1-x}N$ is grown at a relatively high growth temperature and $Al_xIn_{1-x}N$ containing In with a relatively high content is grown when the $Al_xIn_{1-x}N$ is grown at a relatively low growth temperature.

[52] The lattice constant of the bowing prevention layer 232 comprising $Al_xIn_{1-x}N$ where the content of In is lower than 18% is greater than that of the n-type semiconductor layers 222 and 224, and the lattice constant of the defect propagation prevention layer 234 comprising $Al_xIn_{1-x}N$ where the content of In is 18% is equal to that of the n-type semiconductor layers 222 and 224.

[53] Subsequently, the superlattice layer 240 may be grown on the second n-type semiconductor layer 224. The superlattice layer 240 may be a stacked structure which is formed by stacking Group III-N based compound semiconductor layers(e.g., an (Al, Ga, In)N semiconductor layers), e.g. repetitively stacking InN and InGaN layers, or InGaN and GaN layers.

[54] The superlattice layer 240 is grown before the active layer 250 which will be described later is formed, so that it may prevent dislocations or defects from being transferred into the active layer 250. Thus, the superlattice layer can serve to reduce the formation of the dislocations or defects in the active layer 250 and to improve crystallinity of the active layer 250. The superlattice layer 240 may be omitted if necessary.

[55] The active layer 250 may be grown on the superlattice layer 240.

[56] The active layer 250 may be formed of a Group III-N based compound semiconductor, e.g., an (Al, Ga, In)N semiconductor. The active layer 250 may be single- or multi-layered and emit light of at least a predetermined wavelength. The active layer 250 may be formed to have a single quantum well structure including one well layer (not shown) or a multiple quantum well structure in which well and barrier layers (not shown) are alternately stacked. In this case, any one or both of the well and barrier layers (not shown) may be formed to have a superlattice structure.

[57] Subsequently, the electron blocking layer 260 may be grown on the active layer 250.

[58] The electron blocking layer 260 may be formed between the active layer 250 and the p-type semiconductor layer 270 which will described later. The electron blocking layer may be provided in order to improve recombination efficiency between electrons and holes and formed of a material having a relatively wide bandgap.

[59] The electron blocking layer 260 may be formed of an (Al, In, Ga)N-based Group III nitride semiconductor, or include a p-AlGaN layer doped with an impurity, particularly, a p-AlGaN layer doped with Mg.

[60] Next, the p-type semiconductor layer 270 may be grown on the electron blocking layer 260.

[61] The p-type semiconductor layer 270 may be formed of a Group III-N based compound semiconductor doped with a p-type impurity, e.g., an (Al, In, Ga)N-based Group III nitride semiconductor. The p-type semiconductor layer 270 may be a GaN layer doped with a p-type impurity, i.e., a p-GaN layer. The p-type semiconductor layer 270 may be single- or multiple-layered. For example, the p-type semiconductor layer 270 may be formed to have a superlattice structure.

[62] Thus, in the light emitting diode according to one embodiment of the present invention, the bowing prevention layer is grown to reduce and minimize the bowing phenomenon during the process of growing the epitaxial layer, particularly, the n-type semiconductor layer on the growth substrate such as the sapphire substrate and the defect propagation prevention layer is grown to prevent the transfer, diffusion or propagation of lattice defects occurring in the bowing prevention layer, so that it may reduce and minimize the bowing phenomenon of the sapphire substrate on which the light emitting diode is grown. Thus, the fabrication yield of light emitting diode devices, which will be described later, can be improved. Further, it is possible to minimize the lattice defects in the epitaxial layer, particularly, the active layer, thereby fabricating a light emitting diode device with excellent light emitting efficiency.

[63] Fig. 2 is a sectional view of a light emitting diode device according to an embodiment of the present invention.

[64] Referring to Fig. 2, the light emitting diode device 1000 according to the embodiment of the present invention may comprise the light emitting diode according to

the embodiment of the present invention described with reference to Fig. 1.

[65] That is, the epitaxial layers comprising the buffer layer 210, the first n-type semiconductor layer 222, the bowing prevention layer 232, the defect propagation prevention layer 234, the second n-type semiconductor layer 224, the superlattice layer 240, the active layer 250, the electron blocking layer 260 and the p-type semiconductor layer 270 are grown on the growth substrate 100 such as the sapphire substrate.

[66] Subsequently, a partial surface of the second n-type semiconductor layer 224 is exposed by partially mesa-etching the p-type semiconductor layer 270, the electron blocking layer 260, the active layer 250 and the superlattice layer 240.

[67] In this case, the second n-type semiconductor layer 224 may also be partially etched in the mesa-etching process. The reason why the mesa-etching process is performed to expose the surface of the second n-type semiconductor layer 224 is that the bowing prevention layer 232 or the defect propagation prevention layer 234 formed under the second n-type semiconductor layer 224 has no influence on an n-type contact. As considering the mesa-etching process, the bowing prevention layer 232 or the defect propagation prevention layer 234 may be grown to be spaced apart from the active layer 250 by a spacing interval of 1.5 to 2 ㎛.

[68] Subsequently, the n-type contact is formed by forming an n-type electrode 310 on the partial surface of the second n-type semiconductor layer 224 that is exposed by the mesa-etching process.

[69] A p-type electrode 320 is formed on the p-type semiconductor layer 270, thereby forming the light emitting diode device 1000, particularly, a horizontal light emitting diode device. Although not shown in Fig. 2, a transparent electrode such as ITO may be further formed between the p-type semiconductor layer 270 and the p-type electrode 320.

[70] Fig. 3 is a sectional view of a light emitting diode device according to another embodiment of the present invention.

[71] Referring to Fig. 3, a light emitting diode device 2000 according to the embodiment of the present invention may be formed using the light emitting diode according to the embodiment of the present invention described with reference to Fig. 1.

[72] That is, the epitaxial layers comprising the buffer layer 210, the first n-type semiconductor layer 222, the bowing prevention layer 232, the defect propagation prevention layer 234, the second n-type semiconductor layer 224, the superlattice layer 240, the active layer 250, the electron blocking layer 260 and the p-type semiconductor layer 270 are grown on the growth substrate 100 such as the sapphire substrate.

[73] Subsequently, a conductive substrate 330 is formed on the p-type semiconductor layer 270. In this case, the conductive substrate 330 may be formed on the p-type semiconductor layer 270 by depositing process such as physical vapor deposition, chemical

vapor deposition, or the like. The conductive substrate 330 may be formed by adhering to the p-type semiconductor layer using a conductive adhesive layer 340.

[74] Then, a process of removing the growth substrate 100 is performed, and an n-type electrode 360 electrically contacting the n-type semiconductor layer is formed, thereby forming the light emitting diode device 2000, particularly, a vertical light emitting diode device.

[75] In this case, the process of removing the growth substrate 100 may be a process of simultaneously removing at least one of the buffer layer 210, the first n-type semiconductor layer 222, the bowing prevention layer 232 and the defect propagation prevention layer 234, as well as the growth substrate 100. Preferably, all the buffer layer 210, the first n-type semiconductor layer 222, the bowing prevention layer 232 and the defect propagation prevention layer 234 may simultaneously removed while removing the growth substrate 100.

[76] Although the present invention has been described in connection with the preferred embodiments, the present invention is not limited thereto. It will be understood by those skilled in the art that various modifications and changes can be made thereto without departing from the spirit and scope of the invention.

Claims

[Claim 1] A method for fabricating a light emitting diode, the method comprising:
preparing a sapphire substrate;
growing a first n-type semiconductor layer on one surface of the sapphire substrate;
growing a bowing prevention layer comprising $Al_xIn_{1-x}N$ ($x > 0.82$) on the first n-type semiconductor layer;
growing a second n-type semiconductor layer on the bowing prevention layer; and
growing an active layer and a p-type semiconductor layer on the second n-type semiconductor layer.

[Claim 2] The method of claim 1, further comprising growing a defect propagation prevention layer comprising $Al_xIn_{1-x}N$ ($x = 0.82$) on the bowing prevention layer, before growing the second n-type semiconductor layer.

[Claim 3] The method of claim 2, wherein the growth of the bowing prevention layer is performed during cooling from a growth temperature of the first n-type semiconductor layer to a growth temperature of the defect propagation prevention layer.

[Claim 4] The method of claim 2, wherein the growth temperature of the defect propagation prevention layer is 740 to 840℃.

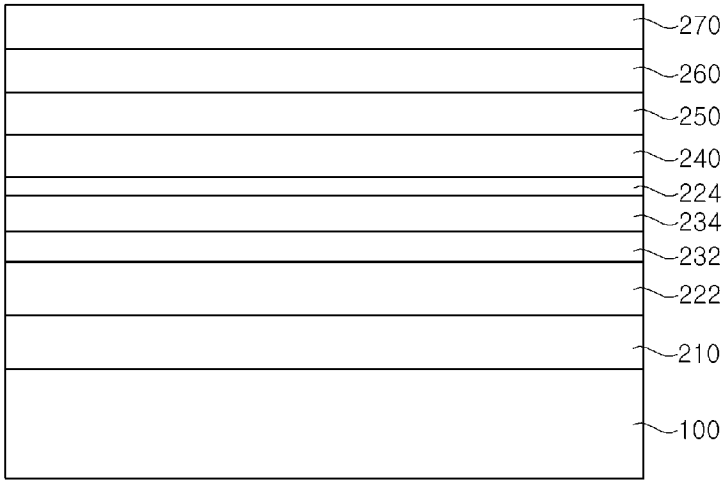
[Claim 5] The method of claim 2, wherein the bowing prevention layer and the defect propagation prevention layer are grown by supplying a source gas containing N, a source gas containing trimethyl indium (TMIn) and a source gas containing trimethyl aluminum (TMAl), and the source gas containing TMIn and the source gas containing TMAl are supplied by 130 to 230 μmol and 15 to 25 μmol, respectively.

[Claim 6] A light emitting diode, comprising:
a sapphire substrate;
a first n-type semiconductor layer formed on one surface of the sapphire substrate;
a bowing prevention layer formed on the first n-type semiconductor layer, and comprising $Al_xIn_{1-x}N$ ($x > 0.82$);
a second n-type semiconductor layer formed on the bowing prevention layer; and
an active layer and a p-type semiconductor layer formed on the second n-type semiconductor layer.

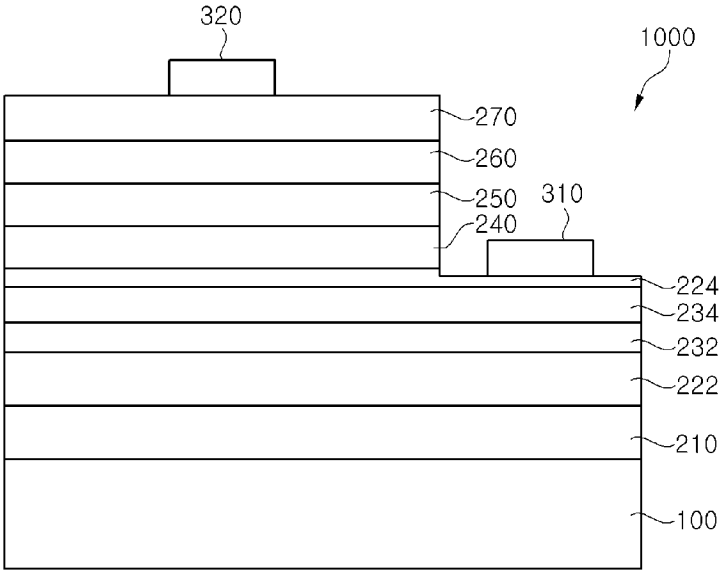
[Claim 7] The light emitting diode of claim 6, further comprising a defect propagation prevention layer comprising $Al_xIn_{1-x}N$ (x = 0.82), wherein the defect propagation prevention layer is formed between the second n-type semiconductor layer and the bowing prevention layer.

[Claim 8] The light emitting diode of claim 6, wherein the bowing prevention layer is formed to have a thickness of 10 to 30 Å

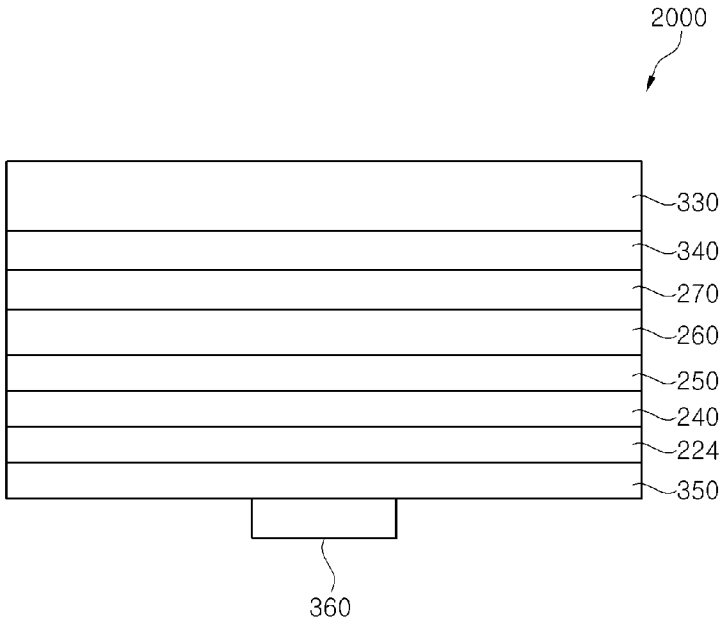
[Fig. 1]



[Fig. 2]



[Fig. 3]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2012/009092

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/14(2010.01)i, H01L 33/30(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/14; H01S 5/323; H01S 5/343; H01L 33/00; H01L 27/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: LED, bowing, prevention layer, defect propagation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2000-261099 A (FUJI ELECTRIC CO,. LTD.) 22 September 2000 See paragraph [0015], claim 1, and figure 1.	1-8
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A	US 6388275 B1 (TAKASHI KANO) 14 May 2002 See abstract, column 4, lines 12-17, claim 1, and figure 1.	1-8
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☐ Further documents are listed in the continuation of Box C.

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