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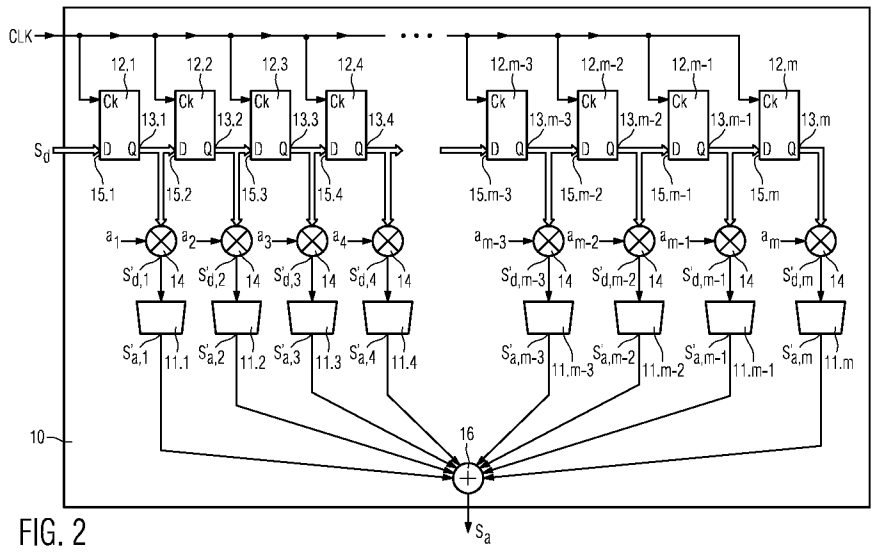

FIG. 2

(57) Abstract: A FIRDAC (10) comprises a Finite Impulse Response filter structure (12.1-12.k) and a plurality of digital to analog converter units (11.1-1 l.k) associated with filter tap weights (a_1- a_m) of the filter structure (12.1-12.k). The clamp value of each digital to analog converter unit (11.1-11.k) depends on its associated filter tap weight (a_1-a_m).

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FIR digital to analog converter

FIELD OF THE INVENTION

The invention relates to an FIR analog to digital converter.

BACKGROUND OF THE INVENTION

Digital to analog converters, abbreviated as DACs are in general known in the art. The structure of FIR digital to analog converters (FIRDACs) simultaneously combines the functions of a DAC with a Finite Impulse Response (FIR) filter.

A DAC block can be implemented as single or multiple bits. Multiple bits are normally coded in a binary fashion, that is the signal amplitude at a given time sample, is represented by one out of a set of discrete states, each state being equally spaced with respect to its neighboring states. The signal is represented by a numerical value coded with n bits, taking a value between 1 and 2^n. Use of discrete set of values create a quantization error, since signal amplitudes that normally lie between these discrete steps are replaced by the closest allowed value, creating an approximation, or coding error.

Considering the quantization step to be equal to ±1/2 bit size, it can be shown that the RMS noise amplitude equals $1/\sqrt{12}$ bit and that an n-bit converter can achieve a peak signal to noise power ratio of $(6 \cdot n + 4)$ dB for a sinusoid output.

We further have:

$$\text{Quantization Noise Power} = \frac{\Delta^2}{12};$$

$$\text{Maximum Sinusoidal Power} = \frac{\Delta^2}{8} \cdot 2^{2n}$$

wherein Δ is the quantization step size and n is the number of bits.

The DAC operating speed is set by a clock frequency at which the signal amplitude samples are updated. This rate determines the bandwidth of a signal that can be reproduced without aliasing errors, as defined by Nyquist. His name is given to the bandwidth limit, equal to half the clock frequency, in which the quantization noise is

considered to be uniformly spread. The quantization error is characterized by a Gaussian distribution.

In practice, the useful signal bandwidth is restricted to a portion of the Nyquist limit, due to the need to implement a reconstruction filter.

In many cases the DAC output is created by summing an integral number of nominally identical unit sources. These may be currents or voltages, across a resistor ladder network. There may be the following advantages to this approach: Each unit source is built with a single device that can be more easily laid out in as symmetrical and as well-matched manner. Also dynamic element matching techniques can be used in a systematic way between all unit sources.

The term "Finite Impulse Response" is given to a filter structure that employs no feedback. The filter output is created by summing weighted samples of the input signal at different time instances. Although this can be implemented in a pure analog way, for instance, with an analog delay line, or to an analog signal with sampled delays introduced by a CCD, mostly FIR filters are realized by digital signal processing.

The time coefficient weights are often chosen in order to perform a wanted frequency domain transfer function. These are often referred to as "windows", since the filter has a limited length. It only takes into account samples within a certain interval, fixed by the number of filter taps and the clock period (or the total analog delay used). Outside this window the filter ignores the input signal, which is equivalent to applying zero coefficients.

A FIRDAC is a circuit that implements many unit DACs, whose digital inputs receive the product of the weighting coefficient and the signal amplitude value at a given sample time. The DAC outputs are then summed. Alternatively, the multiplying coefficients can be implemented by a weighted sum of the DAC outputs, the digital inputs being then just the instantaneous signal value at that sample time. The former implementation is often preferred since digital multiplication can be made arbitrarily precise, or error free, whereas weighted analog sums may suffer in practice by component value errors, due to manufacturing tolerances and random variations.

U.S.-patent No. 6,816,097 B2 discloses features of a finite impulse response (FIR) filter to be incorporated into a multi-bit DAC. The multi-bit DAC includes an *N*-tap delay line and *N* multi-bit sub-DACs. Each multi-bit sub-DAC includes a plurality of binary weighted or unit elements (i.e., substantially equal weighted elements). The elements are driven by a digital signal and produce respective analog output signals which are summed to generate an analog output signal of the relevant multi-bit sub-DAC. The *N*-tap delay line includes *N* multi-bit delay elements. The first of the *N* multi-bit delay elements receives a

multi-bit digital signal and produces a delayed multi-bit output signal therefrom. Each of the other *N* multi-bit delay elements receives a delayed multi-bit output signal from an immediately preceding one of the *N* multi-bit delay elements and produces a respective delayed multi-bit output signal therefrom. Each multi-bit sub-DAC is driven by a respective one of the delayed multi-bit output signals produced by a corresponding one of the *N* multi-bit delay elements and produces an analog output signal therefrom. A sum of the analog outputs from the *N* multi-bit sub-DACs is the analog output signal of the entire multi-bit DAC.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the present invention to provide an FIR digital to analog converter with an improved structure.

The object is achieved in accordance with the invention by means of a FIRDAC, comprising a Finite Impulse Response filter structure and a plurality of digital to analog converter units associated with filter tap weights of the filter structure; wherein the clamp value of each digital to analog converter unit depends on its associated filter tap weight.

As discussed above, a FIRDAC is a digital to analog converter which implements a Finite Impulse Response (FIR) filter structure with several digital to analog (DAC) units. The FIR filter structure may be realized by a sequence of delay elements whose output signals may be weighted (filter tap weight or filter coefficients). The delay elements may be realized by sequentially cascaded flip flops and the filter tap weights may be realized by multiplying the relevant delay digital signal by the relevant filter coefficient.

The filter tap weights may be chosen such that the Finite Impulse Response filter structure has low-pass characteristics, the first half of the filter tap weights may have increasing values and the second half of the filter tap weights have decreasing values, and/or the filter tap weights may be chosen such that the corresponding time window is vertically and horizontally symmetric.

The individual delayed and weighted digital signals are the input signals to the DAC units whose output signals may be added up to create the output signal of the inventive FIRDAC.

Since the level of the weighted tap signals of the filter structure are limited dependent on the relevant tap weight, the clamp value of the DAC units of the inventive FIRDAC are adjusted to the associated filter tap weight.

Generally, different types of digital to analog converters can be used for the inventive FIRDAC. Particularly, the individual digital to analog converter units may

comprise a plurality of unit sources whose output signals add up to an analog signal corresponding to a digital signal fed to the plurality of unit sources. The unit sources may be currents or voltages, across a resistor ladder network. Such DAC units have the advantage that each unit source can be build with a single device that can be more easily laid out in as symmetric and as well-matched manner. Also dynamic element matching techniques can be used in a systematic way between all unit sources.

Such DAC units can be described by the following binary DAC transfer function:

$$S_{out} = \frac{S_{ref}}{2^n} \sum_{i=1,n} b_i 2^{i-1}$$

wherein S_{ref} is a reference value and b_i represents the digital value of the i^{th} bit in an n bit word encoded in the digital signal of the relevant analog to digital converter. The reference value may be a reference voltage or current, depending on the mode of operation of the DAC units. Then, each digital to analog converter unit may comprise the same number of unit sources, wherein the reference value of a given analog digital converter unit is related to its associated filter tap weight. Thus adjusting the reference values of the individual DAC units dependent on their associated filter tap weights adjusts the clamp value of the relative DAC unit. Particularly, the reference value of a given digital to analog converter unit may be proportional to its associated tap weight. In such a FIRDAC, each DAC unit may retain its ability to distinguish signal details across n bits, or 2^n discrete states, the number used to code the signal amplitude of the digital signal input to the FIR filter structure.

Alternatively, the associated tap weight can be obtained by appropriately choosing the reference values. For this embodiment of the inventive FIRDAC the delayed digital signals output by the respective delay elements are not multiplied by the filter coefficients, but the filter coefficients are realized by appropriately adjusting the reference value of the DAC units.

In another embodiment of the inventive FIRDAC, the number of unit sources of a given digital to analog converter is related to its associated filter tap weight. For this variant of the inventive FIRDAC, a product in the digital domain can implement the weighting, i.e. the digital signals by the filter structure are multiplied by the relevant filter coefficients so that an adjusted (weighted) signal level for each tap is fed to its respective DAC unit. Then, particularly whilst keeping the same level of the reference signals for each DAC unit, the inventive FIRDAC can be implemented with reduced and rationed number of unit sources, particularly corresponding to the peak signal that needs to be created. In other words, the

number of unit sources for each of the DAC units is not the same for each DAC unit, but corresponds to the associated filter tap weight. This may have the advantage that each DAC unit has the same absolute quantization noise. A further advantage of this embodiment is that the FIRDAC requires a reduced number of unit sources, reducing the area needed for its implementation. Alternatively, unit sources not needed for a specific DAC unit can be reallocated to DAC units whose input signals have potentially higher levels, resulting in a FIRDAC with a higher quantization.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail hereinafter, by way of non-limiting examples, with reference to the embodiments shown in the drawings.

Fig. 1 shows a DAC unit comprising a plurality of unit sources;

Fig. 2 shows a FIRDAC comprising several DAC units;

Fig. 3 represents the filter characteristics of a FIR filter structure of the FIRDAC; and

Fig. 4 illustrates the allocation of unit sources.

DESCRIPTION OF EMBODIMENTS

Fig. 1 shows an exemplary multi-bit digital to analog converter (DAC) unit 1 which is *per se* known in the art. The DAC unit 1 is configured to convert a digital signal S'_d into a corresponding analog signal S'_a, and comprises k unit sources 2.1-2.k and a summing device 3. The unit sources 2.1-2.k are driven by the digital Signal S'_d and produce k analog output signals 4.1-4.k therefrom. The analog output signals 4.1-4.k are fed to the summing device 3 which adds the analog output signals 4.1-4.k in order to produce the analog signal S'_a. The unit sources 2.1-2.k may, for instance, be identical current or voltage sources and particularly be build as single devices each.

Fig. 2 shows a FIRDAC 10 which is configured to convert a digital signal S_d into a corresponding analog signal S_a. The FIRDAC 10 comprises a plurality of DAC units 11.1-11.m which may be similar to the DAC unit 1 of Fig. 1 for the exemplary embodiment. The FIRDAC 10 further comprises a Finite Impulse Response (FIR) filter structure which may be implemented as sequentially cascaded D-flip flops 12.1-12.m whose output signals 13.1-13.m are multiplied with filter coefficients a_1-a_m, utilizing multiplier devices 14, in order to produce digital signals $S'_{d,1}$ - $S'_{d,m}$ that are weighted digital signals of the FIRDAC 10 at a given sample time. The digital signals $S'_{d,1}$ - $S'_{d,m}$ are the input signals for the individual DAC units 11.1-11.m. For the exemplary embodiment, the FIRDAC 10 comprises m flip

flops 12.1-12.m and m DAC units 11.1-11.m. Each DAC unit 11.1-11.m produces an analog signal $S'_{a,1}$-$S'_{a,m}$ which are added to the analog signal S_a of the FIRDAC 10 utilizing a summing device 16.

The FIR filter structure of Fig. 2 is basically a shift register comprising the plurality of sequentially cascaded flip-flops 12.1-12.m. The digital signal S_d is fed to the input 15.1 of the first flip flop 12.1. The output signal 13.1 of the first flip flop 12.1 is fed to the input 15.2 of the second flip flop 12.2 which produces the output signal 13.2. The output signal 13.2 in turn is fed to the input 15.3 of the third flip flop 12.3, etc. The flip flops 12.1-12.m are further clocked by a clock signal CLK and basically realize delay elements.

Fig. 3 shows examples of filter coefficients a_1-a_m of the FIR filter structure in the form of windows 31-33. For the exemplary embodiment, the filter coefficients a_1-a_m are illustrated as relative weights, wherein m=100. The filter coefficients shown in Fig. 3 correspond to low-pass FIR filters. Other filter characteristics, such as band-pass, high-pass, or stop-pass filter characteristics can also be implemented.

The exemplary embodiment shown in Fig. 3 depicts three different window functions, namely a Hamming window 31, a triangle-window 32, and a Hanning window 33. Associated with each window 31-33 is its frequency domain response. For instance the triangular window 32 (triangular weight function) creates a $\mathrm{Sin}^2(x)/x^2$ frequency response. The raised cosine window (Hanning window 33) gives the best approximation to a so-called brick-wall function - no pass-band attenuation plus total stop-band attenuation. The filter bandwidth is determined by the total delay of the FIR filter structure. This delay is the product of the number of taps (flip flops 12.1-12.m) times the period of the clock signal CLK.

All the low-pass filter approximations shown in Fig. 3 are characterized by windows 31-33 that have increasing value filter coefficients for the first half of the relevant time window, and decreasing value filter coefficients during the second half. The windows 31-33 are symmetric, not only horizontally but also vertically. Particularly between a quarter and three quarters way through the windows 31-33, the corresponding filter coefficient (weight) is above ½, whereas before a quarter and after three quarters way through, the weight is below ½.

Generally, the digital signal S_d for the FIGDAC 10 is coded within a given numerical range. Often time the maximum level is normalized to 1, the number of bits then determines the value of the smallest fraction of the digital signal S_d that can be distinguished (the quantization step). Therefore, the maximum signal to be realized by successive DAC units 11.1-11.m in the FIRDAC 10 reflects the relative weight of the filter coefficient a_1-a_m at

that point. For the exemplary embodiment, the DAC units 11.1-11.m are thus implemented so that their respective clamp values depend on the time step (its position in the window 31-33), i.e. the corresponding filter coefficient a_1-a_m, as illustrated by a waveform 34 of Fig. 3.

Typical binary DAC transfer functions, i.e. the binary transfer functions of the DAC units 11.1-11.m, can be represented by

$$S_{out} = \frac{S_{ref}}{2^n} \sum_{i=1,n} b_i 2^{i-1}$$

wherein b_i represents the digital value of the i^{th} bit in an n bit word. The signals S_{out} and S_{ref} may particularly be voltages (V_{out} and V_{ref}) or currents (I_{out} and I_{ref}), dependent on the mode the DAC units 11.1-11.m are operating.

Thus, the individual DAC units 11.1-11.m receive each two input signals, the reference signal S_{ref} and the digital word.

In a first embodiment, the clamp functions of the individual DAC units 11.1-11.m are performed by adjusting the level of the respective reference signal S_{ref}. For the exemplary embodiment, each DAC unit 11.1-11.k has the same number of k unit sources 2.1-2.k, wherein k may particularly equal n. Only the reference signals S_{ref} for the individual DAC units 11.1-11.m are adjusted in accordance with the corresponding filter coefficient a_1-a_m of the FIR filter structure.

For the exemplary embodiment, m equals 100 and the FIR filter structure has low-pass characteristics, wherein the filter coefficient a_1-a_{100} are described by the windows 31, 32, or 32. In order to adjust the reference signals S_{ref} for the individual DAC units 11.1-11.100 they may particularly be adjusted as illustrated by the waveform 34 of Fig. 3, such that the reference signals S_{ref} for the first half DAC units 11.1-11.50 increases for the individual DAC units 11.1-11.50 and decreases for the second half DAC units 11.51-11.100. Particularly for the exemplary embodiment and using normalized values for the reference signals S_{ref}, the reference signals S_{ref} for the individual DAC units 11.1-11.3 is 0,1, for the individual DAC units 11.4-11.9 is 0,23, for the individual DAC units 11.10-11.15 is 0,37, for the individual DAC units 11.16-11.21 is 0,5, for the individual DAC units 11.22-11.27 is 0,63, for the individual DAC units 11.28-11.32 is 0,77, for the individual DAC units 11.33-11.38 is 0,89, for the individual DAC units 11.39-11.61 is 1,0, for the individual DAC units 11.62-11.67 is 0,89, for the individual DAC units 11.68-11.73 is 0,77, for the individual DAC units 11.74-11.79 is 0,63, for the individual DAC units 11.80-11.85 is 0,5, for the individual DAC units 11.86-11.91 is 0,37, for the individual DAC units 11.92-11.97 is 0,23, and for the

individual DAC units 11.98-11.100 is 0,1.

In this embodiment, each DAC unit 11.1-11.m can retain its ability to distinguish signal details across n bits, or 2^n discrete states, the number used to code the signal amplitude through the cascaded flip flops 12.1-12.m.

In a second embodiment, no multiplier devices 14 are used for the FIRDAC 10 and the filter coefficient a_1-a_m are realized by choosing the reference signals S_{ref} for the individual DAC units 11.1-11.m according to the desired values of the filter coefficients a_1-a_m.

In a third embodiment, a product in the digital domain can implement the weighting, an adjusted signal level for each tap is fed to its respective DAC unit 11.1-11.m. Then, whilst keeping the same level of the reference signals S_{ref} for each DAC unit 11.1-11.m, the FIRDAC 10 can be implemented with reduced and rationed number of unit sources 4.1-4.k, corresponding to the peak signal that needs to be created. In other words, the number k of unit sources 4.1-4.k for each of the DAC units 11.1-11.m is not the same for each DAC unit 11.1-11.m, but corresponds to the associated filter coefficient a_1-a_m.

If implementing the filter characteristics as described by the windows 31-33, then the number of unit sources 4.1-4.k increases for the first half DAC units 11 and decreases for the second half DAC units 11. As a result, for a given total area spent on unit sources 4 for the FIRDAC 10, unused unit sources that are thus liberated can be devoted to the part of the window 31-33 that has higher weighting. In other word, for a transfer function whose average coefficient weight across the window is close to 0,5, unit sources can be reattributed to create weights varying between 0 and 2, with an average close to 1. In this way the highest level signals S'_a, in the middle of the relevant window 31-33, can be coded with twice the previous signal strength (at a constant absolute quantization noise value). This is equivalent to adding an extra bit.

Fig. 4 illustrates the case of unit sources 4 used to provide a triangular window function. Each square represents the contribution of a unit source 4. It also can represent the die area per unit source for the FIRDAC 10. A rectangular area 40 with edge lengths a, b represents a FIRDAC whose DAC units have each the same number of unit sources. This area is transformed by reallocating unit sources corresponding to a first triangularly shaped area 41, which is a sub-area of the rectangular area 40, to a second triangularly shaped area 42, and unit sources corresponding to a third triangularly shaped area 43, which is a sub-area of the rectangular area 40, to a fourth triangularly shaped area 44. Thus, the window functions presenting both horizontal and vertical symmetry can profit from such transformation. The total number of unit sources stays constant, as can be verified by

counting the squares.

For the embodiments described above, each DAC unit 11.1-11.m of the FIRDAC 10 comprises the summing devices 3. These summing devices 3 can be omitted such that the corresponding signals of the unit sources 4 are added by the summing device 16.

Finally, it should be noted that the aforementioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. In a device claim enumerating several means, several of these means may be embodied by one and the same item of software or hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A FIRDAC comprising:

a Finite Impulse Response filter structure (12.1-12.k); and

a plurality of digital to analog converter units (11.1-11.k) associated with filter tap weights (a_1-a_m) of the filter structure (12.1-12.k); wherein the clamp value of each digital to analog converter unit (11.1-11.k) depends on its associated filter tap weight (a_1-a_m).

2. The FIRDAC of claim 1, wherein each of the digital to analog converter units (11.1-11.k) comprises a plurality of unit sources (4.1-4k) whose output signals (4.1-4.k) add up to an analog signal (S'_a) corresponding to a digital signal (S'_d) fed to the plurality of unit sources (4.1-4.k).

3. The FIRDAC of claim 2, wherein the unit sources (4.1-4.k) are current or voltage sources.

4. The FIRDAC of claim 2, wherein each digital to analog converter unit (11.1-11.k) comprises the same number of unit sources (4.1-4.k) and the output signals (S'_a) of the digital to analog converters (11.1-11.k) are described by

$$S'_a = \frac{S_{ref}}{2^n} \sum_{i=1,n} b_i 2^{i-1}$$

wherein S_{ref} is a reference value and b_i represents the digital value of the i^{th} bit in an n bit word encoded in the digital signal (S'_d) of the relevant analog to digital converter (11.1-11.k); and wherein the reference value of a given analog digital converter unit (11.1-11.k) is related to its associated filter tap weight (a_1-a_m).

5. The FIRDAC of claim 4, wherein the unit sources (4.1-4.k) are unit current sources and the reference value is a reference current; or wherein the unit sources (4.1-4.k) are voltage sources and the reference value is a reference voltage.

6. The FIRDAC of claim 4, wherein the reference value of a given digital to analog converter unit (11.1-11.k) is proportional to its associated tap weight (a_1-a_m).

7. The FIRDAC of claim 2, wherein the number of unit sources (4.1-4.k) of a given digital to analog converter (11.1-11.k) is related to its associated filter tap weight (a_1-a_m).

8. The FIRDAC of claim 1, wherein

the filter tap weights (a_1-a_m) are chosen such that the Finite Impulse Response filter structure (12.1-12.k) has low-pass characteristics;

the first half of the filter tap weights (a_1-a_m) have increasing values and the second half of the filter tap weights (a_1-a_m) have decreasing values; and/or

the filter tap weights (a_1-a_m) are chosen such that the corresponding time window (31-33) is vertically and horizontally symmetric.

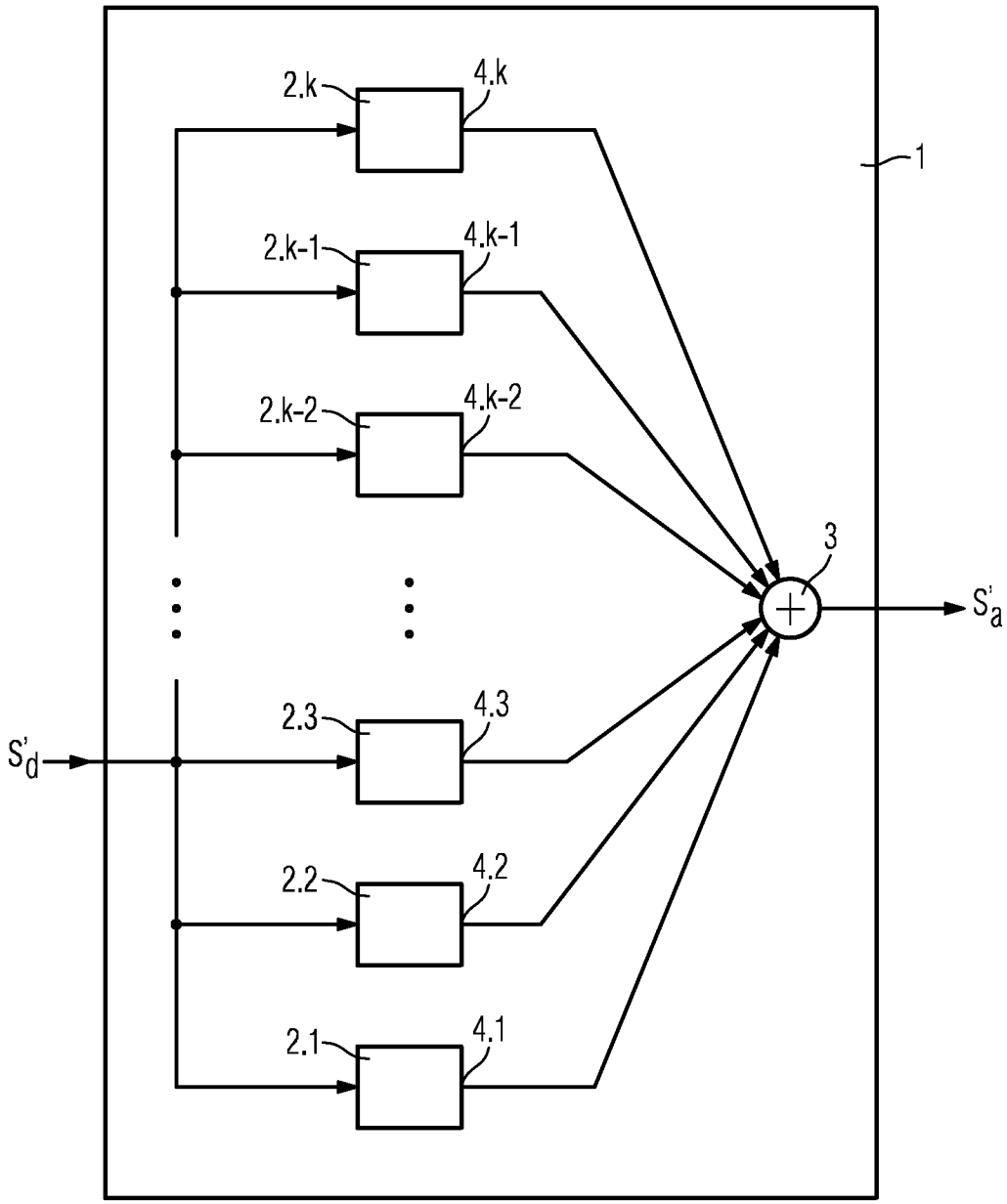
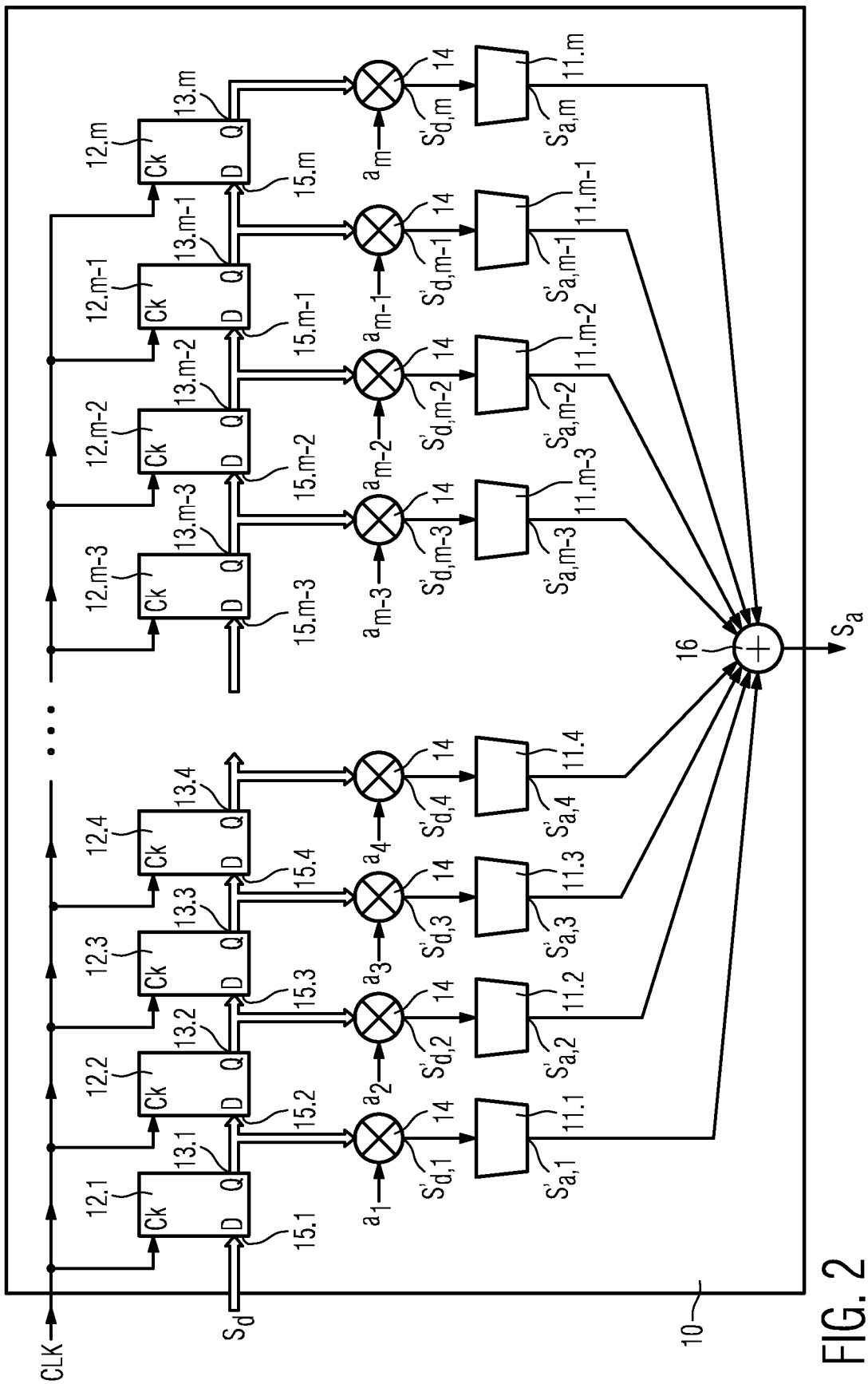


FIG. 1


CLK
S_d
10
16
S_a
12.1
12.2
12.3
12.4
12.m-3
12.m-2
12.m-1
12.m
13.1
13.2
13.3
13.4
13.m-3
13.m-2
13.m-1
13.m
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15.2
15.3
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$S'_{a,4}$
$S'_{a,m-3}$
$S'_{a,m-2}$
$S'_{a,m-1}$
$S'_{a,m}$
11.1
11.2
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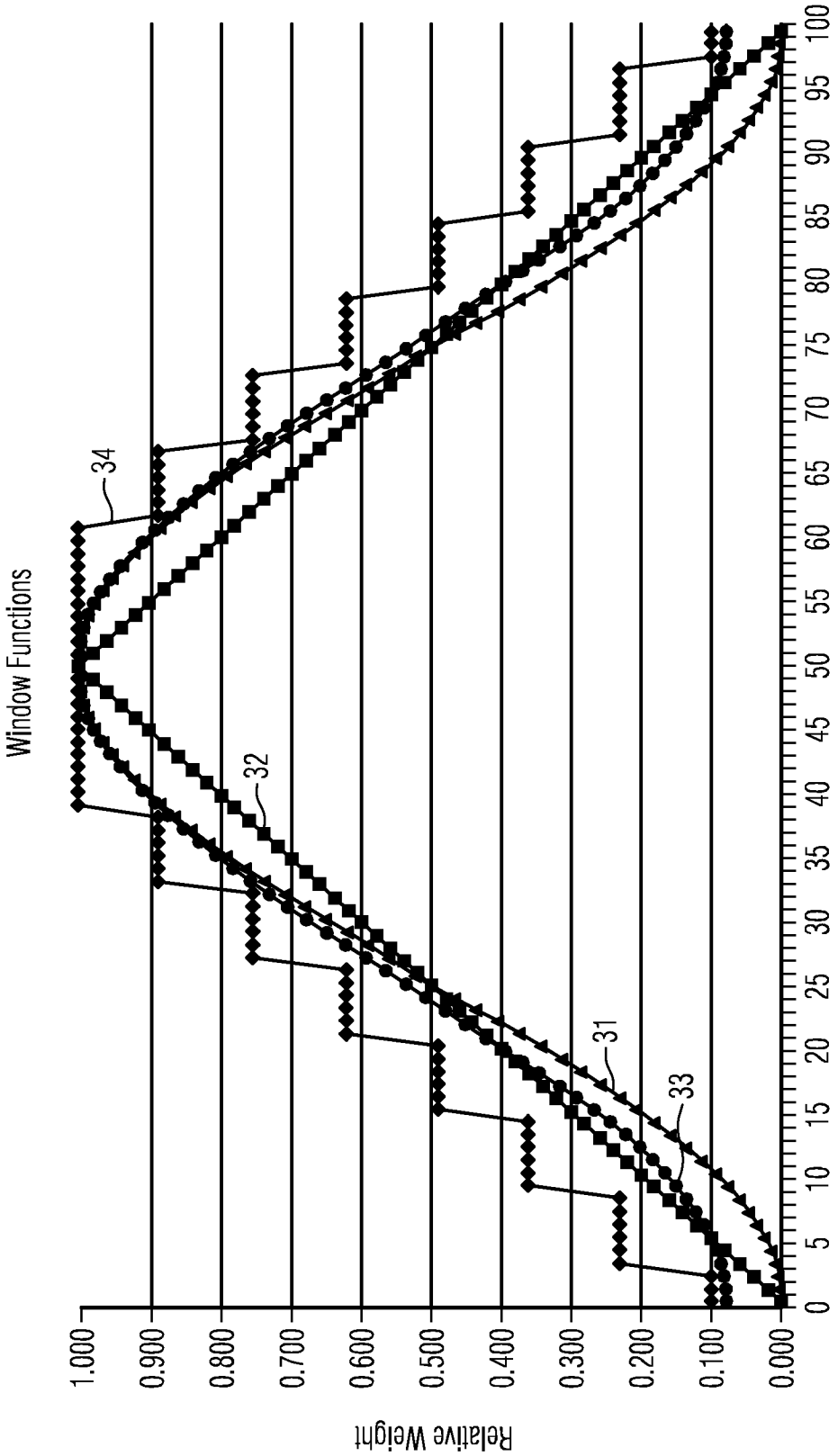
11.m-1
11.m
14
Ck
D
Q

FIG. 2


Window Functions
Relative Weight
Time Sample
1.000
0.900
0.800
0.700
0.600
0.500
0.400
0.300
0.200
0.100
0.000
0
5
10
15
20
25
30
35
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80
85
90
95
100
31
32
33
34

FIG. 3

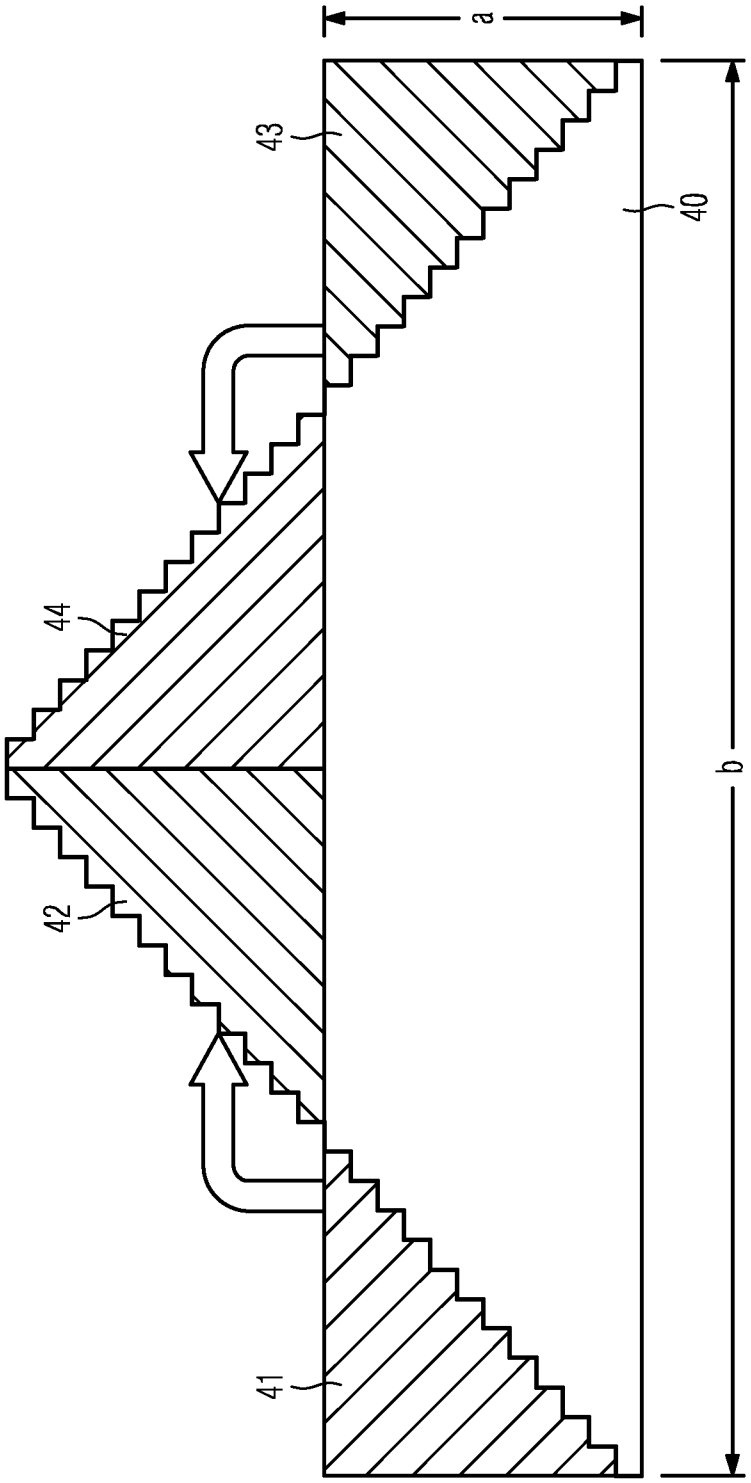

FIG. 4