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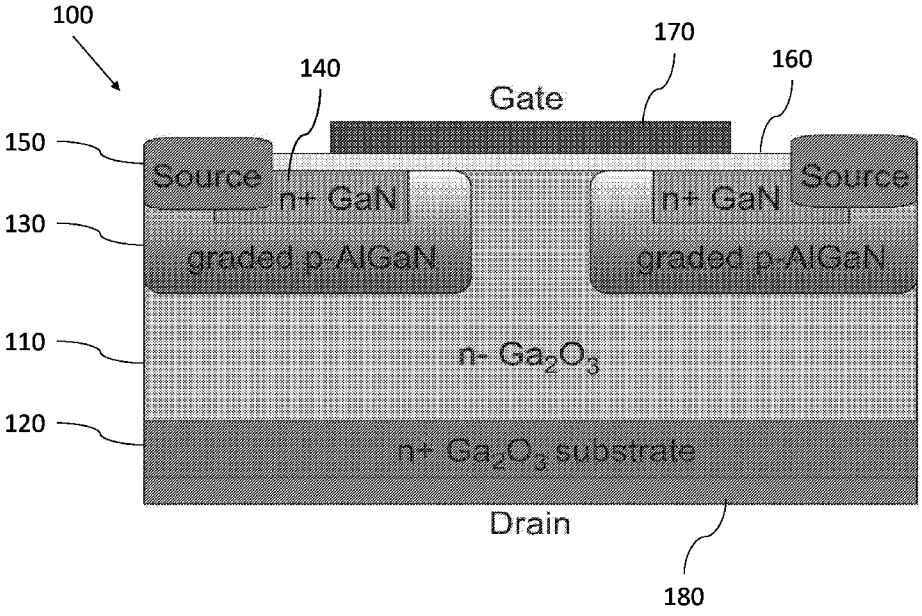
(54) Title: NORMALLY-OFF GALLIUM OXIDE BASED VERTICAL TRANSISTORS WITH P-TYPE ALGAN BLOCKING LAYERS

FIG. 1



(57) Abstract: A field-effect transistor includes an n-type gallium oxide substrate having a first doping concentration; an n-type gallium oxide drift layer on a first side of the substrate and having a second doping concentration smaller than the first doping concentration, a p-type Ill-nitride first base layer on the drift layer, and an n-type Ill- nitride source layer on the first base layer and having a third doping concentration larger than the second doping concentration. A method of forming the field-effect transistor includes providing an n-type gallium oxide drift layer having a first doping concentration on a first side of an n-type gallium oxide substrate having a second doping concentration larger than the first doping concentration, forming a p-type Ill- nitride first base layer on the drift layer, and forming an n-type Ill-nitride source layer on the first base layer and having a third doping concentration larger than the first doping concentration.

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[Continued on next page]

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NORMALLY-OFF GALLIUM OXIDE BASED VERTICAL TRANSISTORS WITH P-TYPE AlGaN BLOCKING LAYERS

BACKGROUND

1. Field

[0001] Aspects of embodiments of the present invention relate to Gallium oxide based vertical transistors.

2. Description of Related Art

[0002] Most semiconductor transistor designs feature a normally-on operation and with a lateral (or horizontal) layout. Transistors with vertical structures, however, have been developed in silicon-based technology. Vertical diodes having only two terminals have also been developed, but lack a transistor capability.

SUMMARY

[0003] Aspects of embodiments of the present invention are directed toward a normally-off vertical transistor structure utilizing n-type gallium oxide as the drift layer, p-type III-nitride (such as aluminum gallium nitride and/or gallium nitride) as the blocking layer, and n-type III-nitride (such as gallium nitride) for source contacts. Further aspects are directed toward gallium oxide based vertical transistors having p-type aluminum gallium nitride layers, which avoid the lack of p-type dopant for gallium oxide. Still further aspects are directed toward three-terminal vertical transistors utilizing gallium oxide as the drift layer.

[0004] According to an embodiment of the present invention, a field-effect transistor is provided. The field-effect transistor includes an n-type gallium oxide substrate having a first doping concentration, an n-type gallium oxide drift layer on a first side of the substrate and having a second doping concentration smaller than the first doping concentration, a p-type III-nitride first base layer on the drift layer, and an n-type III-nitride source layer on the first base layer and having a third doping concentration larger than the second doping concentration.

[0005] The field-effect transistor may include further include: a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer; and a gate electrode on the gate insulator layer.

[0006] The field-effect transistor may further include: a drain ohmic contact on a second side of the substrate, the second side facing away from the first side; and source ohmic contacts in contact with the source layer and the first base layer.

[0007] The first base layer may include aluminum gallium nitride.

[0008] The first base layer may include a constant composition of aluminum.

[0009] The first base layer may include a graded composition of aluminum having a greatest composition of aluminum at a boundary with the drift layer and a least composition of aluminum proximal to the source layer.

[0010] The greatest composition of aluminum may be at least 70% of the molar composition of aluminum and gallium in the first base layer.

[0011] The field-effect transistor may further include a p-type gallium nitride second base layer between the first base layer and the source layer.

[0012] The source layer may include gallium nitride.

[0013] According to another embodiment of the present invention, a method of forming a field-effect transistor is provided. The method includes providing an n-type gallium oxide drift layer having a first doping concentration on a first side of an n-type gallium oxide substrate having a second doping concentration larger than the first doping concentration, forming a p-type III-nitride first base layer on the drift layer, and forming an n-type III-nitride source layer on the first base layer and having a third doping concentration larger than the first doping concentration.

[0014] The method may further include: forming a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer; and forming a gate electrode on the gate insulator layer.

[0015] The method may further include: forming a drain ohmic contact on a second side of the substrate, the second side facing opposite to the first side; and forming source ohmic contacts contacting the source layer and the first base layer.

[0016] The first base layer may include aluminum gallium nitride.

[0017] The forming of the first base layer may include grading a composition of aluminum such that a greatest composition of aluminum is at a boundary with the drift layer and a least composition of aluminum is proximal to the source layer.

[0018] The greatest composition of aluminum may be at least 70% of the molar composition of aluminum and gallium in the first base layer.

[0019] The method may further include forming a p-type gallium nitride second base layer between the first base layer and the source layer.

[0020] The forming of the first base layer may include selectively etching the drift layer, and regrowing the first base layer in the selectively etched drift layer.

[0021] The regrowing of the first base layer in the selectively etched drift layer may include regrowing an n-type III-nitride layer in the selectively etched drift layer, and regrowing the first base layer on the regrown n-type III-nitride layer.

[0022] The forming of the source layer may include selectively etching the first base layer, and regrowing the source layer in the selectively etched first base layer.

[0023] The method may further include regrowing a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer.

[0024] The method may further include: selectively etching the gate insulator layer; forming source ohmic contacts contacting the source layer, the first base layer, and the selectively etched gate insulator layer; and forming a gate electrode on the gate insulator layer.

[0025] The above and other embodiments of the present invention provide for gallium oxide based vertical transistors with p-type III-nitride layers that are capable of handling higher power density than comparable designs, and enabling better breakdown voltage (BV) scaling without increasing device footprint. Such transistors are useful for power electronics applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The patent or application file contains at least one drawing executed in color. Copies of this patent or patent application publication with color drawing(s) will be provided by the Office upon request and payment of the necessary fee.

[0027] The accompanying drawings, together with the specification, illustrate example embodiments of the present invention. These drawings, together with the description, serve to better describe aspects and principles of the present invention.

[0028] FIG. 1 is a schematic cross-section of an example gallium oxide-based vertical transistor according to an embodiment of the present invention.

[0029] FIG. 2 is a band diagram of a comparable Ga_2O_3/GaN junction.

[0030] FIG. 3 is a band diagram of an example Ga_2O_3/AlGaN junction according to an embodiment of the present invention.

[0031] FIG. 4 is a schematic cross-section of an example p-type AlGaN base layer design according to an embodiment of the present invention.

[0032] FIG. 5 is a schematic cross-section of an example p-type AlGaN and GaN base layer design according to an embodiment of the present invention.

[0033] FIG. 6 is a flow diagram of an example method of creating a gallium oxide-based vertical field-effect transistor according to an embodiment of the present invention.

[0034] FIGs. 7–32 are schematic cross-sections illustrating an example method of manufacturing a gallium oxide-based vertical field-effect transistor according to an embodiment of the present invention.

[0035] FIG. 33 is a transmission electron microscopy (TEM) image of a cross section of a comparable gallium nitride on gallium oxide substrate device.

DETAILED DESCRIPTION

[0036] The following description is provided to enable one of ordinary skill in the art to make and use embodiments of the present invention and to incorporate such

embodiments in the context of particular applications. Various modifications, as well as a variety of uses in different applications will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to a wide range of embodiments. Thus, the present invention is not intended to be limited to the embodiments presented, but is to be accorded the widest scope consistent with the aspects, principles, and novel features disclosed herein.

[0037] As used herein, the term "substantially," "about," and similar terms are used as terms of approximation and not as terms of degree, and are intended to account for the inherent deviations in measured or calculated values that would be recognized by those of ordinary skill in the art.

[0038] In addition, any numerical range recited herein is intended to include all sub-ranges of the same numerical precision subsumed within the recited range. For example, a range of "1.0 to 10.0" is intended to include all subranges between (and including) the recited minimum value of 1.0 and the recited maximum value of 10.0, that is, having a minimum value equal to or greater than 1.0 and a maximum value equal to or less than 10.0, such as, for example, 2.4 to 7.6. Any maximum numerical limitation recited herein is intended to include all lower numerical limitations subsumed therein and any minimum numerical limitation recited in this specification is intended to include all higher numerical limitations subsumed therein. Accordingly, Applicant reserves the right to amend this specification, including the claims, to expressly recite any sub-range subsumed within the ranges expressly recited herein.

[0039] In the detailed description that follows, numerous specific details are set forth in order to provide a more thorough understanding of some of the embodiments of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without necessarily being limited to these specific details. In other instances, well-known structures and devices may be shown in block diagram form, rather than in detail, in order to avoid obscuring aspects of the present invention.

[0040] The reader's attention is directed to all papers and documents that are filed concurrently with this specification and that are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference. All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same, equivalent, or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is only one example of a generic series of equivalent or similar features. Similarly, unless indicated to the contrary, features of one embodiment may be

incorporated into other embodiments without departing from the spirit and scope of the present invention.

[0041] Furthermore, any element in a claim that does not explicitly state "means for" performing a specified function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. § 112(f). In particular, the use of "step of" or "act of" in the claims herein is not intended to invoke the provisions of 35 U.S.C. § 112(f).

[0042] By way of example, various embodiments of the present invention are directed toward normally-off gallium oxide based vertical transistors. However, these embodiments are presented as examples and the present invention is not limited thereto.

[0043] Embodiments of the present invention are directed to utilizing p-type nitride materials (e.g., III-nitride materials such as aluminum gallium nitride and/or gallium nitride), that have established (or mature) p-doping techniques as well as high breakdown properties, in vertical transistor designs. On-resistance is an important parameter for transistors. Lower on-resistance may lower power consumption, which may improve transistor design. Embodiments of the present invention provide for a way to reduce the on-resistance utilizing the positive conduction band offset between aluminum gallium nitride and gallium oxide. Such transistors may play an important role in power electronics development.

[0044] A figure of merit is a quantity that characterizes a device's performance (relative to comparable devices). In power semiconductor devices, the Baliga figure of merit (FOM) may be used to measure how suitable a material is for high frequency devices based on the intrinsic properties of the material. The FOM is defined as $\varepsilon\mu E_g^3$, where ε is the (static) dielectric constant, μ is the electron mobility, and E_g is the band gap of the semiconductor. Using this FOM, gallium oxide (e.g., Ga_2O_3) has the highest figure of merit compared to comparable materials, such as Si (more than 300× better), SiC (more than 4× better), and gallium nitride (e.g., GaN). The manufacturing method for the gallium oxide substrates may be similar to that used for Si. Therefore, gallium oxide may be suitable to be used for low-cost high power electronics where low power consumption and relatively high frequency applications are desired. Gallium oxide, for example, has potential to reduce energy loss by 50% in electric vehicle motor drives and may be used in modern electronics from battery chargers to smart-grid components.

[0045] Example embodiments of the present invention will now be described in more detail with reference to the accompanying drawings. In the drawings, the same or similar reference numerals refer to the same or similar elements throughout. Expressions such as "at least one of," "one of," or "selected from," when preceding a

list of elements, modify the entire list of elements and do not modify the individual elements of the list. Herein, the use of the term "may," when describing embodiments of the present invention, refers to "one or more embodiments of the present invention." In addition, the use of alternative language, such as "or," when describing embodiments of the present invention, refers to "one or more embodiments of the present invention" for each corresponding item listed.

[0046] FIG. 1 is a schematic cross-section of an example gallium oxide-based vertical transistor 100 according to an embodiment of the present invention.

[0047] Referring to FIG. 1, the vertical transistor 100 uses lightly doped (such as $\leq 10^{17}/cm^3$ doping concentration) n-type gallium oxide (such as gallium (III) oxide, e.g., Ga_2O_3) as a drift layer 110, which is grown on a first side (such as a front side) of a heavily doped (e.g., conductive or degenerate) n-type gallium oxide substrate 120 (for example, as available from commercial substrate vendors, such as a 500 μm gallium oxide substrate). The drift layer 110 may be at least 0.5 μm thick, and as much as 12 μm (or more) thick (the thicker the drift layer 110, the more voltage that can be processed by the transistor 100). The drift layer thickness may determine the device breakdown voltage and the resistance of the device. A thin drift layer may lead to low breakdown voltage and a low on-resistance. The breakdown voltage may be selected based on the application requirement. A low on-resistance may reduce the energy loss from power electronics. In general, there is not a fundamental limit for the drift layer thickness.

[0048] Herein, unless otherwise specified, the use of relative terms such as "lightly doped" and "heavily doped" are as would be interpreted by someone of ordinary skill in the art. For example, lightly doped may be $\leq 10^{17}/cm^3$ doping concentration, while heavily doped may be enough to produce a degenerate (e.g., conductive) semiconductor. In other embodiments, the gallium oxide in the drift layer 110 may be a ternary or quaternary compound, such as tin gallium oxide.

[0049] The n-type gallium oxide drift layer 110 may be patterned and etched (e.g., selectively etched) for p-type blocking layer regrowth. By applying regrowth techniques as known by those of ordinary skill in the art, p-type (e.g., lightly doped p-type) III-nitride, such as aluminum gallium nitride (e.g., AlGaN, such as $Al_xGa_{1-x}N$, $0 < x < 1$, or an alloy of AlN and GaN in different proportions) may be grown or annealed as a blocking layer 130 (or base layer). The blocking layer 130 may serve to block the vertical electron flow (such as from source to drain) when the transistor is turned off. The thickness of the blocking or base layer 130 may be between 300 nm and 1 μm (or more, such as 2 μm or even 10 μm, provided the processing technique allows such a base layer to be formed).

[0050] The blocking layer should not be too thin. Otherwise, there may be punch-through breakdown that may limit the device when working under high voltage. On the other hand, if the blocking layer is too thick, it may result in processing difficulties, such as having to etch very deeply into a gallium oxide (e.g., Ga_2O_3) epitaxial drift layer. However, as long as the processing technique allows such fabrication, a thicker drift should be possible.

[0051] In some embodiments, the percentage composition (e.g., molar composition) of aluminum may be constant throughout the blocking layer 130 (e.g., a constant composition of aluminum). In other embodiments, in order to enhance the p-type conductivity utilizing the nitride polarization effect, the AlGaN blocking layer 130 may be an alloy of AlN and GaN graded from a high percentage or greatest composition of aluminum (e.g., 70%) at the bottom of the AlGaN blocking layer 130 (close to the drift layer 110) to a low percentage of aluminum (e.g., as low as 0%) at the top of the AlGaN blocking layer 130 to produce a graded composition of aluminum. For example, Al and Ga may be deposited together to form the AlGaN blocking layer 130, with the Al/Ga ratio adjusted during deposition. In some embodiments, the AlN and GaN are grown (such as by epitaxial growth) on the drift layer 110 (or in selectively etched portions of the drift layer 110).

[0052] In some embodiments, the graded p-type AlGaN blocking layer 130 may even be all p-type GaN at the top, or a lightly doped p-type GaN layer may be present at the top of the AlGaN blocking layer 130. Here, the percentage of Al may be molar concentration with respect to the total metal (e.g., Al and Ga) content in the AlGaN blocking layer 130.

[0053] The AlGaN blocking layer 130 may be patterned and etched (e.g., selectively etched) and a heavily doped n-type III-nitride (e.g., GaN, or ternary III-nitride alloy such as AlGaN or InGaN, or quaternary III-nitride alloy) layer 140 (or source layer) regrown on or in the patterned and etched AlGaN blocking layer 130 to form a source for the transistor 100. The source layer 140 may be at least 200 nm thick.

[0054] Ohmic metal (e.g., metal forming an ohmic contact) may be deposited on and contact both the heavily doped n-type GaN source layer 140 and the lightly doped p-type AlGaN blocking layer 130 to function as a source electrode 150. An insulator layer 160 may be deposited on the n-type GaN source layer, the p-type AlGaN blocking layer 130, and the n-type Ga_2O_3 drift layer 110 to serve as a dielectric layer 160 with gate metal 170 deposited on the top. Meanwhile, a drain electrode 180 may be formed by coating a second side (such as a back side, which faces away from or opposite to the front side) of the Ga_2O_3 substrate 120 with ohmic metal 180 (e.g., metal forming an ohmic contact with the Ga_2O_3 substrate 120).

[0055] FIG. 2 is a band diagram 200 of a comparable Ga_2O_3/GaN junction. FIG. 3 is a band diagram 300 of an example Ga_2O_3/AlGaN junction according to an embodiment of the present invention.

[0056] FIG. 2 illustrates an example conduction band offset, such as 0.1 eV, exhibited between gallium oxide (e.g., Ga_2O_3) and gallium nitride (e.g., GaN) in a comparable circuit to the transistor 100 in FIG. 1, but without any graded p-type AlGaN blocking layer 130. FIG. 33 is a transmission electron microscopy (TEM) image of a cross section of such a comparable gallium nitride on gallium oxide substrate device. In FIG. 33, the location of where an AlGaN blocking layer would appear according to an embodiment of the present invention is shown.

[0057] When a portion of the gallium nitride (e.g., GaN) is replaced by aluminum gallium nitride (e.g., AlGaN, such as an alloy of AlN and GaN), however, such as in the transistor 100 of FIG. 1, the comparable band diagram is shown in FIG. 3. As the molar concentration of Al in the AlGaN alloy increases, the conduction band of AlGaN is higher than that of Ga_2O_3 and GaN (as illustrated in FIG. 2), indicating the conduction band offset ΔEc becomes positive. During the transistor operation (such as with the transistor 100 of FIG. 1), the electrons flow first from the heavily doped n-type GaN layer 140 into the lightly doped p-type graded AlGaN blocking layer 130 and then into the lightly doped n-type Ga_2O_3 drift layer. Due to the positive ΔEc, the electrons gain high velocity when they are injected into the Ga_2O_3 drift layer, thereby resulting in low on-resistance.

[0058] FIG. 4 is a schematic cross-section of an example p-type AlGaN base layer design 400 according to an embodiment of the present invention.

[0059] The design 400 may include a p-type AlGaN base layer 410 between a Ga_2O_3 drift layer 420 and a heavily doped n-type GaN source layer 430. The AlGaN base layer 410 may be an alloy with, for example, constant Al composition throughout or graded Al composition (e.g., continuously varying composition) from a higher Al percentage (Al%=x) at the AlGaN/Ga_2O_3 interface 440 to a lower Al percentage (Al%=y) at the AlGaN/GaN interface 450, as shown in FIG. 4 (e.g., $x>y\geq 0$). In embodiments of the base layer design 400, x may be larger than y in the graded AlGaN layer 410. The composition y may be zero, in which case at the top of the p-type AlGaN base layer 410 (e.g., at interface 450), there may be a layer of p-type GaN that is adjacent to the heavily doped n-type GaN source layer 430. It should be noted that the band gap energy of the p-type AlGaN layer may increase in the direction from the Ga_2O_3 drift layer to the n+ GaN source layer.

[0060] The critical electric field of Ga_2O_3 is 8 MV/cm. To match this breakdown field, in some embodiments of the base layer design 400, x should be at least 70%

so that the breakdown property will not be limited at the AlGaN side 410 of the AlGaN/Ga_2O_3 interface 440.

[0061] FIG. 5 is a schematic cross-section of an example p-type AlGaN and GaN base layer design 500 according to an embodiment of the present invention.

[0062] The design 500 may include a p-type GaN first base layer 510 (e.g., a lightly doped base layer) between an n-type Ga_2O_3 drift layer 520 (e.g., a lightly doped drift layer) and a lightly doped p-type GaN second base layer 515. A heavily doped n-type GaN source layer 530 may be formed on the p-type GaN second base layer 515. The AlGaN first base layer 510 may be an alloy with, for example, constant Al composition throughout or graded Al composition from a higher Al percentage (such as 70% Al) at the AlGaN/Ga_2O_3 interface 540 to a lower Al percentage (such as 0% or nearly 0% Al) at the p-type AlGaN/GaN interface 550.

[0063] FIG. 6 is a flow diagram of an example method of creating a gallium oxide-based vertical field-effect transistor (such as the vertical transistor 100 of FIG. 1) according to an embodiment of the present invention.

[0064] Referring to FIG. 6, in step 610, a lightly doped n-type gallium oxide drift layer (such as the drift layer 110 of FIG. 1) is formed on a first side (e.g., a front side) of a heavily doped n-type gallium oxide substrate (such as the substrate 120 of FIG. 1). In step 620, a p-type III-nitride base layer (such as the AlGaN base layer 130 of FIG. 1) is formed on the drift layer. In step 630, a heavily doped n-type III-nitride source layer (such as the GaN source layer 140 of FIG. 1) is formed on the base layer.

[0065] In step 640, a dielectric gate insulator layer (such as the gate insulator layer 160 of FIG. 1) is formed on the source layer, the base layer, and the drift layer. In step 650, source ohmic contacts (such as the source electrodes 150 of FIG. 1) are formed contacting the n-type source layer and the p-type base layer. In step 660, a gate electrode (such as the gate electrode 170 of FIG. 1) is formed on the gate insulator layer. In step 670, a drain ohmic contact (such as the drain electrode 180 of FIG. 1) is formed on a second side (e.g., a backside) of the substrate.

[0066] FIGs. 7–32 are schematic cross-sections illustrating an example method of manufacturing a gallium oxide-based vertical field-effect transistor according to an embodiment of the present invention.

[0067] In FIG. 7, a heavily doped gallium oxide substrate is provided, on which is grown (such as by epitaxy) a lightly doped gallium oxide drift layer. In FIG. 8, a first mask is used to pattern and form an iso mark (illustrated schematically on the upper right corner of the drawing). The iso-mark (or i-mark) may be a mark formed by etching into the wafer, and may be used for alignment purposes for the processing steps that follow (e.g., to help align the remaining masks to this mark, which helps

make sure the device will be processed as designed. In FIG. 9, a first layer of silicon dioxide (silica) is formed, such as by plasma-enhanced chemical vapor deposition (PECVD), on the drift layer. In FIG. 10, a first layer of photoresist is formed on the silica layer, and a second mask is used to pattern and form (for example, by lithography) first openings in the first photoresist layer corresponding to the base layers to be formed later.

[0068] In FIG. 11, the first openings are extended (e.g., by wet and dry etching) through the first silica layer and partially into the drift layer to form first channels for the base layers. In FIG.12, the first photoresist layer is removed (e.g., stripped) to reveal the remaining first silica layer. In FIG. 13, lightly doped p-type aluminum gallium nitride base layers are grown, such as by metalorganic chemical vapor deposition (MOCVD), in the exposed first channels. In other embodiments, an n-type nitride layer (such as gallium nitride or aluminum gallium nitride) may be grown in the exposed first channels before growing the p-type aluminum gallium nitride base layers.

[0069] In FIG. 14, the remaining first silica layer is removed, while in FIG. 15, a second silica layer is formed on the drift and base layers, such as by the same PECVD process used to form the first silica layer. In FIG. 16, a second photoresist layer is formed on the second silica layer, and a third mask is used to pattern and form (for example, by the same lithography process used to etch the first photoresist layer) second openings in the second photoresist layer corresponding to the source layers to be formed later.

[0070] In FIG. 17, the second openings are extended (e.g., by wet and dry etching) through the second silica layer and into the base layers to form second channels for the source layers. In FIG.18, the second photoresist layer is removed (e.g., stripped) to reveal the remaining second silica layer. In FIG. 19, heavily doped n-type aluminum gallium nitride source layers are grown, such as by MOCVD, in the exposed second channels.

[0071] In FIG. 20, the remaining second silica layer is removed. In FIG. 21, a gate dielectric layer is formed on the drift, base, and source layers. In FIG. 22, a third photoresist layer is formed on the gate dielectric layer, and a fourth mask is used to pattern and form (for example, by the same lithography process used to etch the first and second photoresist layers) third openings in the third photoresist layer corresponding to the base ohmic contacts to be formed later.

[0072] In FIG. 23, the third openings are extended (e.g., by wet etching) through the gate dielectric layer to expose contacting surfaces of the base layers. In FIG. 24, ohmic contacts are formed in the third openings, e.g., by depositing metal on the third photoresist layer and exposed contacting surfaces of the base layers, removing

the exposed metal and remaining third photoresist layer (e.g., by lift-off) to reveal the metal formed in the third openings, and finishing the metal-semiconductor base ohmic contacts by heat treatment, such as rapid thermal annealing (RTA). In FIG. 25, a fourth photoresist layer is formed on the gate dielectric layer and base ohmic contacts, and a fifth mask is used to pattern and form (for example, by the same lithography process used to etch the first, second, and third photoresist layers) fourth openings in the fourth photoresist layer corresponding to the source ohmic contacts to be formed later, and the fourth openings are extended (e.g., by wet etching) through the gate dielectric layer to expose contacting surfaces of the source layers.

[0073] In FIG. 26, ohmic contacts are formed in the fourth openings, e.g., by depositing metal on the fourth photoresist layer and exposed contacting surfaces of the source layers, and removing the exposed metal and remaining fourth photoresist layer (e.g., by lift-off) to reveal the source ohmic contacts. In some embodiments, the n-metal contacts may be annealed after the metal is deposited. In FIG. 27, a fifth photoresist layer is formed on the gate dielectric layer and base and source ohmic contacts, and a sixth mask is used to pattern and form (for example, by the same lithography process used to etch the first through fourth photoresist layers) fifth openings in the fifth photoresist layer corresponding to the ion implantation areas (e.g., areas of the drift layer outside of and not between the source layers) to be formed later. In FIG. 28, doping is performed (for example, by ion implantation) on the fifth openings (the remaining areas being shielded by the fifth photoresist layer) to form the ion implantation areas in the drift and gate dielectric layers, and the fifth photoresist layer is removed (e.g., stripped) to reveal the ion implantation areas, leaving an I-mark (illustrated schematically on the upper right corner of the drawing).

[0074] In FIG. 29, a sixth photoresist layer is formed on the gate dielectric layer, base and source ohmic contacts, and ion implantation areas, and a seventh mask is used to pattern and form (for example, by the same lithography process used to etch the first through fifth photoresist layers) sixth openings in the sixth photoresist layer corresponding to the gate and source electrode areas to be formed later. In FIG. 30, the gate and source electrodes are formed in the sixth openings, e.g., by depositing metal on the sixth photoresist layer and sixth openings, and removing the exposed metal and remaining sixth photoresist layer (e.g., by lift-off) to reveal the gate and source electrodes. In FIG. 31, an eighth mask is used to metal plate the gate and source electrodes.

[0075] In FIG. 32, metal is applied to the backside of the gallium oxide substrate to form the drain electrode. In some embodiments, the backside metal may be annealed after it is applied to the backside of the gallium oxide substrate.

[0076] While the present invention has been described in connection with certain example embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

WHAT IS CLAIMED IS:

1. A field-effect transistor comprising:

an n-type gallium oxide substrate having a first doping concentration;

an n-type gallium oxide drift layer on a first side of the substrate and having a second doping concentration smaller than the first doping concentration;

a p-type III-nitride first base layer on the drift layer; and

an n-type III-nitride source layer on the first base layer and having a third doping concentration larger than the second doping concentration.

2. The field-effect transistor of claim 1, further comprising:

a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer; and

a gate electrode on the gate insulator layer.

3. The field-effect transistor of claim 2, further comprising:

a drain ohmic contact on a second side of the substrate, the second side facing away from the first side; and

source ohmic contacts in contact with the source layer and the first base layer.

4. The field-effect transistor of claim 1, wherein the first base layer comprises aluminum gallium nitride.

5. The field-effect transistor of claim 4, wherein the first base layer comprises a constant composition of aluminum.

6. The field-effect transistor of claim 4, wherein the first base layer comprises a graded composition of aluminum having a greatest composition of aluminum at a boundary with the drift layer and a least composition of aluminum proximal to the source layer.

7. The field-effect transistor of claim 6, wherein the greatest composition of aluminum is at least 70% of the molar composition of aluminum and gallium in the first base layer.

8. The field-effect transistor of claim 4, further comprising a p-type gallium nitride second base layer between the first base layer and the source layer.

9. The field-effect transistor of claim 1, wherein the source layer comprises gallium nitride.

10. A method of forming a field-effect transistor, the method comprising:

providing an n-type gallium oxide drift layer having a first doping concentration on a first side of an n-type gallium oxide substrate having a second doping concentration larger than the first doping concentration;

forming a p-type III-nitride first base layer on the drift layer; and

forming an n-type III-nitride source layer on the first base layer and having a third doping concentration larger than the first doping concentration.

11. The method of claim 10, further comprising:

forming a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer; and

forming a gate electrode on the gate insulator layer.

12. The method of claim 11, further comprising:

forming a drain ohmic contact on a second side of the substrate, the second side facing opposite to the first side; and

forming source ohmic contacts contacting the source layer and the first base layer.

13. The method of claim 10, wherein the first base layer comprises aluminum gallium nitride.

14. The method of claim 13, wherein the forming of the first base layer comprises grading a composition of aluminum such that a greatest composition of aluminum is at a boundary with the drift layer and a least composition of aluminum is proximal to the source layer.

15. The method of claim 14, wherein the greatest composition of aluminum is at least 70% of the molar composition of aluminum and gallium in the first base layer.

16. The method of claim 13, further comprising forming a p-type gallium nitride second base layer between the first base layer and the source layer.

17. The method of claim 10, wherein the forming of the first base layer comprises:

selectively etching the drift layer; and

regrowing the first base layer in the selectively etched drift layer.

18. The method of claim 17, wherein the regrowing of the first base layer in the selectively etched drift layer comprises:

regrowing an n-type III-nitride layer in the selectively etched drift layer; and

regrowing the first base layer on the regrown n-type III-nitride layer.

19. The method of claim 17, wherein the forming of the source layer comprises:

selectively etching the first base layer; and

regrowing the source layer in the selectively etched first base layer.

20. The method of claim 10, further comprising regrowing a dielectric gate insulator layer on the source layer, the first base layer, and the drift layer.

21. The method of claim 20, further comprising:

selectively etching the gate insulator layer;

forming source ohmic contacts contacting the source layer, the first base layer, and the selectively etched gate insulator layer; and

forming a gate electrode on the gate insulator layer.

FIG. 1

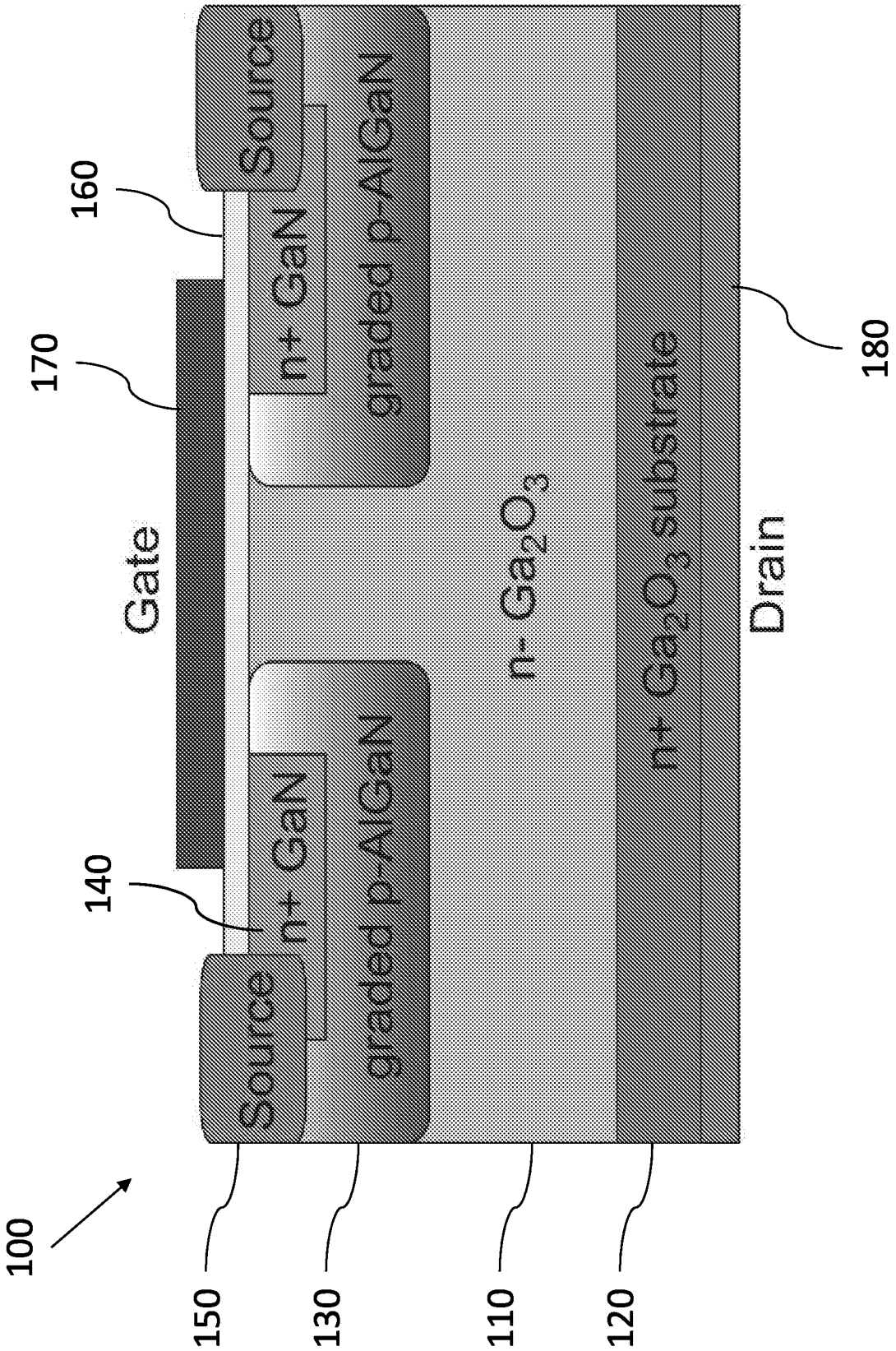

Source
n+ GaN
graded p-AlGaN
Gate
n+ GaN
graded p-AlGaN
Source
n- Ga_2O_3
n+ Ga_2O_3 substrate
Drain
100
150
130
110
120
140
170
160
180

FIG. 2

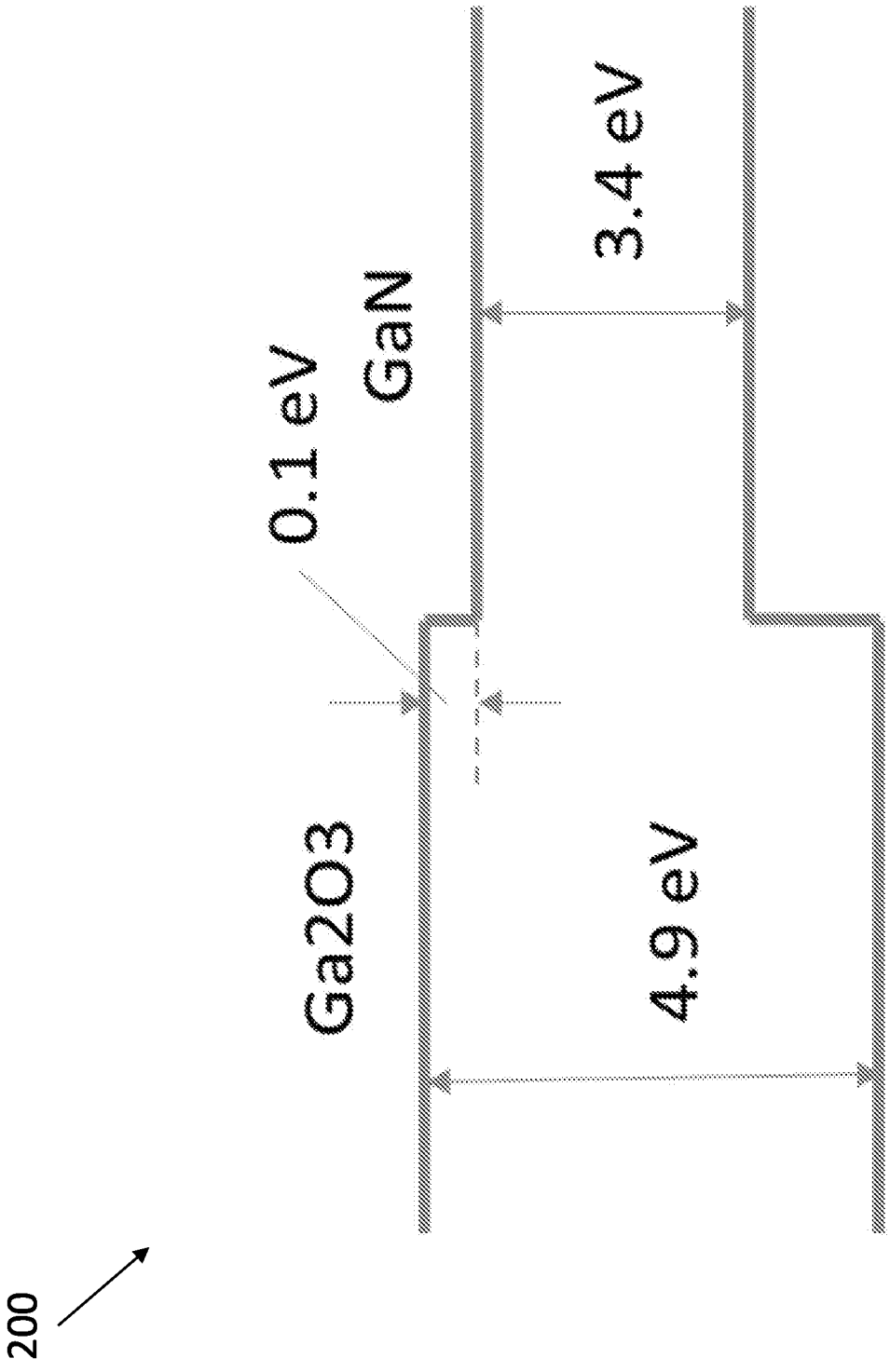


FIG. 3

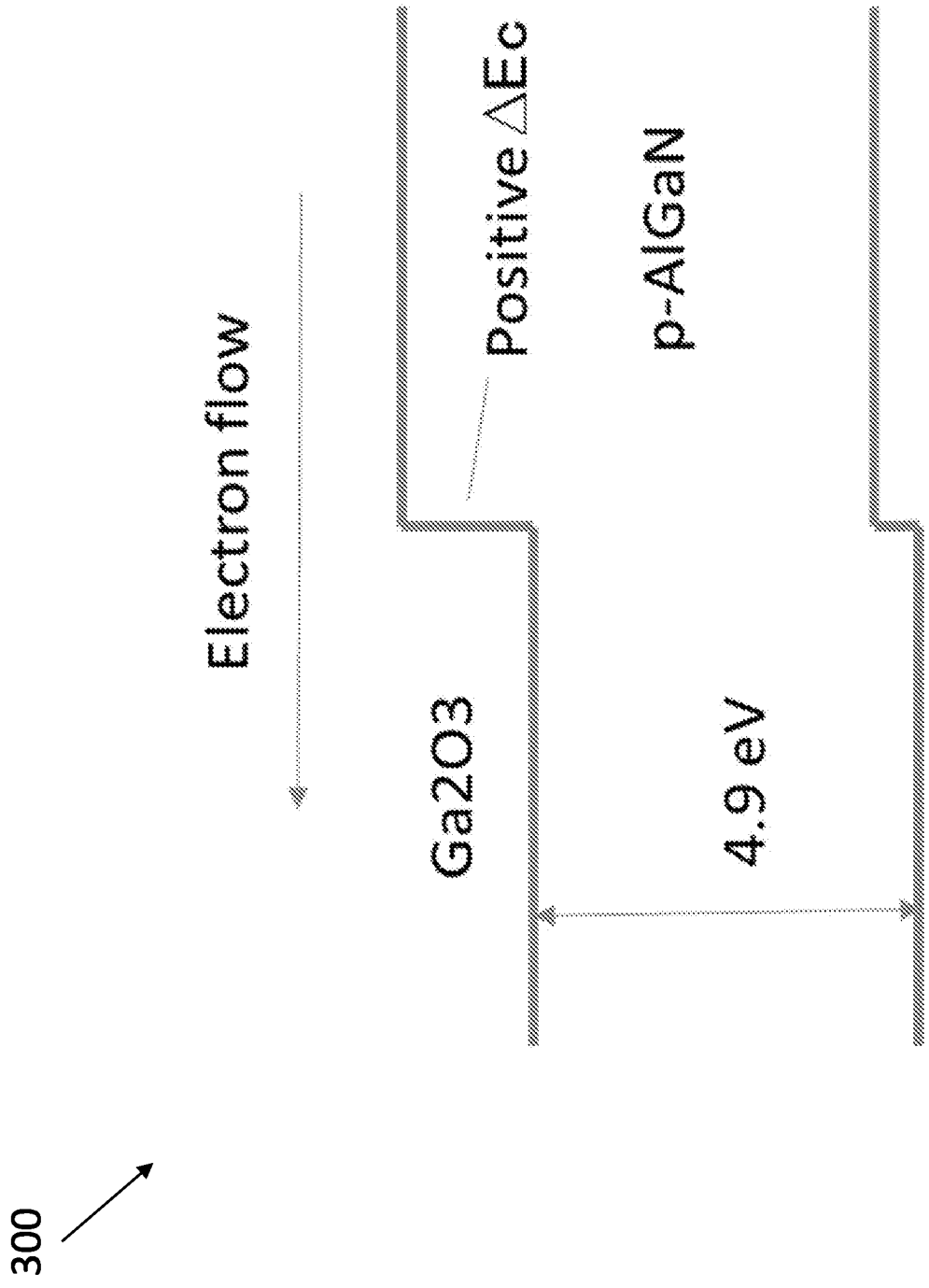


FIG. 4

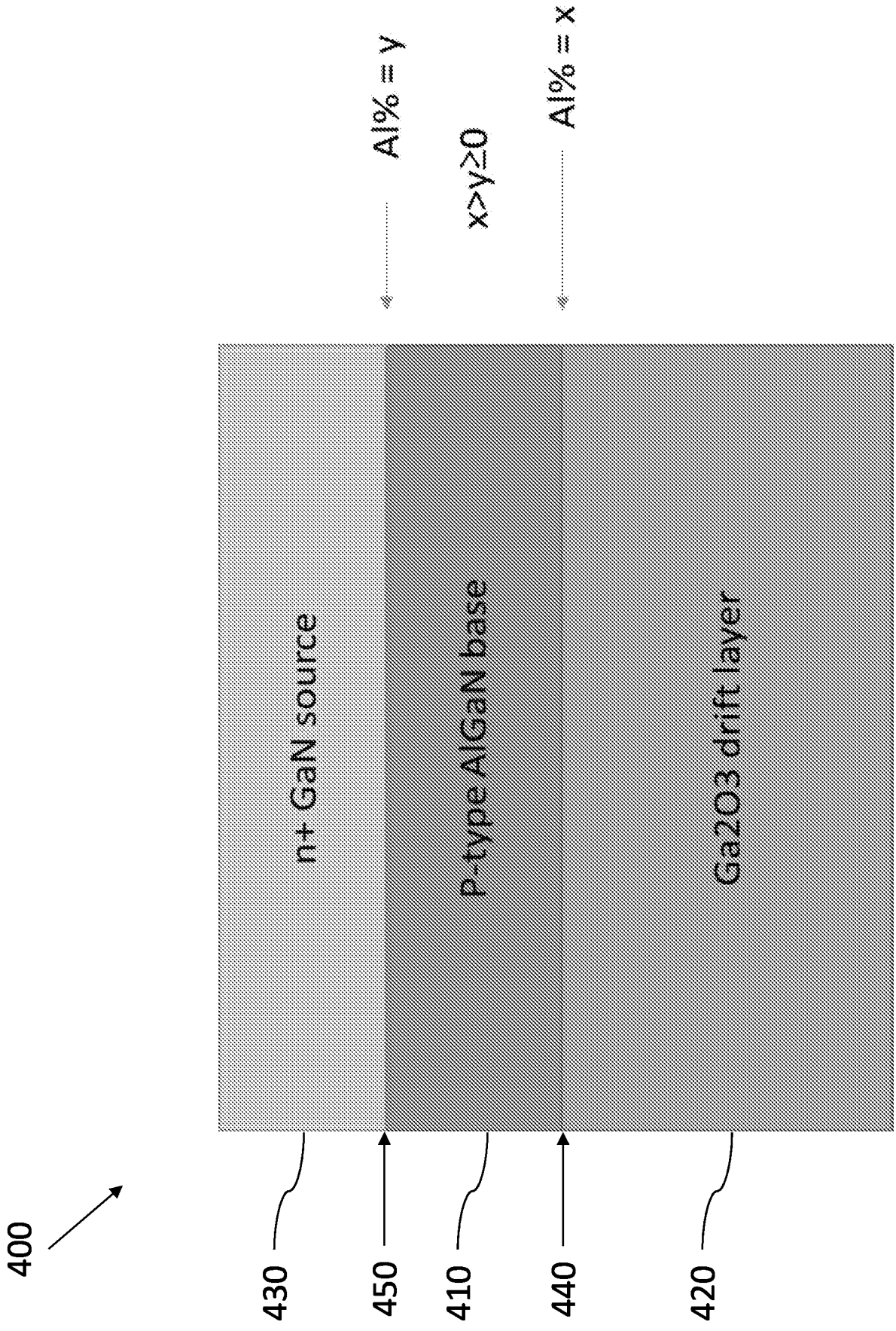

400
430
450
410
440
420
n+ GaN source
P-type AlGaN base
Ga2O3 drift layer
Al% = y
x>y≥0
Al% = x

FIG. 5

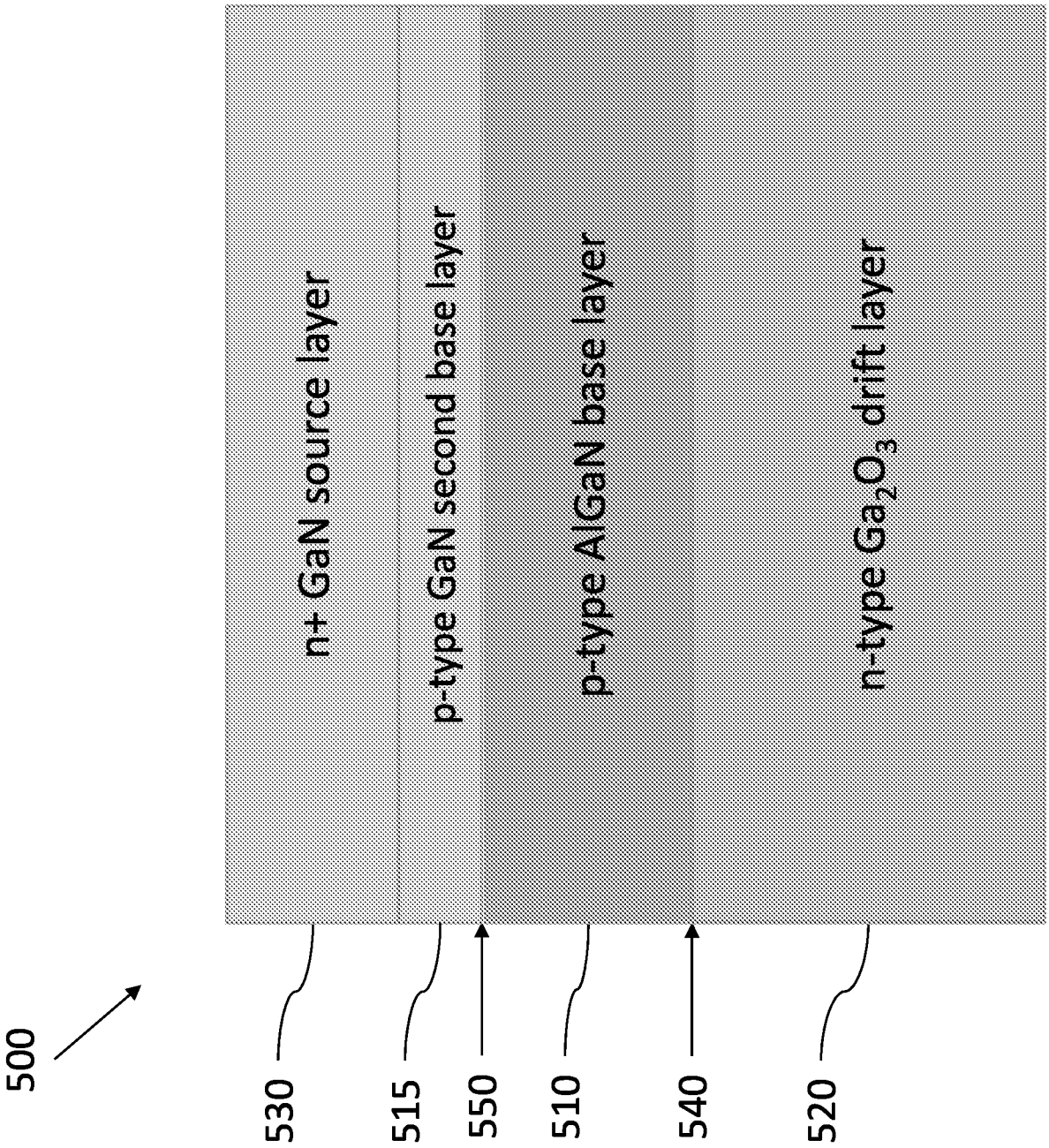

500
530
515
550
510
540
520
n+ GaN source layer
p-type GaN second base layer
p-type AlGaN base layer
n-type Ga_2O_3 drift layer

FIG. 6

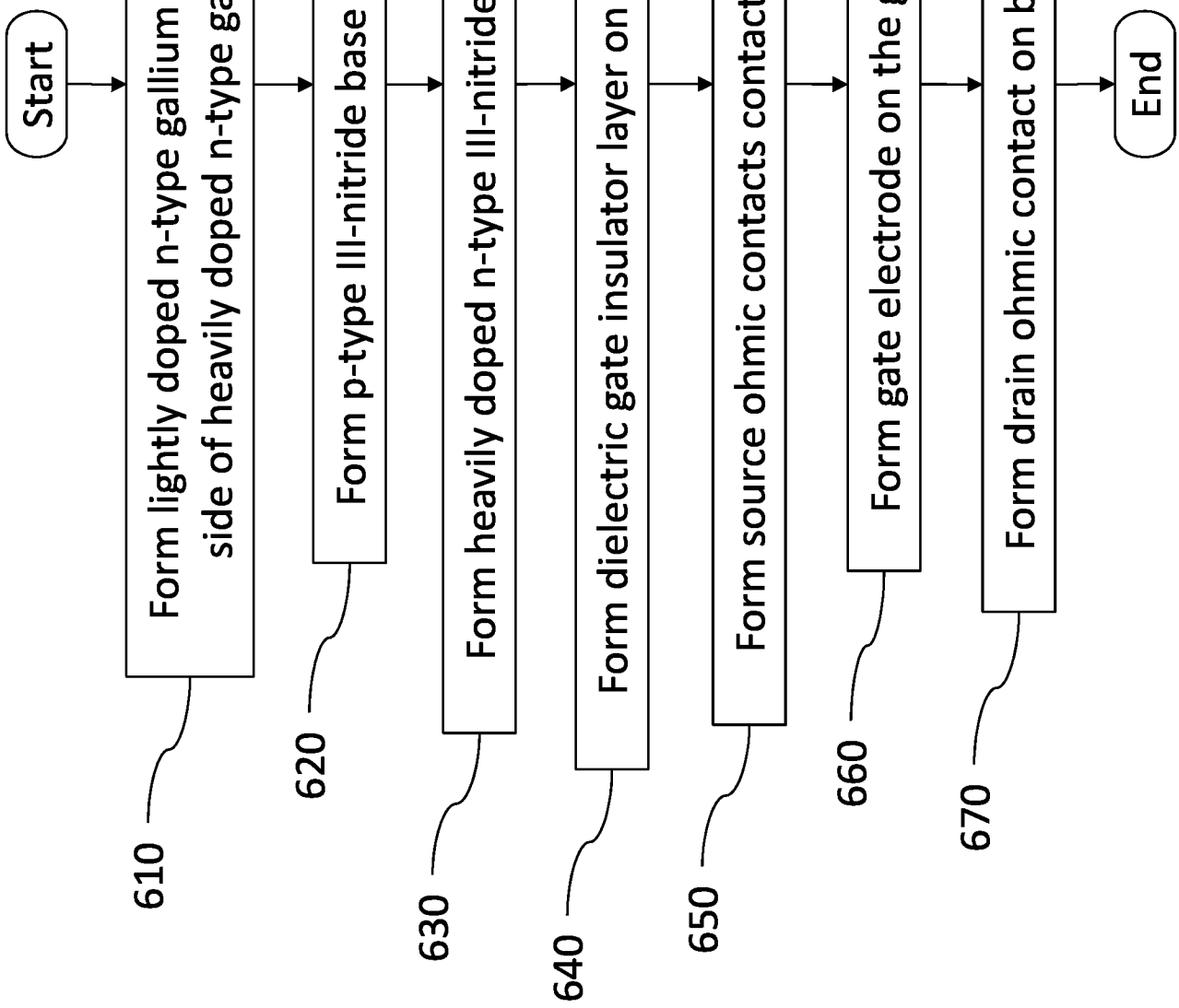
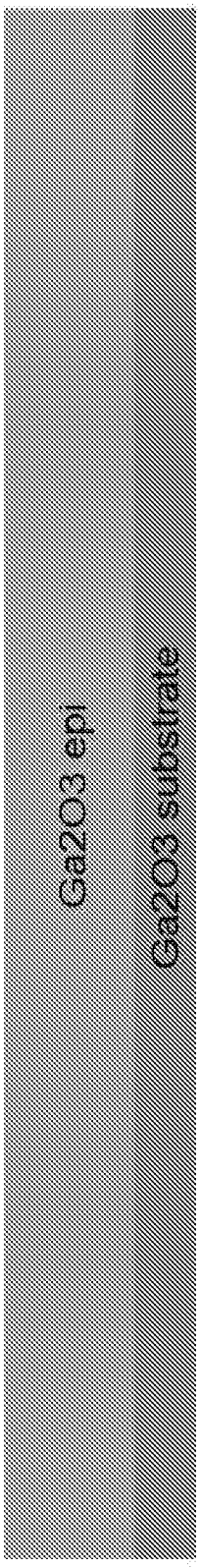
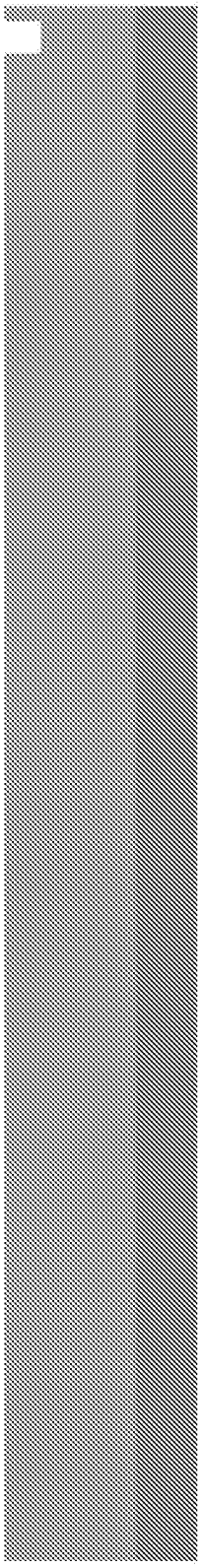

Start
Form lightly doped n-type gallium oxide drift layer on front side of heavily doped n-type gallium oxide substrate
610
Form p-type III-nitride base layer on drift layer
620
Form heavily doped n-type III-nitride source layer on base layer
630
Form dielectric gate insulator layer on source, base, and drift layers
640
Form source ohmic contacts contacting source and base layers
650
Form gate electrode on the gate insulator layer
660
Form drain ohmic contact on back side of substrate
670
End

FIG. 7



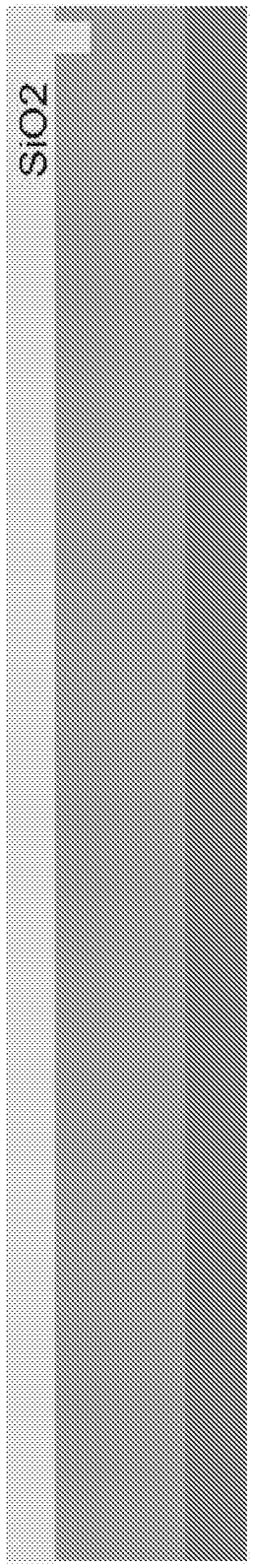
1. Ga2O3 wafer

FIG. 8



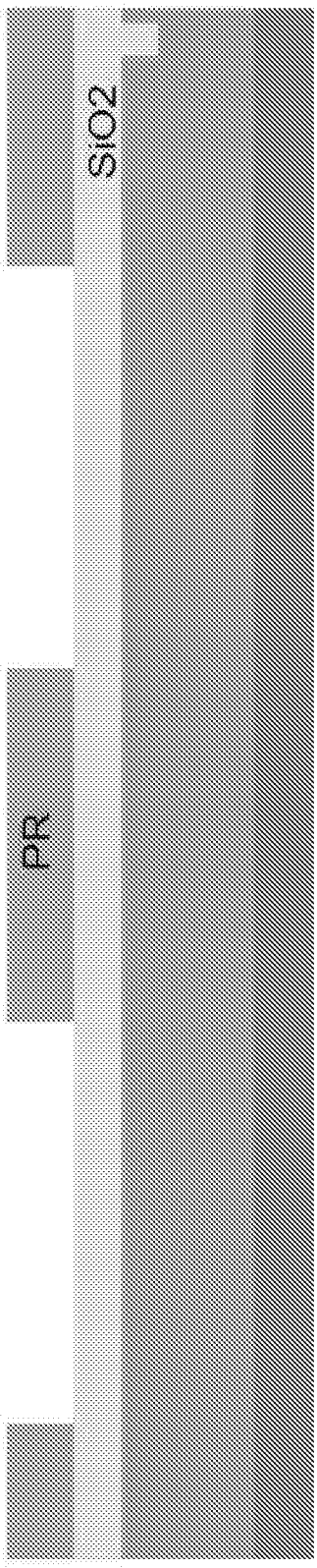
2. Iso mark - Mask 1

FIG. 9



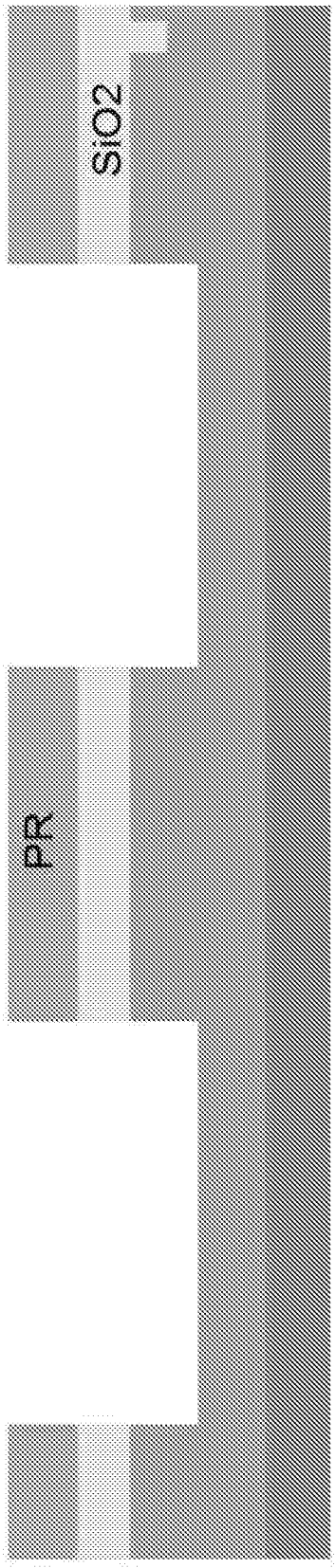
3. PECVD-1

FIG. 10



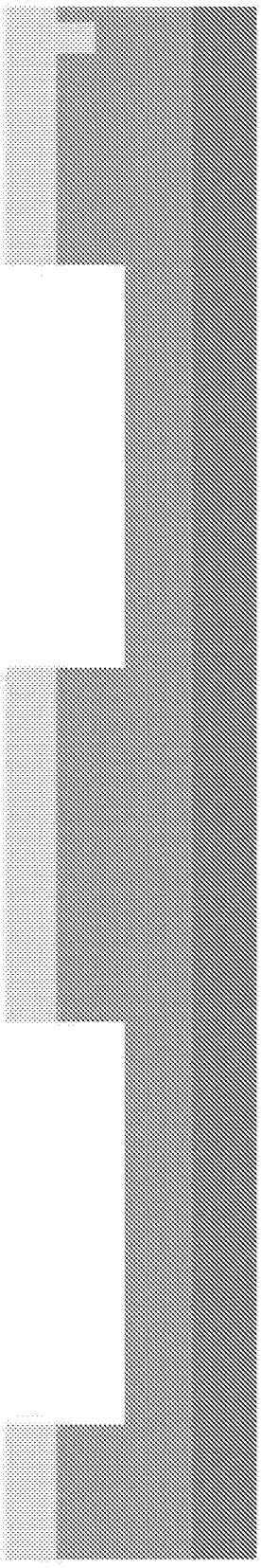
4. Litho for VIA01 - Mask 2

FIG. 11



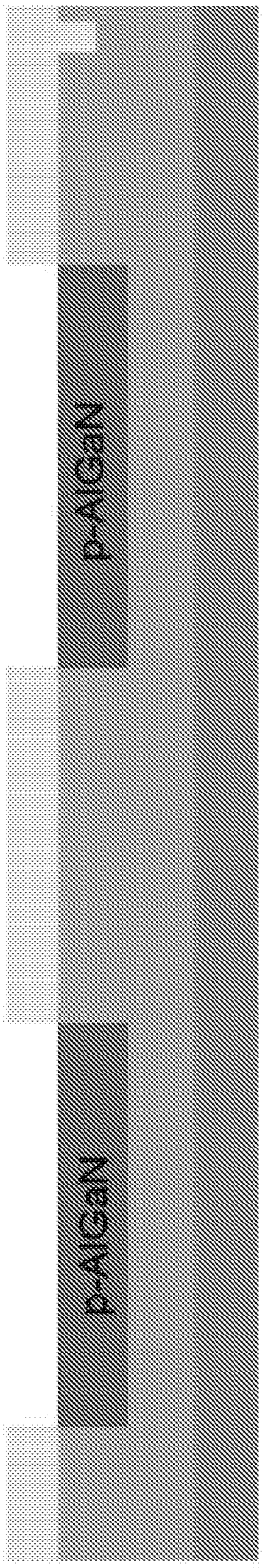
5. VIA01 by wet & dry etching

FIG. 12



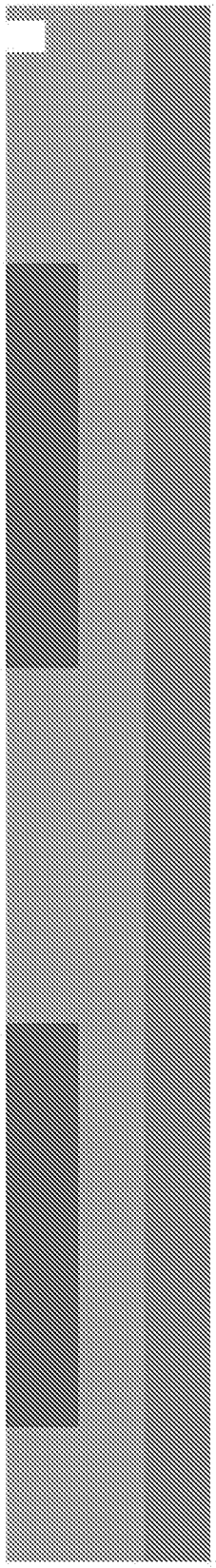
6. PR strip

FIG. 13



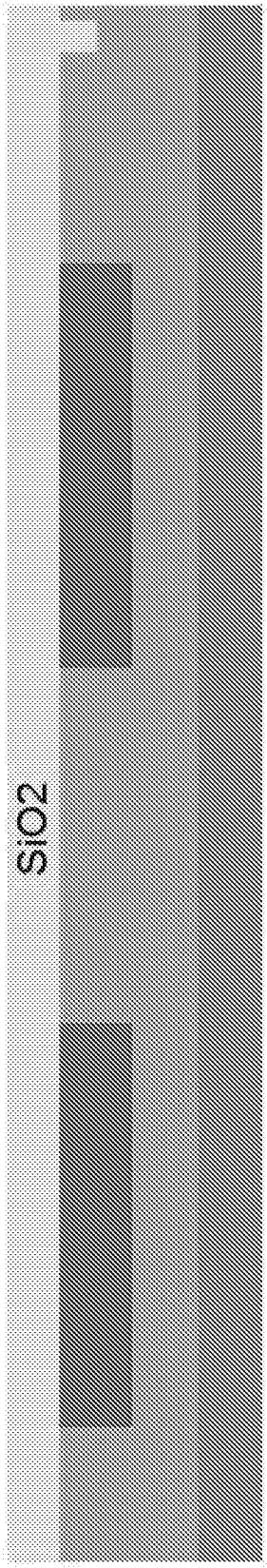
7. p-AlGaN regrowth by MOCVD

FIG. 14



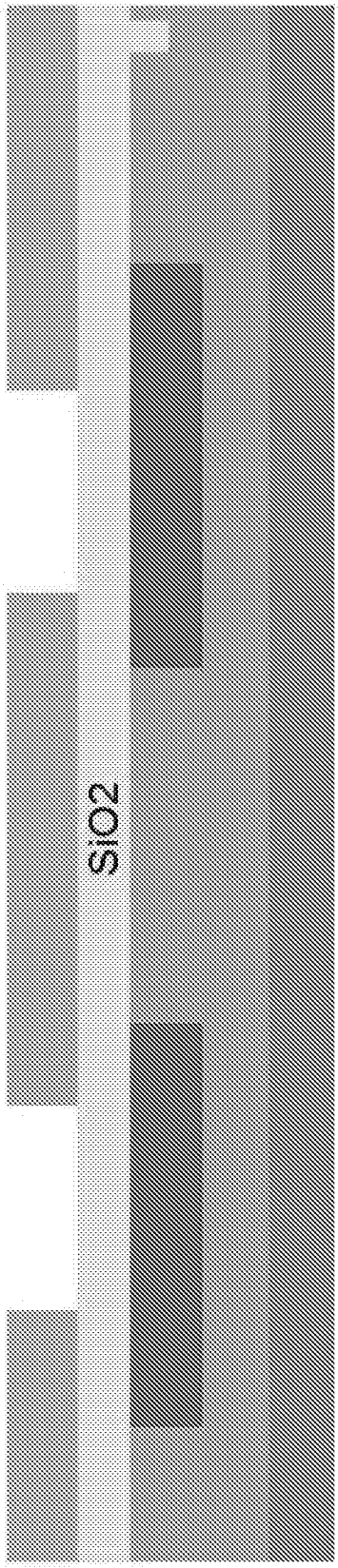
8. SiO2 removal

FIG. 15



9. PECVD-2

FIG. 16



10. Litho for VIA02 - Mask 3

FIG. 17

11. VIA03 by wet & dry etching

FIG. 18

12. PR strip

FIG. 19

13. n-AlGaN regrowth by MOCVD

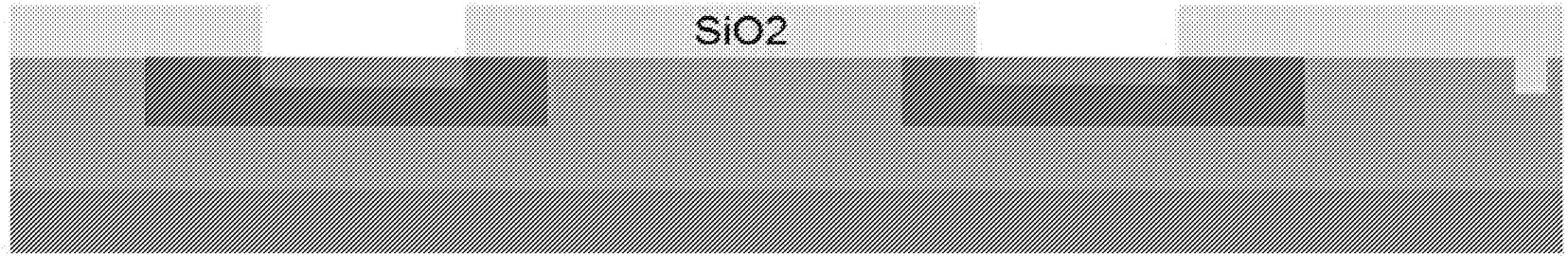
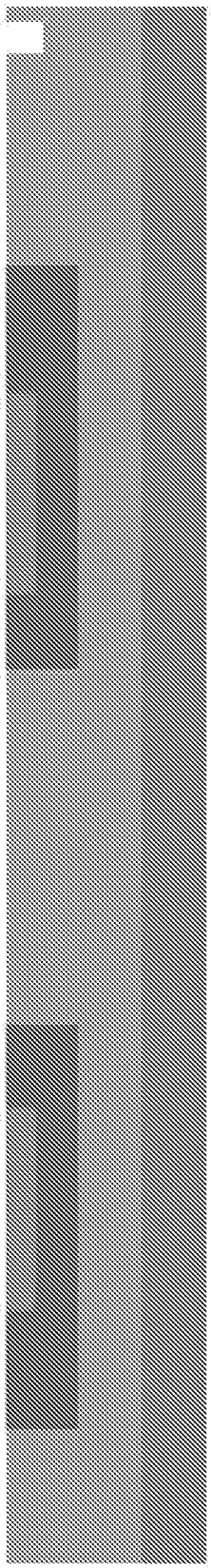
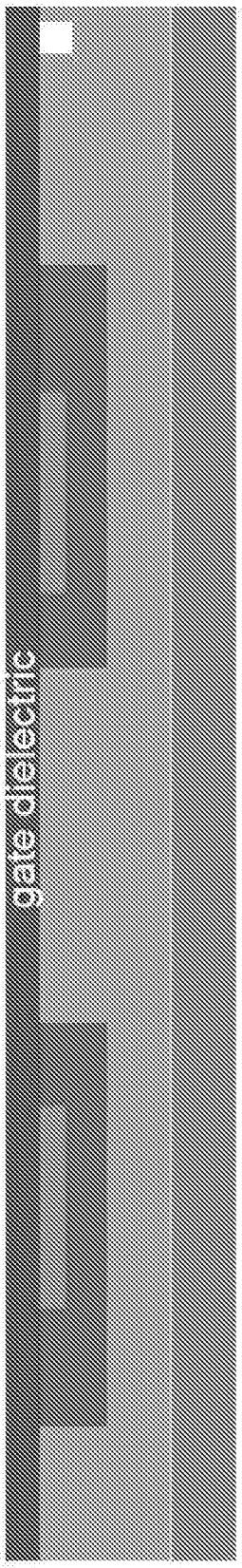


FIG. 20



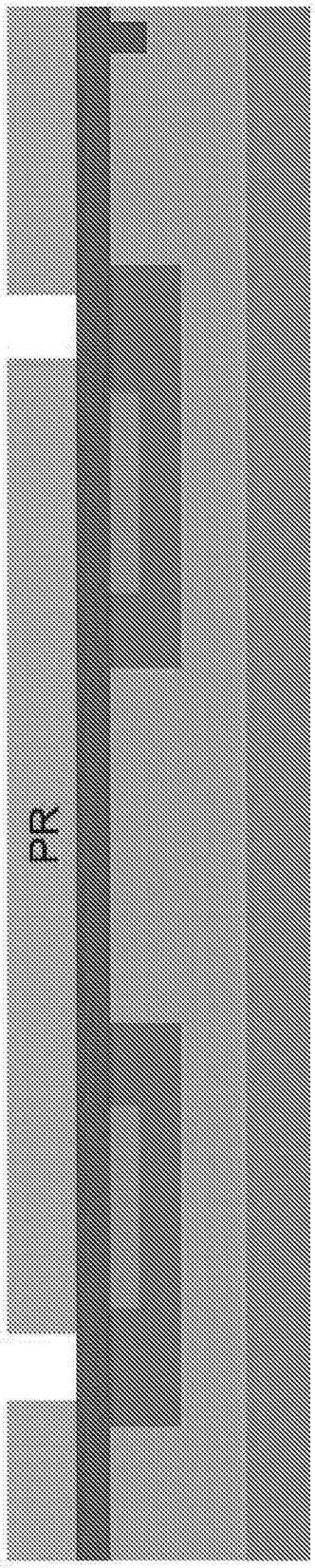
14. SiO2 removal

FIG. 21



15. Gate dielectric

FIG. 22



16. Litho for p-Ohmic - Mask 4

FIG. 23

17. VIA04 by wet etching

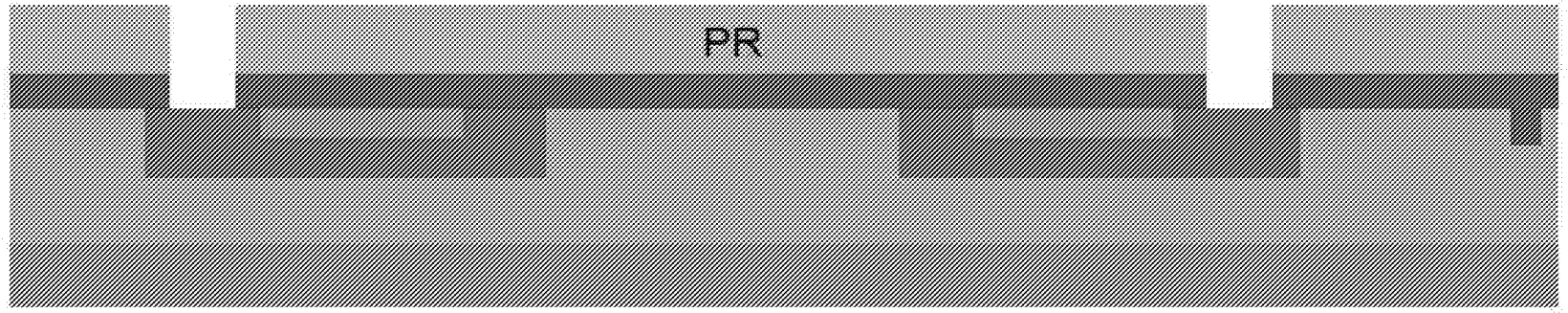


FIG. 24

18. p-Ohmic, lift off & RTA

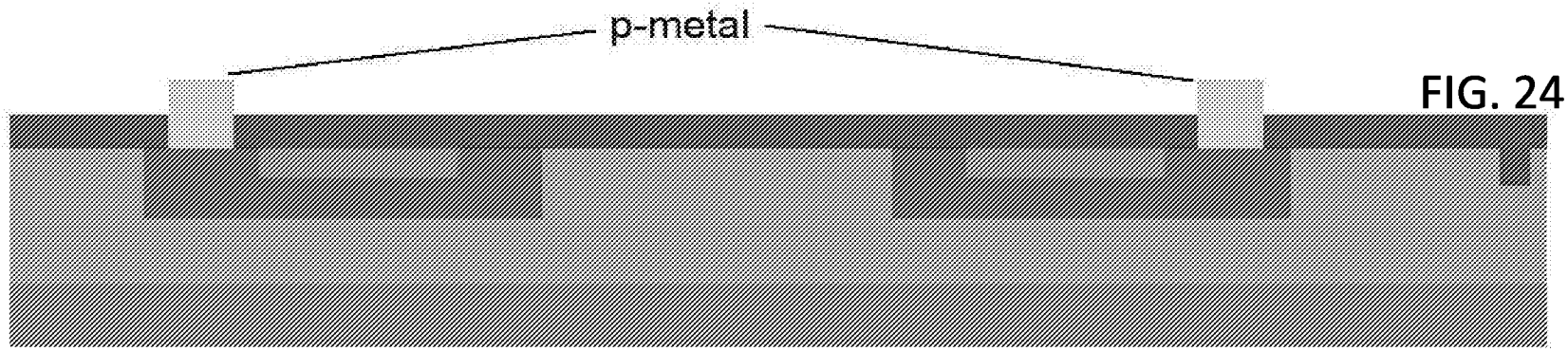


FIG. 25

19. Litho for n-Ohmic & VIA05 by wet etching - Mask 5

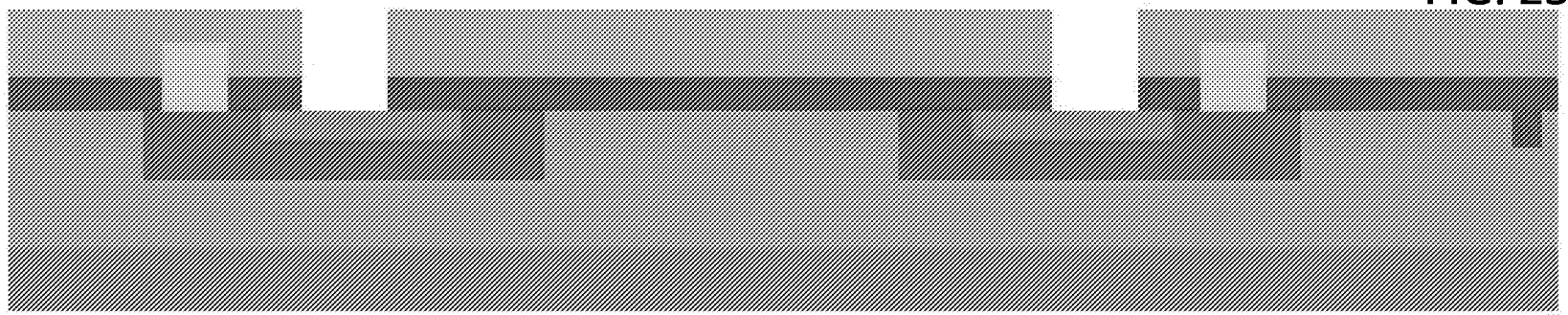


FIG. 26

20. n-Ohmic & lift off

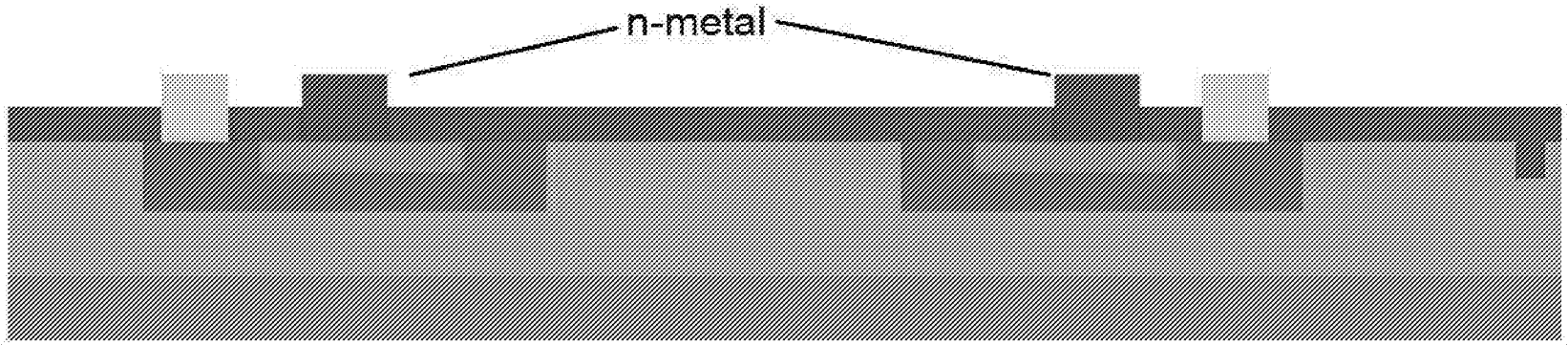


FIG. 27

21. Litho for implantation - Mask 6

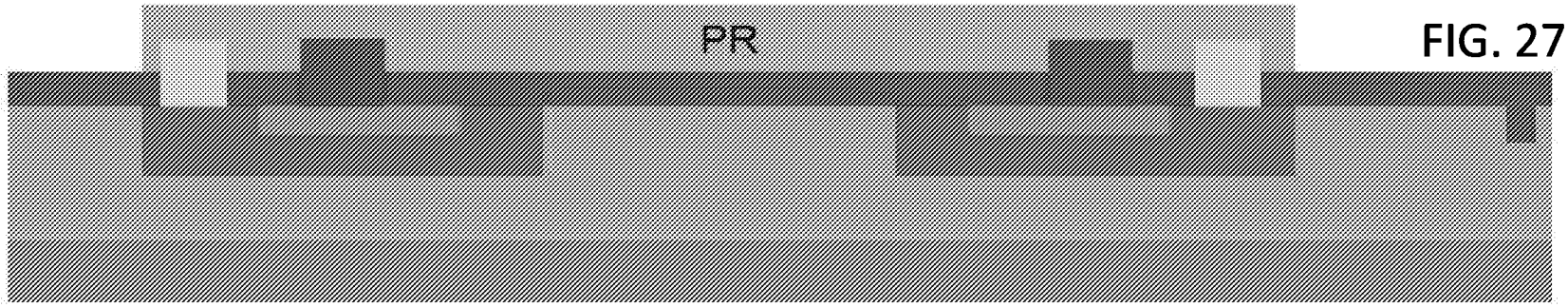


FIG. 28

22. Ion implantation & PR strip

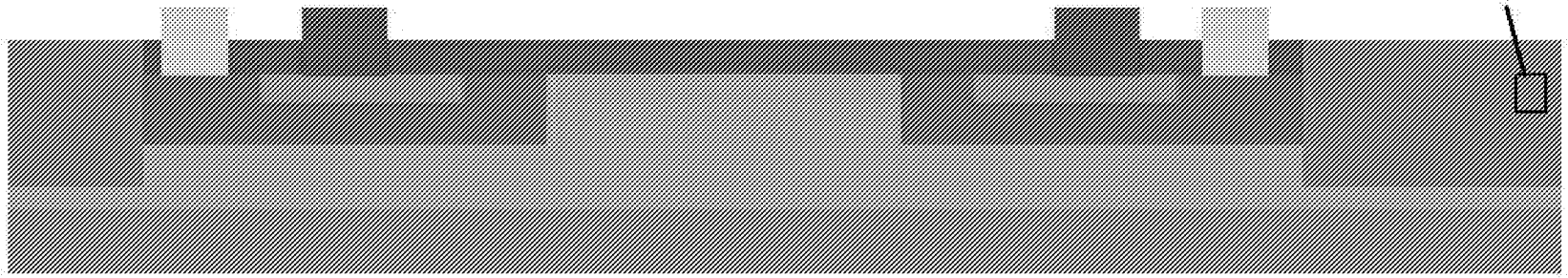


FIG. 29

23. Litho for gate - Mark 7

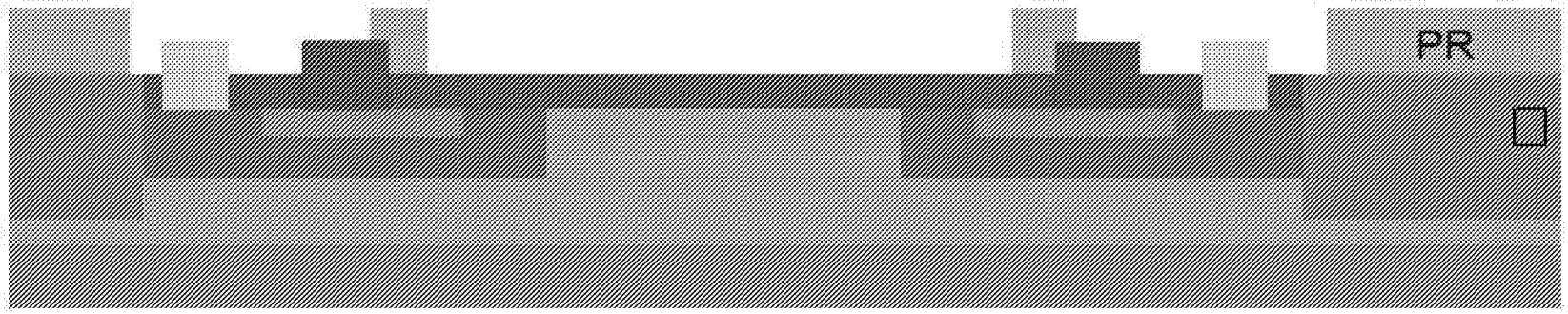


FIG. 30

24. Gate metal & lift off

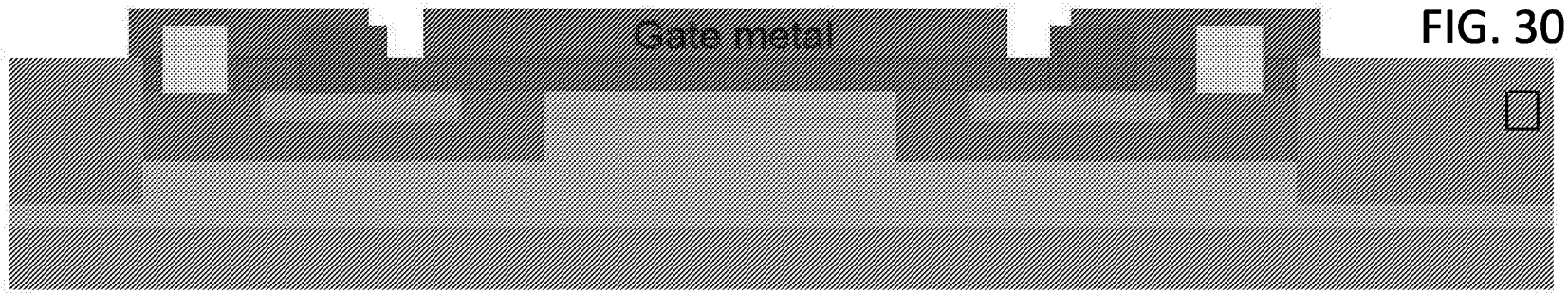


FIG. 31

25. Metal plating (optional) - Mask 8

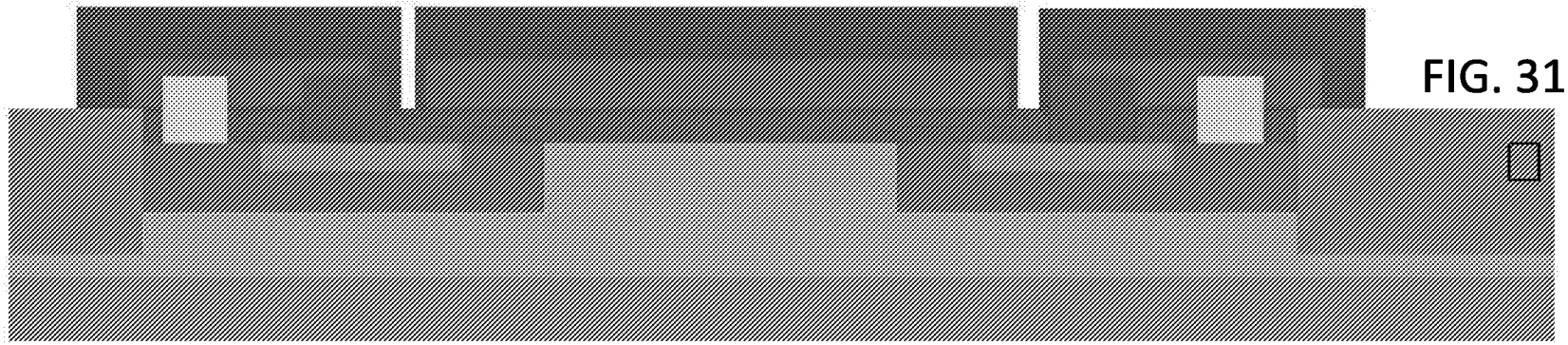


FIG. 32

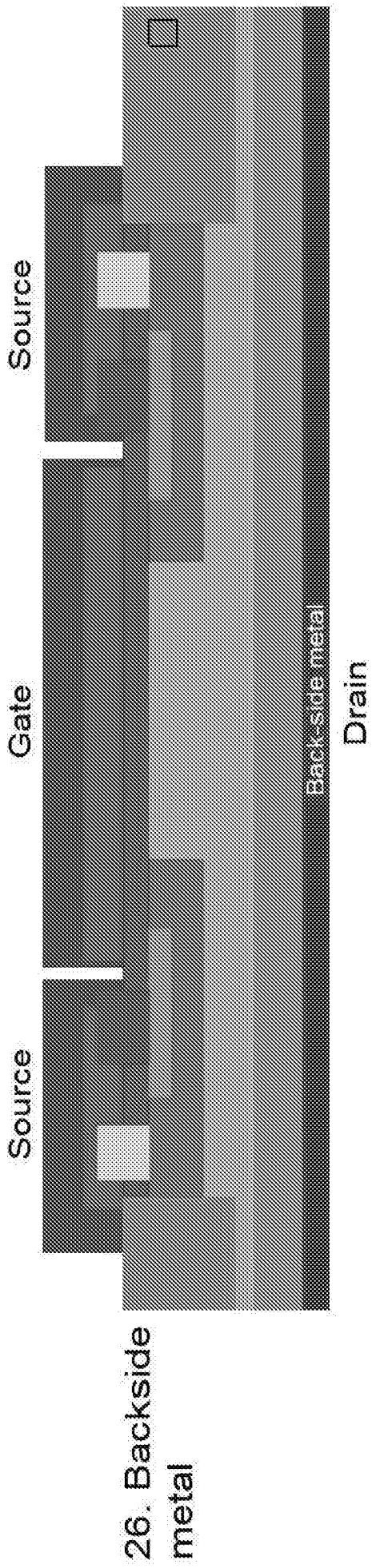
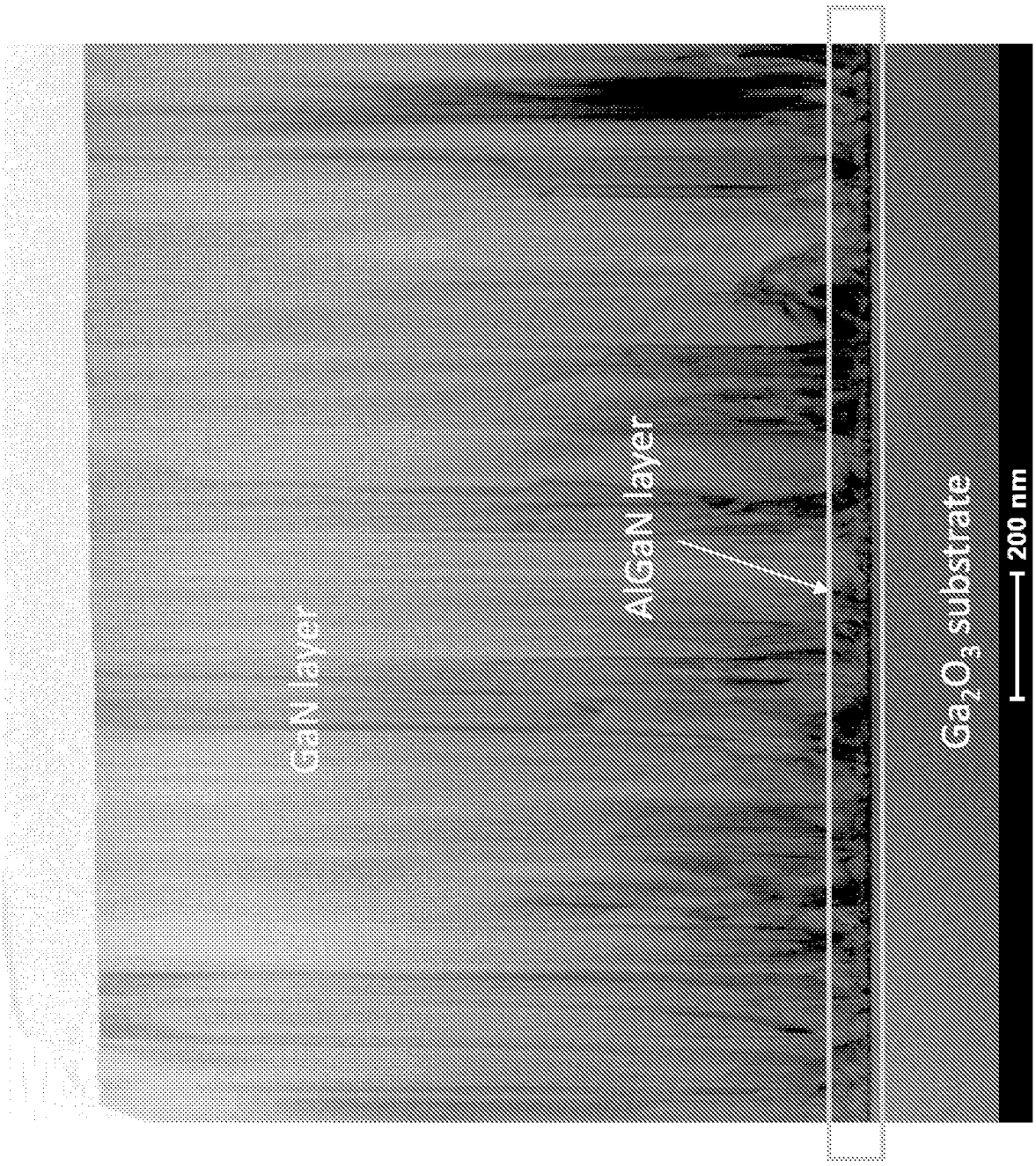


FIG. 33



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/049625

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/772(2006.01)i, H01L 29/423(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/772; H01L 21/336; H01L 29/78; H01L 33/00; H01L 29/06; H01L 21/02; H01L 29/76; H01L 29/10; H01L 29/24; H01L 29/423; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: fingerprint sensor, electrode, aperture, illumination, collimator

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0217405 A1 (SASAKI et al.) 07 August 2014 See paragraphs [0032]-[0044], [0064], [0089]; and figures 1-2, 4.	1-21
Y	US 2010-0123167 A1 (MOON) 20 May 2010 See paragraph [0035]; and figures 1, 4.	1-21
A	US 8957462 B2 (YAMAZAKI et al.) 17 February 2015 See figures 1A-1C.	1-21
A	US 9245749 B2 (TAMURA CORPORATION et al.) 26 January 2016 See figures 7-10.	1-21
A	US 2008-0197405 A1 (PFIRSCH et al.) 21 August 2008 See figure 2.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 December 2017 (14.12.2017)	**14 December 2017 (14.12.2017)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
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Authorized officer
KIM, Sung Gon
Telephone No. +82-42-481-8746

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/049625

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 2765610 A4	06/05/2015
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