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(71) Applicant: SUN MICROSYSTEMS, INC. [US/US]; 901 San Antonio Road, M/S PAL01-521, Palo Alto, CA 94303 (US).

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(72) Inventors: TREMBLAY, Marc; 140 Hanna Way, Menlo Park, CA 94025 (US). MURPHY, Graham, R.; 1495 Yukon, Sunnyvale, CA 94087 (US).

(74) Agents: TERRILE, Stephen, A. et al.; Skjerven, Morrill, MacPherson, Franklin & Friel, LLP, Suite 700, 25 Metro Drive, San Jose, CA 95110 (US). (81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

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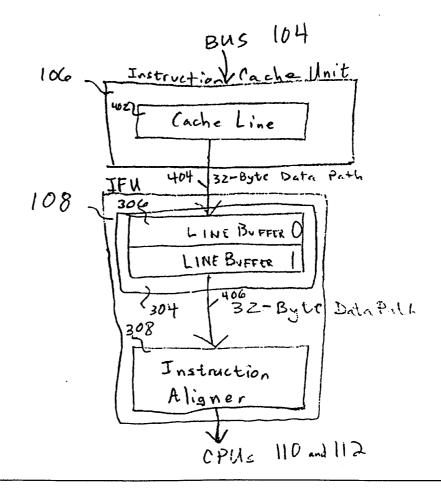
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(54) Title: DUAL LINE BUFFERS FOR AN INSTRUCTION FETCH UNIT

(57) Abstract

The present invention provides dual line buffers for an instruction fetch unit. In one embodiment an apparatus for a microprocessor includes an instruction cache unit that stores power of two size instruction cache lines and dual line buffers of an instruction fetch unit connected to the instruction cache unit, in which the dual line buffers store power of two size instruction cache lines fetched from the instruction cache unit, and the fetched instruction cache lines include a non-power of two size instruction.



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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 G06F9/30 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

 $\begin{array}{ll} \mbox{Minimum documentation searched (classification system followed by classification symbols)} \\ \mbox{IPC 7} & \mbox{G06F} \end{array}$

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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