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(54) **Title**: POWER CONTROL

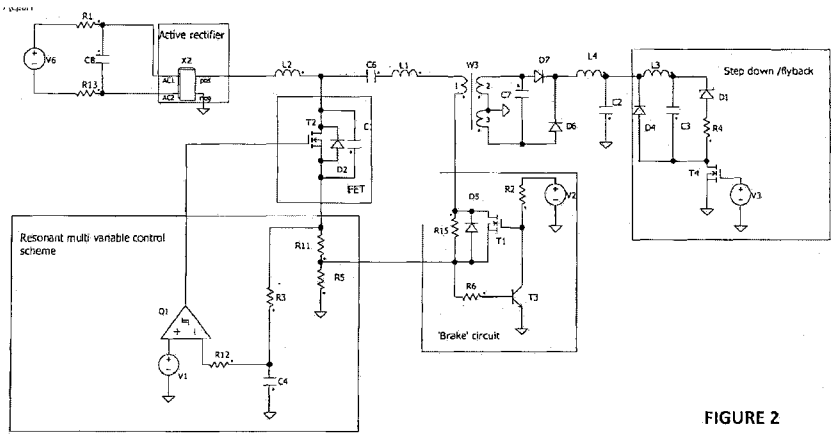

FIGURE 2

(57) **Abstract**: A Class E amplifier having a FET with a transistor (T2) connected via a serial "LC" circuit to the load, and connected to a supply voltage via a constant current source, the amplifier further including a resonant controller, wherein the resonant controller provides power control for an AC application and includes resonance tracking system of an input inductor being fed by a power source with the resonance tracking system using a resistor resonance detector having two sense resistor loads in series.

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POWER CONTROL

Field of the Invention

This invention relates to power control and in particular to distinct control of switching to achieve power control. Even more particular the invention provides improved means of power control in silicon topologies but is not limited to such.

Whilst the invention may be applied to a range of power sources from low voltage to mains voltage and for Direct Current or Alternating Current (DC or AC), for convenience sake it shall be described herein in terms of a control of Light Emitting Diodes (LEDs) for a range of voltages. In particular it will be described with regard to a class E amplifier. However the scope of the invention is not limited thereto and can include one or more of the sections for other power control uses.

Background to the Invention

Important concerns in power control circuits are power loss and power storage. In switch-mode power supplies, power loss occurs in a variety of ways. Some of the dominant methods are:

1. Ohmic power P losses resulting from current I through a resistive R device described by the equation:

   $$P = I^2 \times R$$

2. When a switch such as a FET is transitioning from either on or off, and if either current or voltage was in or across the FET, the transition period will result in both current and voltage across said FET, equating to power loss.
3. Hard switching is the event where a FET, previously off and having voltage V across it, switches on. Parasitic capacitance C across the outputs will retain 30 energy E

   $$E . 0.5 \times C \times V^2.$$

   Each time the FET turns on under this condition the energy stored is dissipated as power loss.

4. Gate drive losses in the form of an equivalent RC circuit where the C is the gate capacitance, and the R is the connecting gate resistor. RC circuits dissipate power proportionally to the

Frequency F, capacitance C and Voltage V squared:

$$P = FxcxV^2$$

One particular form of power control is the class E amplifier. A standard Class E amplifier is as shown in Figure 1 and has a FET with a transistor (T2) connected via a serial "LC" circuit to the load (R1), and is connected to the supply voltage (not 5 shown) via a large inductor (L2). L2 acts as a rough constant current source. The class-E amplifier adds a capacitor (C1) across the transistor output leading to ground. However such a power amplifier incurs a number of power losses.

Accordingly, it is an object of the present invention to overcome or substantially ameliorate one or more of the disadvantages of the prior art or at least provide an effective alternative.

Summary of the Invention

The present invention provides a means and method of power control using state based control. The invention provides a number of different modifications that *can* be used separately or together.

The power control for an AC application can include resonance tracking system of an input inductor being fed by a power source wherein the resonance tracking system 20 uses a resistor resonance detector having two sense resistor loads in series to ground and receiving feedback of the input inductor between the two sense resistor loads with the first sense resistor load leading to ground and the second sense resistor load feeding to comparator to provide the output controlling drive signal in comparison to an input of a reference voltage.

It can be seen that the arrangement of the sense resistors loads are clearly a voltage summing node for the two respective signals. The first sense resistor load to ground can detect DC variations of input. The second sense resistor load feeding to comparator can detect AC fluctuations.

The feed to the comparator from the second resistor load can be modified by an RC filter.

The power control can include a brake circuit having detection means including RC circuit on

voltage input feedback for ensuring no overcurrent.

The power control can include an active rectifier of input power to guarantee FET gate is within threshold in which there is a FET controller in combination with a linear regulator. The linear regulator can incorporate a large Resistor and small Zener voltage so as to minimise power losses through minimising current in control switching.

The power control can include a rectifier formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa. Preferably there are a pair of pairs of P and N 10 doped MOSFETs.

In this way operation of FETs with voltages of less than 1 Volt are still controlled by the rectifier. This also avoids punch through as operation of a pair of MOSFETs cannot occur at the same is impossible.

In one form of the invention there is provided with a state switching in regulation with switching in cycles being resonant and powered in compensation to each other to limit power usage and power losses.

The invention can provide substantial improvements in one form to an E class amplifier.

In a preferred embodiment the power control can relate to an E class amplifier and include any one or more of the following sections. These sections include:

A. Resonance tracking
B. Brake Circuit
C. Rectifier
D. Step Down

However these sections could also be used in other power control systems to perform analogous benefits.

It can be seen that the invention provides in one form a new method of class E topology control is presented. Whilst self resonant, the new approach has little in common with other self resonant systems where FET drive controls are coupled from other components such as transformers. Problems with such applications includepoorly defined

start/stop conditions, as well as limited room for wave form control.

The proposed method embeds real time, cycle by cycle digital control in simple components, with design freedom and advantages. Multiple analogue signals of differing values and frequencies are summed and thresholded by a single point of comparison. The control of these parameters allows precise resonant control from DC through to the physical limit of the resonant circuit of a large range of input voltages, with extraordinary efficiency, speed, and power factor.

Brief Description of the Drawings

In order that the invention can be more readily understood a specific embodiment will be described by way of non-limiting example wherein:

Figure 1 is a circuit diagram of a class E amplifier of the prior art;

Figure 2 is a circuit diagram of a power control of the invention in the form of a resonant driver in use in a class E amplifier of an embodiment of the invention;

Figure 3 is a circuit diagram of power control of one embodiment of the invention showing control with AC sense and no brake;

Figure 4 is an operational trace of V and I of power control circuit of Figure 3;

Figure 5 is a circuit diagram of power control of one embodiment of the invention showing brake;

Figure 6 is an operational trace of V and I of power control circuit of Figure 5;

Figure 7 is a circuit diagram of power control of one embodiment of the invention showing rectifier;

Figure 8 is a circuit diagram of power control of rectifier of prior art shown for comparative purposes;

Figure 9 is an operational trace of V and I of power control circuit of Figure 8;

Figure 10 is a circuit diagram of power control of one embodiment of the invention showing rectifier with active pulldown;

Figure 11 is an operational trace of V and 1 of power control circuit of Figure10;

Figures 12 and 13 are N and P FET equivalent sub circuits respectively showing the details of FETS X1 to X4 of Figure 10 in combination with linear regulator;

Figure 14 is a circuit diagram of power control of one embodiment of add on voltage control element to load of the invention showing step down and flyback alternatives;

Figure 15 is an operational trace of V and I of power control circuit using step down of Figure 14 for 9V at 10ms;

Figure 16 is an operational trace of V and I of power control circuit of Figure 15 at micro level.

Description of a Preferred Embodiment of the Invention

With reference to the drawings in this preferred embodiment, as shown in Figure 2 the invention provides an E class amplifier having all sections of

A, Resonance tracking

B. Brake Circuit

C. Rectifier

D. Step Down / Fly Back

A. Resonance tracking

As shown in Figure 1 one particular form of power control is the class E amplifier. A standard Class E amplifier has a FET with a transistor (T2) connected via a serial "LC" circuit to the load (R1), and is connected to the supply voltage (not shown) via a large inductor (L2), which acts as a rough constant current source.

However expanding this to an AC application, either low or high voltage, is shown in Figure 3. Here is the inclusion of the new resonant controller with components 01, V1 (reference voltage), R2 (resonance sensor) and R5 (input current sensor).

The power control for an AC application includes resonance tracking system of an input inductor being fed by a power source wherein the resonance tracking system uses a resistor resonance detector having two sense resistor loads in series. In this case the sense resistor loads are first and second sense resistors R5 and R11 to ground. Feedback of the input inductor L2 is received between the two sense resistor loads with the first sense resistor R5 leading to ground and the second sense resistor R11 feeding to comparator 01 to provide the output controlling drive signal in comparison to an input of a reference voltage Vl.

It can be seen that the arrangement of the sense resistors loads are clearly a voltage summing node for the two respective signals. The first sense resistor R5 to ground can detect DC variations of input. The second sense resistor R11 feeding to

comparator 01 can detect AC fluctuations.

The primary role of R5 is to track the desired current in L2. This way the system power can be controlled easily. Note that due to inevitable ripple current in L2, R5 does indeed contain ripple information. It is therefore feasible that normal operation can occur without the inclusion of R11. In practice, over the large voltage range imposed on the system by a rectified AC waveform, the necessity to amplify the ripple component becomes apparent. This is the point of R11; its inclusion ensures that adequate signal strengths is present. Note that the ratios of R11 and R5 also allow control of the system power factor.

Once the AC signal is adequate, it may be necessary to match the system resonance frequency with the digital system latencies. This can easily be achieved by the addition of optional phase lagging RC filters shown as R3 and C4 in Figure 2. Additional latency control at the output of the comparator 01 may be performed in the digital section as needed.

FIG 4 illustrates how the above successfully ensures correct and regular operation 15 *over* 1 *mains* half cycle which in macro view illustrates how the system always Zero Voltage Switches (ZVS) paramount to high speed, low loss operation.

B. Brake Circuit

With reference to the circuit of Figure 3 with no brake, it can be seen that without a brake over current conditions can result in a variety of issues. AC signal is biased by DC ripple providing signal of resonance. Then this is slowed down by RC system including R12 and C4 thereby self resonating system. However if resonant and current pulsed are added there is the overcurrent condition and failure. This is a major source of concern and prior art solutions use substantial power.

The circuit with brake is shown in Figure 5 with brake elements provided by R3 and transistor T3. In other form shown in Figure 2 the R6 and T3 provide the brake element. An important effect is that the brake element turns off FET of T1 if overshoot allowing flow through R15. With reference to Figure 5 and operational trace in Figure 6 it is shown that there is provided stoppage means or brake for any overcurrent. In particular switching occurs only after powering off of other signal control and thereby avoiding possibility of overcurrent.

C. Rectifier

A prior art active rectifier circuit can be seen in Figure 8 with operational trace in Figure 9. In particular the FETs being either A type or N type are connected to external resistors such as R4 which are of the order of 100 Ohm and therefore allow substantial current flow and corresponding power loss. In particular the trace of Figure 9 shows the input at the top and the effective output in the middle. However as shown by the lower trace there is substantial power losses throughout operation.

However the invention as shown in Figures 7 in its simplest form and Figures 10, 12 and 13 in detail with trace in Figure 11 shows a rectifier which can make use of the power control including an active rectifier of input power to guarantee FET gate is within threshold. This is achieved by a FET controller in combination with a linear regulator. The linear regulator can incorporate a large Resistor R4 of the order of 100K Ohm' and voltage close to operative voltage of the FET so as to minimise power losses through minimising current in control switching. In contrast to the trace of Figure 9 the trace in Figure 11 of the invention of Figure 10 shows the input at the top and the effective output in the middle. However as shown by the lower trace there is minimal intermittent power losses throughout operation.

As shown in Figure 10, the power control can include a rectifier formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa. In this case there are a pair of pairs of P and N doped MOSFETs with each of X1 to X4 comprising an NFET or PFET of Figures 12 and 13.

In this way operation of FETs with voltages of less than 1 Volt are still controlled by the rectifier. This also avoids punch through as operation of a pair of MOSFETs cannot occur at the same time and therefore cannot add voltages beyond threshold.

Particularly in low voltage, high current applications, AC to DC rectification can be more efficiently performed with a FET full bridge rather than diodes (Schottky, PN, carbide etc) as they need not have a forward conduction voltage drop anywhere near as large. There are some considerations in implementation:

1. If the maximum voltages exceed the FET gate values, protection must be implemented to ensure the MOSFETs are not destroyed. This is the

purpose of the Zener/resistor arrangement in the schematic provided.

2. The Zener should be just slightly smaller than the max gate voltage, otherwise conduction through the Zener consume large amounts of energy, this unfortunately means that the gate capacitance has far more energy than is necessary to turn the FET on.
3. The resistor must be large enough to limit current when input voltage exceeds the Zener, but small enough to keep the turn on and off time small enough, and to prevent FET shoot through.
4. As MOSFETs have gate capacitance, any resistance used as with the example cause issues with turn on and turn off delay,
5. The gate capacitance and resistor form an RC filter, which will consume energy when any AC is present on the input, worsening with frequency and amplitude

The new configuration shown in Figure 10 looks similar to the prior art of Figure 8. However clear differences are shown with further inspection into the X modules is given in 'SCH NFET basic' and 'SCH PFET basic of Figures 12 and 13. Each sub circuit (N and P) are designed to replace the MOSFET, Zener and resistor in the prior art, with the N's on the bottom, P's on the top of the bridge.

Examining the N FET subcircuit, the complete FET model is represented within the box. External to the Box is the added circuitry, a diode and FET (which would be only one device as MOSFETs always have body diodes) a resistor and a Zener. The addition of the MOSFET has a large impact on the circuit, such as:

1. The Zener can now be only large enough to ensure the rectifier FET is turned on, keeping the transfer of energy low.
2. The MOSFETs impedance is low during the charge of the bridge MOSFET, which allows for rapid charge, but becomes very high once the Zener voltage is reached, ensuring no leakage regardless of what AC signal is on the input.
3. As the Zener bias resistor is no longer charging the bridge MOSFET gate cap, its value can be very large, using very little energy.
4. When the gate signal pulls low, D1 (Ti's body diode) discharges the bridge gate capacitance.

The P FET subcircuit is identical in operation, just in a negative voltage sense as it is a P FET.

Referring to the Trace files of prior art Figure 9 and new active rectifier Figure 11, the red (top) trace shows a constructed wave form, a base signal of 12VRMS (+-17 volt peak to peak) AC, with a 5Vpp signal at much higher frequency. The next trace indicates the current from the source, the green is the voltage on the load resistor R1, the final trace is the current going into one half bridge P/N FET pair. The greatest indicator of improvement is the trace of Figure 11, as is illustrated the *new* active rectifier has, with the exception of switching currents, no visible current. Measurements have indicated that with a simple comparison to Figure 9, the new system is 98% efficient versus the old of 95%. This divide would become much greater over large input voltage ranges as the Zeners in the prior art conduct more and more, or if the frequency was increased.

Finally the next iteration of Fig 10 shows an enhancement which allow the bridge FET's threshold voltage to be lower than the body diode of the new gate drive FET. Signals are shared between N and P subcircuits to ensure the FETs are shutdown.

In each N or P pair, the opposing drive FET now also drives the other's newly added 'pull down' FET.

D. Step Down I Fly Back

The step down/ fly back component as shown in Figures 14 is often needed to connect at the output across Capacitor C2 as shown in Figure 2 for power control of LEDs due to operational voltage limitation. However such system may not be required in other power control areas.

Due to the constant forward voltage nature of Light Emitting Diodes (LEDs) the usable energy in a capacitor connected in parallel is very limited. This is because any voltage in the capacitor above the LED Vf (forward voltage) is quickly discharged at higher currents, until the voltage falls to Vf, at which point conduction stops. A simple approach to this is to have a resistor in series, which limits the current at voltages over Vf. The drawback to this is of course wasted energy in the resistor.

A more elaborate method is to implement a full 'buck' circuit. Done well this can minimize the additional power loss, at the expense of complexity and cost. A potential issue with this is the introduction of a 'negative impedance'- as voltage goes up, current-goes down and vice versa. This is in contrast to a 'positive impedance' which has current and voltage moving up and down together, proportionally or otherwise. In a standalone circuit a buck's negative impedance may not be an issue, but if used in conjunction with

another control scheme this may become problematic.

Another problem with having a capacitor directly in parallel with a LED occurs when we are using a boost topology. As the output voltage must always be greater than the input voltage, LED Vf's must therefore be relatively high. In the case of MR16 where the input voltage can reach over 17V peak (12VRMS) this limits the product to 20V+ dies. If we wish to use a lower voltage LED, a natural solution is to introduce a buck stage after the boost. However this introduces a problem where the individual boost and buck stages 'fight' each other, which is why despite the large capacitive energy reserve buffering between, the booster frequently turns off due to over voltage output conditions caused by a negative impedance load (the buck).

The present invention includes a much simpler step down mechanism to be introduced, which is much cheaper to implement, and still provides the boost with a positive impedance.

Referring to the Figure 14, there is shown a general possible combination. These can be used for a 9V and a 21V LED solution. Even though the 21V LED already meets the greater voltage requirements, the ripple current in the LED over mains frequencies (50-60Hz) is much better due to the more readily available energy reserve due to the large operational voltage range now available.

There are advantage of bucks in the prior art including allowing precise load regulation down to the load voltage if buck, or complete range if flyback. However there are also issues with bucks and flybacks including:

1. Expensive,
2. Complex closed loop systems and inefficient particularly if a high side FET drive is necessary (in buck configurations)
3. Imposes negative impedance characteristics on the voltage supply
4. Complexity and stability requirements generally limits maximum speed, which in turn requires larger passive components to implement

Similarly there are advantages of fixed frequency and duty step down or flyback

1. Open loop (no feedback) so very cheap and easy to implement
2. Only ever need low side switching so easy to implement
3. Imposes positive impedance at all times, easy to combine with regulation stage such as boost
4. Simplicity means that upper speeds are only limited by resonant source

drive capabilities, so can be incredibly high.

Issues with fixed frequency and duty step down or flyback

1. Open loop means that operation is limited to fixed transformation of input voltage- ie no adaption possible.

The operation of the present invention is with reference to the drawings but noting that Figure 14, R4 is included in series with D1 to represent a 'real' LED made up of desired and parasitic components. The Step down referred to in the 9V Schematic and Traces, has a very simple operation implements an oscillating source of any type capable of driving a FET, in this example V3. When the FET is biased on, current begins to rise in L3 the LED (D1) and C3. When the FET turns off, the inductor discharges into D1 and C3. C3 acts purely as an AC bypass to keep the current ripple in the LED to a minimum, and can therefore be extremely small. This simple action results in L3 appearing as an additional impedance in series with the LED, varying only with the difference in voltage between the LED Vf and the reservoir C3. This impedance can be varied by either changing the inductance of L1, or the frequency/duty cycle ratio of the inverter.

The flyback referred to in the 21V Traces and Schematics, as above the implementation is remarkably simple and also generally *shown* in Figure 14. When the FET is biased on, L1 begins to charge. When the FET is turn off, Ll discharges into C4 and the LED. Again, C4 is included to merely bypass AC, providing DC current to the LED. This circuit differs to the step down in that it is possible to discharge C4 below the LED voltage. Whilst desirable with a large Vf such as 21 V, this is highly undesirable with voltages already lower than the minimum allowed boost voltage. As with the step down, the Inductor appears as a roughly linear, positive impedance, so long as the frequency and duty cycle ratio are fixed.

Note that any frequency and duty can be implemented, there are advantages to some adjustments, such as:

1. Frequency Jitter- this can help if Electro Magnetic Interference (EMI) *are* encountered

2. Duty cycles ratios other than 50/50 (as used in the examples) may be useful particularly if lower Vf's are desired, setting the duty to say 15/85 on/off would allow step down voltages as low as 3Volts (single LED die) without adding any more complexity or feedback, depending on the oscillator source used.

While we have described herein a particular embodiment of a power control, it is further envisaged that other embodiments of the invention could exhibit any number and combination of any one of the features previously described. However, it is to be understood that any variations and modifications can be made without departing from the spirit and scope thereof

Claims

1. A Class E amplifier having a FET with a transistor (T2) connected via a serial "LC" circuit to the load, and connected to a supply voltage via a constant current source, the amplifier further including a resonant controller.

2. The amplifier according to claim 1 wherein the resonant controller provides power control for an AC application and includes resonance tracking system of an input inductor being fed by a power source with the resonance tracking system using a resistor resonance detector having two sense resistor loads in series.

3. The amplifier according to claim 2 wherein the resonant controller includes components reference voltage, resonance sensor and first input current sensor.

4. The amplifier according to claim 2 or 3 wherein the resonant controller includes sense resistor loads being first and second sense resistors R5 and R11 to ground with feedback of the input inductor L2 received between the two sense resistor loads with the first sense resistor R5 leading to ground and the second sense resistor R11 feeding to comparator to provide the output controlling drive signal in comparison to an input of a reference voltage.

5. The amplifier according to claim 4 wherein the resonant controller includes the arrangement of the first and second sense resistors loads forming a voltage summing node for the two respective signals with the first sense resistor R5 to ground detecting DC variations of input and the second sense resistor R11 feeding to comparator detecting AC fluctuations.

6. The amplifier according to any one of the preceding claims wherein the resonant controller includes first sense resistor R5 having primary role to track the desired current in L2 such that the system power is controlled.

7. The amplifier according to claim 4 wherein the resonant controller includes using ripple information on the sense resistor loads R5 due to ripple current in L2.

8. The amplifier according to claim 4 wherein the resonant controller includes

first sense resistor loads R5 in combination with R11 to amplify the ripple component to ensure adequate signal strengths over the large voltage range imposed on the system by a rectified AC waveform.

9. The amplifier according to claim 8 wherein the resonant controller includes the ratios of R11 and R5 selected to allow control of the system power factor.

10. The amplifier according to claim 4 wherein the resonant controller includes matching the system resonance frequency with the digital system latencies once the AC signal is adequate.

11. The amplifier according to claim 10 wherein the matching the system resonance frequency with the digital system latencies once the AC signal is achieved by the addition of optional phase lagging RC filters.

12. The amplifier according to claim 11 wherein the matching the system resonance frequency with the digital system latencies at the output of the comparator is performed in the digital section.

13. The amplifier according to claim 4 wherein the system resonance control successfully ensures correct and regular operation 15 *over* 1 *mains* half cycle allowing the system to Zero Voltage Switches (ZVS) paramount to high speed, low loss operation.

14. The amplifier according to any one of the preceding claims further including a brake circuit having brake elements provided by arrangement of FET and resistor load R3 and transistor T3 in output of FET of amplifier and in feedback circuit to input of FET of amplifier following determination of feedback of input inductor feed such that the brake element turns off FET of brake circuit if overshoot of current allowing flow through resistor load and thereby providing stoppage means or brake for any overcurrent.

15. The amplifier according to claim 14 wherein brake circuit switching occurs only after powering off of other signal control and thereby avoiding possibility of overcurrent.

16. The amplifier according to any one of the preceding claims further including an active rectifier which uses the power control including an active rectifier of input

power to guarantee FET gate is within threshold, by using a FET controller in combination with a linear regulator.

17. The amplifier according to claim 16 wherein the linear regulator incorporates a large resistor R4 of the order of 100K Ohm' and voltage close to operative voltage of the FET so as to minimise power losses through minimising current in control switching.

18. The amplifier according to claim 16 or 17 wherein the rectifier is formed of a plurality of pairs of P and N doped MOSFETs wherein gate of one P doped MOSFETs is connected to drain of N doped MOSFET and vice versa.

19. The amplifier according to claim 18 wherein the rectifier includes a pair of pairs of NFET or PFET, wherein operation of FETs with voltages of less than 1 Volt are controlled by the rectifier.

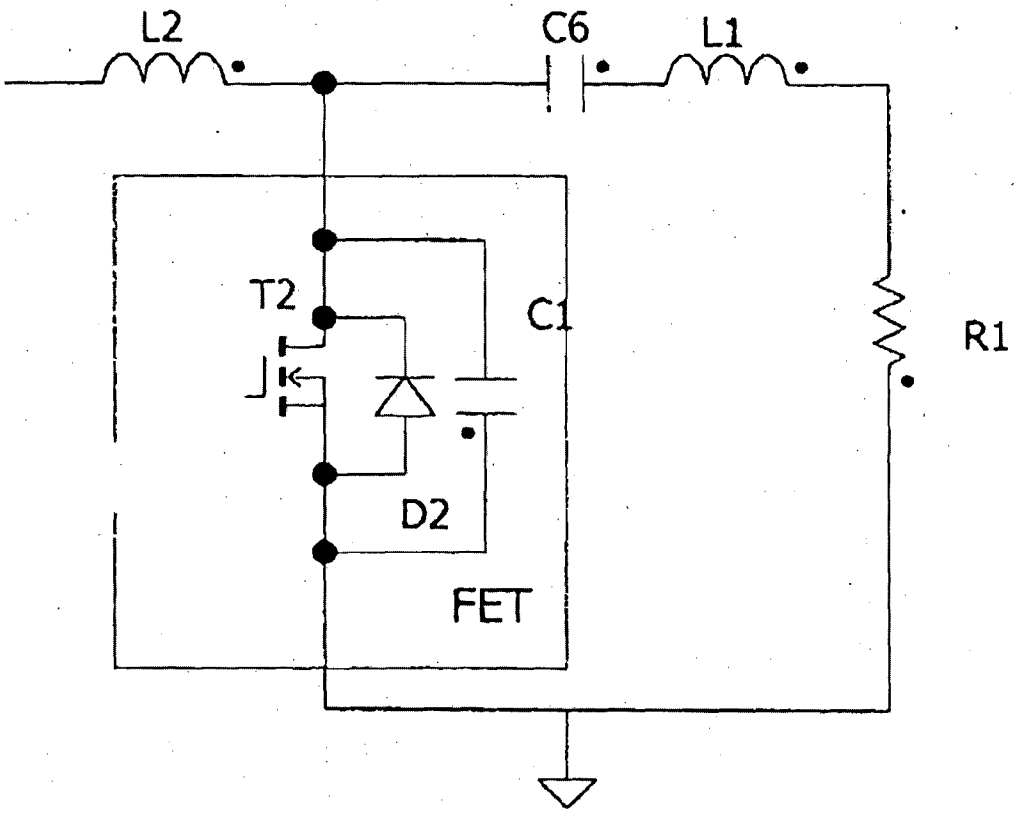
20. The amplifier according to claim 19 wherein the rectifier includes a Zener/resistor arrangement connecting between the pair of pairs of P and N doped MOSFETs.

21. The amplifier according to claim 19 wherein the Zener is only large enough to ensure the rectifier FET is turned on, keeping the transfer of energy low.

22. The amplifier according to claim 19 wherein the MOSFETs impedance is low during the charge of the bridge MOSFET, which allows for rapid charge, but becomes very high once the Zener voltage is reached, ensuring no leakage regardless of what AC signal is on the input.

23. The amplifier according to claim 19 wherein the Zener bias resistor value can be very large, using very little energy as it is not charging the bridge MOSFET gate cap.

24. The amplifier according to claim 19 wherein, when the gate signal pulls low, D1 (Ti's body diode) discharges the bridge gate capacitance.



Class E prior art

FIGURE 1

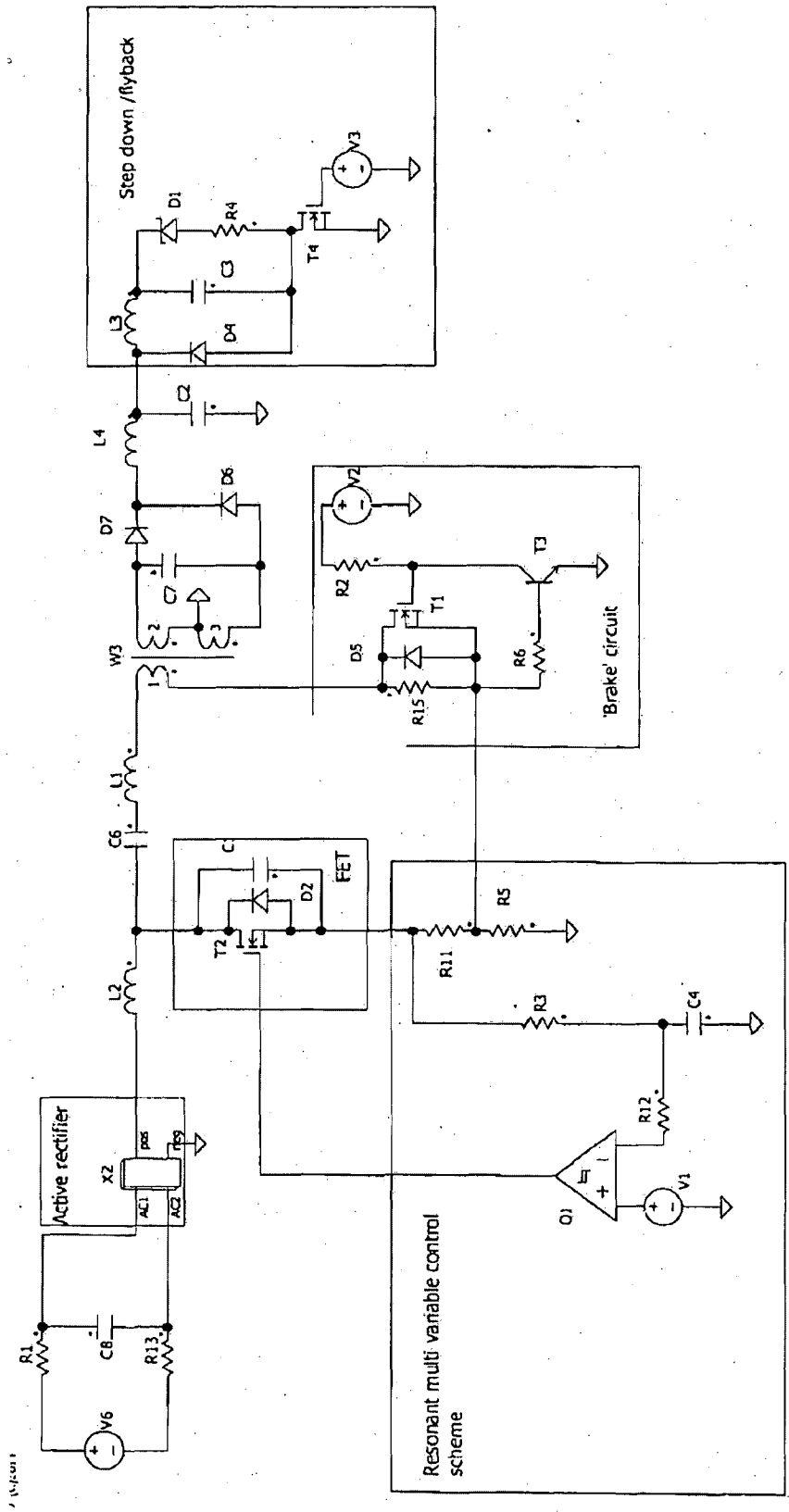

Step down /flyback
D1
R4
V3
T4
C3
L3
D4
C2
L4
D6
D7
C5
W2
W3
L1
C6
V2
R2
T3
T1
D5
R6
R15
'Brake' circuit
C
FET
D2
T2
L2
R5
R11
R3
C4
R12
V1
O1
Resonant multi variable control scheme
Active rectifier
X2
pos
neg
AC1
AC2
R1
C8
R13
V6

FIGURE 2

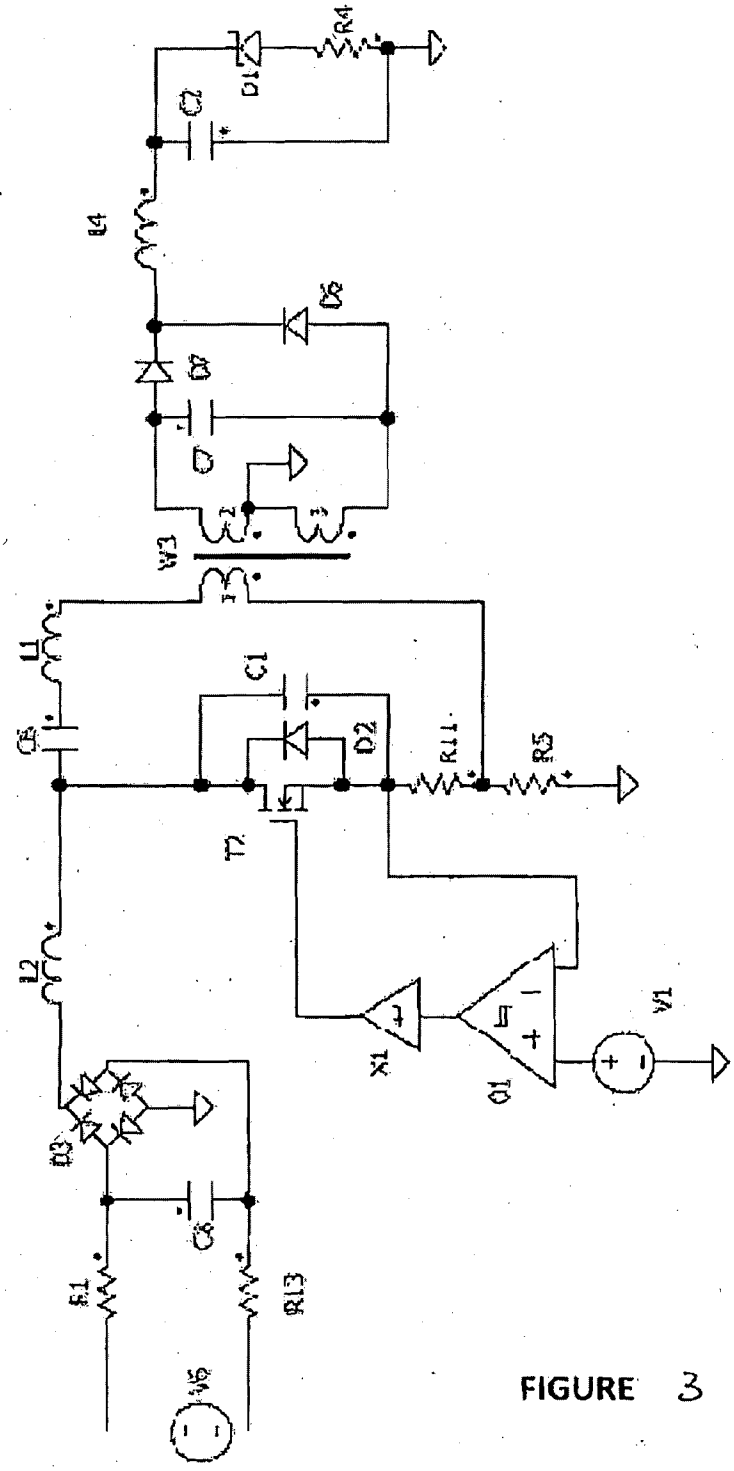

R4
D1
C2
L4
D8
D8
C
D
L3
L1
C5
C1
D2
R11
R5
T1
L2
X1
U1
V1
D3
C6
R1
R13
V6

FIGURE 3

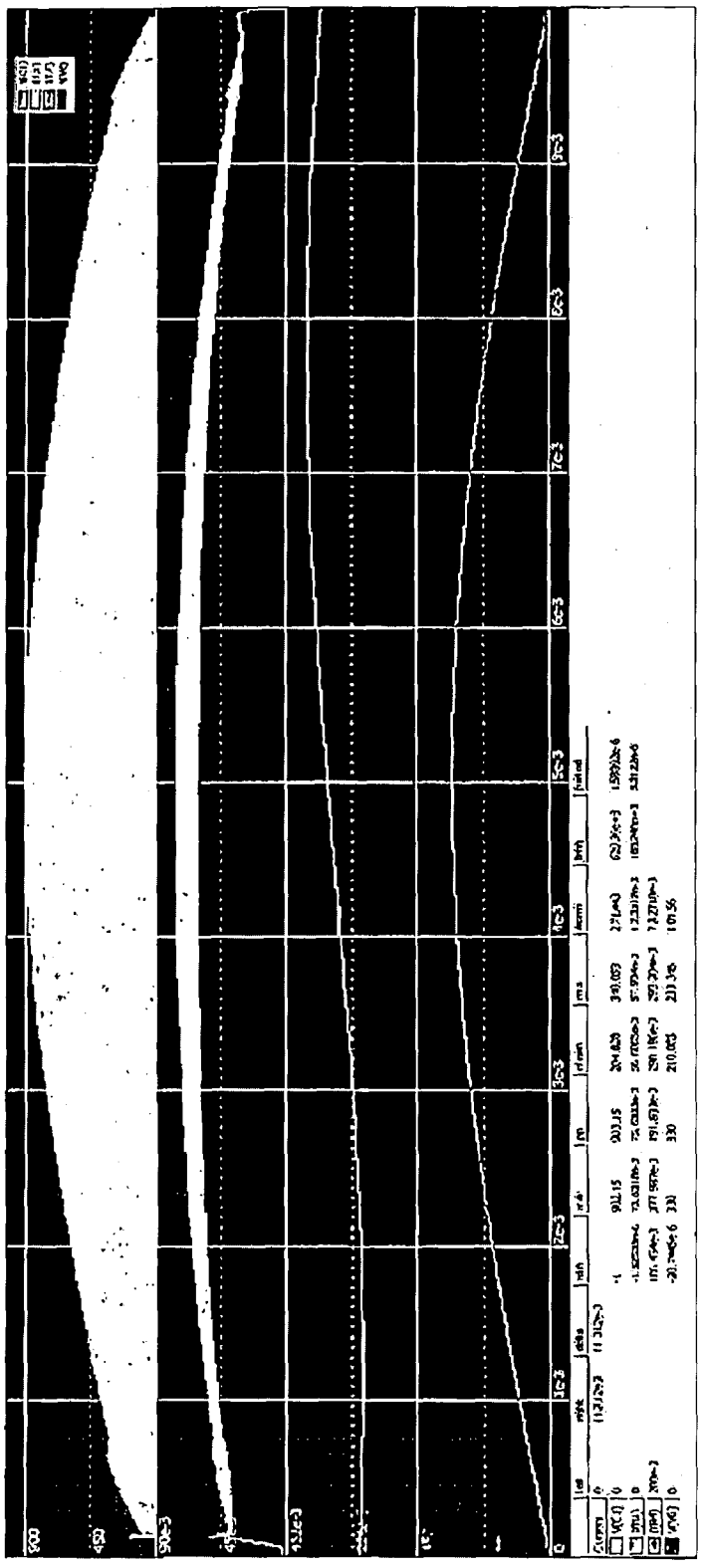


FIGURE 4

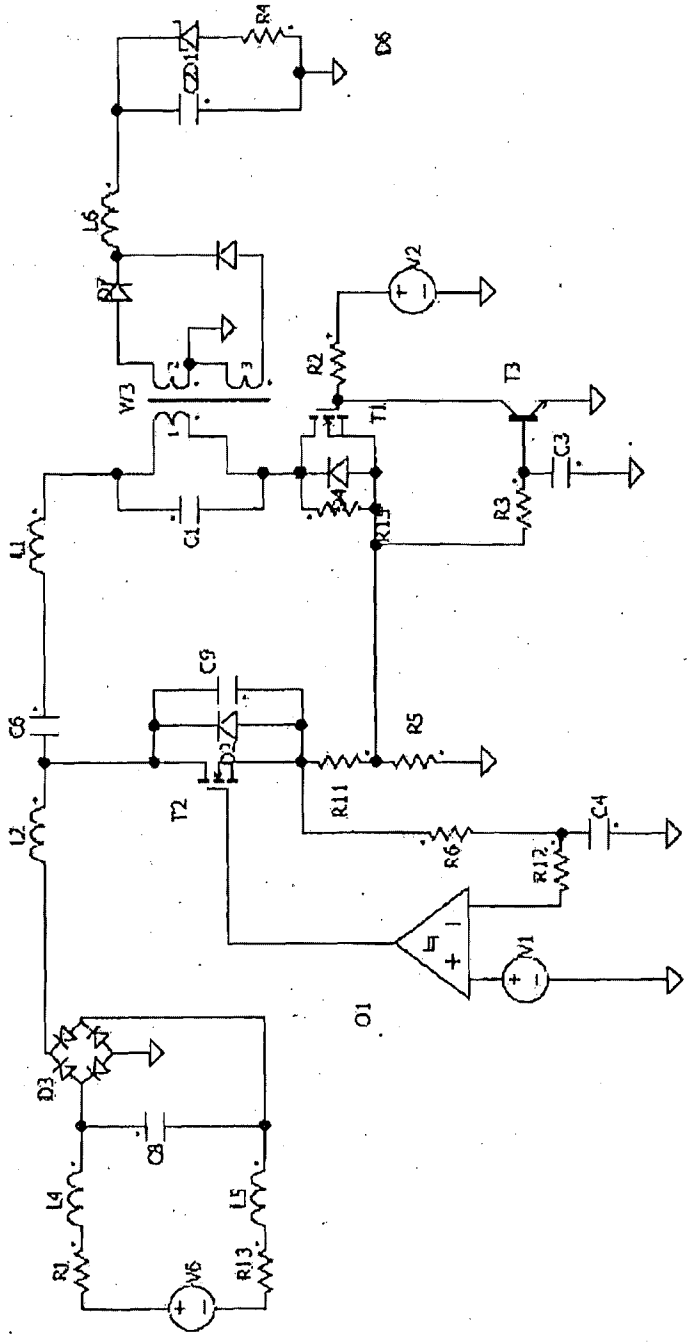

R4
D6
D12
L6
D7
V2
R2
T3
T1
V3
L3
C3
C1
R3
R15
L1
C9
C6
R5
D2
T2
R11
C4
L2
R6
R12
V1
O1
D3
C8
L4
L5
R1
R13
V6

FIGURE 5

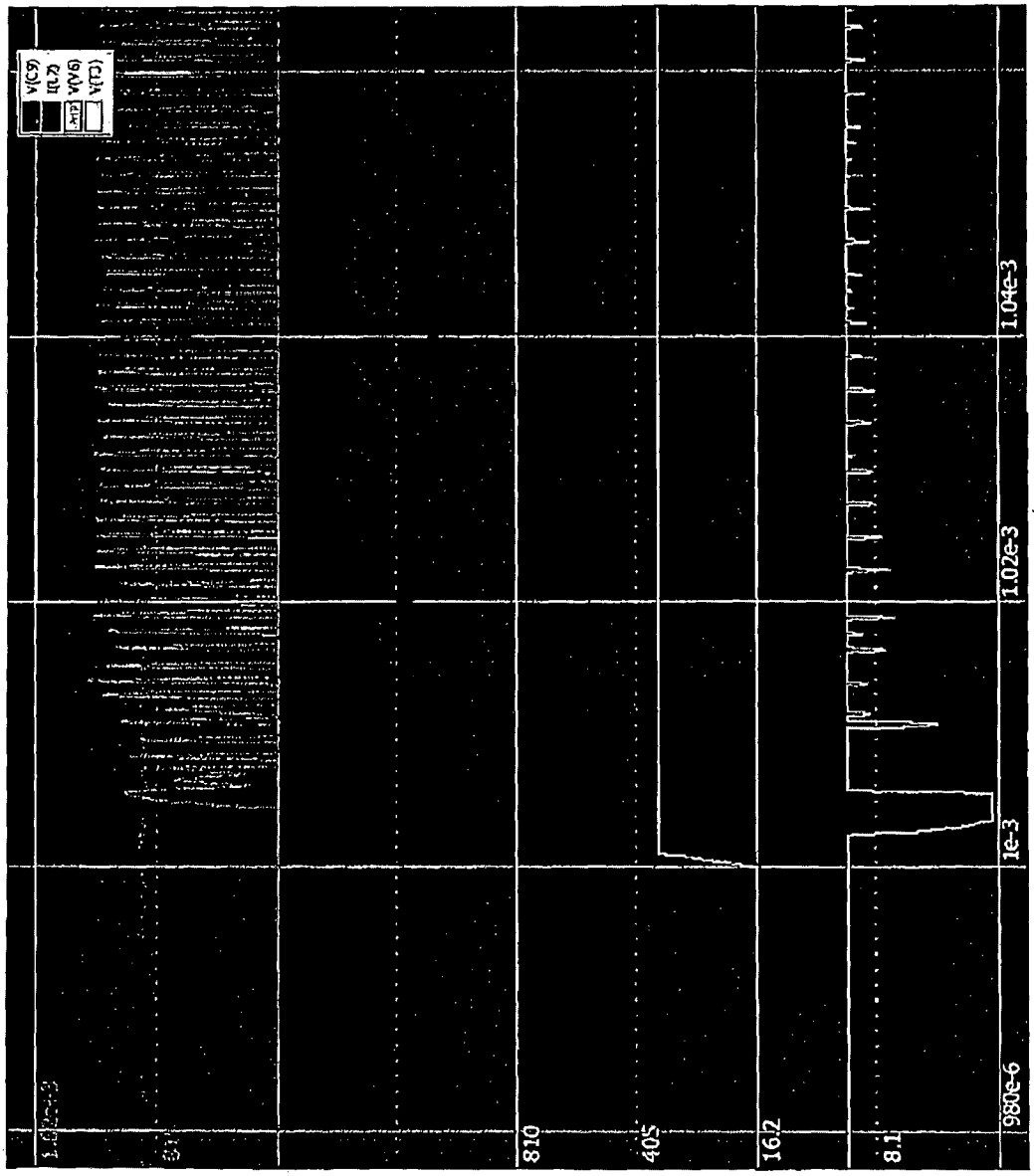


FIGURE 6

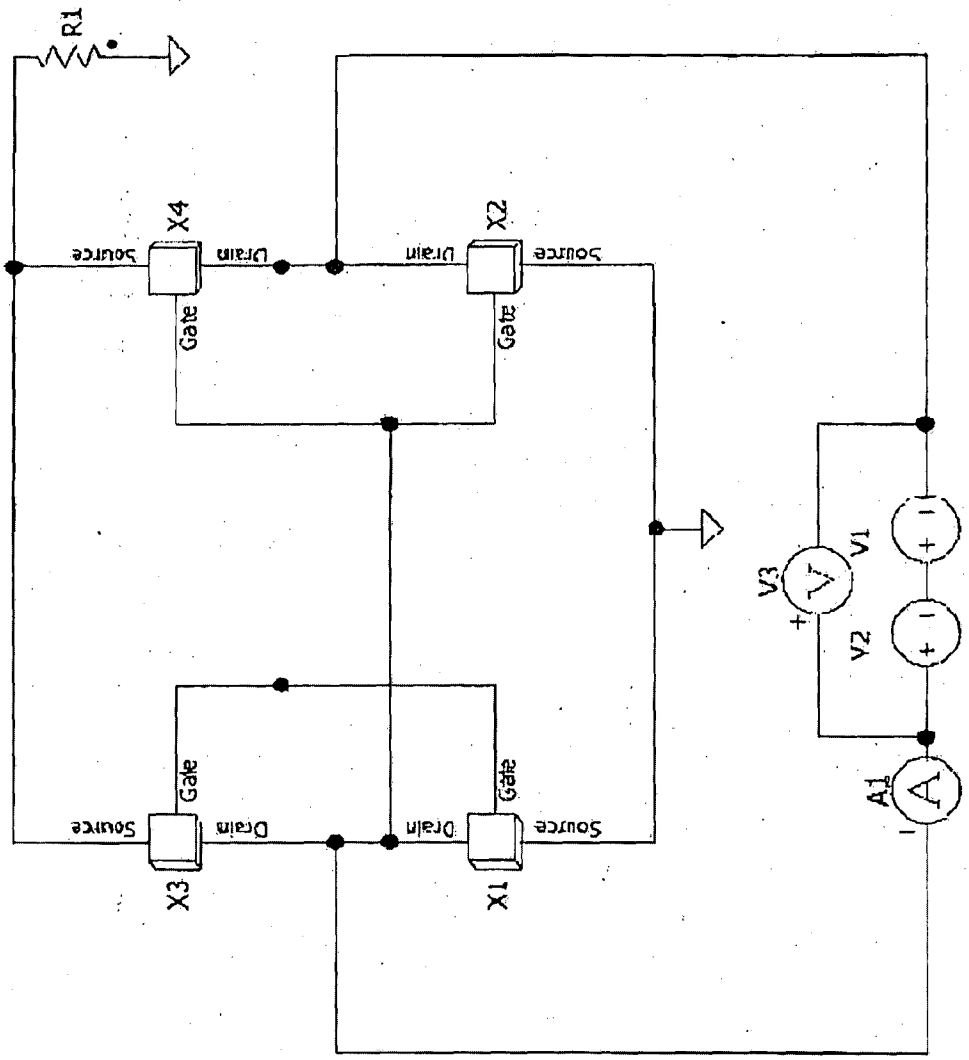

R1
X4
Source
Drain
Gate
X2
Drain
Source
Gate
V3
V1
V2
A1
Gate
Source
Drain
X3
Drain
Source
Gate
X1

FIGURE 7

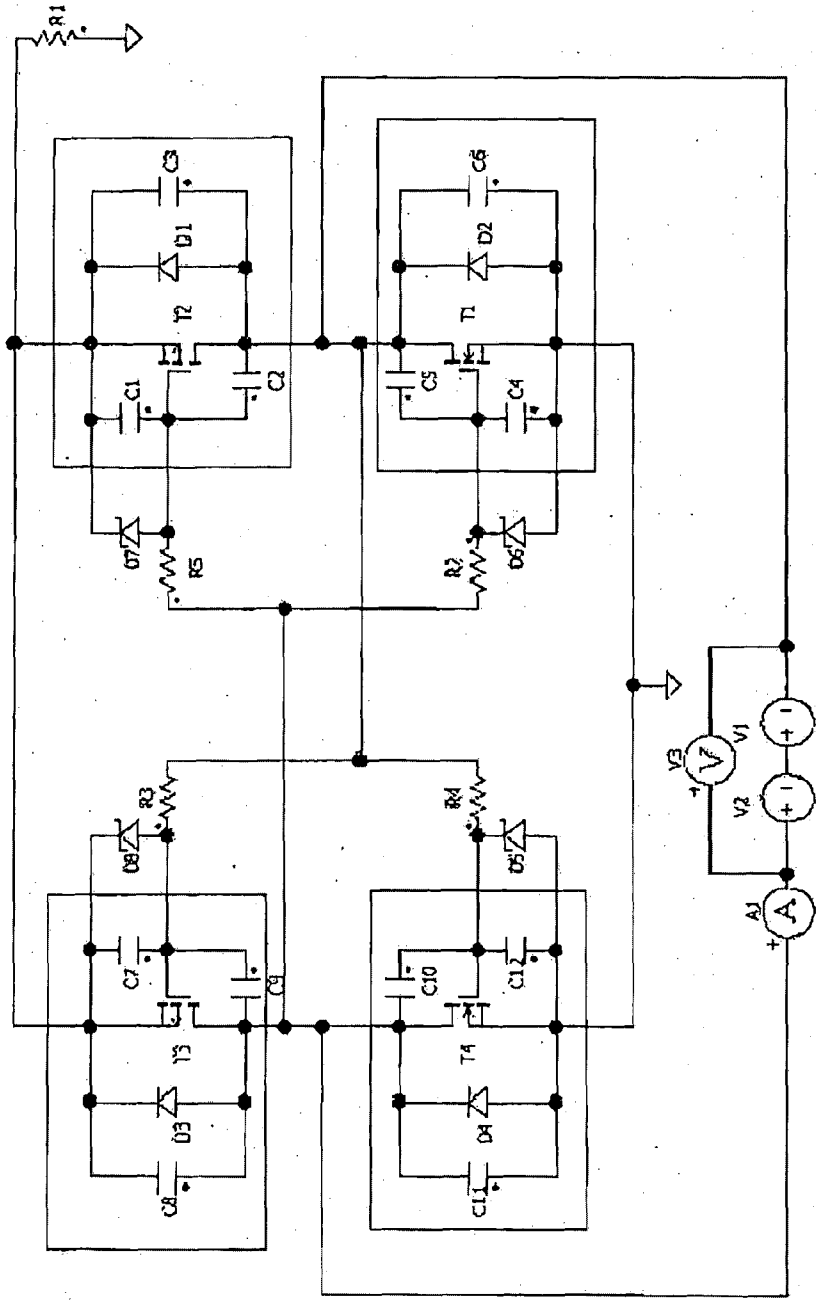

R1
C3
D1
T2
C1
C2
C6
D2
T1
C5
C4
D7
R5
R2
D6
R3
R4
D8
D5
C7
C9
C10
C12
T3
T4
D3
D4
C8
C11
V3
V1
V2
A1

FIGURE 8

FIGURE 9

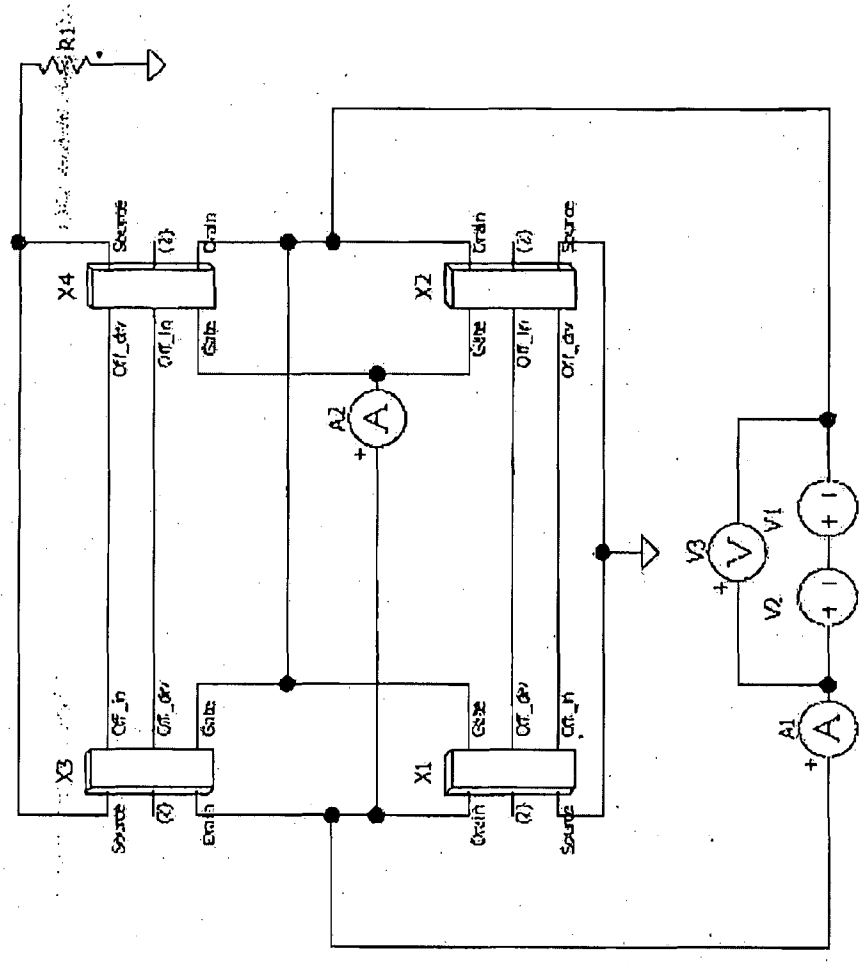


FIGURE 10

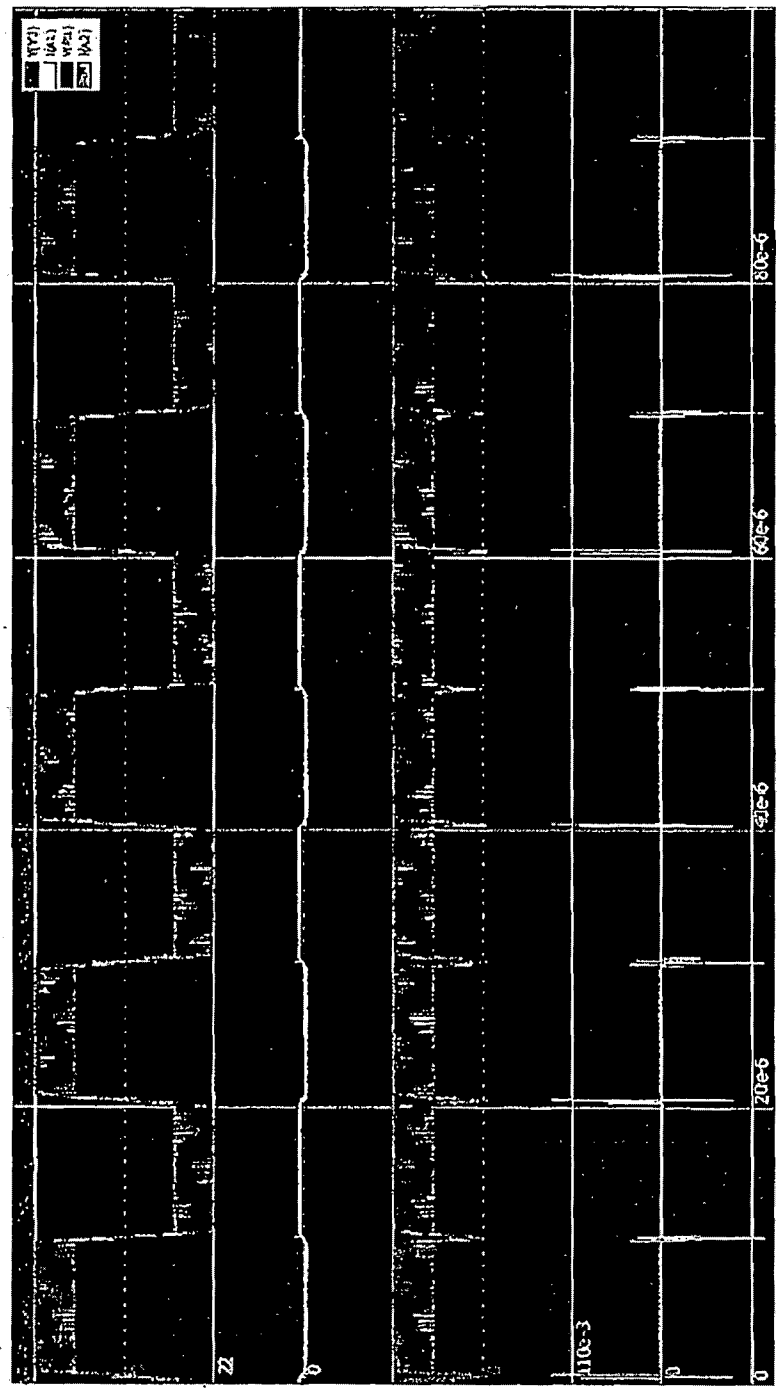


FIGURE 11

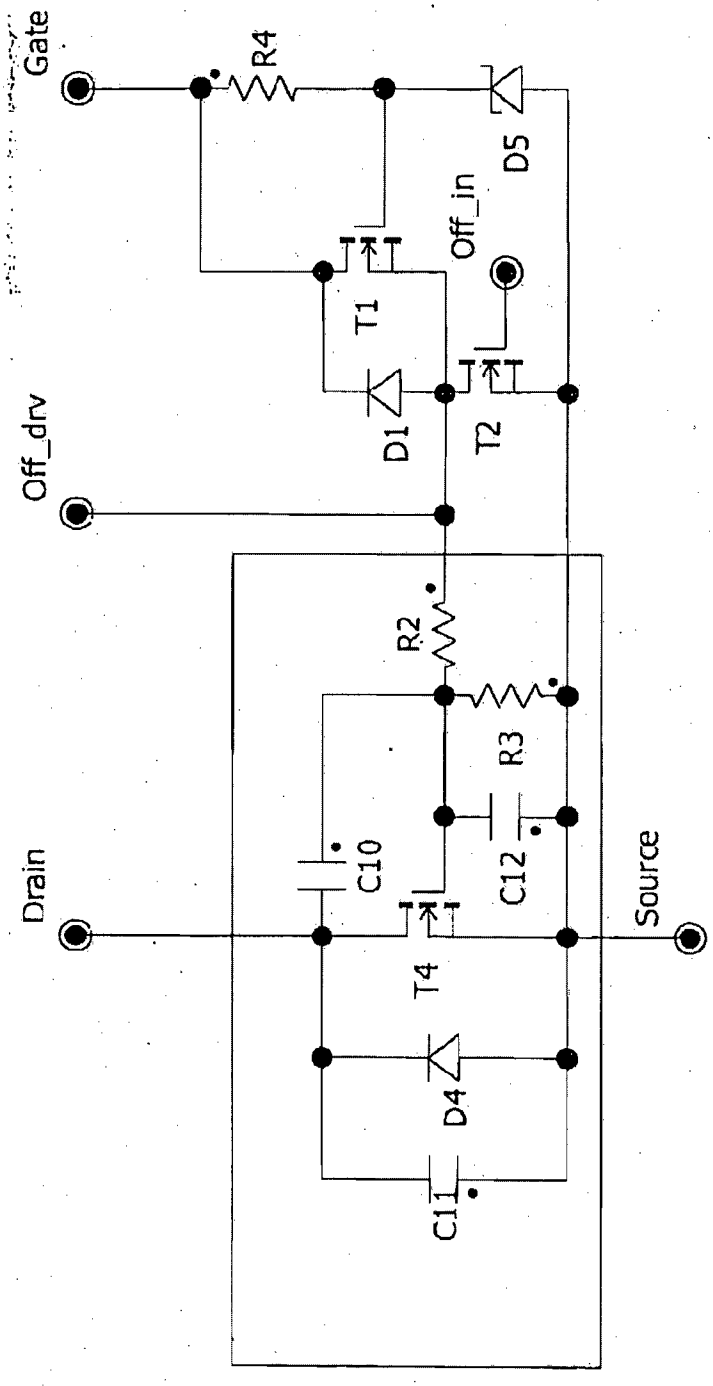

Gate
R4
D5
Off_in
T1
D1
T2
Off_drv
R2
R3
C10
C12
Drain
Source
T4
D4
C11

FIGURE 12

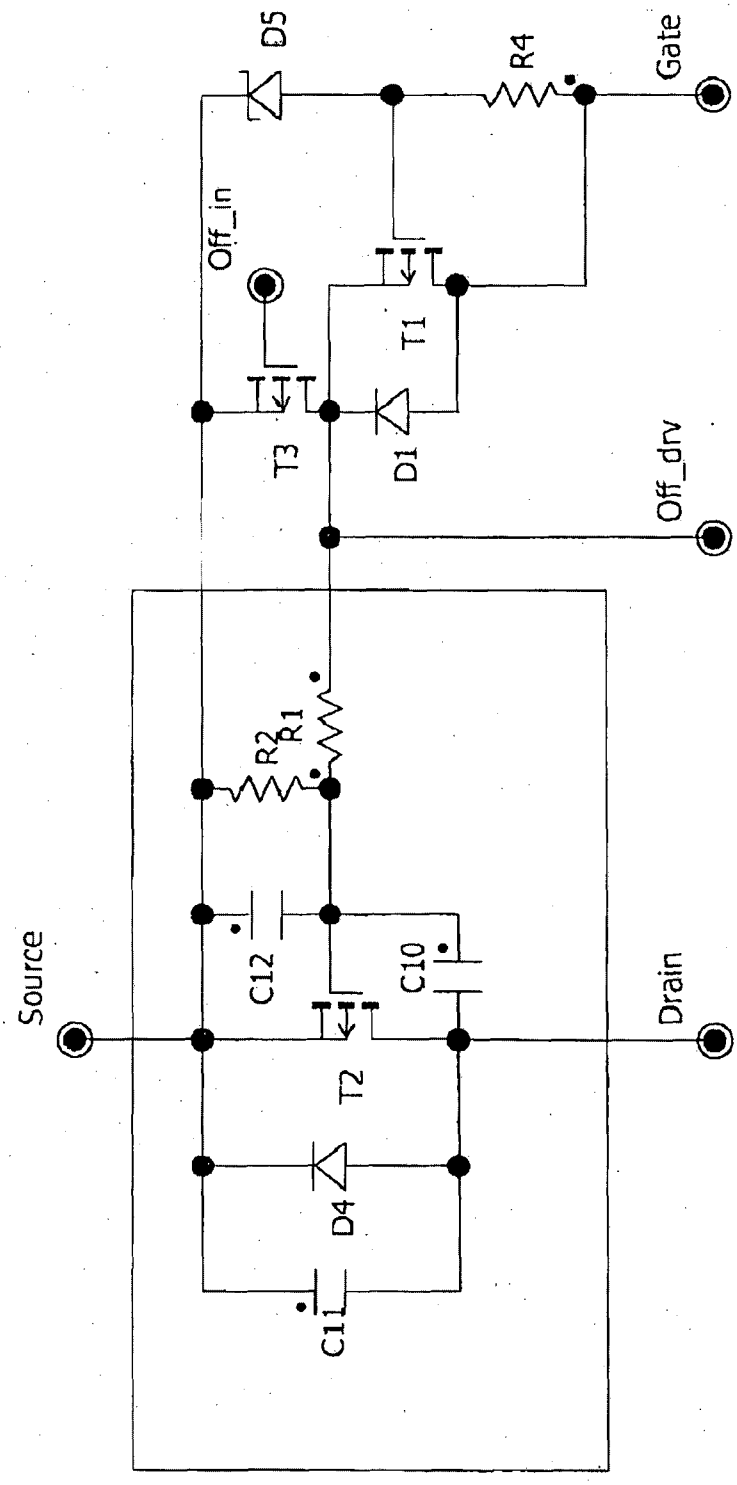

D5
R4
Gate
Off_in
T1
T3
D1
Off_drv
R2
R1
C12
C10
Source
Drain
T2
D4
C11

FIGURE 13

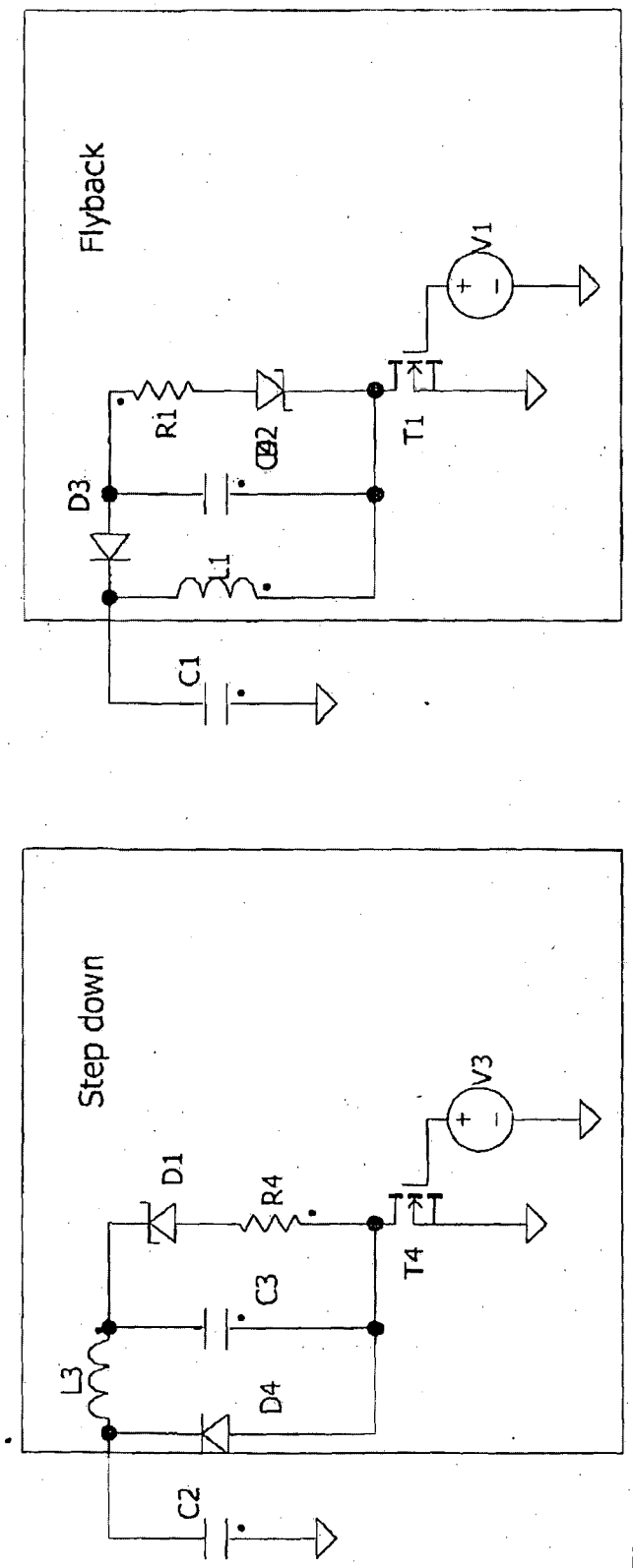


FIGURE 14

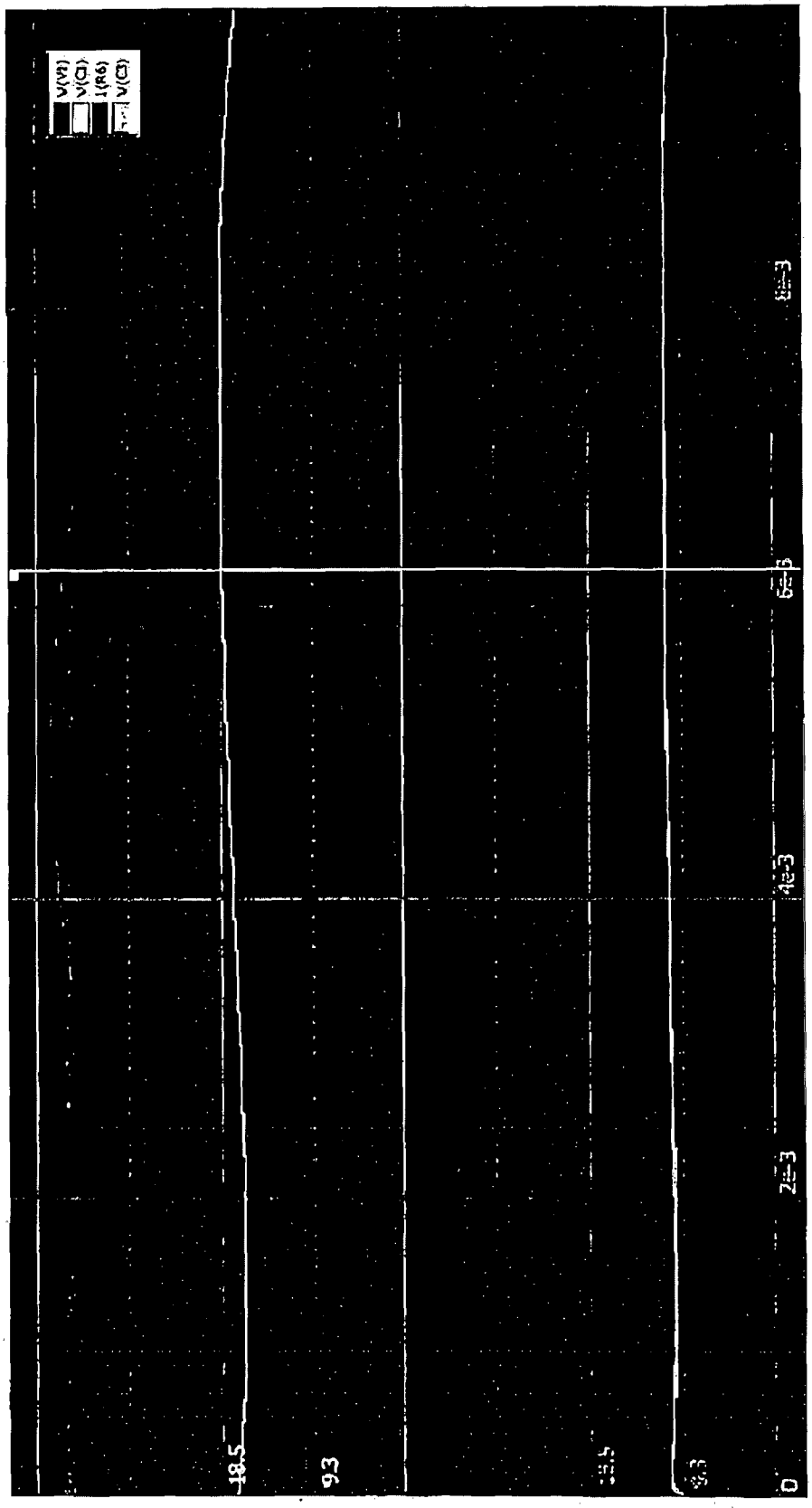


FIGURE 15

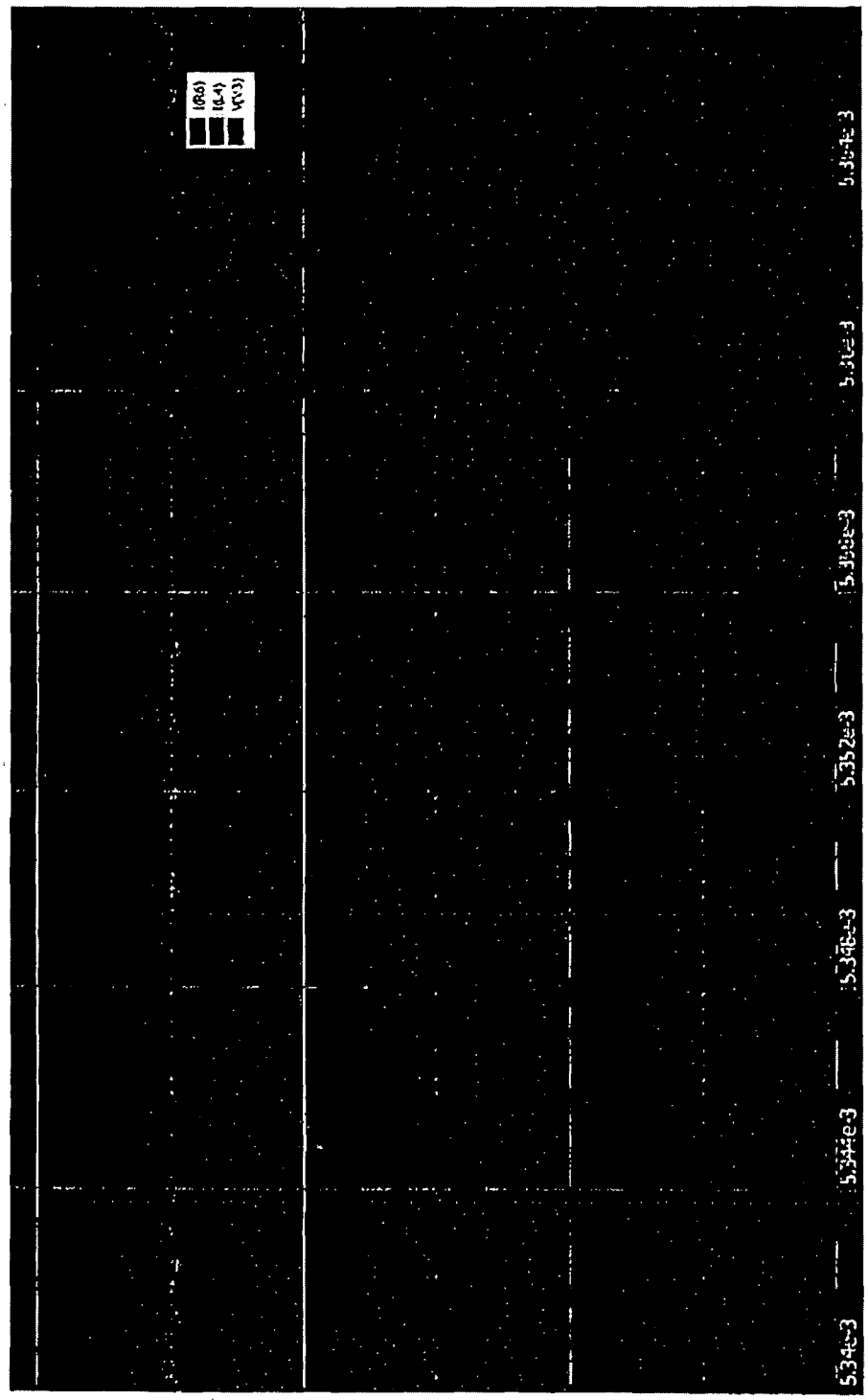


FIGURE 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2012/001246

A. CLASSIFICATION OF SUBJECT MATTER

H02M 3/335 (2006.01) H02M 7/539 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, WPI, TXTUS0, TXTUS1, TXTUS2, TXTUS3, TXTUS4, TXTEP1, TXTGB1, TXTWO1, Google Patents, Espacenet: fet, amplifier, sense, resistor, current, resonant and like key words.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 January 2013	25 January 2013

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Telephone No. 0262832879

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/AU2012/001246**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2005/0281061 A1 (RADECKER ET AL.) 22 December 2005 Fig.7-8, para.[0028], [0046], [0067]-[0070] Fig.5, 5A, 6-8, para.[0015], [0028], [0046], [0067]-[0070], [0095]-[0099]	1-6 7-24
Y	JP 01-186170 A (FUJII DENKI KOGYO KK) 25 July 1989 Abstract, fig.3	14-15
Y	EP 2333947 A1 (HARRIS CORPORATION) 15 June 2011 Abstract, fig.1, para.[0067]	16-24

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2012/001246

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Supplemental Box

Continuation of: **Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Claims 1-13 are directed to a class E amplifier. Claim 1 can be grouped with any one of the three groups. However, for the simplicity, claim 1 is included in this group.. The feature of the means to track system using resistor resonance detector having two sense resistor loads in series is specific to this group of claims.

- Claims 14-15 are directed to a class E amplifier.. The feature of the means to provide stoppage or brake for any overcurrent by using a brake circuit having brake elements such as FET, load R3, transistor T3 in the output of the amplifier is specific to this group of claims.

- Claims 16-24 are directed to a class E amplifier.. The feature of the means to guarantee FET gate is within threshold by providing an active rectifier by using a FET controller in combination with a linear regulator is specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. The only feature common to all of the claimed inventions and which provides a technical relationship among them is a Class E amplifier having a FET with the transistor connected via a serial LC circuit to the load, and connected to a supply voltage via a constant current source, the amplifier further including a resonant controller.

However this feature does not make a contribution over the prior art because it is disclosed in:
Fig.7, para. [0028], [0046] of D1: US 2005/0281061 A1 (RADECKER ET AL.) 22 December 2005

Therefore in the light of this document this common feature cannot be a special technical feature. Therefore there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a posteriori*.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2012/001246**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
US 2005/0281061 A1	22 Dec 2005	CN 1729613 A	01 Feb 2006
		DE 10259088 A1	22 Jul 2004
		US 2005281061 A1	22 Dec 2005
		US 7218533 B2	15 May 2007
		WO 2004055962 A2	01 Jul 2004
JP 01-186170 A	25 Jul 1989	JP 1186170 A	25 Jul 1989
EP 2333947 A1	15 Jun 2011	EP 2333947 A1	15 Jun 2011
		US 2011141782 A1	16 Jun 2011
		US 8045350 B2	25 Oct 2011

End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.