

(43) International Publication Date
7 July 2011 (07.07.2011)(10) International Publication Number
WO 2011/081998 A2(51) International Patent Classification:
H04R 19/04 (2006.01)**Lance, W.** [US/US]; 222 Cliffbrook Drive, Wylie, TX 75098 (US).(21) International Application Number:
PCT/US2010/061240(74) Agents: **FRANZ, Warren, L.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O.Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).(22) International Filing Date:
20 December 2010 (20.12.2010)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/291,760 31 December 2009 (31.12.2009) US
12/969,784 16 December 2010 (16.12.2010) US(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 12/969,784 (CON)
Filed on 16 December 2010 (16.12.2010)(71) Applicant (for all designated States except US): **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O.Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant (for JP only): **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventors; and

Declarations under Rule 4.17:

(75) Inventors/Applicants (for US only): **DENISON, Marie** [BE/US]; 9817 Sota Grande Drive, Plano, TX 75025 (US). **GOODLIN, Brian, E.** [US/US]; 6409 Dunmoor Drive, Plano, TX 75093 (US). **SHIH, Wei-Yan** [US/US]; 2332 Eldger Drive, Plano, TX 75025 (US). **BARRON,**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

— as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT FORMED WITH MICROPHONE TRANSDUCER

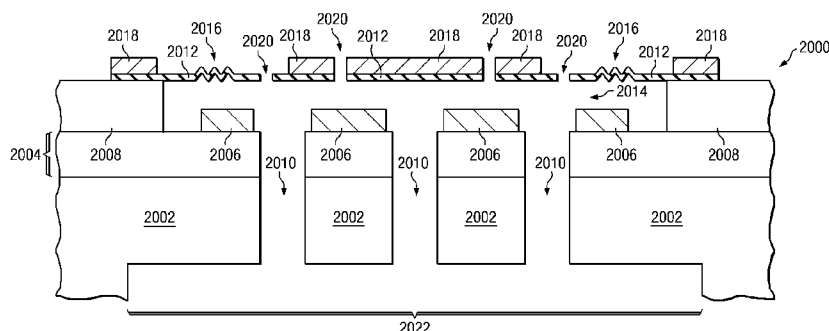


FIG. 2

(57) Abstract: A capacitive microphone transducer integrated into an integrated circuit (2000) includes a fixed plate (2006) and a membrane (2012) formed in or above an interconnect region (2004) of the integrated circuit. A process of forming an integrated circuit containing a capacitive microphone transducer includes etching access trenches (2010) through the fixed plate (2006) to a region defined for the back cavity (2014), filling the access trenches with a sacrificial material, and removing a portion of the sacrificial material from a back side of the integrated circuit.



Published:

- *without international search report and to be republished
upon receipt of that report (Rule 48.2(g))*

INTEGRATED CIRCUIT FORMED WITH MICROPHONE TRANSDUCER

[0001] This invention relates to the field of integrated circuits. More particularly, this invention relates to microphone transducers in integrated circuits.

BACKGROUND

[0002] Integration of microphone transducers including backside cavities into integrated circuits has been problematic.

SUMMARY

[0003] A capacitive microphone transducer integrated into an integrated circuit includes a fixed plate and a membrane formed in or above an interconnect region of the integrated circuit. A process of forming the capacitive microphone transducer includes etching access trenches through the fixed plate, forming a back cavity, forming a sacrificial fill region of sacrificial material, and removing a portion of the sacrificial material from a back side of the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Example embodiments are described with reference to the accompanying drawings, wherein:

[0005] FIGS. 1A - 1G are cross-sectional views illustrating successive stages of fabrication of an integrated circuit including a capacitive microphone transducer according to an example embodiment.

[0006] FIG. 2 is a cross-sectional view of an integrated circuit including a capacitive microphone transducer according to an example embodiment.

[0007] FIGS. 3A - 3D are cross-sectional views illustrating successive stages of fabrication of an integrated circuit including a capacitive microphone transducer according to an example embodiment.

[0008] FIGS. 4A - FIG. 4B are cross-sectional views illustrating successive stages of fabrication of an integrated circuit including a capacitive microphone transducer according to an example embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0009] A capacitive microphone transducer formed in an integrated circuit includes a fixed plate of a microphone transducer capacitor, a membrane plate, referred to herein as a membrane, of the microphone transducer capacitor, and a back cavity. The membrane responds to acoustic waves in an ambient above the integrated circuit by moving up and down relative to the fixed plate. The back cavity is an open region located below the fixed plate and membrane, extending through a substrate of the integrated circuit.

[0010] A capacitive microphone transducer may be integrated into an integrated circuit by forming the fixed plate and the membrane of interconnect elements of the integrated circuit. The capacitive microphone transducer may further be integrated into the integrated circuit by forming access trenches through the fixed plate, forming a back cavity, forming a sacrificial fill region of sacrificial material, and removing a portion of the sacrificial material from a back side of the integrated circuit.

[0011] FIGS. 1A - 1G illustrate stages in the fabrication of an integrated circuit including a capacitive microphone transducer according to an example embodiment. The integrated circuit may include digital circuits such as complementary metal oxide semiconductor (CMOS) circuits, analog circuits, or a combination of digital and analog circuits. The integrated circuit may contain components such as inductors, capacitors, a charge pump for example to provide power to the capacitive microphone transducer, an amplifier such as a junction field effect transistor (JFET) based amplifier, or other components.

[0012] Referring to FIG. 1A, the integrated circuit 1000 is formed in and on a substrate 1002, which may be a single crystal silicon wafer, or may be a silicon-on-insulator (SOI) wafer, or other material appropriate for fabrication of the integrated circuit 1000. The integrated circuit 1000 includes a first interconnect region 1004 of one or more layers of interconnect levels and dielectric layers formed over the substrate 1002. In one realization of the instant embodiment, a top surface of the first interconnect region 1004 in a microphone transducer area 1006 defined for the capacitive microphone transducer is substantially free of metal interconnect elements such as contacts, metal interconnect lines or vias. In one realization of the instant embodiment, the microphone

transducer area 1006 may be between 100 microns and 2 millimeters wide. A fixed plate 1008 of the capacitive microphone transducer is formed on a top surface of the first interconnect region 1004. In one realization of the instant embodiment, the fixed plate 1008 may be formed concurrently with horizontal interconnect elements (not shown in FIG. 1A) in the integrated circuit 1000. In a further embodiment, the fixed plate 1008 may include copper. In an alternate embodiment, the fixed plate 1008 may include aluminum or aluminum with copper. Cavity access openings 1010 are formed in the fixed plate 1008 to accommodate cavity access trenches formed in subsequent fabrication steps. Membrane terminals 1012 may be formed over the first interconnect region 1004.

[0013] FIGS. 1B and 1C depict alternate processes for forming access trenches in the integrated circuit 1000.

[0014] Referring to FIG. 1B, an access trench photoresist pattern 1014 is formed on an existing top surface of the integrated circuit 1000 to define areas for access trenches 1016. In the realization of the instant embodiment depicted in FIG. 1B, the access trench photoresist pattern 1014 overlaps edges of the fixed plate 1008. In one realization of the instant embodiment, the access trenches 1016 may be between 500 nanometers and 10 microns wide, and between 1 micron and 100 microns deep. The access trenches 1016 are formed by an access trench etch process 1018, for example a reactive ion etch (RIE) process using a fluorine containing plasma. Other processes, such as laser ablation, which may be used to form the access trenches 1016 are within the scope of the instant embodiment. In one realization of the instant embodiment, the access trench photoresist pattern 1014 may be removed after formation of the access trenches 1016 is completed, for example by exposing the integrated circuit 1000 to an oxygen containing plasma, followed by a wet cleanup.

[0015] Referring to FIG. 1C, an alternate access trench photoresist pattern 1020 is formed on an existing top surface of the integrated circuit 1000 to define areas for access trenches 1016. In the realization of the instant embodiment depicted in FIG. 1C, the alternate access trench photoresist pattern 1020 does not overlap edges of the fixed plate 1008. Access trenches 1016 are formed as described in reference to FIG. 1B.

[0016] Referring to FIG. 1D, a cavity fill sacrificial layer 1022 is formed on the fixed plate 1008 extending into the access trenches 1016. The cavity fill sacrificial layer

1022 can be removed in a subsequent fabrication step while removing substantially no material from the first interconnect region 1004. In one realization of the instant embodiment, the cavity fill sacrificial layer 1022 may include an organic polymer such as photoresist, polyimide, or phenolic resin. In an alternate embodiment, the cavity fill sacrificial layer 1022 may include a compound of silicon and oxygen, such as a porous silicon dioxide. In a further embodiment, the cavity fill sacrificial layer 1022 may include another inorganic material. The cavity fill sacrificial layer 1022 is sized for a desired spacing between the fixed plate 1008 and a membrane of the capacitive microphone transducer. If the membrane terminals 1012 are present, terminal via holes 1024 may be formed in the cavity fill sacrificial layer 1022. The cavity fill sacrificial layer 1022 may optionally be planarized to provide a desired thickness and surface planarity. In one realization of the instant embodiment, patterned planarization buffers 1026 may be formed on a top surface of the cavity fill sacrificial layer 1022 to provide more uniform planarization, for example during a chemical mechanical polishing (CMP) process. The patterned planarization buffers 1026 may be completely removed during the planarization process.

[0017] Referring to FIG. 1E, a first membrane layer 1028 is formed on a top surface of the cavity fill sacrificial layer 1022. In one realization of the instant embodiment, the first membrane layer 1028 may be formed concurrently with liner metal elements of interconnects (not shown in FIG. 1E) in the integrated circuit 1000. In a further embodiment, the first membrane layer 1028 may include tantalum nitride (Ta₂N₃), titanium nitride (TiN), titanium aluminum (TiAl) or a combination thereof. In other embodiments, the first membrane layer 1028 may include aluminum or aluminum with copper. In yet other embodiments, the first membrane layer 1028 may include dielectric materials such as silicon nitride, silicon oxy-nitride, silicon carbide, silicon nitride carbide or silicon oxy-nitride carbide. In some embodiments, the first membrane layer 1028 may be formed of combinations of the aforementioned materials. The first membrane layer 1028 may contact membrane terminals 1012, if present. The first membrane layer 1028 may include optional performance enhancement features 1030, such as corrugations or other stress relief configurations, which may increase responsiveness of the capacitive microphone transducer to acoustic waves. If terminal

via holes 1024 are present, the first membrane layer 1028 may be formed on sidewalls of the terminal via holes 1024 and exposed surfaces of the membrane terminals 1012.

[0018] An optional second membrane layer 1032 is formed on a top surface of the first membrane layer 1028. In one realization of the instant embodiment, the second membrane layer 1032 may be formed concurrently with elements of interconnects (not shown in FIG. 1E) in the integrated circuit 1000. If terminal via holes 1024 are present, the second membrane layer 1032 may be formed in the terminal via holes 1024. In a further embodiment, the second membrane layer 1032 may include copper. In an alternate embodiment, the second membrane layer 1032 may include aluminum or aluminum with copper. In one realization of the instant embodiment, lateral edges of the second membrane layer 1032 do not extend to lateral edges of the first membrane layer 1028. Pressure equalization apertures 1034 may be formed in the first membrane layer 1028 and/or through the combined first membrane layer 1028 and second membrane layer 1032, for example by patterning areas for the pressure equalization apertures 1034 concurrently with patterning areas for the first membrane layer 1028 and/or the second membrane layer 1032.

[0019] After formation of the first membrane layer 1028 and the second membrane layer 1032 if present, a sacrificial protective layer 1036 is formed over the first membrane layer 1028 and the second membrane layer 1032. The sacrificial protective layer 1036 includes a sacrificial material that can be removed in a subsequent fabrication step while removing substantially no material from the first membrane layer 1028 and the second membrane layer 1032. In one realization of the instant embodiment, the sacrificial protective layer 1036 may contain substantially the same material as the cavity fill sacrificial layer 1022.

[0020] Referring to FIG. 1F, a backside cavity 1038 is formed in the substrate 1002 which connects to the access trenches 1016. The backside cavity 1038 may be formed, for example by a deep RIE (DRIE) process or a wet etch process. A portion of the sacrificial material in the cavity fill sacrificial layer 1022 is removed from the access trenches 1016 using a backside sacrificial material removal process 1040. In one realization of the instant embodiment, the backside sacrificial material removal process 1040 may include an RIE step using an oxygen containing plasma. In an alternate

embodiment, the backside sacrificial material removal process 1040 may include an ashing step using reactive oxygen species. In a further embodiment, the backside sacrificial material removal process 1040 may include a step using ozone. Other means of removing sacrificial material from the access trenches 1016 are within the scope of the instant embodiment.

[0021] Referring to FIG. 1G, the sacrificial material in the sacrificial protective layer 1036 and in the cavity fill sacrificial layer 1022 is removed, for example by exposing the integrated circuit 1000 to a reactive ambient 1042 containing any combination of reactive oxygen species, reactive fluorine species, reactive hydrogen species and reactive nitrogen species. In one realization of the instant embodiment, the reactive ambient 1042 containing the reactive species may be generated in a downstream asher, which produces reactive species in a plasma, which subsequently diffuse from the plasma to an electric field-free region containing the integrated circuit 1000. In an alternate embodiment, the reactive ambient 1042 may be generated by an ozone generator.

[0022] FIG. 2 illustrates another example embodiment of an integrated circuit including a capacitive microphone transducer.

[0023] The integrated circuit 2000 is formed in and on a substrate 2002 as described in reference to FIG. 1A. A first interconnect region 2004 is formed over the substrate 2002 as described in reference to FIG. 1A. A fixed plate 2006 of the capacitive microphone transducer is formed on a top surface of the first interconnect region 2004. In one realization of the instant embodiment, the fixed plate 2006 may be formed concurrently with horizontal interconnect elements (not shown in FIG. 2) in the integrated circuit 2000. In a further embodiment, the fixed plate 2006 may include copper. In an alternate embodiment, the fixed plate 2006 may include aluminum. Cavity spacers 2008, possibly including interconnect regions of the integrated circuit 2000 are formed on the first interconnect region 2004 adjacent to a region defined for a microphone transducer plate cavity.

[0024] Access trenches 2010 are formed through the first interconnect region 2004 and into the substrate 2002, as described in reference to FIG. 1B. A first membrane layer 2012 is formed over a microphone transducer plate cavity 2014 using sacrificial

material as described in reference to FIG. 1D through FIG. 1G. In the instant embodiment, the first membrane layer 2012 overlaps the cavity spacers 2008. In one realization of the instant embodiment, the first membrane layer 2012 may be formed concurrently with liner metal elements of interconnects (not shown in FIG. 2) of the integrated circuit 2000. The first membrane layer 2012 may include optional performance enhancement features 2016, such as corrugations or other stress relief configurations, as described in reference to FIG. 1E.

[0025] An optional second membrane layer 2018 may be formed on a top surface of the first membrane layer 2012, as described in reference to FIG. 1E. In one realization of the instant embodiment, the second membrane layer 2018 may be formed concurrently with elements of interconnects (not shown in FIG. 1E) in the integrated circuit 2000. Pressure equalization apertures 2020 may be formed in the first membrane layer 2012 and/or through the first membrane layer 2012 and second membrane layer 2018, as described in reference to FIG. 1E. A backside cavity 2022 is formed in the substrate 2002 which connects to the access trenches 2010, as described in reference to FIG. 1E.

[0026] FIGS. 3A - 3D illustrate steps in the fabrication of another example embodiment of an integrated circuit including a capacitive microphone transducer.

[0027] Referring to FIG. 3A, the integrated circuit 3000 is formed in and on a substrate 3002 which includes a base layer 3004, an etch stop layer 3006 and a top layer 3008. The base layer 3004 may be a silicon wafer or other material with suitable mechanical properties for the integrated circuit 3000. The etch stop layer 3006 may be silicon dioxide or other dielectric material, or may be a heavily doped silicon layer, for example a p-type layer with a dopant density above 10^{21} cm^{-2} . The top layer 3008 may be single crystal silicon, an epitaxial semiconductor layer, a polycrystalline silicon layer, or other material with suitable electrical properties for the integrated circuit 3000. In one realization of the instant embodiment, the substrate 3002 may be a SOI wafer, in which the etch stop layer 3006 includes a buried oxide layer of the SOI wafer.

[0028] An interconnect region 3010 is formed over the top layer 3008. A fixed plate 3012 is formed over the interconnect region 3010. An access trench photoresist pattern 3014 is formed over the interconnect region 3010. An access trench etch process 3016 as described in reference to FIGS. 1B and 1C removes material from the

interconnect region 3010 and the top layer 3008 to form access trenches 3018 which extend to and possibly into the etch stop layer 3006.

[0029] Referring to FIG. 3B, a cavity fill sacrificial layer 3020 formed over the interconnect region 3010 and in the access trenches 3018 as described in reference to FIG. 1D. Microphone transducer membranes 3022 are formed on the cavity fill sacrificial layer 3020 as described in reference to FIG. 1E. A sacrificial protective layer 3024 is formed over the microphone transducer membranes 3022 as described in reference to FIG. 1E. A backside cavity 3026 is formed in the base layer 3004 by a backside cavity etch process 3028, for example an RIE process, possibly combined with a wet etch using an aqueous solution of tetraethyl ammonium hydroxide (TEAH) or potassium hydroxide (KOH). The backside cavity 3026 extends to and possibly into the etch stop layer 3006.

[0030] Referring to FIG. 3C, an etch stop layer punch through process 3030 is performed which removes material from the etch stop layer 3006 between the access trenches 3018 and the backside cavity 3026, exposing the cavity fill sacrificial layer 3020 at bottoms of the access trenches 3018. The etch stop layer punch through process 3030 may be a dry etch process such as an RIE process, a wet etch process such as an aqueous solution of dilute or buffered hydrofluoric acid (HF), or a vapor phase etch process such as exposing the etch stop layer 3006 to vapor phase anhydrous HF. In realizations of the instant embodiment in which the etch stop layer is crystalline silicon, the etch stop layer punch through process 3030 may be a wet etch including HF, nitric acid and acetic acid.

[0031] Referring to FIG. 3D, the cavity fill sacrificial layer 3020 in FIG. 3C and sacrificial protective layer 3024 in FIG. 3C are removed as described in reference to FIG. 1G, for example by exposing the integrated circuit 3000 to a reactive ambient 3032. The access trenches 3018 are connected to the backside cavity 3026.

[0032] FIGS. 4A and 4B illustrate steps in the fabrication of another example of an integrated circuit containing a capacitive microphone transducer.

[0033] Referring to FIG. 4A, the integrated circuit 4000 is formed on a substrate 4002 which includes a base layer 4004, an etch stop layer 4006 and a top layer 4008 as described in reference to FIG. 3A. An interconnect region 4010 is formed over the top layer 4008, and a fixed plate 4012 is formed over the interconnect region 4010, as

described in reference to FIG. 3A. Access trenches 4014 are formed through the interconnect region 4010 and into the top layer 4008 so as to extend to and possibly into the etch stop layer 3006, as described in reference to FIG. 3A.

[0034] A cavity fill sacrificial layer (not shown) is formed over the interconnect region 4010 and in the access trenches 4014, microphone transducer membranes 4016 are formed on the cavity fill sacrificial layer, and a sacrificial protective layer (not shown) is formed over the microphone transducer membranes 4016 as described in reference to FIG. 3B. A backside cavity 4018 is formed in the base layer 4004 by a backside cavity etch process as described in reference to FIG. 3B. The backside cavity 4018 extends to and possibly into the etch stop layer 4006. The sacrificial protective layer and cavity fill sacrificial layer are removed as described in reference to FIG. 3D, for example by exposing the integrated circuit 4000 to a reactive ambient 4020.

[0035] Referring to FIG. 4B, an etch stop layer punch through process 4022 is performed which removes material from the etch stop layer 4006 between the access trenches 4014 and the backside cavity 4018. The etch stop layer punch through process 4022 may be similar to that described in reference to FIG. 3C. When the etch stop layer punch through process 4022 is completed, the access trenches 4014 are connected to the backside cavity 4018.

[0036] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

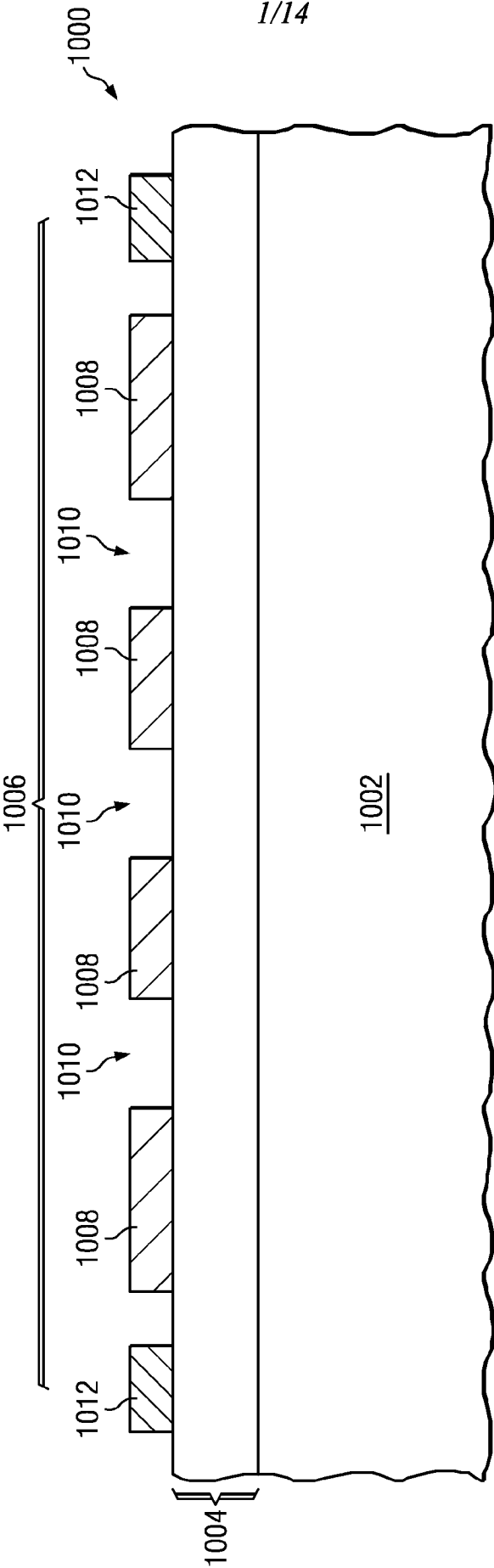
CLAIMS

What is claimed is:

1. An integrated circuit including a capacitive microphone transducer, comprising:
 - a substrate;
 - a first interconnect region formed on a top surface of said substrate;
 - a fixed plate formed on a top surface of said first interconnect region;
 - a first membrane layer formed over said fixed plate, such that a microphone transducer cavity exists between said first membrane layer and said fixed plate;
 - a backside cavity formed in said substrate extending to a bottom surface of said substrate; and
 - access trenches formed through said first interconnect region into said substrate, such that said access trenches connect said microphone transducer cavity with said backside cavity.
2. The integrated circuit of claim 1, wherein said first membrane layer is formed concurrently with liner metal elements of interconnects in said integrated circuit.
3. The integrated circuit of claim 1, wherein said first membrane layer includes material selected from the group consisting of tantalum nitride, titanium nitride, titanium aluminum, aluminum, aluminum with copper, silicon nitride, silicon oxy-nitride, silicon carbide, silicon nitride carbide, and silicon oxy-nitride carbide.
4. The integrated circuit of claim 1, wherein said first membrane layer includes a stress relief configuration.
5. The integrated circuit of claim 1, further including a second membrane layer formed on a top surface of said first membrane layer, such that lateral edges of said second membrane layer do not extend to lateral edges of said first membrane layer.

6. The integrated circuit of claim 5, wherein said second membrane layer is formed concurrently with elements of interconnects in said integrated circuit.
7. The integrated circuit of claim 6, wherein said second membrane layer is selected from the group consisting of copper, aluminum, and aluminum with copper.
8. The integrated circuit of claim 1, wherein said fixed plate is formed concurrently with elements of interconnects in said integrated circuit.
9. The integrated circuit of claim 1, wherein:
 - said substrate includes a base layer, an etch stop layer formed on said base layer, and a top layer formed on said etch stop layer;
 - said backside cavity extends through said base layer; and
 - said access trenches extend through said top layer.
10. A process of forming an integrated circuit including a capacitive microphone transducer, comprising the steps of:
 - providing a substrate;
 - forming a first interconnect region on a top surface of said substrate;
 - forming a fixed plate on a top surface of said first interconnect region;
 - forming access trenches through said first interconnect region into said substrate;
 - forming a sacrificial fill region of sacrificial material above said fixed plate;
 - forming a first membrane layer on a top surface of said sacrificial fill region;
 - forming a sacrificial protective layer of sacrificial material on a top surface of said second membrane layer;
 - forming a backside cavity in said substrate, said backside cavity extending from a bottom surface of said substrate to said access trenches;
 - removing a portion of said sacrificial material in said access trenches by a process of etching from a back side of said integrated circuit; and
 - removing said sacrificial material from said sacrificial fill region.

11. The process of claim 12, wherein said first membrane layer is formed concurrently with liner metal elements of interconnects in said integrated circuit.
12. The process of claim 10, wherein said first membrane layer is selected from the group consisting of tantalum nitride, titanium nitride, titanium aluminum, aluminum, aluminum with copper, silicon nitride, silicon oxy-nitride, silicon carbide, silicon nitride carbide, and silicon oxy-nitride carbide.
13. The process of claim 10, wherein said first membrane layer is formed so as to include a stress relief configuration.
14. The process of claim 10, further including forming a second membrane layer on a top surface of said first membrane layer, so that lateral edges of said second membrane layer do not extend to lateral edges of said first membrane layer.
15. The process of claim 14, wherein said second membrane layer is formed concurrently with elements of interconnects in said integrated circuit.
16. The process of claim 15, wherein said second membrane layer is selected from the group consisting of copper, aluminum, and aluminum with copper.
17. The process of claim 10, wherein said fixed plate is formed concurrently with elements of interconnects in said integrated circuit.
18. The process of claim 10, wherein:
 - said substrate includes a base layer, an etch stop layer formed on said base layer, and a top layer formed on said etch stop layer;
 - said step of forming said backside cavity is performed so that said backside cavity extends through said base layer; and
 - said step of forming said access trenches is performed so that said access trenches extend through said top layer.



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FIG. 1A

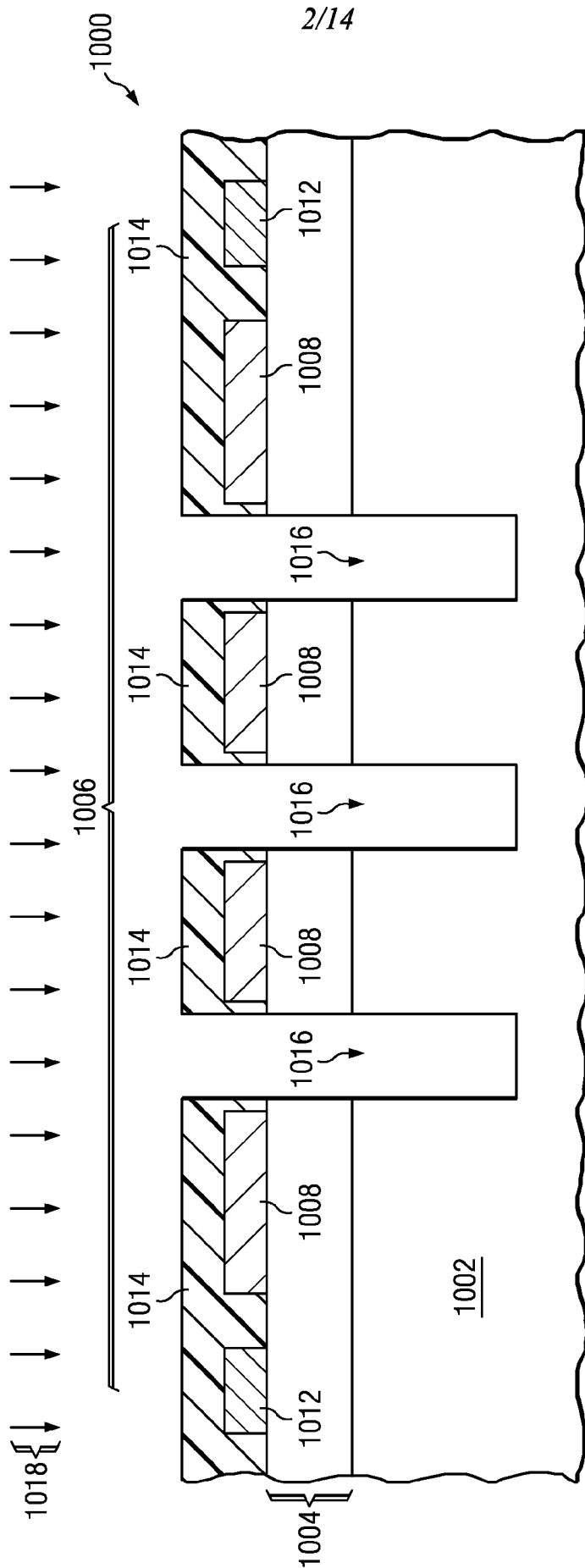


FIG. 1B

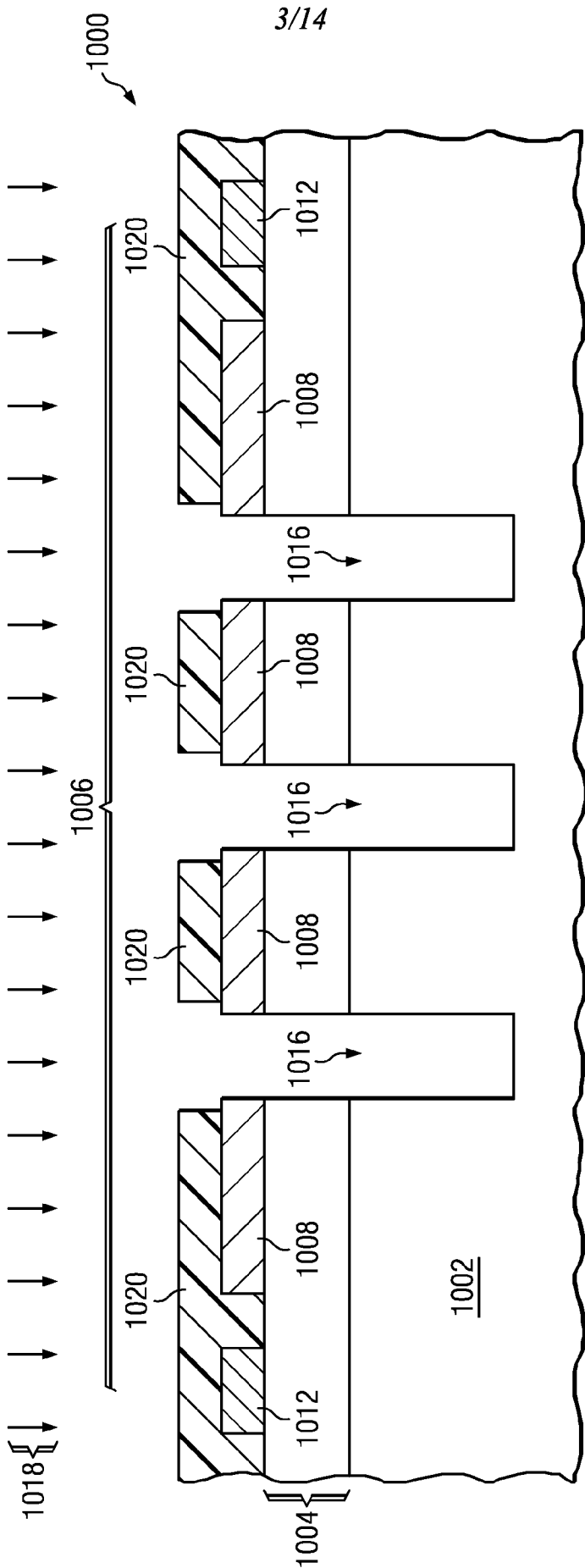


FIG. 1C

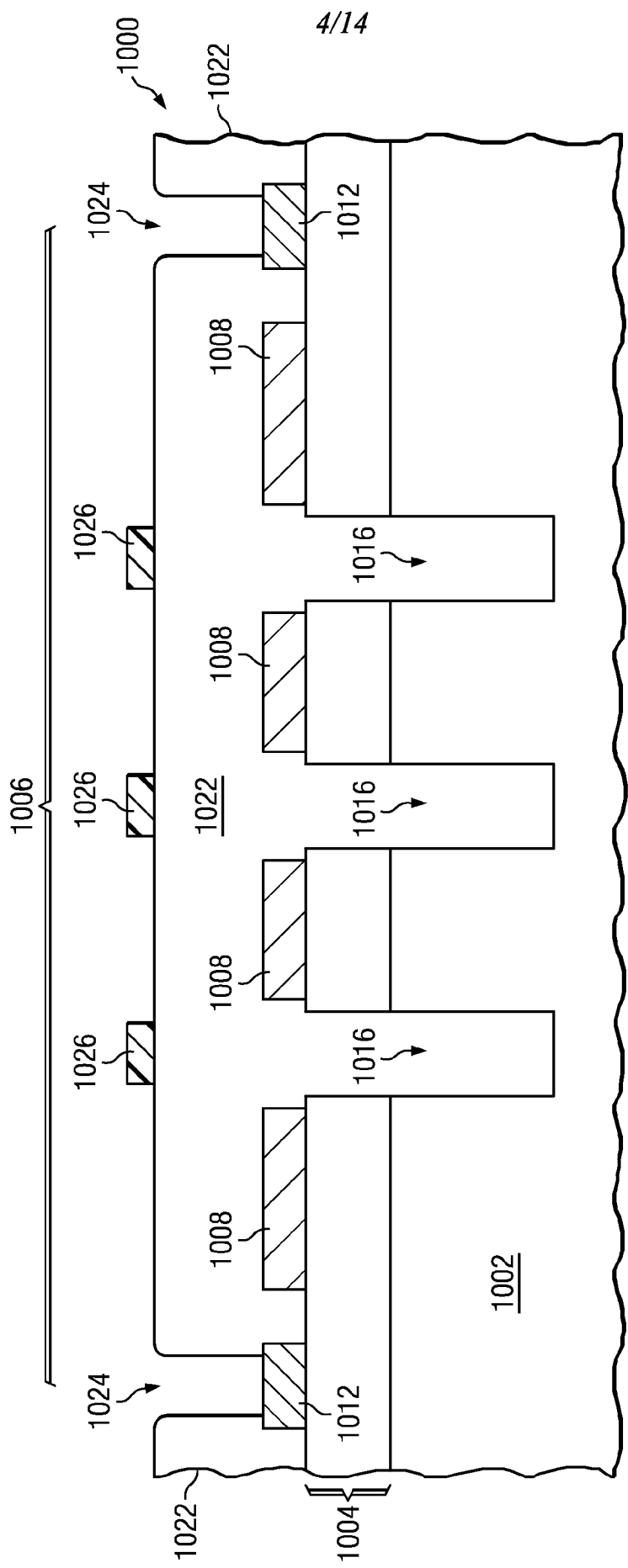


FIG. 1D

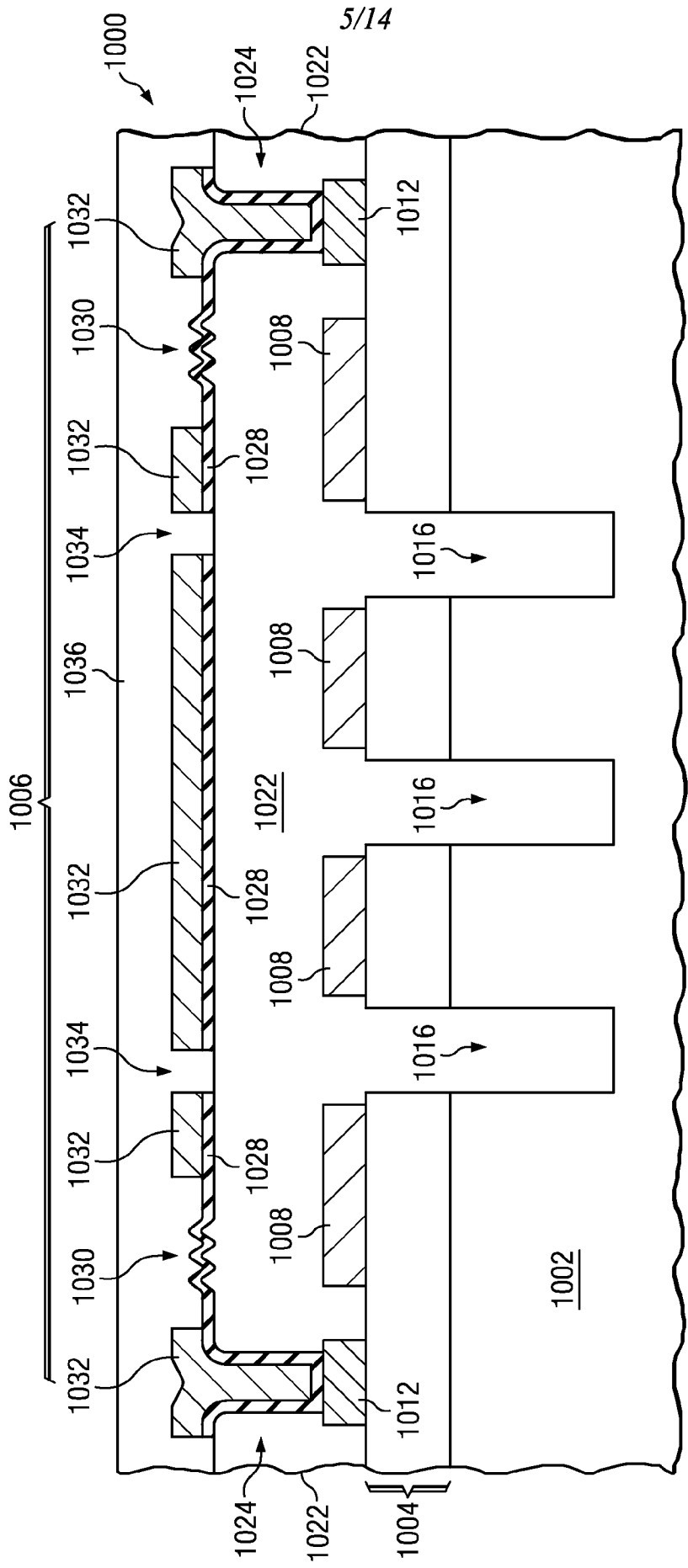


FIG. 1E

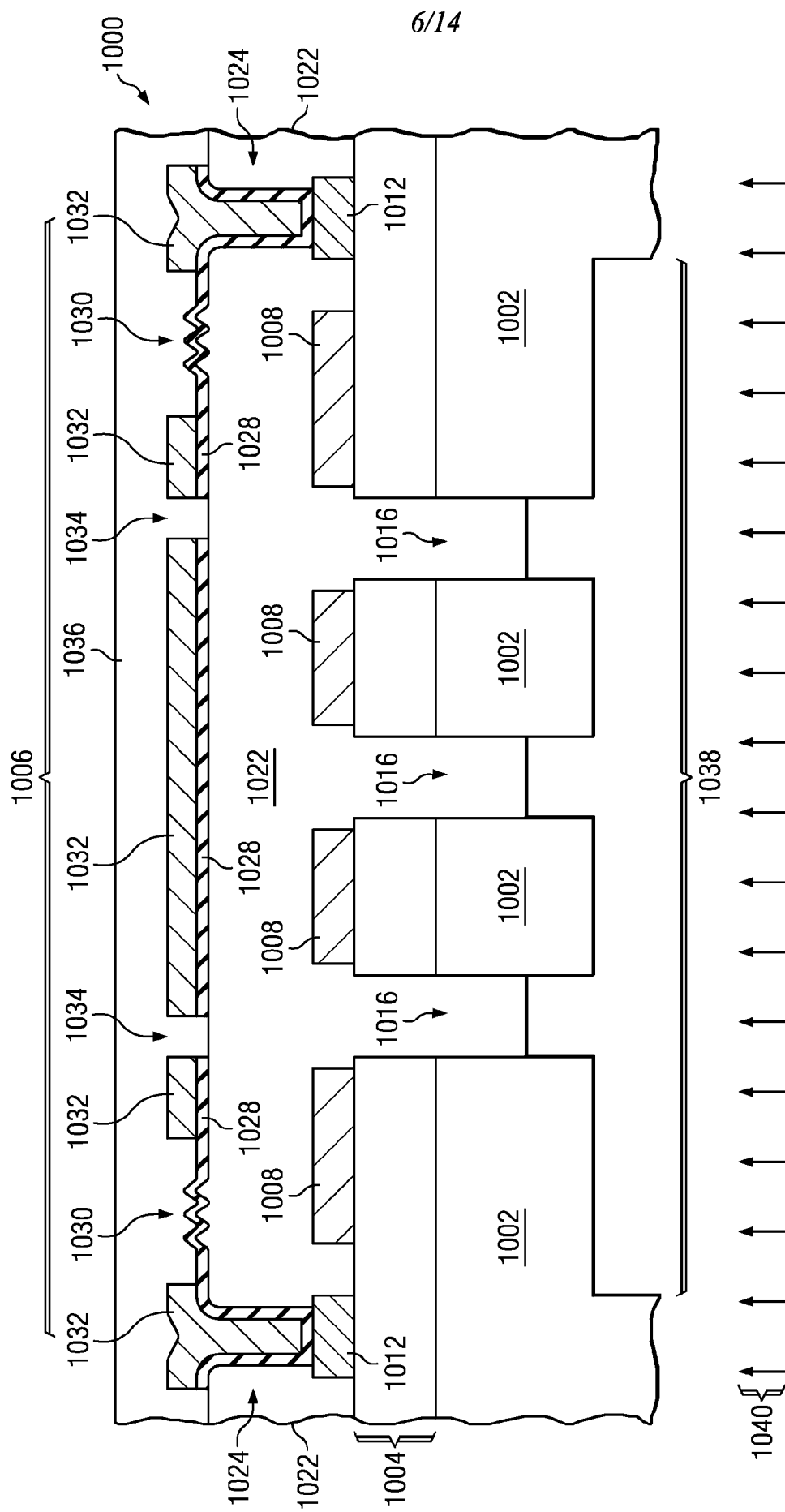


FIG. 1F

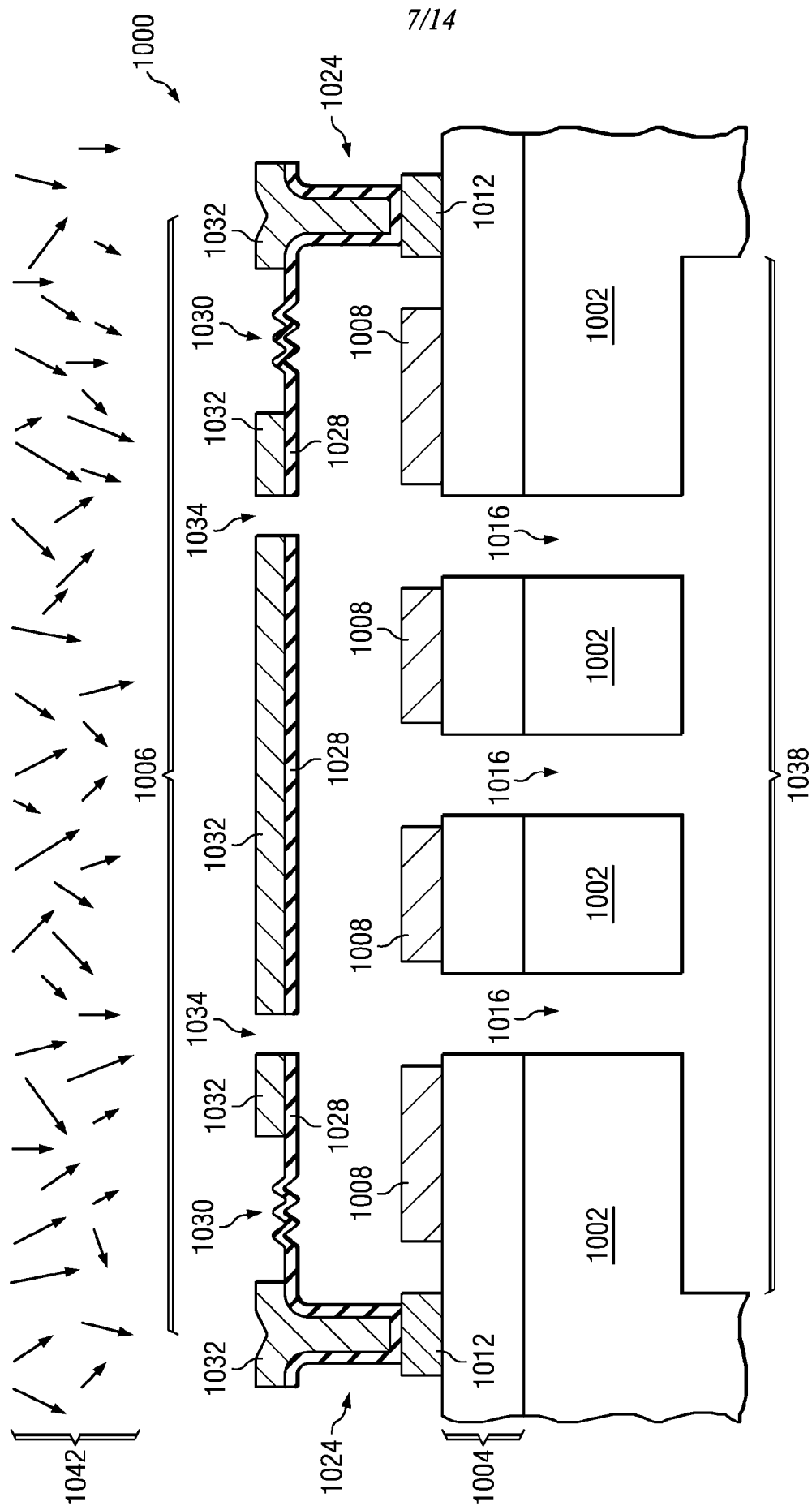


FIG. 1G

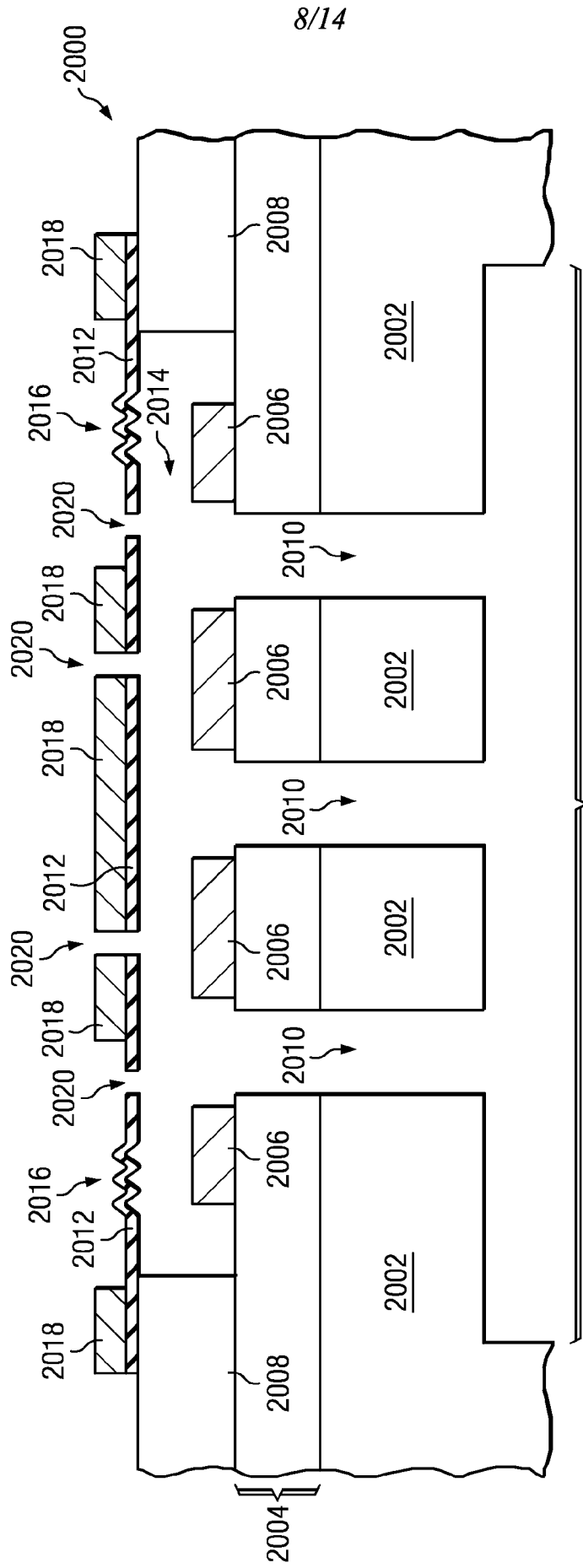


FIG. 2

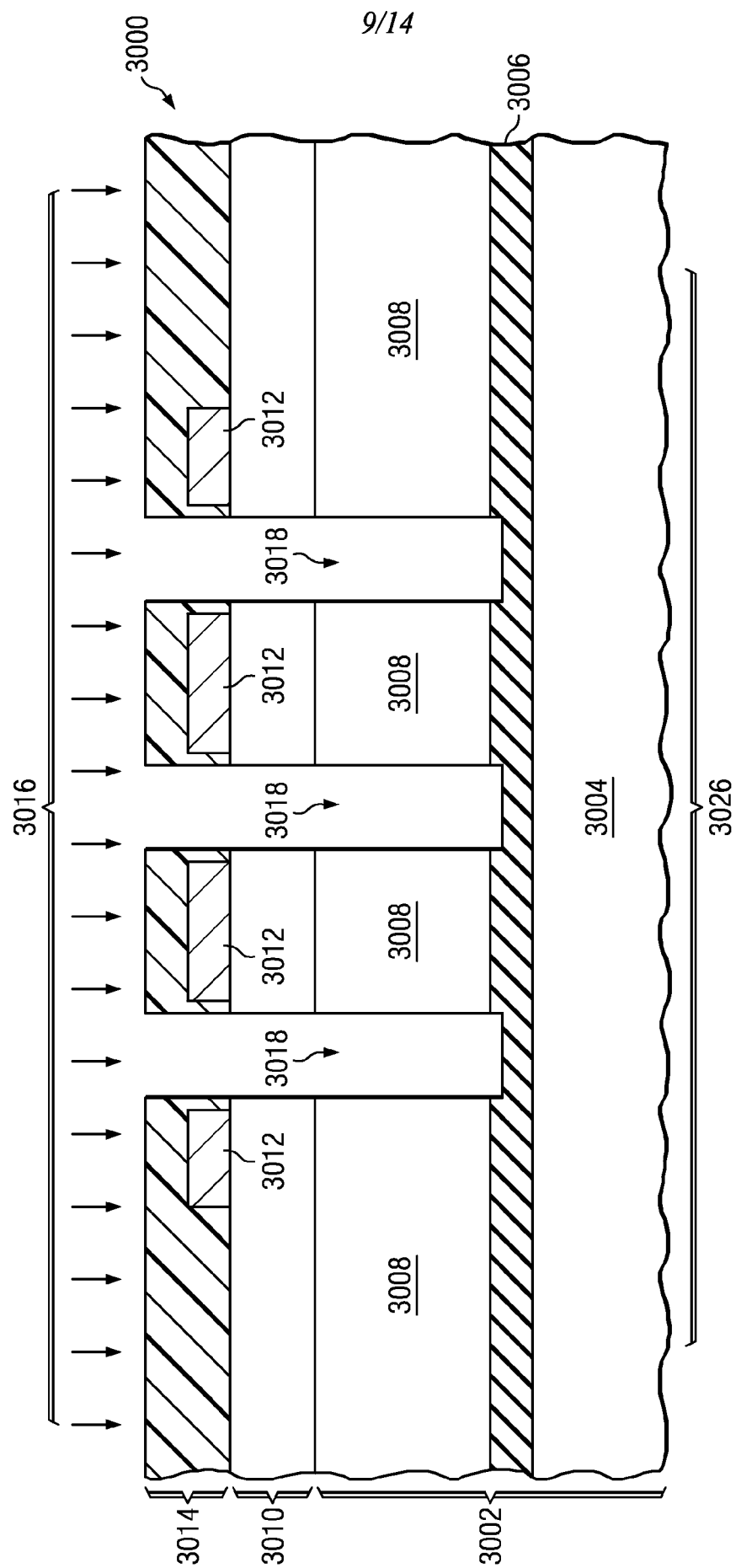


FIG. 3A

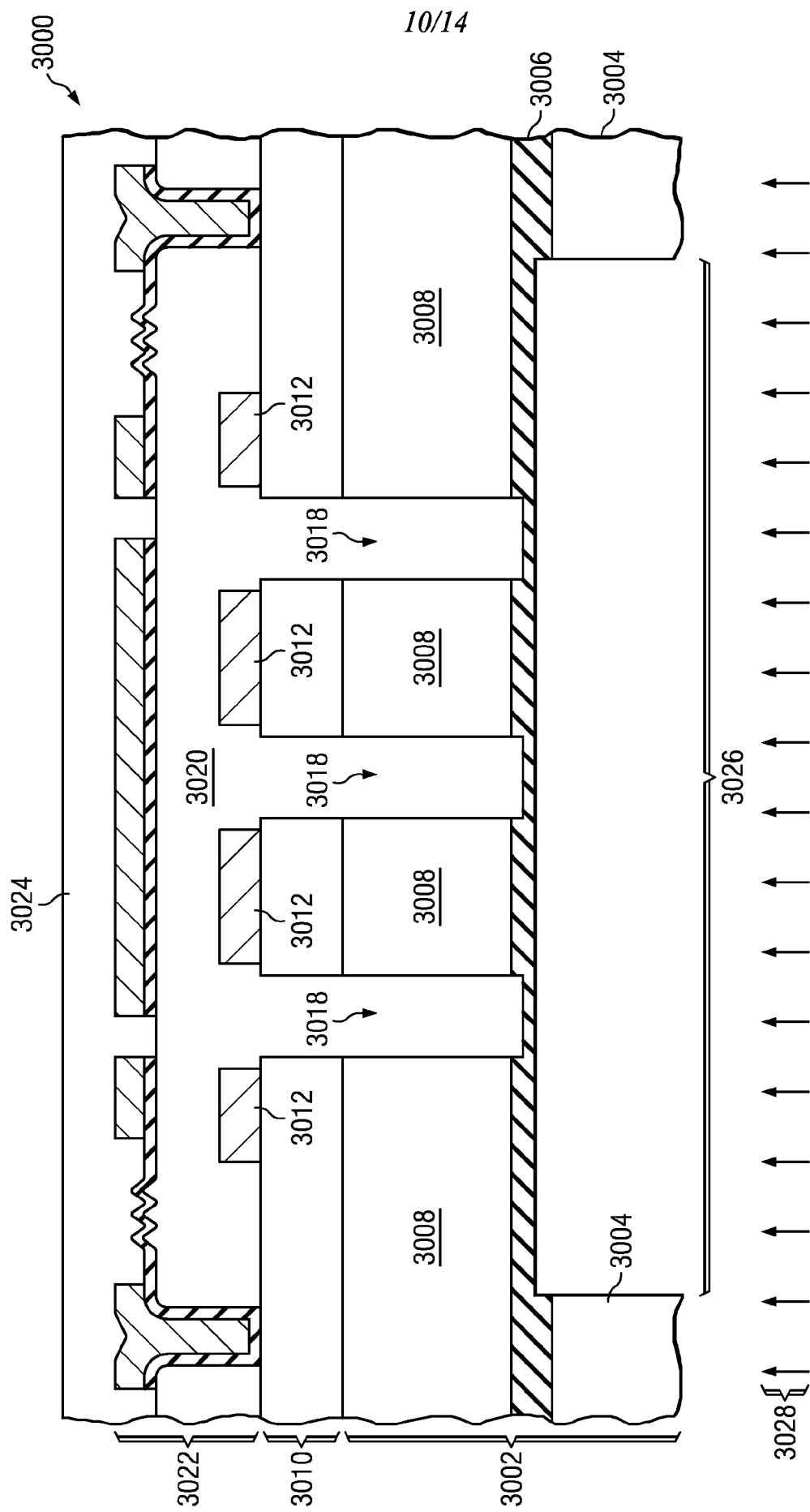


FIG. 3B

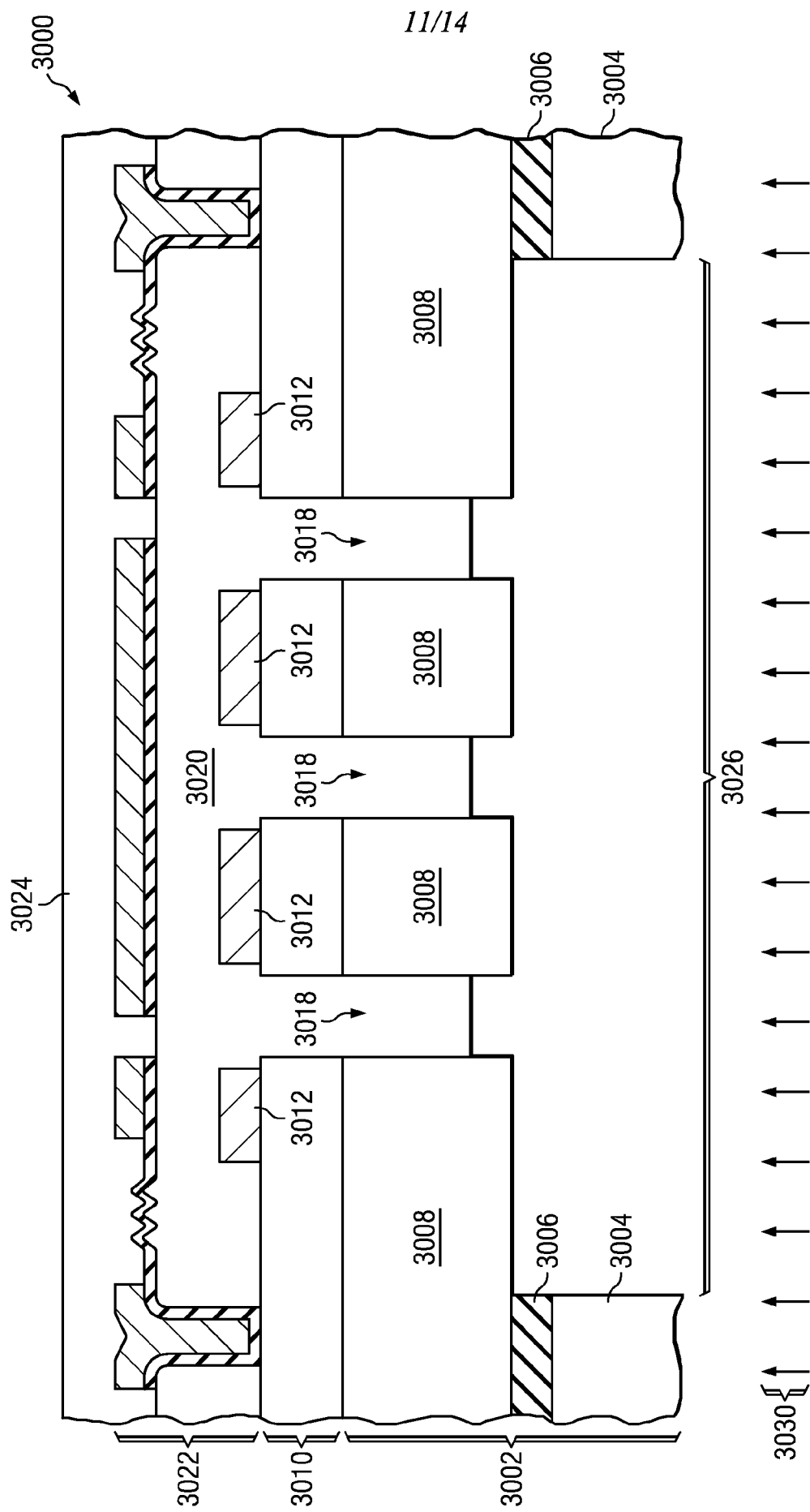


FIG. 3C

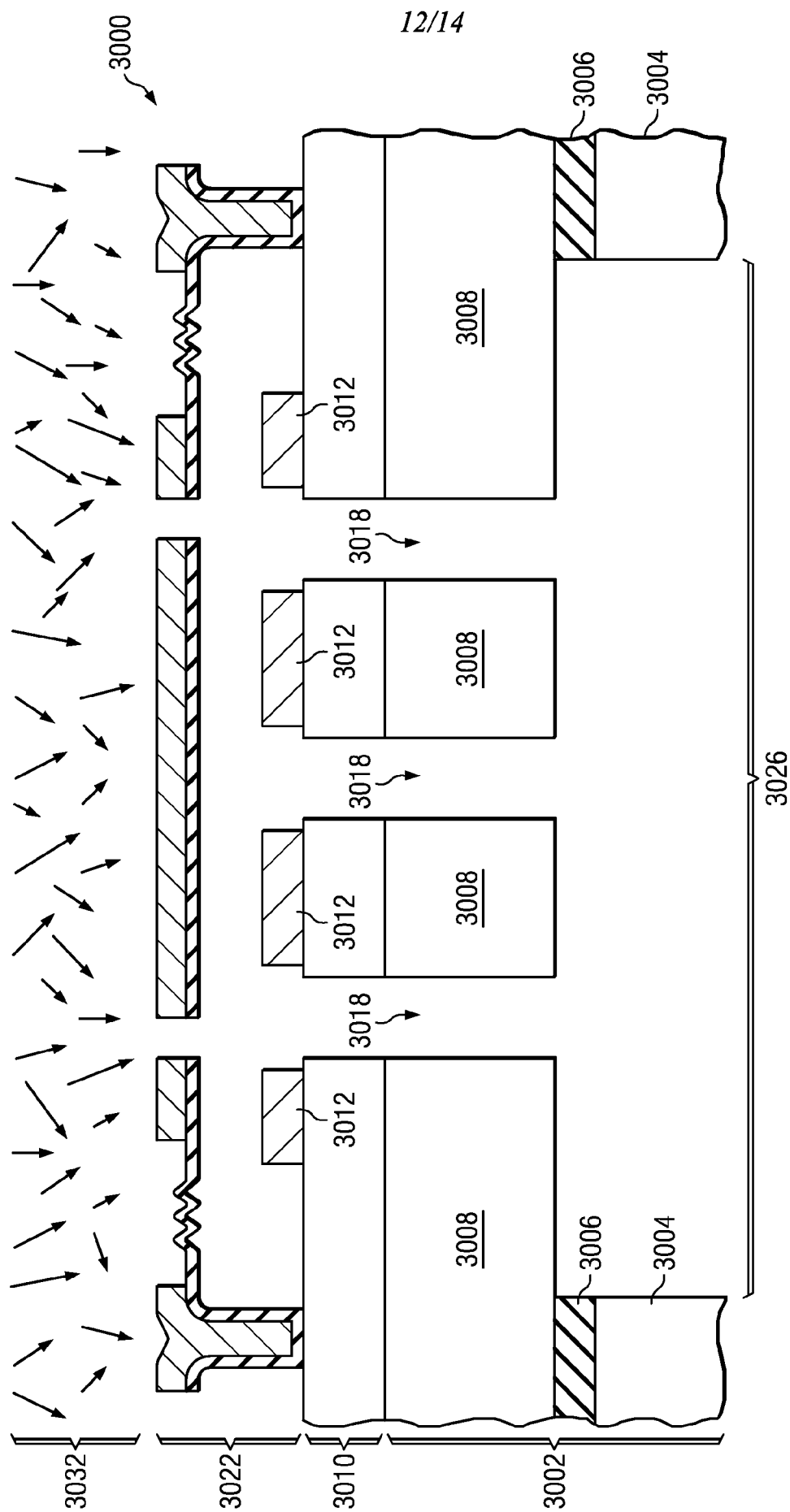


FIG. 3D

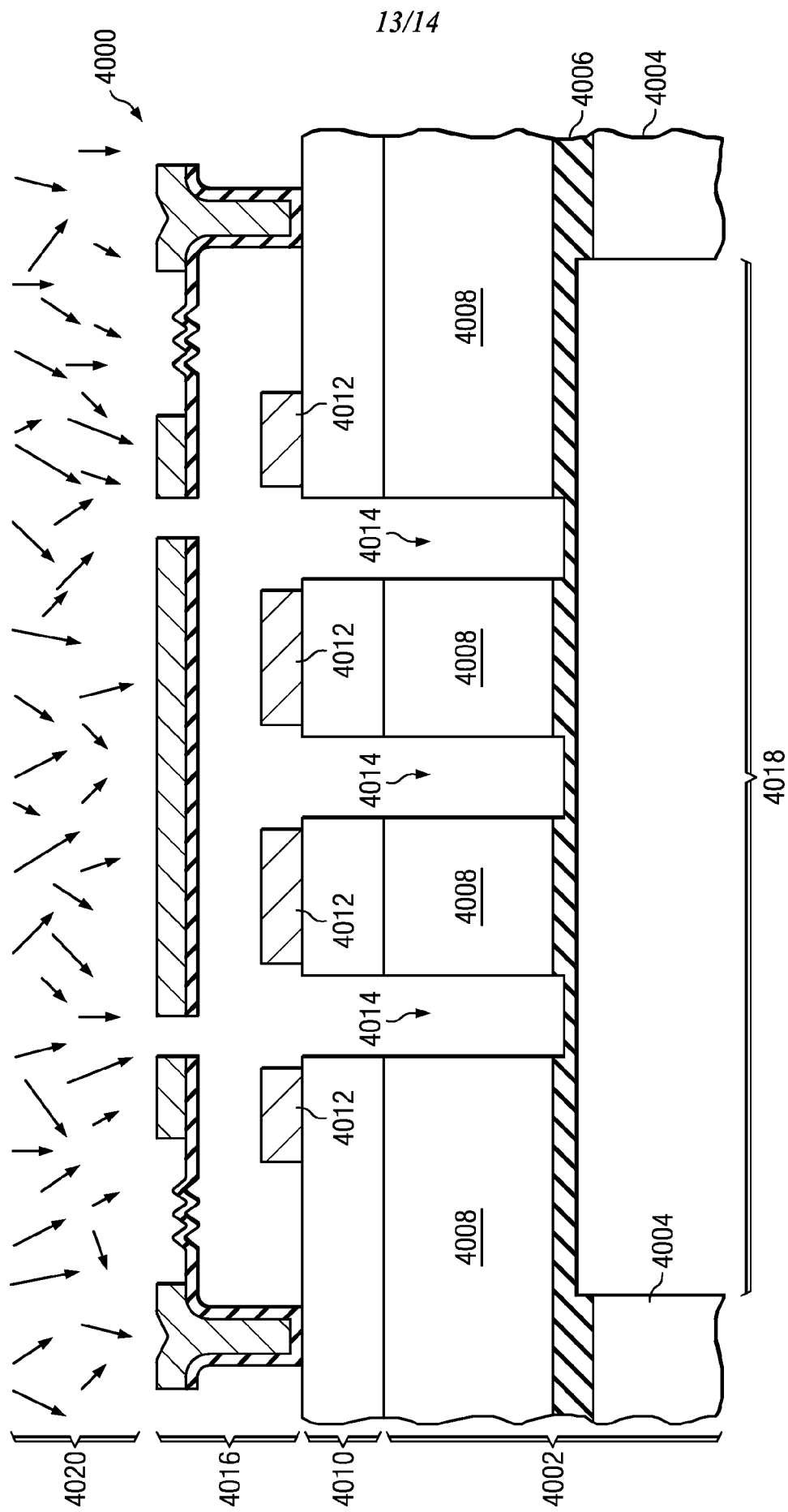


FIG. 4A

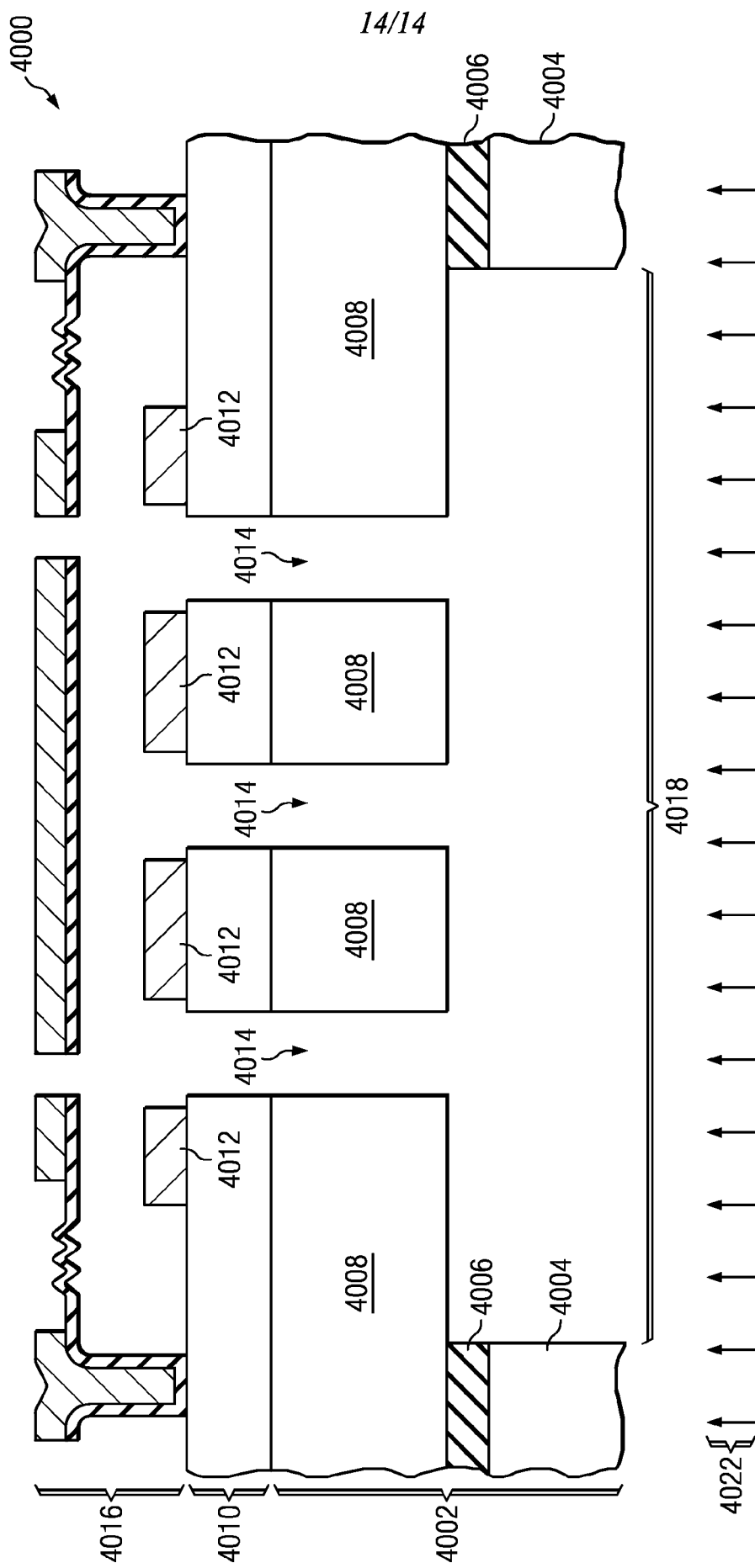


FIG. 4B