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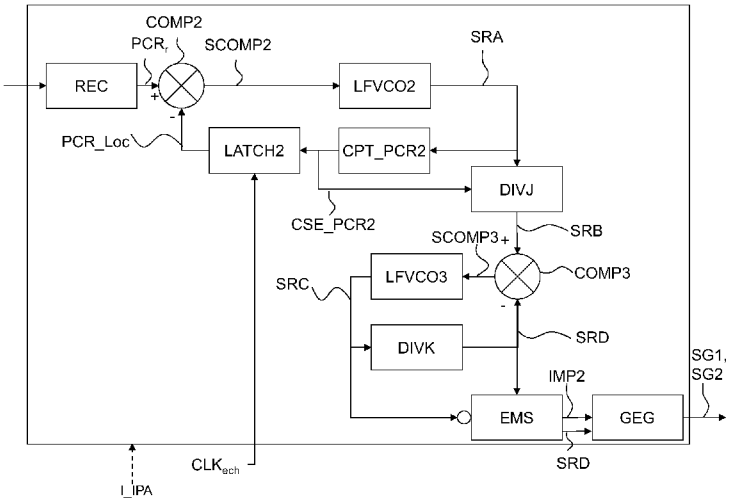
(54) Title: SYSTEM FOR TRANSMISSION OF A SYNCHRONIZATION SIGNAL



(57) Abstract: The present invention relates to the domain of video equipment. Specifically it relates to a transmission device able to transmit packets in a packet communication network, said device comprising the means (EXS) to extract clock signals (CLK) and pulses (IMP1) at frequency FV synchronous with signals (CLK) from a synchronization signal (SGO), According to the invention the device also comprises: - the means (DIVP) to produce, from the pulses (IMP1) and said clock signals (CLK), a signal (SA) at frequency FA such that FA = FV/P where P is an integer number, - the means (LFVO1) to produce from a signal (SCOMP1) a signal (SB) at frequency FB greater than FA, - the means (DIVQ) to produce, from the signal (SB), a signal (SC) at frequency FC so that FC = FB/Q where Q is an integer number, - the means (DIVR) to produce, from the signal (SC), a signal (CLR) at frequency FCLR so that FCLR = FC/R where R is an integer number, - the means (COMP1) to compare the signal (SA) with the signal (SB), said means (COMP1) delivering a comparison signal (SCOMP1), - a counter (CPT_PCR1) whose rate is determined by the signal (SB) and initialized by the signal (CLR), said counter (CPT_PCR1) produced from counting ramps (CSE_PCR), - the means (LATCH1) to realize the samples (PCR_e) of ramps (CSE_PCR) via a signal (CLKech) from a time base synchronized on all the devices connected to said network, and - the means (INTE) to transmit a packet comprising the sample (PCR_e) in the communications network.

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SYSTEM FOR TRANSMISSION OF A SYNCHRONIZATION SIGNAL

Scope of the invention

The present invention relates to the domain of video equipment.

The present invention relates more specifically to a system for transmission of a synchronization signal between two items of equipment connected by a communications network. The invention is particularly useful when the items of equipment are video equipment, for example a video source and a display device, both using a common video frequency, for example 27MHz, the synchronization signal being realized from a frequency signal at 1 GHz. The communications network is a packet switching network, for example of IP (Internet Protocol) type, whether the network is wired (for example Ethernet (IEEE802.3)) or wireless (for example IEEE 802.16 D-2004).

Prior art

Progress in the ability of IP networks to transport all types of signal (data or video) has made it possible to use these networks as the “backbone” architecture for video studios. Of capital importance to this evolution is therefore having a single infrastructure for the transport of data. Whereas in the past, several media were necessary to transport different signal types between items of equipment, the multiplexing properties offered by the IP layer enable a reduction in the number of media necessary: an IP network that links the different items of equipment.

In the prior art, the synchronisation of items of video equipment (cameras, etc.) in a studio is carried out by the transmission of a synchronisation signal commonly called “Genlock” or “Black burst”. For example, the Genlock signal comprises two synchronisation signals, one is repeated every 40 ms and indicates the start of the video frame, the other is repeated every 64 μs (for a standard format and less for an HD format) and indicates the start of lines in the video frame. The waveforms of

synchronisation signals are a function of the format of the image transmitted on the network. For example, for a high definition image, the signal synchronisation has a tri-level form (-300mV, 0V, +300 mV).

When a synchronisation signal is routed to different items of equipment to be synchronised by a dedicated coaxial cable, a constant transmission time, without jitter is ensured. From such a signal, all items of equipment are able to reconstruct a timing clock that is specific to its functioning, which guarantees that its functioning is rigorously in phase with all the equipment connected to the same network. For example, two cameras synchronised by a Genlock signal circulating on a dedicated coaxial cable each generate a video with different contents but rigorously in frequency and in phase with one another.

A known disadvantage presented by an IP/Ethernet network is that it introduces a strong jitter in a transmission of signals, and particularly for the transmission of a synchronisation signal. When such a signal is routed by an IP/Ethernet connection to different items of equipment for synchronising, this jitter results in fluctuations in the length of time required for the information carried by the synchronisation signal to reach the equipment.

In the prior art, for a set of devices, for example cameras, connected to an IP network, devices are known to reconstruct at the level of each camera, a timing clock specific to this camera enabling it to overcome jitter. The underlying principle of these devices is a high attenuation of the synchronisation signal jitter amplitude at the level of reception. In such a way, it can be guaranteed that an image generated by a camera is rigorously in phase with all of the images generated by neighbouring cameras connected to the same network.

Examples of such video synchronisation devices for jitter attenuation are described in the international PCT application FR2007/050918, they act on program clock reference (PCR) signals that represent reference clock signals. These very precise digital signals are provided to cameras via a network so that they can locally reconstruct clock signals that are in phase with the reference clock. The creation of the digital signal transported on the

network and the reconstruction of clock signals are realised by a sampling clock CLKech common to the transmission device and the reception devices. Specifically this clock CLKech must be perfectly identical for the transmission device and all the reception devices.

A disadvantage of the systems of the prior art is that the transported digital signal of the transmission device to the reception devices is created from a counting ramp comprising temporal steps whose duration correspond to the frequency of the clock signal of the synchronization signal.

However it can be shown that this counting ramp can also be used to carry out a time labelling service and transmit temporal markers from the transmission side to the reception side: an example of such a transmission application is described in the French patent application FR 0852687. In this case, the minimum precision that can be expected on the temporal marker also corresponds to the duration of a counting ramp step. For a video application where the clock frequency transmitted in the synchronization signal is equal to 27MHz, the duration of the step corresponds to 37 nanoseconds. It is therefore not possible to transmit a temporal marker with a better temporal precision than 37 ns: This can constitute an inconvenient restriction.

Moreover, some users prefer to work with standard temporal references of a period equal to one second, one microsecond, or one nanosecond. In this case, remaining in the context of a video application there is an interest in finding a means of working with a frequency decoupled from the video frequency (27 MHz), for example a frequency equal to 1 GHz, to create a counting ramp while ensuring a correct and synchronous synchronization transmission of a 27 MHz clock

One of the purposes of the present invention is to overcome this disadvantage in or to create counting ramps for which the steps have a duration that is different to the period of the clock frequency of the synchronization signal to be transmitted.

Summary of the invention

The technical problem that the present invention proposes to resolve is to ensure a decoupling between the duration of steps of the counting ramps used to create a synchronization signal between a transmission device and a reception device and the working frequency of said devices.

For this purpose, the present invention relates to, according to a first aspect, a transmission device able to transmit packets in a packet communication network, said device comprising the means (EXS) to extract clock signals (CLK) and pulses (IMP1) at frequency FV synchronous with signals (CLK) from a synchronization signal (SG0). According to the invention the device also comprises:

- the means (DIVP) to produce, from the pulses (IMP1) and said clock signals (CLK), a signal (SA) at frequency FA such that FA = FV/P where P is an integer number,
- the means (LFVO1) to produce from a signal (SCOMP1) a signal (SB) at frequency FB greater than FA,
- the means (DIVQ) to produce, from the signal (SB), a signal (SC) at frequency FC so that FC = FB/Q where Q is an integer number,
- the means (DIVR) to produce, from the signal (SC), a signal (CLR) at frequency FCLR so that FCLR = FC/R where R is an integer number,
- the means (COMP1) to compare the signal (SA) with the signal (SC), said means (COMP1) delivering a comparison signal (SCOMP1),
- a counter (CPT_PCR1) whose rate is determined by the signal (SB) and initialized by the signal (CLR), said counter (CPT_PCR1) produced from counting ramps (CSE_PCR),
- the means (LATCH1) to realize the samples (PCR_e) of ramps (CSE_PCR) via a signal (CLKech) from a time base synchronized on all the devices connected to said network, and
- the means (INTE) to transmit a packet comprising the sample (PCR_e) in the communications network.

The present invention relates to, according to a second aspect, a reception device able to receive packets in a packet communication network,

said device comprising the means (REC) to receive packets from said network, said packets comprising the samples (PCR_r), said samples (PCR_r) coming from data sampled by a signal (CLKech) from a time base synchronized on all the devices connected to said network, the means (REC) extracting said samples (PCR_r) from packets received. According to the invention the device also comprises:

- the means (LFVCO2) to produce from a comparison signal (SCOMP2) a signal (SRA) at frequency FRA,

- a counter (CPT_PCR2) cadenced by the signal (SRA), said counter (CPT_PCR2) produced by counting ramps (CSR_PCR2),

- the means (LATCH2) to realize the local samples (PCR_Loc) of ramps (CSR_PCR2) via the signal (CLKech), and

- the means (COMP2) to compare said samples (PCR_r) with said local samples (PCR_Loc), said means of comparison (COMP2) delivering the comparison signal (SCOMP2),

- the means (DIVJ) to produce from the signal (SRA) and the counting ramps (CSR_PCR2), a signal (SRB) at frequency FRB such that FRB = FRA/J where J is an integer number,

- the means (LFVCO3) to produce from a signal (SCOMP3) a signal (SRC) at frequency FRC,

- the means (DIVK) to produce, from the signal (SRC), a signal (SRD) at frequency FRD so that FRD = FRC/K where K is an integer number,

- the means (COMP3) to compare the signal (SRD) with the signal (SRB), said comparison means (COMP3) delivering a comparison signal (SCOMP3),

- the means (EMS) to produce pulses (IMP2) at a frequency (FV) from the signal (SRC) and the signal (SRD),

- the means to reconstitute a synchronization signal from said pulses (IMP2) and the signal (SRD).

The present invention relates to, according to a third aspect, a synchronization system comprising a transmission device as defined earlier and at least one reception device as described previously.

Advantageously, the frequency FRA of the signal SRA of the reception device or devices is identical to the frequency FB of the transmission device.

Advantageously, the frequency FRC of the reception device or devices is identical to the frequency FV of the pulses IMP1 of the transmission device.

According to an embodiment, the frequency FB of the transmission device of a synchronization system according to the invention is identical to the frequency FRA of the signal SRA of the reception device or devices.

Brief description of the drawings

The invention will be better understood from the following description of an embodiment of the invention provided as an example by referring to the annexed figures, wherein:

- figure 1 shows the transmission of genlock information between two cameras linked via an IP/Ethernet network,
- figure 2 shows the interfacing between the analogue domain and the IP/Ethernet network,
- figure 3 shows the regeneration of the Genlock signal on the reception side according to the prior art,
- figure 4 diagrammatically shows a phase-locked loop architecture of a reception device according to the prior art,
- figure 5 shows the interfacing between the analogue domain and an IP/Ethernet network according to the invention,
- figure 6 shows the regeneration of the Genlock signal on the reception side according to the invention.

Detailed description of the embodiments of the invention

The current analogue domain is interfaced with the IP/Ethernet network on the transmission side, and the IP/Ethernet network is interfaced with the analogue domain on the reception side, as illustrated in figure 1.

In the same figure, the transmission side comprises a “Genlock master” MGE that is connected to an IP/Analogue interface I_AIP. The Genlock master MGE sends a Genlock signal SG0 to the interfaces I_AIP.

The reception side comprises two cameras (CAM1, CAM2) each connected to an IP/Analogue interface I_IPA. The interfaces I_IPA that will eventually be included in the cameras themselves are responsible for reconstructing the Genlock signals SG1, SG2 intended for cameras CAM1, CAM2. The cameras CAM1, CAM2 each produce a video signal SV1, SV2 that is required to be synchronised perfectly.

The transmission and reception sides are linked together by a packet switching network that is the source of a jitter occurring in the Genlock signal SG0.

A sampling clock, CLKech, with a T_{ech} period, is generated from a first synchronisation layer, for example IEEE1588, and is sent to the transmission and reception sides. Indeed, the PTP protocol (Precision Time Protocol) based on IEEE1588 enables synchronisation to be obtained between the equipment connected on the Ethernet network to an order of microseconds. In other words, the time bases of each item of equipment progress at the same time with a precision close to the order of the microsecond. Each of these time bases can be used in this case to generate its own sampling clock CLKech with a period T_{ech}. Use of the IEEE1588 layer is not a required route. Any system capable of providing a sampling clock of period T_{ech} on the various items of equipment connected on the network could be suitable. For example, a sampling clock with a period of 5ms from a wireless transmission physical layer can be used.

Figure 2 details the processing of the Genlock signal SG0 from MGE, within the interface I_AIP.

First, a module EXS extracts the synchronisation information from the signal SG0 in order to recover a video timing clock (noted as Clk on figure 2). More specifically, the module EXS is responsible for the generation of a pulse (or “top”) triggering each image start. In addition, the module EXS comprises an image counter, for example a 40 ms counter, which is not shown in Figure 2. The output of this image counter progresses according to the counting ramp, crossing 0 at each image start, that is, every 40 ms in the case of the image counter cited in the aforementioned example.

“Counting ramp” designates a stair-step signal. The steps have a unitary height. The “counting ramp range" is the term applied to the difference in level between the highest steps and the lowest steps.

For example the counting ramp range delivered by the image counter is equal to $40ms.F_{out}$, where F_{out} is the frequency of the video clock CLK. The image counter successively delivers all of the integer values from 0 to $40\ ms.F_{out}-1$.

The timing video clock is used to determine the rhythm of a counter CPT_PCR. The output of the counter CPT_PCR is a counting ramp, CSE_PCR whose period is m image periods. Every “m” image, the counter CPT_PCR is reset, that is to say that the counting ramp CSE_PCR is reset to 0.

The counting ramp range delivered by the image counter is equal to $m.40ms.F_{out}$ The counter CPT_PCR delivers successively all of the integer values from 0 to $m.40\ ms.F_{out}-1$.

Next, a module LCH samples the counting ramp CSE_PCR at a rate provided by the sampling clock CLKech, that is to say with a period T_{ech} and thus produces the samples PCR_e that are sent on the network and circulate via an interface the network (block INTE) to the reception side.

Figure 3 shows the reception side according to the prior art. The interface I_IPA recovers the PCR_e samples that have been sent on the network. These samples PCR_e are received by a network interface (module INTR) with a delay linked to the transport between the transmission device and the reception device: the module INTR produces the samples PCR_r. The

samples PCR_e, which are produced at regular T_{ech} intervals on the transmission side, arrive at irregular intervals on the reception side: this is largely due to the jitter introduced during transport on the network. The samples PCR_r are taken into account at regular T_{ech} intervals and hence, the majority of the jitter introduced during packet transport is eliminated.

The imprecision between the transmission and reception sampling times is absorbed by a phase-locked loop PLL_1 whose bandwidth is appropriated. The characteristics of the phase-locked loop PLL_1 guarantee a reconstituted clock generation CLK_out_1 with a reduced jitter.

The phase-locked loop PLL_1 acts as a system receiving PCR_r samples and delivering:

- a reconstituted clock CLK_out_1,
- a counting ramp CSR_PCR_1 and,
- local samples PCR_loc_1.

When the loop PLL_1 operates in a steady state, the samples PCR_r are noticeably equal to the samples PCR_loc_1.

The reconstituted clock CLK_out_1 determines the timing of a CPT image counter similar to the image counter on the transmission side, for example a 40 ms counter. The image counter CPT is reset each time the counting ramp CSR_PCR_1 crosses 0. Between two successive initialisations, the image counter CPT progresses freely and produces top image that supplies a local Genlock generator, GEG to produce a reconstructed Genlock signal SG1, SG2 designed to synchronise the cameras CAM1, CAM2.

The reconstructed Genlock signal SG1, SG2 that is generated from the counting ramp CSR_PCR_1 and the reconstituted clock CLK_out_1 is in phase with the Genlock signal SG0 on the transmission side, to the nearest clock pulse.

Figure 4 diagrammatically shows a PLL_1 phase-locked loop architecture used in an I_IPA interface according to the prior art. As shown in figure 4, the phase locking loop PLL_1 comprises:

- a sample comparator CMP_1 that compares the samples PCR_r and local samples delivering a comparison result of the samples , or an error signal ERR,

- a corrector COR_1 receiving the signal ERR and delivering a corrected error signal ERC,

- a configurable oscillator VCO_1 receiving the corrected error signal ERC and delivering a reconstituted clock CLK_out_1, the clock CLK_out_1 has a frequency F_{out} that depends on the signal ERC,

- a counter CPT_PCR_1 that produces a counting ramp CSR_PCR_1 according to a rate that is printed by the reconstituted clock CLK_out_1 and having a rage of m.40 ms.F_{out},

- a value maintenance system $LATCH_1$ that generates local samples PCR_loc_1 from the values of the counting ramp CSR_PCR_1 at the instants defined by the sampling clock CLK_{ech}.

Figure 5 shows in simplified form the different components constituting the transmission device I_AIP according to the invention assuring the interface between the analogue domain and an IP/Ethernet network.

The device I_AIP comprises the means EXS to extract clock signals CLK and pulses IMP1 at frequency FV, synchronous with signals CLK from a synchronization signal SG0.

To simplify the explanation, the frequency of the clock signal CLK is equal to 27MHz and the frequency FV is equal to 25 Hz.

The device I_AIP comprises:

- the means DIVP to produce, from the pulses IMP1 and clock signals CLK, a signal SA at frequency FA such that FA = FV/P where P is an integer number,

- the means LFVO1 to produce from a signal SCOMP1 a signal SB at frequency FB greater than FA, the means LFVO1 have a function similar to the blocks COR_1 and VCO_1,

- the means DIVQ to produce, from the signal SB, a signal SC at frequency FC so that FC = FB/Q where Q is an integer number,

- the means COMP1 to compare the signal SA with the signal SC, said means COMP1 delivering a comparison signal SCOMP1,

Signals for which the frequency has a value facilitating the calculations are selected. For example, a frequency value FA equal to one second is selected and the value 1 GHz is imposed for FB. This imposes P = 25 and Q = 10^9 in such a way that a comparison between the signal SA and the signal SB is possible.

In an established regime, the signals SA and SB are both constituted of pulses at 1Hz and are equal.

From these selections, the period of the counting ramp CPT_PCT1 is defined, preferably in such a way that it is different than the period of pulses IMP1. To do this are used:

- a counter CPT_PCR1 whose rate is determined by the signal SB, at 1GHz in the example. The counter CPT_PCR1 is initialized by a signal CLR and produces counting ramps CSE_PCR, of unitary steps,

- the means DIVR to produce, from the signal SC, a signal CLR at frequency FCLR so that FCLR = FC/R where R is an integer number. Following the previous example R defines in seconds the period of the counting ramp, for example R = 1001,

- the means LATCH1 to realize the samples PCR_e of ramps CSE_PCR via a signal CLKech from a time base synchronized on all the devices connected to said network, and

- the means INTE to transmit a packet comprising the sample PCR_e in the communications network.

Figure 6 shows in a simplified way the different components constituting a reception device of an interface I_IPA according to the invention. As in the prior art, the reception device comprises the means REC to receive packets from the network. The packets comprise samples PCR_r from data sampled by a signal CLKech from a time base synchronized on all the devices connected to said network. The means REC extract the samples PCR_r from received packets.

The device I_IPA comprises a first stage operating at the frequency FB. This first stage is constituted of:

- the means LFVCO2 to produce from a comparison signal SCOMP2 a signal SRA at frequency FRA, A frequency FRA equal to FB, or 1GHz is selected for example,

- a counter CPT_PCR2 whose rate is determined by the signal SRA at frequency FRA. The counter CPT_PCR2 produces counting ramps (CSR_PCR2), and of a range determined as a function of m of FRB and FV. For example the range EXC of the counter is selected to be equal to m.FB/FV,

- the means LATCH2 to realize the local samples PCR_Loc of ramps CSR_PCR2 via the signal CLKech, and

- the means COMP2 to compare the samples PCR_r to local samples PCR_Loc. The comparison means COMP2 deliver a comparison signal SCOMP2.

The device I_IPA also comprises the means DIVJ to produce from the signal SRA and the counting ramps CSR_PCR2, a signal SRB at frequency FRB such that FRB = FRA/J where J is an integer number, In particular the means DIVJ have their rate determined by the signal SRA and reset at each passage of the counting ramp CPT_PCR2 by a specific value PCR_REF comprised between 0 and ECC-1. The means DIJ deliver a synchronous pulse at the instant where the remainder of the division of CSR_PCR2 by J equals 0. For example $J = 10^9$.

- the means LFVCO3 to produce from a comparison signal SCOMP3 a signal SRC of period FRC equal to FV. For example FRC = 25Hz,

- the means DIVK to produce, from the signal SRC, a signal SRD at frequency FRD so that FRD = FRC/K where K is an integer number, For example K = 25, thus FRD equals 1Hz and the comparison between SRB and SRD can be operated,

- the means COMP3 to compare the signal SRD with the signal SRB, said comparison means COMP3 delivering a comparison signal SCOMP3.

The device also comprises the means EMS to produce pulses IMP2 at a frequency FV from the signal SRC and the signal SRD. In particular the means EMS have their rates determined by the signal SRTD and the signal SRC constitutes a reset signal or a reset to 0. The device also comprises the means GEG to reconstruct a synchronization signal from the pulses IMP2 and the signal SRD.

The invention is described in the preceding text as an example. It is understood that those skilled in the art are capable of producing variants of the invention without leaving the scope of the patent.

CLAIMS

1. A transmission device able to transmit packets in a packet communication network, said device comprising the means (EXS) to extract clock signals (CLK) and pulses (IMP1) at frequency FV synchronous with said signals (CLK) from a synchronization signal (SG0),

characterized in that the device also comprises:

- the means (DIVP) to produce, from the pulses (IMP1) and said clock signals (CLK), a signal (SA) at frequency FA such that FA = FV/P where P is an integer number,
- the means (LFVO1) to produce from a comparison signal (SCOMP1) a signal (SB) at frequency FB greater than FA,
- the means (DIVQ) to produce, from the signal (SB), a signal (SC) at frequency FC so that FC = FB/Q where Q is an integer number,
- the means (DIVR) to produce, from the signal (SC), a signal (CLR) at frequency FCLR so that FCLR = FC/R where R is an integer number,
- the means (COMP1) to compare the signal (SA) with the signal (SC), said means (COMP1) delivering a comparison signal (SCOMP1),
- a counter (CPT_PCR1) whose rate is determined by the signal (SB) and initialized by the signal (CLR), said counter (CPT_PCR1) produced from counting ramps (CSE_PCR),
- the means (LATCH1) to realize the samples (PCR_e) of ramps (CSE_PCR) via a signal (CLKech) from a time base synchronized on all the devices connected to said network, and
- the means (INTE) to transmit a packet comprising the sample (PCR_e) in the communications network.

2. A reception device able to receive packets in a packet communication network, said device comprising the means (REC) to receive packets from said network, said packets comprising the samples (PCR_r), said samples (PCR_r) coming from data sampled by a signal (CLKech) from a time base

synchronized on all the devices connected to said network, the means (REC) extracting said samples (PCR_r) from packets received.

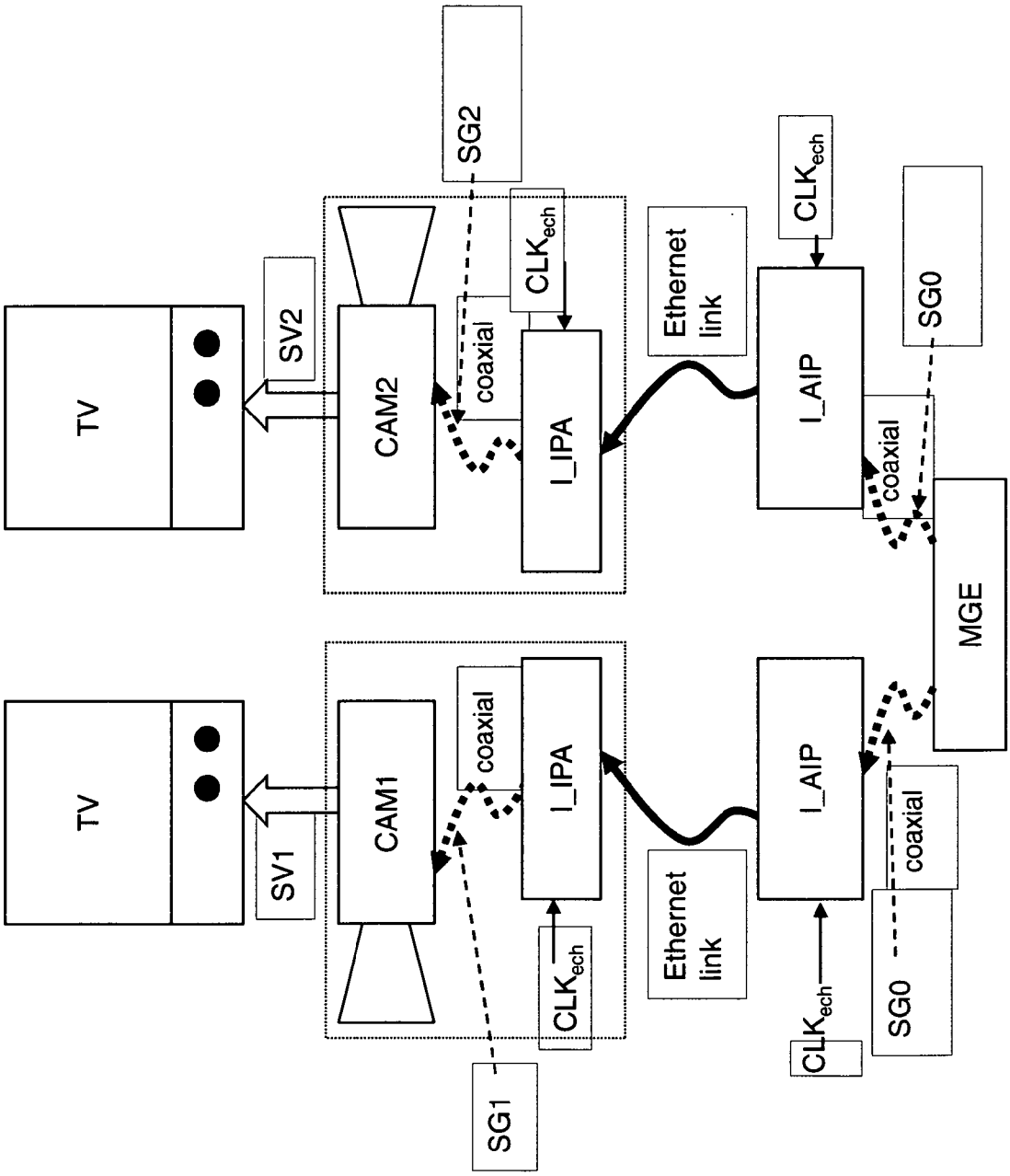
characterized in that the device also comprises:

- the means (LFVCO2) to produce from a comparison signal (SCOMP2) a signal (SRA) at frequency FRA,
- a counter (CPT_PCR2) whose rate is determined by the signal (SRA), said counter (CPT_PCR2) produced by counting ramps (CSR_PCR2),
- the means (LATCH2) to realize the local samples (PCR_Loc) of ramps (CSR_PCR2) via the signal (CLKech), and
- the means (COMP2) to compare said samples (PCR_r) with said local samples (PCR_Loc), said means of comparison (COMP2) delivering the comparison signal (SCOMP2),
- the means (DIVJ) to produce from the signal (SRA) and the counting ramps (CSR_PCR2), a signal (SRB) at frequency FRB such that FRB = FRA/J where J is an integer number,
- the means (LFVCO2) to produce from a comparison signal (SCOMP3) a signal (SRC) at frequency FRC,
- the means (DIVK) to produce, from the signal (SRC), a signal (SRD) at frequency FRD so that FRD = FRC/K where K is an integer number,
- the means (COMP3) to compare the signal (SRD) with the signal (SRB), said comparison means (COMP3) delivering a comparison signal (SCOMP3),
- the means (EMS) to produce pulses (IMP2) at a frequency (FV) from the signal (SRC) and the signal (SRD),
- the means to reconstitute a synchronization signal from said pulses (IMP2) and the signal (SRD).

3. System for synchronization comprising a transmission device according to claim 1 and at least one device for reception according to claim 2.

4. System for synchronization according to the preceding claim characterized in that the frequency (FRA) of the signal (SRA) of the reception device(s) is identical to the frequency (FB) of the transmission device.

5. System for synchronization according to the preceding claim characterized in that the frequency (FRC) of the reception device is identical to the frequency (FV) of the pulse (IMP1 of the transmission device.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SG1
Ethernet link
I_AIP
CLKech
SG0
coaxial

Figure 1

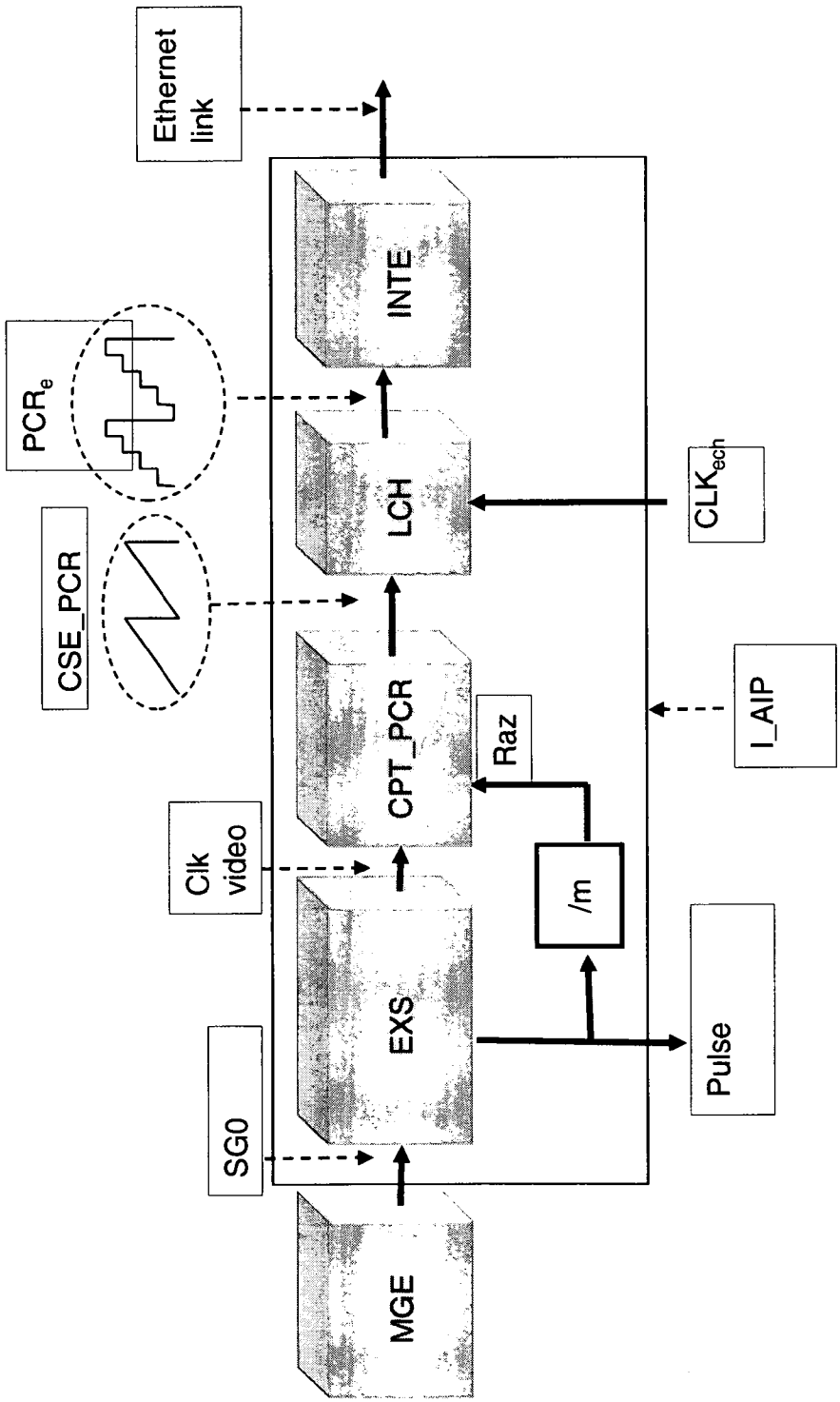
Ethernet link
INTE
LCH
CPT_PCR
EXS
MGE
PCR$_e$
CSE_PCR
Clk video
SG0
Raz
/m
CLK$_{ech}$
I_AIP
Pulse

Figure 2

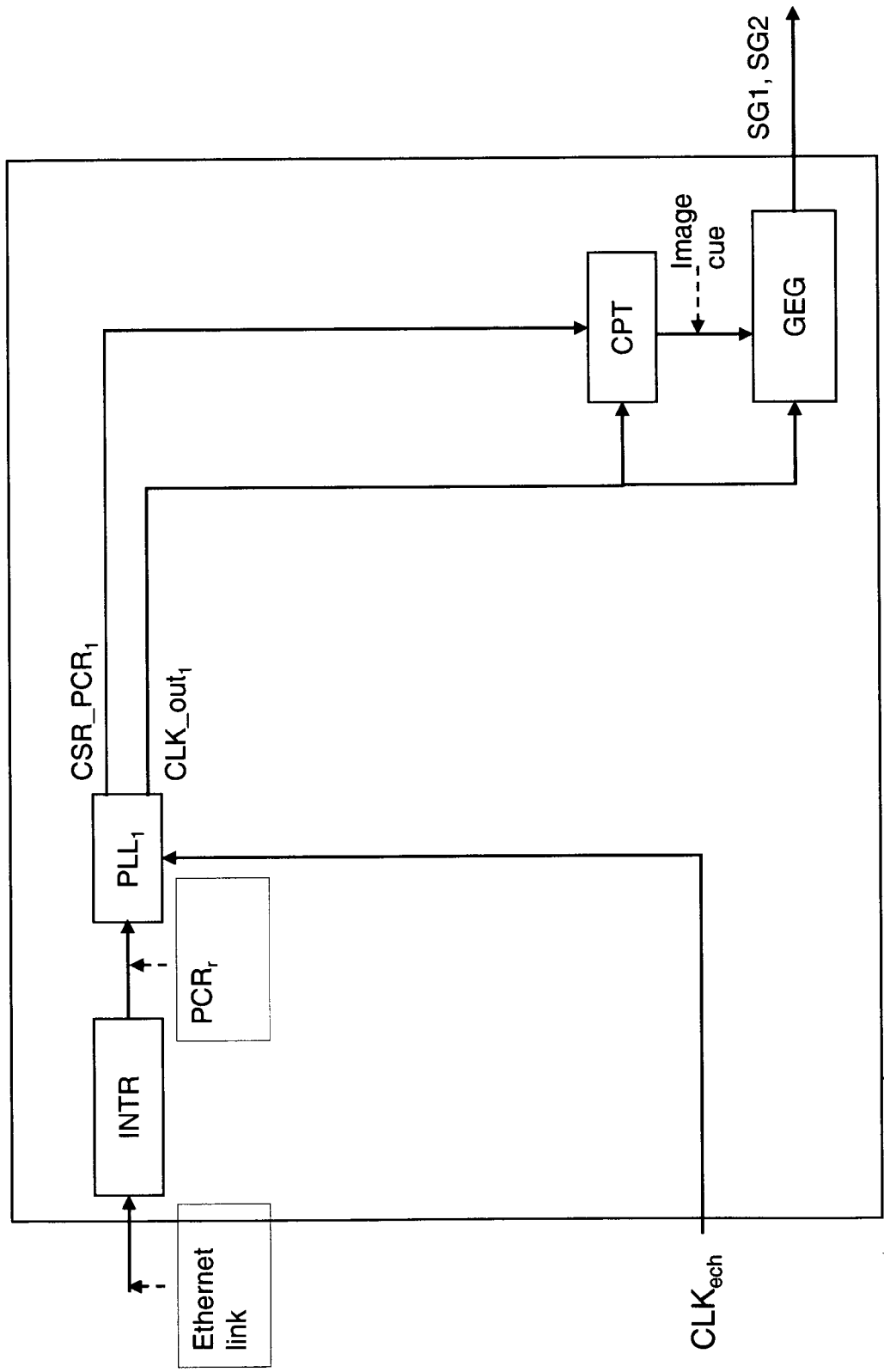
SG1, SG2
Image cue
CPT
GEG
CSR_PCR1
CLK_out1
PLL1
PCRr
INTR
Ethernet link
CLKech
I_IPA

Figure 3

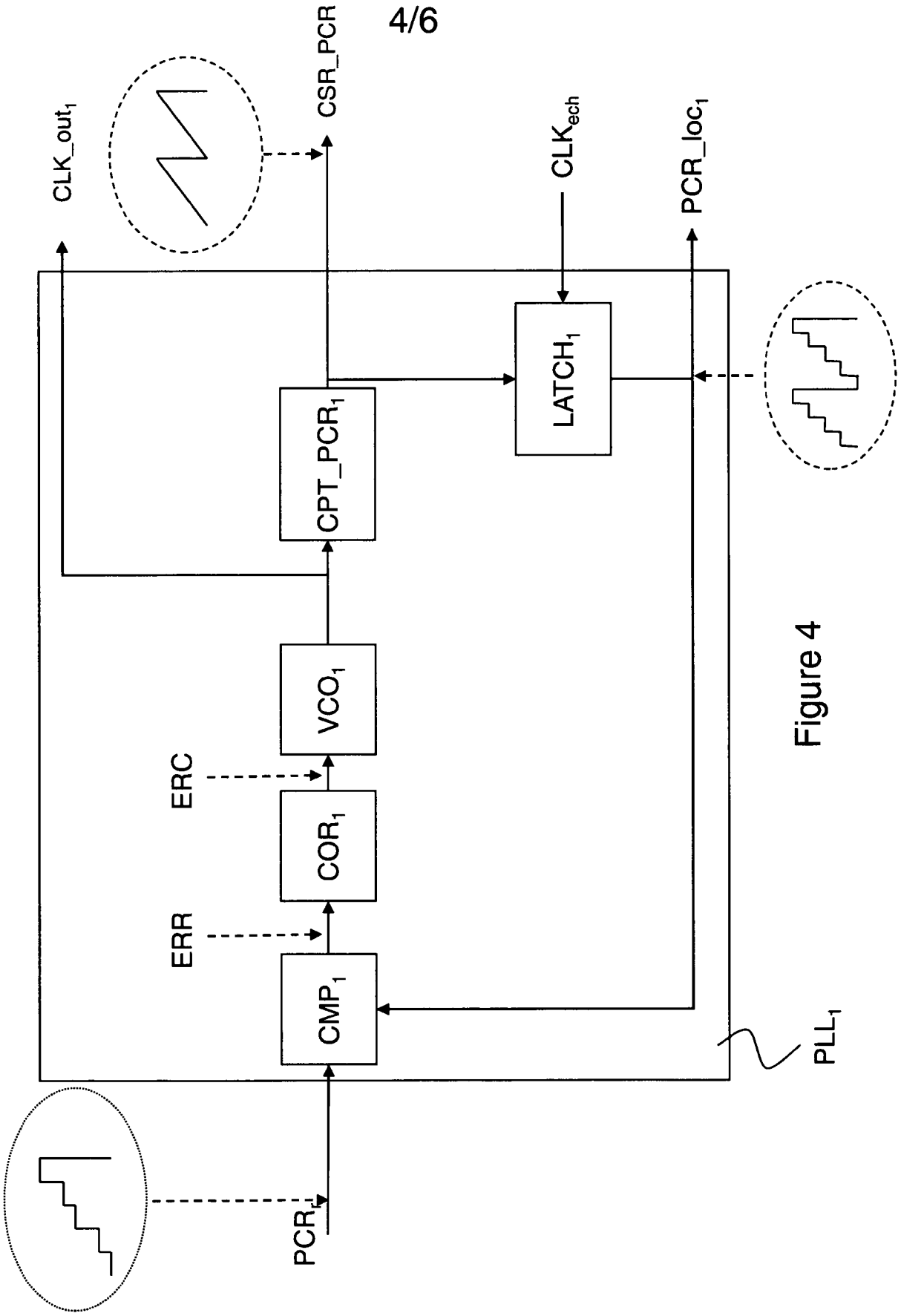
CLK_out1
CSR_PCR
CLKech
PCR_loc1
LATCH1
CPT_PCR1
VCO1
ERC
COR1
ERR
CMP1
PLL1
PCRi

Figure 4

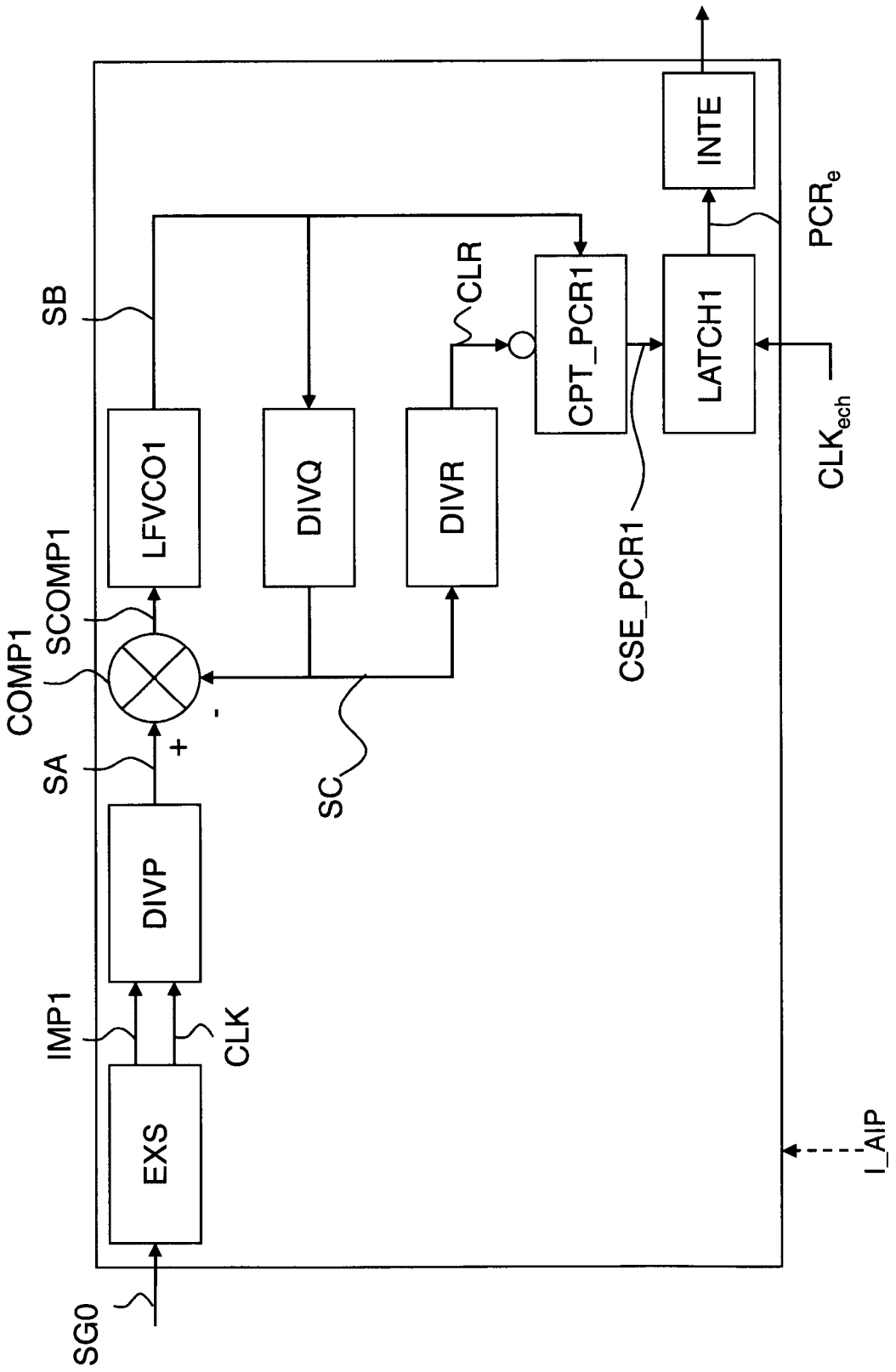
SG0
EXS
IMP1
CLK
DIVP
SA
COMP1
SCOMP1
LFVCO1
SB
DIVQ
DIVR
SC
CLR
CPT_PCR1
CSE_PCR1
LATCH1
INTE
PCR$_e$
CLK$_{ech}$
I_AIP

Figure 5

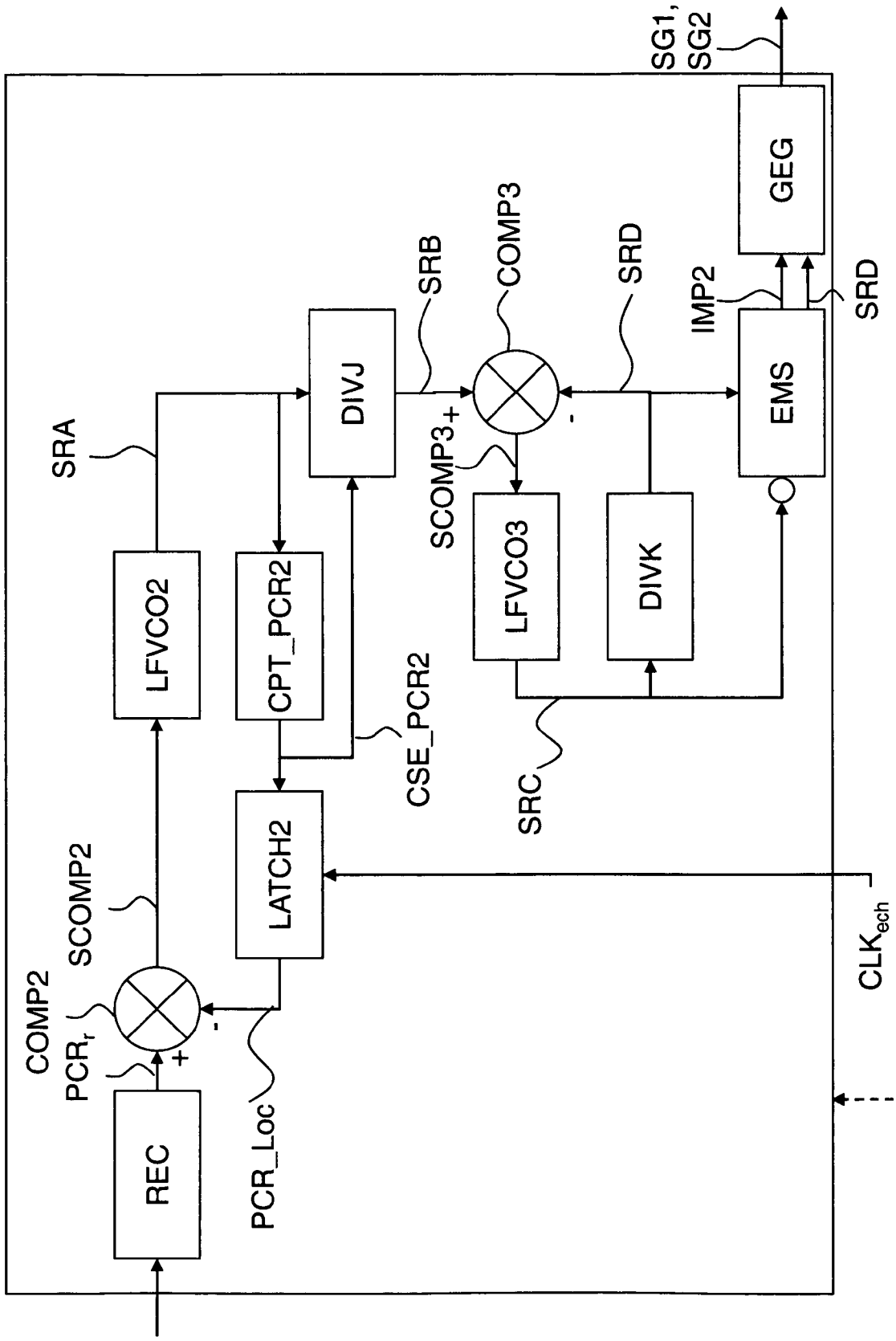
SG1, SG2
GEG
EMS
IMP2
SRD
DIVJ
SRB
COMP3
SRD
SRA
SCOMP3
LFVCO3
DIVK
LFVCO2
CPT_PCR2
CSE_PCR2
SRC
LATCH2
SCOMP2
COMP2
PCR_r
REC
PCR_Loc
CLK_ech
I_IPA

Figure 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064542

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N7/62 H04N5/04 H03L7/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007/104891 A2 (THOMSON LICENSING) 20 September 2007 (2007-09-20) page 4, line 5 - page 5, line 30 page 7, line 4 - page 10, line 12 figures 3-7	1-5
A	EP 1 947 865 A (THOMSON LICENSING) 23 July 2008 (2008-07-23) paragraph [0013] - paragraph [0023] paragraph [0029] - paragraph [0045] paragraph [0048] - paragraph [0068] paragraph [0077] - paragraph [0087] figures 1,2,4	1-5

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2009	04/12/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fragua, Miguel Angel

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064542

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 471 745 A (SONY) 27 October 2004 (2004-10-27) paragraph [0005] - paragraph [0008] paragraph [0019] - paragraph [0051] figures 1,4	1-5
A	US 2008/129870 A1 (CHAMPION ET AL) 5 June 2008 (2008-06-05) paragraph [0018] paragraph [0056] - paragraph [0068] figure 6	2-4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/064542

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2007104891 A2	20-09-2007	EP 2022273 A2	11-02-2009
		FR 2898453 A1	14-09-2007
		JP 2009530885 T	27-08-2009
		US 2009175271 A1	09-07-2009
EP 1947865 A	23-07-2008	CN 101227268 A	23-07-2008
		FR 2911460 A1	18-07-2008
		JP 2008178098 A	31-07-2008
		US 2008170588 A1	17-07-2008
EP 1471745 A	27-10-2004	CN 1543193 A	03-11-2004
		GB 2400255 A	06-10-2004
		JP 2004304809 A	28-10-2004
		US 2004257469 A1	23-12-2004
US 2008129870 A1	05-06-2008	NONE	